8051 Embedded Micro Controller with Flash OSD and ISP

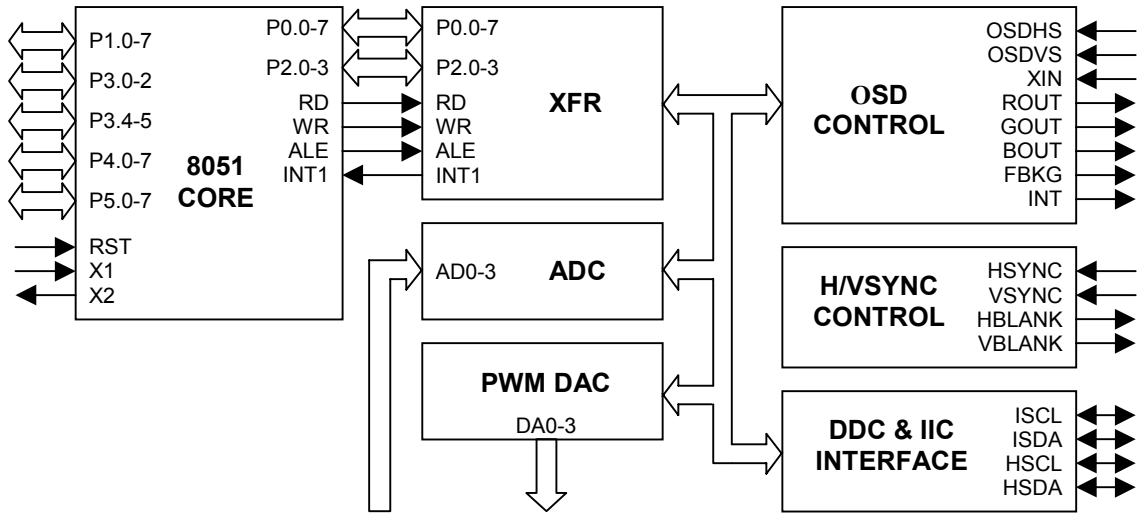
FEATURES

- 8051 core, 12MHz operating frequency with double CPU clock option, 3.3V power supply.
- 1024-byte RAM, 64K-byte program Flash-ROM.
- Maximum 4 channels of 5V open-drain PWM DAC.
- Maximum 32 bi-directional I/O pins.
- SYNC processor for composite separation/insertion, H/V polarity/frequency check and polarity adjustment.
- Built-in low power reset circuit.
- Compliant with VESA DDC2B/2Bi/2B+ standard.
- Dual slave IIC addresses.
- Single master IIC interface for internal device communication.
- Maximum 4-channel 6-bit ADC.
- Watchdog timer with programmable interval.
- OSD controller features:
  . Full-screen display consists of 15 (rows) by 30 (columns) characters.
  . Programmable OSD menu positioning for display screen center.
  . 512 Flash-ROM fonts, with 12x18 dot matrix, including 480 standard fonts and 32 multi-color fonts.
  . 15 character foreground color and 7 character background color selectable character by character.
  . Character (per row) and window intensity control.
  . Character bordering, shadowing and blinking effect.
  . Character height control (18 to 71 lines), double height and/or width control.
  . 4 programmable windows with multi-level operation and programmable shadowing width/height/color.
- In System Programming function (ISP).
- 42-pin SDIP or 44-pin PLCC/QFP package.

GENERAL DESCRIPTIONS

The MTV230M64 micro-controller is an 8051 CPU core embedded device specially tailored to LCD Monitor applications. It includes an 8051 CPU core, 1024-byte SRAM, OSD controller, 4 built-in PWM DACs, VESA DDC interface, 4-channel A/D converter, a 64K-byte internal program Flash-ROM and a 9K-word internal OSD character Flash-ROM.

BLOCK DIAGRAM



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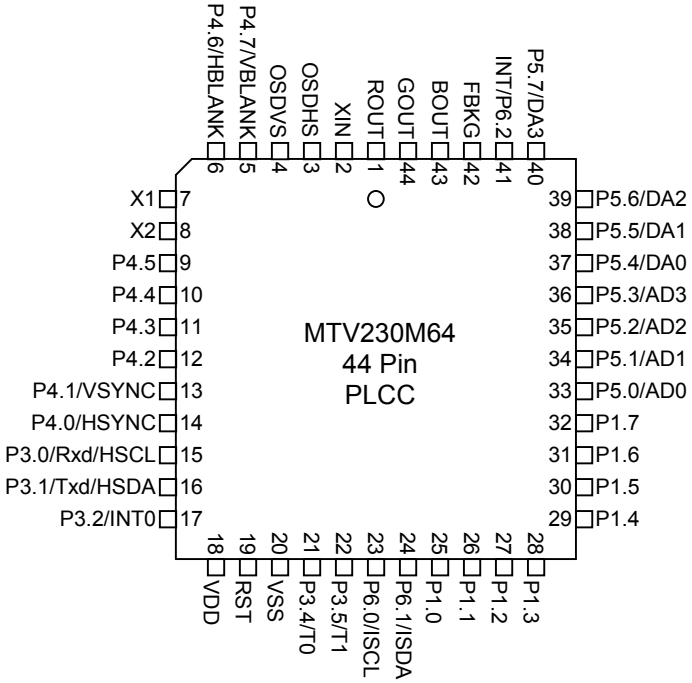
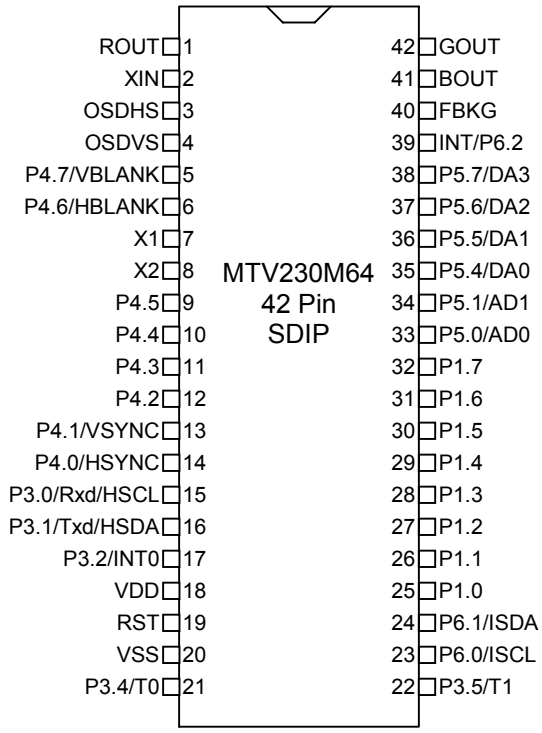
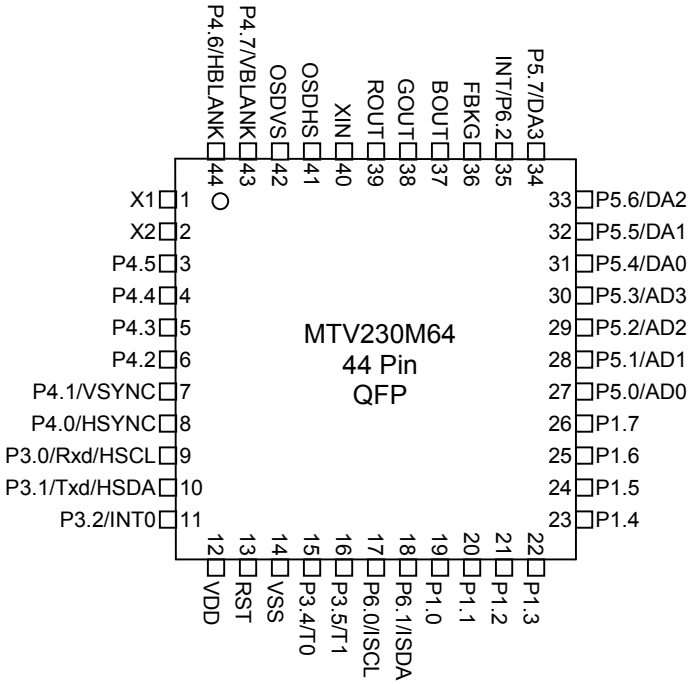
PIN CONNECTION





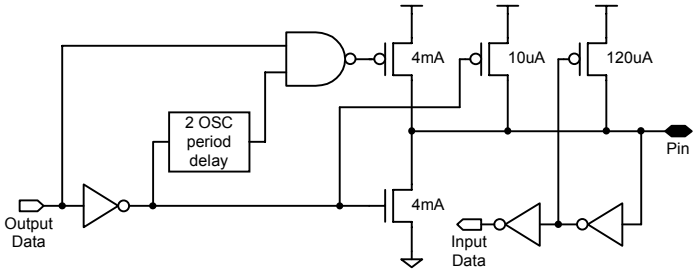


PIN CONFIGURATION

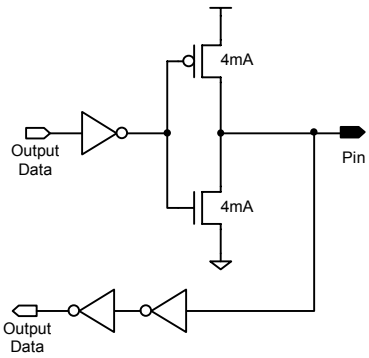
A “CMOS pin” can be used as Input or Output mode. To use these pins as output mode, S/W needs to set the corresponding output enable control bit “Pxxoe” to 1. Otherwise, the “Pxxoe” should clear to 0. In output mode, these pins can sink and drive at least 4mA current.

A “open drain pin” means it can sink at least 4mA current but no drive current to VDD. It can be used as input or output function and need an external pull up resistor.

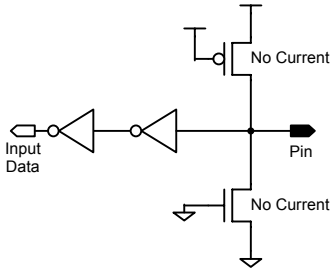
A “8051 standard pin” is a pseudo open drain pin. It can sink at least 4mA current when output low level, and drive at least 4mA current for 160nS when output transit from low to high, then keep drive 100uA to maintain the pin at high level. It can be used as input or output function. It need an external pull up resistor when drive heavy load device.



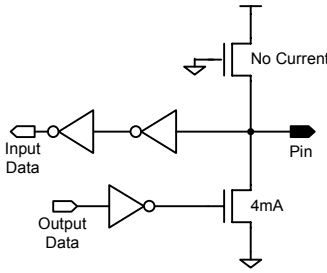
8051 Standard Pin



CMOS Pin (Output Mode)
Pxxoe=1



CMOS Pin (Input Mode)
Pxxoe=0



5V Open Drain Pin

PIN DESCRIPTION

Name	Type	#44/42	Description
RST	I	19	Active high reset.
VDD	-	18	Positive Power Supply.
VSS	-	20	Ground.
X2	O	8	Oscillator output.
X1	I	7	Oscillator input.
P1.0	I/O	25	General purpose I/O (8051 standard).
P1.1	I/O	26	General purpose I/O (8051 standard).
P1.2	I/O	27	General purpose I/O (8051 standard).
P1.3	I/O	28	General purpose I/O (8051 standard).
P1.4	I/O	29	General purpose I/O (8051 standard).
P1.5	I/O	30	General purpose I/O (8051 standard).
P1.6	I/O	31	General purpose I/O (8051 standard).
P1.7	I/O	32	General purpose I/O (8051 standard).
P3.0/Rxd/HSCL	I/O	15	General purpose I/O / Rxd / Slave IIC clock (5V open drain).
P3.1/Txd/HSDA	I/O	16	General purpose I/O / Txd / Slave IIC data (5V open drain).
P3.2/INT0	I/O	17	General purpose I/O / INT0 (8051 standard).
P3.4/T0	I/O	21	General purpose I/O / T0 (8051 standard).
P3.5/T1	I/O	22	General purpose I/O / T1 (8051 standard).
P4.7/VBLANK	I/O	5	General purpose I/O / Vertical blank output (CMOS).
P4.6/HBLANK	I/O	6	General purpose I/O / Horizontal blank output (CMOS).
P4.5/HCLAMP	I/O	9	General purpose I/O / Hclamp output (CMOS).
P4.4	I/O	10	General purpose I/O (CMOS).
P4.3	I/O	11	General purpose I/O (CMOS).
P4.2	I/O	12	General purpose I/O (CMOS).
P4.1/VSYNC	I/O	13	General purpose I/O / Vsync input (5V open drain).
P4.0/HSYNC	I/O	14	General purpose I/O / Hsync or Xsync input (5V open drain).
P5.7/DA3	I/O	40/38	General purpose I/O / PWM DAC output (5V open drain).
P5.6/DA2	I/O	39/37	General purpose I/O / PWM DAC output (5V open drain).
P5.5/DA1	I/O	38/36	General purpose I/O / PWM DAC output (5V open drain).
P5.4/DA0	I/O	37/35	General purpose I/O / PWM DAC output (5V open drain).
P5.3/AD3	I/O	36/-	General purpose I/O / ADC Input (CMOS).
P5.2/AD2	I/O	35/-	General purpose I/O / ADC Input (CMOS).
P5.1/AD1	I/O	34	General purpose I/O / ADC Input (CMOS).
P5.0/AD0	I/O	33	General purpose I/O / ADC Input (CMOS).
P6.0/ISCL	I/O	23	General purpose output / Master IIC clock (5V open drain).
P6.1/ISDA	I/O	24	General purpose output / Master IIC data (5V open drain).
INT/P6.2	O	41/39	OSD intensity output / General purpose output (CMOS).
FBKG	O	42/40	OSD fast blanking output (CMOS).
BOUT	O	43/41	OSD blue color video signal output (CMOS).
GOUT	O	44/42	OSD green color video signal output (CMOS).
ROUT	O	1	OSD red color video signal output (CMOS).
XIN	I	2	OSD pixel clock input (CMOS).
OSDHS	I	3	OSD vertical SYNC input (CMOS).
OSDVS	I	4	OSD horizontal SYNC input (CMOS).

FUNCTIONAL DESCRIPTIONS

1. 8051 CPU Core

The CPU core of MTV230M64 is compatible with the industry standard 8051, which includes 256 bytes RAM, Special Function Registers (SFR), two timers, five interrupt sources and serial interface. The CPU core fetches its program code from the 64K bytes Flash in MTV230M64. It use Port0 and Port2 to access the “external special function register” (XFR) and external auxiliary RAM (AUXRAM).
The CPU core can run at double rate when FclkE is set. Once the bit is set, the CPU runs as if a 24MHz X’tal is applied on MTV230M64, but the peripherals (IIC, DDC, H/V processor …) still run at the original frequency.

Note: All registers listed in this document reside in 8051’s external RAM area (XFR). For internal RAM memory map please refer to 8051 spec.

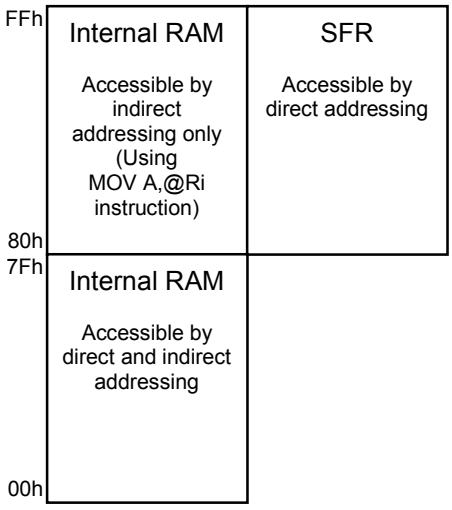
2. Memory Allocation

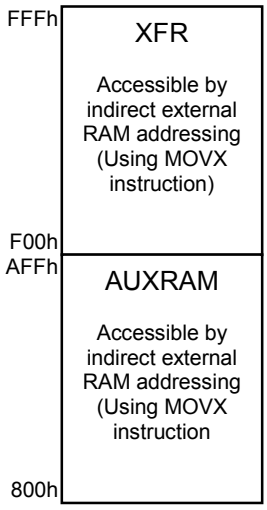
2.1 Internal Special Function Registers (SFR)
The SFR is a group of registers that are the same as standard 8051.

2.2 Internal RAM
There are total 256 bytes internal RAM in MTV230M64, the same as standard 8052.

2.3 External Special Function Registers (XFR)
The XFR is a group of registers allocated in the 8051 external RAM area F00h - FFFh. These registers are used for OSD control or other special function. Program can use "MOVX" instruction to access these registers.

2.4 Auxiliary RAM (AUXRAM)
There are total 768 bytes auxiliary RAM allocated in the 8051 external RAM area 800h - AFFh. Program can use "MOVX" instruction to access the AUXRAM.





3. Chip Configuration

The Chip Configuration registers define the chip pins function, as well as the functional blocks' connection, configuration and frequency.

Reg name	addr	bit7	bit6	bit5	Bit4	bit3	bit2	bit1	bit0
PADMOD	F2Bh (w)	HIICE	IIICE	HVE	HclpE			FclkE	P62E
PADMOD	F2Ch (w)	DA3E	DA2E	DA1E	DA0E	AD3E	AD2E	AD1E	AD0E
PADMOD	F2Dh (w)	P47oe	P46oe	P45oe	P44oe	P43oe	P42oe	P41oe	P40oe
PADMOD	F2Eh (w)	P57oe	P56oe	P55oe	P54oe	P53oe	P52oe	P51oe	P50oe
OPTION	F2Fh (w)	PWMF	DIV253	SlvAbs1	SlvAbs0	ENSCL	Msel	MIICF1	MIICF0

PADMOD (w) : Pad mode control registers. (All are "0" in Chip Reset)

HIICE = 1 → pin “P3.0/Rxd/HSCL” is HSCL; pin “P3.1/Txd/HSDA” is HSDA
= 0 → pin “P3.0/Rxd/HSCL” is P3.0/Rxd; pin “P3.1/Txd/HSDA” is P3.1/Txd
IIICE = 1 → pin “P6.1/ISDA” is ISDA; pin “P6.0/ISCL” is ISCL
= 0 → pin “P6.1/ISDA” is P6.1; pin “P6.0/ISCL” is P6.0
HVE = 1 → pin “P4.7/VBLANK” is VBLANK; pin “P4.6/HBLANK” is HBLANK
= 0 → pin “P4.7/VBLANK” is P4.7; pin “P4.6/HBLANK” is P4.6
HclpE = 1 → pin “P4.5/HCLAMP” is HCLAMP
= 0 → pin “P4.5/HCLAMP” is P4.5
FclkE = 1 → CPU running at double rate
= 0 → CPU running at normal rate
P62E = 1 → pin “INT/P6.2” is P6.2
= 0 → pin “INT/P6.2” is INT
DA3E = 1 → pin “P5.7/DA3” is DA3
= 0 → pin “P5.7/DA3” is P5.7
DA2E = 1 → pin “P5.6/DA2” is DA2
= 0 → pin “P5.6/DA2” is P5.6
DA1E = 1 → pin “P5.5/DA1” is DA1
= 0 → pin “P5.5/DA1” is P5.5
DA0E = 1 → pin “P5.4/DA0” is DA0
= 0 → pin “P5.4/DA0” is P5.4
AD3E = 1 → pin “P5.3/AD3” is AD3
= 0 → pin “P5.3/AD3” is P5.3
AD2E = 1 → pin “P5.2/AD2” is AD2
= 0 → pin “P5.2/AD2” is P5.2
AD1E = 1 → pin “P5.1/AD1” is AD1
= 0 → pin “P5.1/AD1” is P5.1
AD0E = 1 → pin “P5.0/AD0” is AD0
= 0 → pin “P5.0/AD0” is P5.0
P47oe = 1 → P4.7 is output pin
= 0 → P4.7 is input pin
P46oe = 1 → P4.6 is output pin
= 0 → P4.6 is input pin
P45oe = 1 → P4.5 is output pin
= 0 → P4.5 is input pin
P44oe = 1 → P4.4 is output pin
= 0 → P4.4 is input pin
P43oe = 1 → P4.3 is output pin
= 0 → P4.3 is input pin
P42oe = 1 → P4.2 is output pin
= 0 → P4.2 is input pin

P41oe = 1 → P4.1 is output pin
= 0 → P4.1 is input pin
P40oe = 1 → P4.0 is output pin
= 0 → P4.0 is input pin
P57oe = 1 → P5.7 is output pin
= 0 → P5.7 is input pin
P56oe = 1 → P5.6 is output pin
= 0 → P5.6 is input pin
P55oe = 1 → P5.5 is output pin
= 0 → P5.5 is input pin
P54oe = 1 → P5.4 is output pin
= 0 → P5.4 is input pin
P53oe = 1 → P5.3 is output pin
= 0 → P5.3 is input pin
P52oe = 1 → P5.2 is output pin
= 0 → P5.2 is input pin
P51oe = 1 → P5.1 is output pin
= 0 → P5.1 is input pin
P50oe = 1 → P5.0 is output pin
= 0 → P5.0 is input pin

OPTION (w) : Chip option configuration (All are "0" in Chip Reset).
PWMF = 1 → select 94KHz PWM frequency.
= 0 → select 47KHz PWM frequency.
DIV253 = 1 → PWM pulse width is 253 step resolution.
= 0 → PWM pulse width is 256 step resolution.
SlvAbs1,SlvAbs0 : Slave IIC block A's slave address length.
= 1,0 → 5-bits slave address.
= 0,1 → 6-bits slave address.
= 0,0 → 7-bits slave address.
ENSCL = 1 → Enable slave IIC block to hold HSCL pin low while MTV230M64 can't catch-up the external master's speed.
Msel = 1 → Master IIC block connect to HSCL/HSDA pins.
= 0 → Master IIC block connect to ISCL/ISDA pins.
MIICF1,MIICF0 = 1,1 → select 400KHz Master IIC frequency.
= 1,0 → select 200KHz Master IIC frequency.
= 0,1 → select 50KHz Master IIC frequency.
= 0,0 → select 100KHz Master IIC frequency.

4. I/O Ports

4.1 Port1
Port1 is a group of pseudo open drain pins. It can be use as general purpose I/O. Port1's behavior is the same as standard 8051.

4.2 P3.0-2, P3.4-5
If these pins are not set as IIC pins, Port3 can be used as general purpose I/O, interrupt, UART and Timer pins. Port3's behavior is the same as standard 8051.

4.3 Port4, Port5 and Port6
Port4 and Port5 are used as general purpose I/O. S/W needs to set the corresponding P4(n)oe and P5(n)oe to define these pins are input or output. Port6 is pure output.

Reg name	addr	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
PORT4	F30h(r/w)								P40
PORT4	F31h(r/w)								P41
PORT4	F32h(r/w)								P42
PORT4	F33h(r/w)								P43
PORT4	F34h(r/w)								P44
PORT4	F35h(r/w)								P45
PORT4	F36h(r/w)								P46
PORT4	F37h(r/w)								P47
PORT5	F38h(r/w)								P50
PORT5	F39h(r/w)								P51
PORT5	F3Ah(r/w)								P52
PORT5	F3Bh(r/w)								P53
PORT5	F3Ch(r/w)								P54
PORT5	F3Dh(r/w)								P55
PORT5	F3Eh(r/w)								P56
PORT5	F3Fh(r/w)								P57
PORT6	F28h(w)								P60
PORT6	F29h(w)								P61
PORT6	F2Ah(w)								P62

PORT4 (r/w) : Port 4 data input/output value.

PORT5 (r/w) : Port 5 data input/output value.

PORT6 (w) : Port 6 data output value.

5. PWM DAC

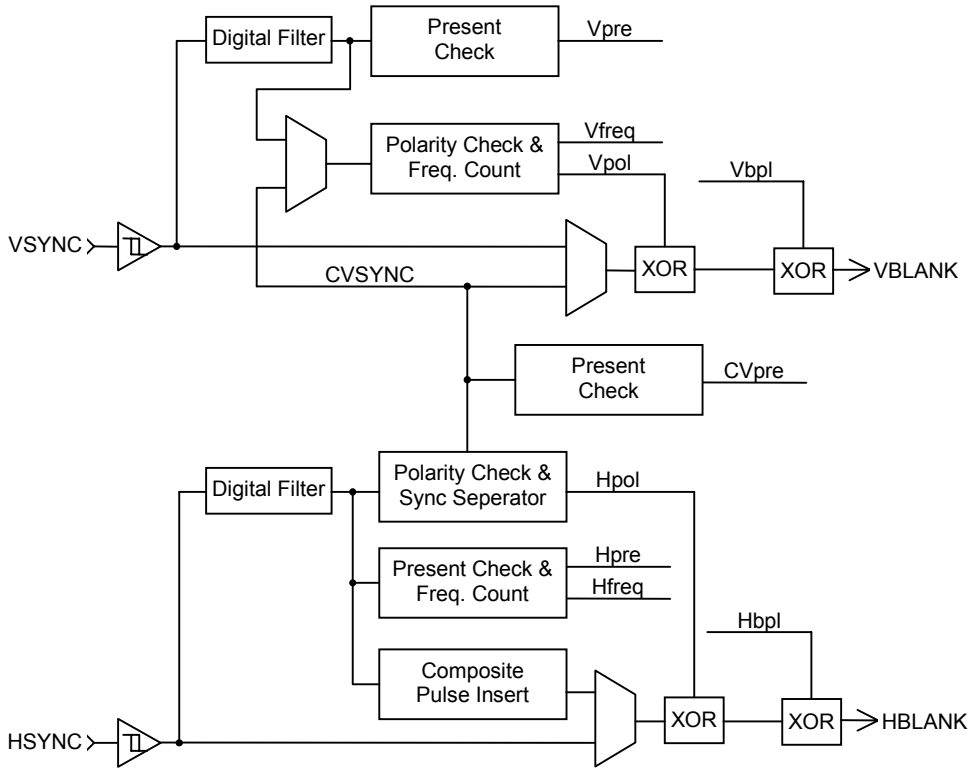
Each PWM DAC converter's output pulse width is controlled by an 8-bit register in XFR. The frequency of PWM clock is 47KHz or 94KHz, selected by PWMF. And the total duty cycle step of these DAC outputs is 253 or 256, selected by DIV253. If DIV253=1, writing FDH/FEH/FFH to DAC register generates stable high output. If DIV253=0, the output will pulse low at least once even if the DAC register's content is FFH. Writing 00H to DAC register generates stable low output.

Reg name	addr	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
DA0	F20h (r/w)	Pulse width of PWM DAC 0							
DA1	F21h (r/w)	Pulse width of PWM DAC 1							
DA2	F22h (r/w)	Pulse width of PWM DAC 2							
DA3	F23h (r/w)	Pulse width of PWM DAC 3							

DA0-3 (r/w) : The output pulse width control for DA0-3.
* All of PWM DAC converters are centered with value 80h after power on.

6. H/V SYNC Processing

The H/V SYNC processing block performs the functions of composite signal separation/insertion, SYNC inputs presence check, frequency counting, polarity detection and H/V output polarity control. The present and frequency function block treat any pulse shorter than one OSC period as noise.



H/V SYNC Processor Block Diagram

6.1 Composite SYNC separation/insertion

The MTV230M64 continuously monitors the input HSYNC, if the vertical SYNC pulse can be extracted from the input, a CVpre flag is set and user can select the extracted "CVSYNC" for the source of polarity check, frequency count, and VBLANK output. The CVSYNC will have 8us delay compared with the original signal. The MTV230M64 can also insert pulse to HBLANK output during composite VSYNC's active time. The insert pulse's width is 1/8 HSYNC period and the insertion frequency can adapt to original HSYNC. The HBLANK's insert pulse can be disable or enable by setting "NoHins" control bit.

6.2 H/V Frequency Counter

MTV230M64 can discriminate HSYNC/VSYNC frequency and saves the information in XFRs. The 14 bits Hcounter counts the time of 64xHSYNC period, then load the result into the HCNTH/HCNTL latch. The output value will be [(128000000/H-Freq) - 1], updated once per VSYNC/CVSYNC period when VSYNC/CVSYNC is present or continuously updated when VSYNC/CVSYNC is non-present. The 12 bits Vcounter counts the time between two VSYNC pulses, then load the result into the VCNTH/VCNTL latch. The output value will be (62500/V-Freq), updated every VSYNC/CVSYNC period. An extra overflow bit indicates the condition of H/V counter overflow. The VFchg/HFchg interrupt is set when VCNT/HCNT value changes or overflow. Table 6.2.1 and table 6.2.2 shows the HCNT/VCNT value under the operations of 12MHz.

6.2.1 H-Freq Table

H-Freq(KHZ)		Output Value (14 bits) 12MHz OSC (hex / dec)
1	31.5	0FDEh / 4062
2	37.5	0D54h / 3412
3	43.3	0B8Bh / 2955
4	46.9	0AA8h / 2728
5	53.7	094Fh / 2383
6	60.0	0854h / 2132
7	68.7	0746h / 1862
8	75.0	06AAh / 1706
9	80.0	063Fh / 1599
10	85.9	05D1h / 1489
11	93.8	0554h / 1364
12	106.3	04B3h / 1203

6.2.2 V-Freq Table

V-Freq(Hz)		Output value (12bits) 12MHz OSC (hex / dec)
1	56	45Ch / 1116
2	60	411h / 1041
3	70	37Ch / 892
4	72	364h / 868
5	75	341h / 833
6	85	2DFh / 735

6.3 H/V Present Check

The Hpresent function checks the input HSYNC pulse, Hpre flag is set when HSYNC is over 10KHz or cleared when HSYNC is under 10Hz. The Vpresent function checks the input VSYNC pulse, the Vpre flag is set when VSYNC is over 40Hz or cleared when VSYNC is under 10Hz. The HPRchg interrupt is set when the Hpre value changes. The VPRchg interrupt is set when the Vpre/CVpre value change. However, the CVpre flag interrupt may be disabled when S/W disable the composite function.

6.4 H/V Polarity Detect

The polarity functions detect the input HSYNC/VSYNC high and low pulse duty cycle. If the high pulse duration is longer than that of low pulse, the negative polarity is asserted; otherwise, positive polarity is asserted. The HPLchg interrupt is set when the Hpol value changes. The VPLchg interrupt is set when the Vpol value changes.

6.5 Output HBLANK/VBLANK Control and Polarity Adjust

The HBLANK is the mux output of HSYNC and composite Hpulse. The VBLANK is the mux output of VSYNC and CVSYNC. The mux selection and output polarity are S/W controllable.

6.6 VSYNC Interrupt

The MTV230M64 check the VSYNC input pulse and generate an interrupt at its leading edge. The VSYNC flag is set each time when MTV230M64 detects a VSYNC pulse. The flag is cleared by S/W writing a "0".

6.7 H/V SYNC Processor Register

Reg name	addr	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
HVSTUS	F40h (r)	CVpre		Hpol	Vpol	Hpre	Vpre	Hoff	Voff
HCNTH	F41h (r)	Hovf		HF13	HF12	HF11	HF10	HF9	HF8
HCNTL	F42h (r)	HF7	HF6	HF5	HF4	HF3	HF2	HF1	HF0
VCNTH	F43h (r)	Vovf				VF11	VF10	VF9	VF8

VCNTL	F44h (r)	VF7	VF6	VF5	VF4	VF3	VF2	VF1	VF0
HVCTR0	F40h (w)	C1	C0	NoHins				HBpl	VBpl
HVCTR3	F43h (w)		CLPEG	CLPPO	CLPW2	CLPW1	CLPW0		
HVCTR4	F44h (w)							DF	
INTFLG	F48h (r/w)	HPRchg	VPRchg	HPLchg	VPLchg	HFchg	VFchg		Vsync
INTEN	F49h (w)	EHPR	EVPR	EHPL	EVPL	EHF	EVF		EVsync

HVSTUS (r) : The status of polarity, present and static level for HSYNC and VSYNC.

CVpre = 1 → The extracted CVSYNC is present.
= 0 → The extracted CVSYNC is not present.
H_{pol} = 1 → HSYNC input is positive polarity.
= 0 → HSYNC input is negative polarity.
V_{pol} = 1 → VSYNC (CVSYNC) is positive polarity.
= 0 → VSYNC (CVSYNC) is negative polarity.
H_{pre} = 1 → HSYNC input is present.
= 0 → HSYNC input is not present.
V_{pre} = 1 → VSYNC input is present.
= 0 → VSYNC input is not present.
H_{off}* = 1 → HSYNC input's off level is high.
= 0 → HSYNC input's off level is low.
V_{off}* = 1 → VSYNC input's off level is high.
= 0 → VSYNC input's off level is low.
*H_{off} and V_{off} are valid when $H_{pre=0}$ or $V_{pre=0}$.

HCNTH (r) : H-Freq counter's high bits.

Hovf = 1 → H-Freq counter is overflow, this bit is clear by H/W when condition removed.
HF13 - HF8 : 6 high bits of H-Freq counter.

HCNTL (r) : H-Freq counter's low byte.

VCNTH (r) : V-Freq counter's high bits.

Vovf = 1 → V-Freq counter is overflow, this bit is clear by H/W when condition removed.
VF11 - 8 : 4 high bits of V-Freq counter.

VCNTL (r) : V-Freq counter's low byte.

HVCTR0 (w) : H/V SYNC processor control register 0.

C1, C0 = 1,1 → Select CVSYNC as the polarity, freq and VBLANK source.
= 1,0 → Select VSYNC as the polarity, freq and VBLANK source.
= 0,0 → Disable composite function.
= 0,1 → H/W auto switch to CVSYNC when CVpre=1 and VSpre=0.
NoHins = 1 → HBLANK has no insert pulse in composite mode.
= 0 → HBLANK has insert pulse in composite mode.
HB_{pl} = 1 → negative polarity HBLANK output.
= 0 → positive polarity HBLANK output.
VB_{pl} = 1 → negative polarity VBLANK output.
= 0 → positive polarity VBLANK output.

HVCTR3 (w) : HSYNC clamp pulse control register.

CLPEG = 1 → Clamp pulse follows HSYNC leading edge.
= 0 → Clamp pulse follows HSYNC trailing edge.
CLPPO = 1 → Positive polarity clamp pulse output.
= 0 → Negative polarity clamp pulse output.

CLPW2 : CLPW0 : Pulse width of clamp pulse is
[(CLPW2:CLPW0) + 1] x 0.167 μs for 12MHz X'tal selection.

HVCTR4 (w)**:** HSYNC digital filter control register.

DF =0 →The digital filter will treat any HSYNC pulse shorter than one OSC period (83.33ns) as noise, between one and two OSC period (83.33ns to 166.67ns) as unknown region, and longer than two OSC period (166.67ns) as pulse.

=1 →Disable the digital filter for HSYNC.

INTFLG (w) : Interrupt flag. An interrupt event will set its individual flag, and, if the corresponding interrupt enable bit is set, the 8051 core's INT1 source will be driven by a zero level. Software MUST clear this register while serve the interrupt routine.

HPRchg= 1 → No action.
= 0 → Clear HSYNC presence change flag.
VPRchg= 1 → No action.
= 0 → Clear VSYNC presence change flag.
HPLchg= 1 → No action.
= 0 → Clear HSYNC polarity change flag.
VPLchg= 1 → No action.
= 0 → Clear VSYNC polarity change flag.
HFchg = 1 → No action.
= 0 → Clear HSYNC frequency change flag.
VFchg = 1 → No action.
= 0 → Clear VSYNC frequency change flag.
Vsync = 1 → No action.
= 0 → Clear VSYNC interrupt flag.

INTFLG (r) : Interrupt flag.

HPRchg= 1 → Indicates a HSYNC presence change.
VPRchg= 1 → Indicates a VSYNC presence change.
HPLchg= 1 → Indicates a HSYNC polarity change.
VPLchg= 1 → Indicates a VSYNC polarity change.
HFchg = 1 → Indicates a HSYNC frequency change or counter overflow.
VFchg = 1 → Indicates a VSYNC frequency change or counter overflow.
Vsync = 1 → Indicates a VSYNC interrupt.

INTEN (w) : Interrupt enable.

EHPR = 1 → Enable HSYNC presence change interrupt.
EVPR = 1 → Enable VSYNC presence change interrupt.
EHPL = 1 → Enable HSYNC polarity change interrupt.
EVPL = 1 → Enable VSYNC polarity change interrupt.
EHF = 1 → Enable HSYNC frequency change / counter overflow interrupt.
EVF = 1 → Enable VSYNC frequency change / counter overflow interrupt.
EVsync = 1 → Enable VSYNC interrupt.

7. DDC & IIC Interface

7.1 DDC2B Mode

To perform DDC2 function, S/W can config the Slave A IIC block to act as EEPROM behavior. The Slave A block's slave address can be chosen by S/W as 5-bits, 6-bits or 7-bits. For example, if S/W choose 5-bits slave address as 10100b, the slave IIC block A will respond to slave address 10100xxb and save the 2 LSB "xx" in XFR. This feature enables MTV230M64 to meet PC99 requirement.

7.2 Slave Mode IIC function Block

The slave mode IIC block is connected to HSDA and HSCL pins. This block can receive/transmit data using IIC

protocol. There are 2 slave addresses that MTV230M64 can respond to. S/W may write the SLVAADR/SLVBADR register to determine the slave addresses. The SlaveA address can be configured to 5-bits, 6-bits or 7-bits by S/W setting the SlvAbs1 and SlvAbs0 control bits.
In receive mode, the block first detects IIC slave address match condition then issues a SlvAMI/SlvBMI interrupt. If the matched address is slave A, MTV230M64 will save the matched address's 2 LSB bits to SlvAlsb1 and SlvAlsb0 register. The data from HSDA is shifted into shift register then written to RCABUF/RCBBUF register when a data byte is received. The first byte loaded is word address (slave address is dropped). This block also generates a RCAI/RCBI (receive buffer full interrupt) every time when the RCABUF/RCBBUF is loaded. If S/W can't read out the RCABUF/RCBBUF in time, the next byte in shift register will not be written to RCABUF/RCBBUF and the slave block return NACK to the master. This feature guarantees the data integrity of communication. The WadrA/WadrB flag can tell S/W that if the data in RCABUF/RCBBUF is a word address.
In transmit mode, the block first detects IIC slave address match condition then issues a SlvAMI/SlvBMI interrupt. In the mean time, the SlvAlsb1/SlvAlsb0 is also updated if the matched address is slave A, and the data pre-stored in the TXABUF/TXBBUF is loaded into the shift register, resulted in TXABUF/TXBBUF empty and generates a TXAI/TXBI (transmit buffer empty interrupt). S/W should write the TXABUF/TXBBUF a new byte for next transfer before shift register empty. Fail to do this will cause data corrupt. The TXAI/TXBI occurs every time when shift register reads out the data from TXABUF/TXBBUF.
The SlvAMI/SlvBMI is cleared by writing "0" to corresponding bit in INTFLG register. The RCAI/RCBI is cleared by reading RCABUF/RCBBUF. The TXAI/TXBI is cleared by writing TXABUF/TXBBUF. If the control bit ENSCL is set, the block will hold HSCL low until the RCAI/RCBI/TXAI/TXBI is cleared.

*Please see the attachments about "Slave IIC Block Timing".

7.3 Master Mode IIC Function Block
The master mode IIC block can be connected to the ISDA /ISCL pins or the HSDA/HSCL pins, selected by Msel control bit. Its speed can be selected to 50KHz-400KHz by S/W setting the MIICF1/MIICF0 control bit. The software program can access the external IIC device through this interface. A summary of master IIC access is illustrated as follows.

7.3.1. To write IIC Device
1. Write MBUF the Slave Address.
2. Set S bit to Start.
3. After the MTV230M64 transmit this byte, a MbufI interrupt will be triggered.
4. Program can write MBUF to transfer next byte or set P bit to stop.

* Please see the attachments about "Master IIC Transmit Timing".

7.3.2. To read IIC Device
1. Write MBUF the Slave Address.
2. Set S bit to Start.
3. After the MTV230M64 transmit this byte, a MbufI interrupt will be triggered.
4. Set or reset the MAckO flag according to the IIC protocol.
5. Read out MBUF the useless byte to continue the data transfer.
6. After the MTV230M64 receives a new byte, the MbufI interrupt is triggered again.
7. Read MBUF also trigger the next receive operation, but set P bit before read can terminate the operation.

* Please see the attachments about "Master IIC Receive Timing".

Reg name	addr	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
IICCTR	F00h (r/w)						MAckO	P	S
IICSTUS	F01h (r)	WadrB	WadrA	SlvRWB	SAckIn	SLVS		SlvAlsb1	SlvAlsb0
IICSTUS	F02h (r)	MAckIn							
INTFLG	F03h (r)	TXBI	RCBI	SlvBMI	TXAI	RCAI	SlvAMI		MbufI
INTFLG	F03h (w)			SlvBMI			SlvAMI		MbufI
INTEN	F04h (w)	ETXBI	ERCBI	ESlvBMI	ETXAI	ERCAI	ESlvAMI		EMbufI
MBUF	F05h (r/w)	Master IIC receive/transmit data buffer							

RCABUF	F06h (r)	Slave A IIC receive buffer	
TXABUF	F06h (w)	Slave A IIC transmit buffer	
SLVAADR	F07h (w)	ENSlvA	Slave A IIC address
RCBBUF	F08h (r)	Slave B IIC receive buffer	
TXBBUF	F08h (w)	Slave B IIC transmit buffer	
SLVBADR	F09h (w)	ENSlvB	Slave B IIC address

IICCTR (r/w) : IIC interface control register.

MAckO = 1 → In master receive mode, NACK is returned by MTV230M64.
= 0 → In master receive mode, ACK is returned by MTV230M64.
S, P = ↑, 0 → Start condition when Master IIC is not during transfer.
= X, ↑ → Stop condition when Master IIC is not during transfer.
= 1, X → Will resume transfer after a read/write MBUF operation.

IICSTUS (r) : IIC interface status register.

WadrB = 1 → The data in RCBBUF is word address.
WadrA = 1 → The data in RCABUF is word address.
SlvRWB = 1 → Current transfer is slave transmit
= 0 → Current transfer is slave receive
SAckIn = 1 → The external IIC host respond NACK.
SLVS = 1 → The slave block has detected a START, cleared when STOP detected.
SlvAlsb1,SlvAlsb0 : The 2 LSB which host send to Slave A block.
MAckIn = 1 → Master IIC bus error, no ACK received from the slave IIC device.
= 0 → ACK received from the slave IIC device.

INTFLG (w) : Interrupt flag. A interrupt event will set its individual flag, and, if the corresponding interrupt enable bit is set, the 8051 INT1 source will be driven by a zero level. Software MUST clear this register while serve the interrupt routine.

SlvBMI = 1 → No action.
= 0 → Clear SlvBMI flag.
SlvAMI = 1 → No action.
= 0 → Clear SlvAMI flag.
MbufI = 1 → No action.
= 0 → Clear Master IIC bus interrupt flag (MbufI).

INTFLG (r) : Interrupt flag.

TXBI = 1 → Indicates the TXBBUF need a new data byte, clear by writing TXBBUF.
RCBI = 1 → Indicates the RCBBUF has received a new data byte, clear by reading RCBBUF.
SlvBMI = 1 → Indicates the slave IIC address B match condition.
TXAI = 1 → Indicates the TXABUF need a new data byte, clear by writing TXABUF.
RCAI = 1 → Indicates the RCABUF has received a new data byte, clear by reading RCABUF.
SlvAMI = 1 → Indicates the slave IIC address A match condition.
MbufI = 1 → Indicates a byte is sent/received to/from the master IIC bus.

INTEN (w) : Interrupt enable.

ETXBI = 1 → Enable TXBBUF interrupt.
ERCBI = 1 → Enable RCBBUF interrupt.
ESlvBMI = 1 → Enable slave address B match interrupt.
ETXAI = 1 → Enable TXABUF interrupt.
ERCAI = 1 → Enable RCABUF interrupt.
ESlvAMI = 1 → Enable slave address A match interrupt.
EMbufI = 1 → Enable Master IIC bus interrupt.

Mbuf (w) : Master IIC data shift register, after START and before STOP condition, write this register will resume MTV230M64's transmission to the IIC bus.

Mbuf (r) : Master IIC data shift register, after START and before STOP condition, read this register will resume MTV230M64's receiving from the IIC bus.

RCABUF (r) : Slave IIC block A receive data buffer.

TXABUF (w) : Slave IIC block A transmit data buffer.

SLVAADR (w) : Slave IIC block A's enable and address.
ENslvA = 1 → Enable slave IIC block A.
= 0 → Disable slave IIC block A.
bit6-0 : Slave IIC address A to which the slave block should respond.

RCBBUF (r) : Slave IIC block B receive data buffer.

TXBBUF (w) : Slave IIC block B transmit data buffer.

SLVBADR (w) : Slave IIC block B's enable and address.
ENslvB = 1 → Enable slave IIC block B.
= 0 → Disable slave IIC block B.
bit6-0 : Slave IIC address B to which the slave block should respond.

8. Low Power Reset (LVR) & Watchdog Timer

When the voltage level of power supply is below 2.6V (+/-0.15V) for a specific time, the level triggering LVR will generate a chip reset signal. After the power supply is above 2.6V (+/-0.15V), LVR maintains in reset state for 144 Xtal cycle to guarantee the chip exit reset condition with a stable X'tal oscillation.

The WatchDog Timer automatically generates a device reset when it is overflow. The interval of overflow is 0.25 sec x N, where N is a number from 1 to 8, and can be programmed via register WDT(2:0). The timer function is disabled after power on reset, user can activate this function by setting WEN, and clear the timer by set WCLR.

9. A/D converter

The MTV230M64 is equipped with four 6-bit A/D converters, S/W can select the current convert channel by setting the SADC1/SADC0 bit. The refresh rate for the ADC is OSC freq./12288. The ADC compare the input pin voltage with internal VDD*N/64 voltage (where N = 0 - 63). The ADC output value is N when pin voltage is greater than VDD*N/64 and smaller than VDD*(N+1)/64.

Reg name	addr	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
ADC	F10h (w)	ENADC				SADC3	SADC2	SADC1	SADC0
ADC	F10h (r)			ADC convert Result					
WDT	F18h (w)	WEN	WCLR				WDT2	WDT1	WDT0

WDT (w) : Watchdog Timer control register.
WEN = 1 → Enable WatchDog Timer.
WCLR = 1 → Clear WatchDog Timer.
WDT2: WDT0 = 0 → overflow interval = 8 x 0.25 sec.
= 1 → overflow interval = 1 x 0.25 sec.
= 2 → overflow interval = 2 x 0.25 sec.
= 3 → overflow interval = 3 x 0.25 sec.

= 4 → overflow interval = 4 x 0.25 sec.
= 5 → overflow interval = 5 x 0.25 sec.
= 6 → overflow interval = 6 x 0.25 sec.
= 7 → overflow interval = 7 x 0.25 sec.

ADC (w) : ADC control.

ENADC	= 1	→ Enable ADC.
SADC0	= 1	→ Select ADC0 pin input.
SADC1	= 1	→ Select ADC1 pin input.
SADC2	= 1	→ Select ADC2 pin input.
SADC3	= 1	→ Select ADC3 pin input.

ADC (r) : ADC convert result.

10. In System Programming function (ISP)

The two Flash memories (OSD Flash and Code Flash) can be programmed by a specific WRITER in parallel mode, or by IIC Host in serial mode while the system is working. The ISP's feature is outlined as below:

1. Single 3.3V power supply for Program/Erase/Verify.
2. Block Erase: 512 Byte for Program Code or 256 words for OSD fonts, both are 10mS time
3. Whole Flash erase (Blank): 10mS
4. Byte/Word programming Cycle time: 60uS per byte, 120uS per word
5. Read access time: 40ns
6. Only two pin IIC bus(shared with DDC2) is needed for ISP in user/factory mode
7. IIC Bus clock rate up to 140KHz
8. Whole 64K-byte/9K-word Flash programming within 6/2 Sec
9. CRC check provide 100% coverage for all single/double bit errors

After power on/Reset, The MTV230M64 is running the original Program Code. Once the S/W detect a ISP request (by key or IIC), S/W can accept the request by the steps below:

1. Clear watchdog to prevent reset during ISP period
2. Disable all interrupt to prevent CPU wake-up
3. Write ISP slave's IIC address to ISPSLV for communication
4. Write 93h to ISP enable register (ISPEN) to enable ISP
5. Enter 8051 idle mode

When ISP is enable, the MTV230M64 will disable Watchdog reset and switch the Flash interface to ISP host in 15-22.5uS. So S/W MUST enter idle mode immediately after enable ISP. In the 8051 idle mode, PWM DACs and I/O pins keep running at its old status. There are 4 types of IIC bus transfer protocol in ISP mode.

```
Command Write
    S-tttttt10k-cccccxxBk-AAAAAAAk-P
Command Read
    S-tttttt11k-cccccXXBK-AAAAAAAK-aaaaaaaaK-RRRRRRRRK-rrrrrrrrK-P
Data Write
    S-tttttt00k-aaaaaaaak-ddddddddk-dddddddk- ... -ddddddddk-dddddddk-P
Data Read
    S-tttttt00k-aaaaaaaak-(P)-
    S-tttttt01k-ddddddddK-dddddddK- ... -ddddddddK-dddddddK-P
where
    S = start or re-start              P = stop
    K = ack by host (0 or 1)           k = ack by slave
    tttttt = ISP slave address         ccccc = command
    B = OSD/Code select (1=OSD)
```

```
x = don't care                      X = not defined
AAAAAAAA = Code_address[15:8]       aaaaaaaa = Code_address[7:0]
AAAAAAA = OSD_address[13:7]         aaaaaaa = OSD_address[6:0]
RRRRRRRR = CRC_register[15:8]       rrrrrrrr = CRC_register[7:0]
ddddddddd-ddddddddd = Code_data     dddd-ddddddddd = OSD_data
ccccc = 10100 → Program
ccccc = 00110 → Page Erase 512 bytes or 256 words (Erase)
ccccc = 01101 → Erase entire Flash (Blank)
ccccc = 11010 → Clear CRC_register (Clr_CRC)
ccccc = 01001 → Reset MTV230M64 (Reset_CPU)
```

10.1 ISP Command Write

The 2nd byte of "Command Write" can define the operating mode of MTV230M64 in its "Data write" stage, clear CRC register, or reset MTV230M64. The bit 0 of 2nd byte select the target Flash to be operated (1=OSD, 0=Code). The 3rd byte of Command Write defines the page address (A15-8 of Code Flash, A13-7 of OSD Flash). A Command Write may consist of 1,2 or 3 bytes.

10.2 ISP Command Read

The 2nd byte echoes the current command in ISP slave. The 3rd and 4th byte reflects the current Flash address. The 5th and 6th byte reports the CRC result. A Command Read may consist of 2,3,4,5 or 6 bytes.

10.3 ISP Data Write

The 2nd byte defines the Flash's low address (A7-0 for Code, A6-0 for OSD). After receiving the 3rd byte, the MTV230M64 will execute a Program/Erase/Blank command depends on the preceding "Command Write". If Code area is select, the Code Flash's low address will increase every time when ISP slave acknowledges the data byte. If OSD Flash is selected, the OSD Flash's low address will increase every 2 data bytes received. The Blank/Erase command need one data byte (content is "don't care"). The executing time is 10mS. During the 10mS period, the ISP slave won't accept any command/data and returns non-ack to any IIC bus activity. The Program command may have 1-256 data byte for Code Flash, and have 1-128 word(256 byte) for OSD Flash. The program cycle time is 60us. If the ISP slave can't complete the program cycle in time, it will return non-ack to the following data byte. In the meantime, the low address won't increase and the CRC won't count the non-acked data byte. A Data Write may consist of 1,2 or more bytes.

```
Data Write (Blank/Erase)
    S-tttttt00k-aaaaaaaak-ddddddddk-P ... S-ttttttxxk-
                                  |----Min. 10mS----|

Data Write (Program)
    S-tttttt00k-aaaaaaaak-ddddddddk-ddddddddk- ...
                                  |Min. 60uS|
```

10.4 ISP Data Read

The 1st and 2nd byte are the same as "Data write" to define the Flash's low address. Between 2nd and 3rd byte, the ISP host may issue Stop-Start or only Re-Start. From the 4th byte, the ISP slave send Flash's data byte/word to ISP Host. The low address auto increase every time when data byte/word transferred.

10.5 Cyclic Redundancy Check (CRC)

To shorten the verify time, the ISP slave provide a simple way to check if data error occurs during the program data transfer. After the ISP Host send a lot of data byte to ISP slave, Host can use Command Read to check CRC register's result instead of reading every byte in Flash. The CRC register counts every data byte which ISP slave acknowledges during "Data Write" period. However, the low address byte and the data byte of Erase/Blank are not counted. The Clear CRC command will write all "1" to the 16-bit CRC register. The OSD Flash and Code share the same CRC counter. For CRC generation, the 16-bit CRC register is seeded with all "1" pattern (by device reset or Clear CRC command). The data byte shifted into the CRC register is Msb first. The real implementation is described as follows:

```
CRCin = CRC[15]^DATAin;
```

```
CRC[15:0] = {CRC[14]^CRCin, CRC[13:2], CRC[1]^CRCin, CRC[0], CRCin};
      Where ^ = XOR

example:
    data_byte   CRC_register_remainder
                      FFFFH
       F6H            FF36H
       28H            34F2H
       C3H            7031H
```

10.6 Reset Device

After the Flash been program completed and verified OK, the ISP Host can use “Command Write” with Reset_CPU command to wake up MTV230M64.

Reg name	Addr	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
ISPSLV	F0bh (w)	ISP Slave address							
ISPEN	F0ch (w)	Write 93h to enable ISP Mode							

11. On-Screen Display (OSD)

11.1 Horizontal Display control

The horizontal display control is used to generate control timing for horizontal display. The horizontal display size is based on the information of pixel clock input cycle, double width control bit (DWE), and double character width bit (CWS). The horizontal display center could be figured out according to the information of horizontal starting position register (HORD) and OSDHS input. A horizontal display line includes 360 dots for 30 display characters and the remaining dots for blank region. The horizontal delay starting from the leading edge of OSDHS is calculated with the following equation:

Horizontal delay time = (HORD * 6 +49) * P where P = one pixel display time

11.2 Vertical Display control

The vertical display control can generates different vertical display sizes for most display standards in current monitors. The vertical display size is calculated with the information of double character height bit (CHS), character vertical height control register (CH6-CH0). The algorithm of repeating character line display are shown as table below. The programmable vertical size ranges are 270 lines to maximum 2130 lines.

The vertical display center for full screen display could be figured out according to the information of vertical starting position register (VERTD) and OSDVS input. The vertical delay starting from the leading edge of OSDVS is calculated with the following equation:

Vertical delay time = (VERTD * 4 +1) * H where H = one horizontal line display time

Repeat Line Weight of Character

CH6 – CH0	Repeat Line Weight
CH6, CH5 = 11	+18*3
CH6, CH5 = 10	+18*2
CH6, CH5 = 0x	+18
CH4 = 1	+16
CH3 = 1	+8
CH2 = 1	+4
CH1 = 1	+2
CH0 = 1	+1

Repeat Line Number of character

Repeat Line Weight	Repeat Line #																	
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
+1	-	-	-	-	-	-	-	-	v	-	-	-	-	-	-	-	-	-
+2	-	-	-	-	v	-	-	-	-	-	-	-	v	-	-	-	-	-
+4	-	-	v	-	-	-	v	-	-	-	v	-	-	-	v	-	-	-
+8	-	v	-	v	-	v	-	v	-	v	-	v	-	v	-	v	-	-
+16	-	v	v	v	v	v	v	v	v	v	v	v	v	v	v	v	v	-
+17	v	v	v	v	v	v	v	v	v	v	v	v	v	v	v	v	v	-
+18	v	v	v	v	v	v	v	v	v	v	v	v	v	v	v	v	v	v

Note: “v” means the nth line in the character would be repeated once, while “-“ means the nth line in the character would not be repeated.

11.3 Display RAM

The display RAM contains character address, attribute and row control registers. The display registers have 450 locations which are allocated between (row 0, column 0) to (row14, column 29). Each display register has its corresponding character address on ADDRESS bytes, and its corresponding color, blink bit, background color on ATTRIBUTE bytes. The row control register is allocated at column 30 from row 0 to row 14 of address bytes. It is used to set character size to each respective row. If double width character is chosen, only even column characters could be displayed on screen and the odd column characters will be hidden.

There are 4 registers to program display RAM: OSDRA, OSDCA, OSDDT0 and OSDDT1. OSDRA is the row address; OSDCA is the column address; OSDDT0 and OSDDT1 are the programming data byte. The 2 MSB (bit 7 - bit 6) of OSDRA register are used to distinguish ADDRESS byte when they are set to “0, 0” and ATTRIBUTE byte when they are set to “0, 1”. OSDDT0 and OSDDT1 are used to differentiate the MSB (bit 8) of display characters address. The MSB (bit 8) of display characters address will be equal to ”0“ while data byte is filled into OSDDT0, or “1” while data byte is filled into OSDDT1; and OSDDT0 or OSDDT1 are the 8 LSB (bit 7 - bit 0) of display characters address.

The programming row (OSDRA) and column (OSDCA) address of display RAM will be incremented automatically when MCU continues to update OSDDT0 or OSDDT1. It is used to save the program ROM size of MCU while massive data update or full screen data change.

Since bit 8 is fixed on OSDDT0 (OSDDT1) while programming ADDRESS byte, the continued OSDDT0 (OSDDT1) will be the same bank of lower 256 fonts (upper 256 fonts) until program another data byte OSDDT1 (OSDDT0) register.

To program ADDRESS bytes and ATTRIBUTE bytes of the display RAM:

Step 1. Write data into **OSDRA** to determine the programming row address of the display RAM. And define it is the row address of ADDRESS byte (bit7-bit6 = “0, 0”) or ATTRIBUTE byte (bit7-bit6 = “0, 1”).

Step 2. Write data into **OSDCA** to determine the programming column address of the display RAM.

Step 3. Write to **OSDDT0** or **OSDDT1** the address or attribute of the character to be displayed on the screen.

Step 4. Post increment operation is executed in the OSDCA (i.e. OSDCA ← OSDCA + 1) to make it point to the next display RAM location. Overflow of the OSDCA, i.e. overflow from 31, makes itself return to 0 and makes post increment operation executed in the OSDRA (i.e. OSDRA ← OSDRA + 1). Overflow of the OSDRA, i.e. overflow from 15, makes itself return to 0.

It is the step 3 which triggers the load of OSDDT0 or OSDDT1 into the current OSDRA, OSDCA address of the display RAM and the post increment operation. Furthermore, the undefined locations in the display RAM should be filled with dummy data while post increment operation is executed.

So there are three transmission formats shown as below:
Format (a) R-C-D->R-C-D->R-C-D…
Format (b) R-C-D->C-D->C-D->C-D…
Format (c) R-C-D->D->D->D->D…
Where R=OSDRA (row address), C=OSDCA (column address), D=OSDDT0 or OSDDT1 (display data)

Format (a) is suitable for updating small amount of data which will be allocated with different row address and

column address. Format (b) is recommended for updating data that has same row address but different column address. Massive data updating or full screen data change should use format (c) to increase transmission efficiency. The row and column address will be incremented automatically when the format (c) is applied.

The Configuration of Transmission Formats

	Address	b7	b6	b5	b4	b3	b2	b1	b0
ADDRESS Bytes of Display Reg.	OSDRA (row address)	0	0	-	-	R3	R2	R1	R0
	OSDCA (column address)	-	-	-	C4	C3	C2	C1	C0
	OSDDT0 (data, b8=0)	D7	D6	D5	D4	D3	D2	D1	D0
	OSDDT1 ()	D7	D6	D5	D4	D3	D2	D1	D0
ATTRIBUTE Bytes of Display Reg.	OSDRA (row address)	0	1	-	-	R3	R2	R1	R0
	OSDCA (column address)	-	-	-	C4	C3	C2	C1	C0
	OSDDT0 (data, b8=0)	D7	D6	D5	D4	D3	D2	D1	D0
	OSDDT1 (data, b8=1)	D7	D6	D5	D4	D3	D2	D1	D0

ADDRESS Bytes of the Display RAM

Row # (OSDRA)	**Column # (OSDCA)**		
	0 1 ... 28 29	30	31
0 1 13 14	Character ADDRESS of the Display RAM	ROW CTRL REG	R E S E R V E D

ATTRIBUTE Bytes of the Display RAM

Row # (OSDRA)	**Column # (OSDCA)**	
	0 1 ... 28 29	30 31
0 1 13 14	Character ATTRIBUTE of the Display RAM	RESERVED

ADDRESS bytes:

Display characters address (OSDRA 0 ~ 14, OSDCA 0 ~ 29),

B8	B7	B6	B5	B4	B3	B2	B1	B0
CRADDR MSB								LSB

CRADDR : Define Flash-ROM OSD character address from address 0 to 511.
(a) 0 ~ 479 => 480 standard fonts.
(b) 480 ~ 511 => 32 multi-color fonts.

Row control registers (OSDRA 0 ~ 14, OSDCA 30),

B7	B6	B5	B4	B3	B2	B1	B0
-	-	-	-	-	RINT	CHS	CWS

RINT : The displayed character/symbol foreground color intensity control to the respective row. Setting this bit to “0” means low intensity in this row. 15 character foreground color is achievable by this bit.
CHS : Define double height character to the respective row.
CWS : Define double width character to the respective row. If double width character is chosen, only even column characters could be displayed on screen and the odd column characters will be hidden.

ATTRIBUTE bytes:
Display character attribute (OSDRA 0 ~ 14, OSDCA 0 ~ 29),

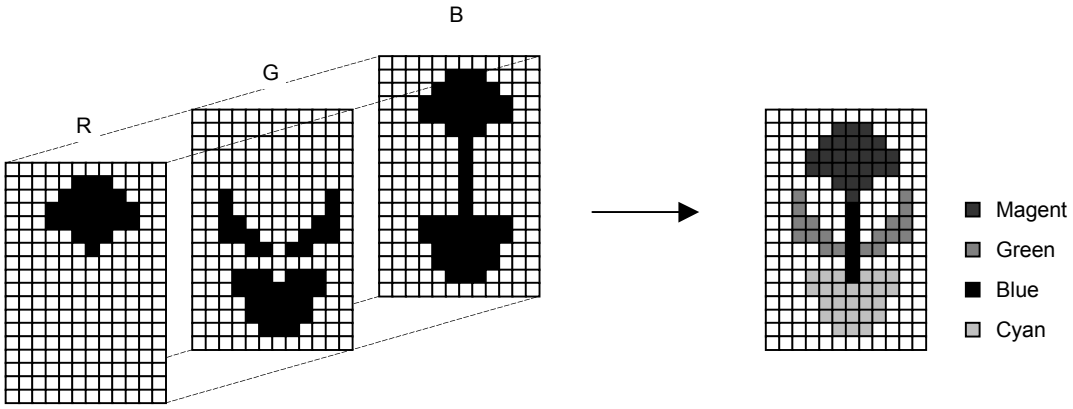
B7	B6	B5	B4	B3	B2	B1	B0
-	BGR	BGG	BGB	BLINK	R	G	B

BGR, BGG, BGB : These three bits define the background color for its relative address character. If these three bits are set to (0, 0, 0), no background will be shown (transparent).Therefore, total 7 background color can be selected.

BLINK = 1 → Enable blink effect for its relative address character. And the blinking is alternate per 32 vertical frames.
= 0 → Disable blink effect for its relative address character.
R, G, B : These three bits are used to specify its relative address character color.

11.4 Character Flash-ROM
MTV230M64 character flash-ROM contains 512 characters and symbols including 480 standard fonts and 32 multi-color fonts. The 480 standard fonts are located from character address 0 to 479. And the multi-color fonts are located from character address 480 to 511. Each character and symbol consists of 12x18 dots matrix. The MTV230M64 font edit tools can be used to design the 512 characters and symbols by software.

11.5 Multi-color Font
The color fonts comprise three different R, G, B fonts. When the code of color font is accessed, the separate R/G/B dot pattern is output to corresponding R/G/B output. See figure below for the sample displayed color font.
Note: No black color can defined in color font, black window or background underline the color font can make the dots become black in color.



Example of Multi-color Font

The Multi-color Font Color Selection

	R	G	B
Background Color	0	0	0
Blue	0	0	1
Green	0	1	0
Cyan	0	1	1
Red	1	0	0

Magent	1	0	1
Yellow	1	1	0
White	1	1	1

11.6 Luminance & Border Generator

There are 3 shift registers included in the design which can shift out of luminance and border dots to color encoder. The bordering and shadowing feature is configured in this block. For bordering effect, the character will be enveloped with blackedge on four sides. For shadowing effect, the character is enveloped with blackedge for right and bottom sides only.

11.7 Window Control

The window size and position controls are specified in W1ROW, W1COL, W2ROW, W2COL, W3ROW, W3COL, W4ROW and W4COL registers. And window 1 has the highest priority, and window 4 has the least, when two windows are overlapping.

The window shadow width and height controls are specified in WINSW and WINSH registers. And each shadow has the same priority with its corresponding window.

11.8 OSD Processor registers

Reg name	Addr	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
OSDRA	FA0h (w)	A1	A0	-	-	R3	R2	R1	R0
OSDCA	FA1h (w)	-	-	-	C4	C3	C2	C1	C0
OSDDT0	FA2h (w)	D7	D6	D5	D4	D3	D2	D1	D0
OSDDT1	FA3h (w)	D7	D6	D5	D4	D3	D2	D1	D0
W1ROW	FC0h (w)	Row start address				Row end address			
W1COL	FC1h (w)	Column start address					WEN	WINT	WSHD
W1COL	FC2h (w)	Column end address					R	G	B
W2ROW	FC3h (w)	Row start address				Row end address			
W2COL	FC4h (w)	Column start address					WEN	WINT	WSHD
W2COL	FC5h (w)	Column end address					R	G	B
W3ROW	FC6h (w)	Row start address				Row end address			
W3COL	FC7h (w)	Column start address					WEN	WINT	WSHD
W3COL	FC8h (w)	Column end address					R	G	B
W4ROW	FC9h (w)	Row start address				Row end address			
W4COL	FCAh (w)	Column start address					WEN	-	WSHD
W4COL	FCBh (w)	Column end address					R	G	B
VERTD	FCCh (w)	Vertical delay							
HORD	FCDh (w)	Horizontal delay							
CH	FCEh (w)	-	Character height						
RSPACE	FD0h (w)	-	-	-	Row to row spacing				
OSDCON	FD1h (r/w)	OSDEN	BSEN	Shadow	FBEN	Blend	WENclr	RAMclr	FBKGC
OSDCON	FD2h (r/w)	-	-	-	DWE	HSP	VSP	-	-
CHSC	FD3h (w)						CSR	CSG	CSB
FSSTP	FD4h (w)	FSW	-	-	-	-	FSR	FSG	FSB
WINSW	FD5h (w)	WW41	WW40	WW31	WW30	WW21	WW20	WW11	WW10
WINSH	FD6h (w)	WH41	WH40	WH31	WH30	WH21	WH20	WH11	WH10
WINSC	FD7h (w)	-	R1	G1	B1	-	R2	G2	B2
WINSC	FD8h (w)	-	R3	G3	B3	-	R4	G4	B4
XDEL	FD9h (w)	-	-	-	-	-	D2	D1	D0

OSDRA (w) :

R3-R0 : This is the row address of the display RAM that next 9-bit data should be written into.

A1-A0 = (0, 0) → Next 9-bit data will be written into ADDRESS byte.
= (0, 1) → Next 9-bit data will be written into ATTRIBUTE byte.

OSDCA (w) : This is the column address of the display RAM that next 9-bit data should be written into.

OSDDT0 (w) : The MSB (bit 8) = 0, 8 LSB (bit 7 ~ bit 0) = OSDDT0. The 9-bit data will be written into current (OSDRA, OSDCA) address of the display RAM. It will also trigger the post increment operation of OSDRA and OSDCA.

OSDDT1 (w) : The MSB (bit 8) = 1, 8 LSB (bit 7 ~ bit 0) = OSDDT1. The 9-bit data will be written into current (OSDRA, OSDCA) address of the display RAM. It will also trigger the post increment operation of OSDRA and OSDCA.

W1ROW, **W1COL** (w) : Window 1 control registers.
Row (column) start (end) address : These registers are used to specify the window 1 size. It should be noted that when the start address is greater than end address, the corresponding window display will be disabled.
WEN : Enable the relative background window 1 display.
WINT : Specify the color intensity of the background window 1. Setting this bit to “0” means low intensity.
WSHD : Enable shadowing on the window 1.
R, G, B : Specify the color of the relative background window 1.

W2ROW, **W2COL** (w) : Window 2 control registers.
Row (column) start (end) address : These registers are used to specify the window 2 size.
WEN : Enable the relative background window 2 display.
WINT : Specify the color intensity of the background window 2. Setting this bit to “0” means low intensity.
WSHD : Enable shadowing on the window 2.
R, G, B : Specify the color of the relative background window 2.

W3ROW, **W3COL** (w) : Window 3 control registers.
Row (column) start (end) address : These registers are used to specify the window 3 size.
WEN : Enable the relative background window 3 display.
WINT : Specify the color intensity of the background window 3. Setting this bit to “0” means low intensity.
WSHD : Enable shadowing on the window 3.
R, G, B : Specify the color of the relative background window 3.

W4ROW, **W4COL** (w) : Window 4 control registers.
Row (column) start (end) address : These registers are used to specify the window 4 size.
WEN : Enable the relative background window 4 display.
WINT : Specify the color intensity of the background window 4. Setting this bit to “0” means low intensity.
WSHD : Enable shadowing on the window 4.
R, G, B : Specify the color of the relative background window 4.

VERTD (w) : Specify the starting position for vertical display. The total steps are 256, and the increment of each step is 4 horizontal display lines. The starting position is calculated as (VERTD*4 + 1) horizontal display lines. The initial value is 4 after power up.

HORD (w) : Specify the starting position for horizontal display. The total steps are 256, and the increment of each step is 6 dots. The starting position is calculated as (HORD*6 + 49) horizontal display dots. The initial value is 15 after power up.

CH (w) : Define the character vertical height, the height is programmable from 18 to 71 lines. The

character vertical height is at least 18 lines if the content of CH6-CH0 is less than 18. For example, when the content is “2”, the character vertical height is regarded as equal to 20 lines. And if the content of CH4-CH0 is greater than or equal to 18, it will be regarded as equal to 17. See table list in section 11.1 for detail description of this operation.

RSPACE (w) : Define the row to row spacing in unit of horizontal line. Extra RSPACE horizontal lines will be appended below each display row, and the maximum space is 31 lines. The initial value is 0 after power up.

OSDCON (r/w) : OSD control registers.

OSDEN = 1 → Activate the OSD operation.
= 0 → Disable the OSD operation.
BSEN = 1 → Enable the character bordering or shadowing effect.
= 0 → Disable bordering and shadowing effect.
Shadow = 1 → Select the character shadowing effect if BSEN bit is set to “1”.
= 0 → Select the character bordering effect if BSEN bit is set to “1”.
FBEN = 1 → Enable the fade-in/fade-out or blending-in/blending-out effect when OSD is turned on from off state or vice versa.
= 0 → Disable the fade-in/fade-out and blending-in/blending-out effect.
Blend = 1 → Select the blending-in/blending-out effect if FBEN bit is set to “1”.
= 0 → Select the fade-in/fade-out effect if FBEN bit is set to “1”.
WENclr = 1 → Clear all WEN bits of window control registers.
= 0 → Normal.
RAMclr = 1 → Clear all ADDRESS bytes, BGR, BGG, BGB and BLINK bits of display RAM.
= 0 → Normal.
FBKGC = 1 → Pin FBKG outputs high only during the displaying of characters.
= 0 → Pin FBKG outputs high during the displaying of characters or windows.
DWE = 1 → Enable double width. The OSD menu will change to half resolution for double character width. And the number of pixels of each line should be even.
= 0 → Normal.
HSP = 1 → Accept positive polarity OSDHS input.
= 0 → Accept negative polarity OSDHS input.
VSP = 1 → Accept positive polarity OSDVS input.
= 0 → Accept negative polarity OSDVS input.

CHSC (w) : Character shadow color select registers.
CSR, CSG, CSB : Define the color of bordering or shadowing color on characters.

FSSTP (w) : Full screen self-test pattern registers.
FSW = 1 → Enable full screen self-test pattern and force pin FBKG outputs high to disable video RGB.
= 0 → Disable full screen self-test pattern.
FSR, FSG, FSB : Define the color of full screen self-test pattern.

WINSW (w) : Window shadowing width control registers.
WW41, WW40 : Determines the shadow width of window 4 when WSHD bit of window 4 is enabled. Please refer to the table below for more details.

(WW41, WW40)	(0, 0)	(0, 1)	(1, 0)	(1, 1)
Shadow Width (unit in Pixel)	2	4	6	8

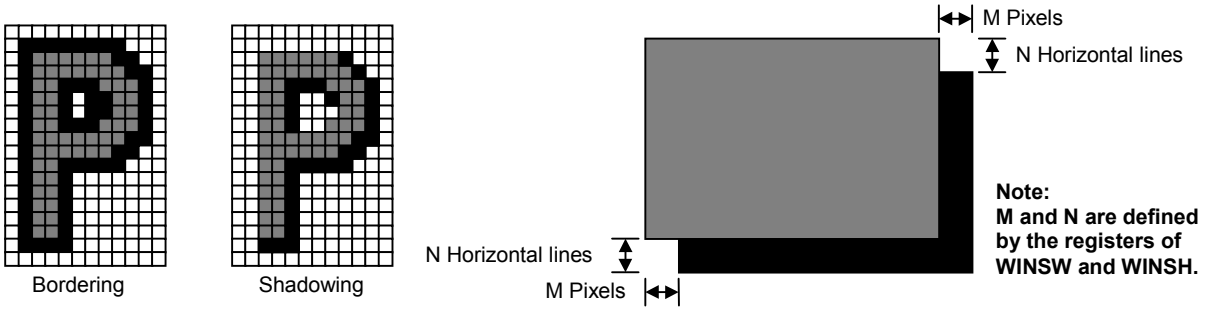
WW31, WW30 : Determines the shadow width of window 3 when WSHD bit of window 3 is enabled.
WW21, WW20 : Determines the shadow width of window 2 when WSHD bit of window 2 is enabled.
WW11, WW10 : Determines the shadow width of window 1 when WSHD bit of window 1 is enabled.

WINSH (w) : Window shadowing height control registers.

WH41, WH40 : Determines the shadow height of window 4 when WSHD bit of window 4 is enabled. Please refer to the table below for more details.

(WH41, WH40)	(0, 0)	(0, 1)	(1, 0)	(1, 1)
Shadow Height (unit in Line)	2	4	6	8

WH31, WH30 : Determines the shadow height of window 3 when WSHD bit of window 3 is enabled.
WH21, WH20 : Determines the shadow height of window 2 when WSHD bit of window 2 is enabled.
WH11, WH10 : Determines the shadow height of window 1 when WSHD bit of window 1 is enabled.

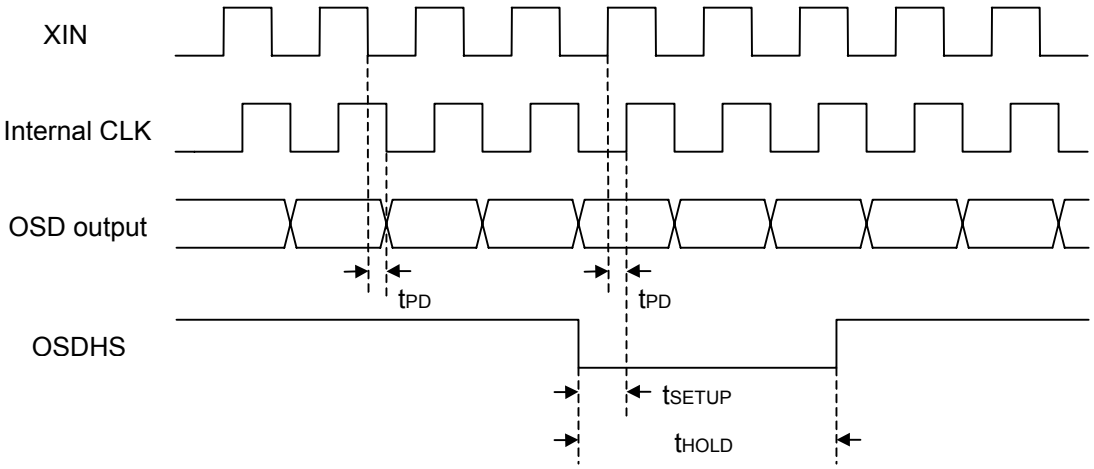


Character Bordering and Shadowing and Shadowing on Window

WINSC (w) : Window shadowing color control registers.

R1, G1, B1 : Define the shadowing color of window 1.
R2, G2, B2 : Define the shadowing color of window 2.
R3, G3, B3 : Define the shadowing color of window 3.
R4, G4, B4 : Define the shadowing color of window 4.

XDEL (w) : Rout, Gout, Bout, FBKG and INT outputs delay reference to pin XIN input falling edge control registers.



Memory Map of XFR

Reg name	addr	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
IICCTR	F00h (r/w)						MAckO	P	S
IICSTUS	F01h (r)	WadrB	WadrA	SlvRWB	SAckIn	SLVS		SlvAlsb1	SlvAlsb0
IICSTUS	F02h (r)	MAckIn							
INTFLG	F03h (r)	TXBI	RCBI	SlvBMI	TXAI	RCAI	SlvAMI		MbufI
INTFLG	F03h (w)			SlvBMI			SlvAMI		MbufI
INTEN	F04h (w)	ETXBI	ERCBI	ESlvBMI	ETXAI	ERCAI	ESlvAMI		EMbufI
MBUF	F05h (r/w)	Master IIC receive/transmit data buffer							
RCABUF	F06h (r)	Slave A IIC receive buffer							
TXABUF	F06h (w)	Slave A IIC transmit buffer							
SLVAADR	F07h (w)	ENSlvA	Slave A IIC address						
RCBBUF	F08h (r)	Slave B IIC receive buffer							
TXBBUF	F08h (w)	Slave B IIC transmit buffer							
SLVBADR	F09h (w)	ENSlvB	Slave B IIC address						
ISPSLV	F0bh (w)	ISP Slave address							
ISPEN	F0ch (w)	Write 93h to enable ISP Mode							
ADC	F10h (w)	ENADC				SADC3	SADC2	SADC1	SADC0
ADC	F10h (r)	ADC convert Result							
WDT	F18h (w)	WEN	WCLR				WDT2	WDT1	WDT0
DA0	F20h (r/w)	Pulse width of PWM DAC 0							
DA1	F21h (r/w)	Pulse width of PWM DAC 1							
DA2	F22h (r/w)	Pulse width of PWM DAC 2							
DA3	F23h (r/w)	Pulse width of PWM DAC 3							
PORT6	F28h(w)								P60
PORT6	F29h(w)								P61
PORT6	F2Ah(w)								P62
PADMOD	F2Bh (w)	HIICE	IIICE	HVE	HclpE			FclkE	P62E
PADMOD	F2Ch (w)	DA3E	DA2E	DA1E	DA0E	AD3E	AD2E	AD1E	AD0E
PADMOD	F2Dh (w)	P47oe	P46oe	P45oe	P44oe	P43oe	P42oe	P41oe	P40oe
PADMOD	F2Eh (w)	P57oe	P56oe	P55oe	P54oe	P53oe	P52oe	P51oe	P50oe
OPTION	F2Fh (w)	PWMF	DIV253	SlvAbs1	SlvAbs0	ENSCL	Msel	MIICF1	MIICF0
PORT4	F30h(r/w)								P40
PORT4	F31h(r/w)								P41
PORT4	F32h(r/w)								P42
PORT4	F33h(r/w)								P43
PORT4	F34h(r/w)								P44
PORT4	F35h(r/w)								P45
PORT4	F36h(r/w)								P46
PORT4	F37h(r/w)								P47
PORT5	F38h(r/w)								P50
PORT5	F39h(r/w)								P51
PORT5	F3Ah(r/w)								P52
PORT5	F3Bh(r/w)								P53
PORT5	F3Ch(r/w)								P54
PORT5	F3Dh(r/w)								P55
PORT5	F3Eh(r/w)								P56
PORT5	F3Fh(r/w)								P57
HVSTUS	F40h (r)	CVpre		Hpol	Vpol	Hpre	Vpre	Hoff	Voff
HCNTH	F41h (r)	Hovf		HF13	HF12	HF11	HF10	HF9	HF8
HCNTL	F42h (r)	HF7	HF6	HF5	HF4	HF3	HF2	HF1	HF0

VCNTH	F43h (r)	Vovf				VF11	VF10	VF9	VF8
VCNTL	F44h (r)	VF7	VF6	VF5	VF4	VF3	VF2	VF1	VF0
HVCTR0	F40h (w)	C1	C0	NoHins				HBpl	VBpl
HVCTR3	F43h (w)		CLPEG	CLPPO	CLPW2	CLPW1	CLPW0		
INTFLG	F48h (r/w)	HPRchg	VPRchg	HPLchg	VPLchg	HFchg	VFchg		Vsync
INTEN	F49h (w)	EHPR	EVPR	EHPL	EVPL	EHF	EVF		EVsync
OSDRA	FA0h (w)	A2	A1	A0	-	R3	R2	R1	R0
OSDCA	FA1h (w)	-	-	-	C4	C3	C2	C1	C0
OSDDT0	FA2h (w)	D7	D6	D5	D4	D3	D2	D1	D0
OSDDT1	FA3h (w)	D7	D6	D5	D4	D3	D2	D1	D0
W1ROW	FC0h (w)	Row start address				Row end address			
W1COL	FC1h (w)	Column start address					WEN	-	WSHD
W1COL	FC2h (w)	Column end address					R	G	B
W2ROW	FC3h (w)	Row start address				Row end address			
W2COL	FC4h (w)	Column start address					WEN	-	WSHD
W2COL	FC5h (w)	Column end address					R	G	B
W3ROW	FC6h (w)	Row start address				Row end address			
W3COL	FC7h (w)	Column start address					WEN	-	WSHD
W3COL	FC8h (w)	Column end address					R	G	B
W4ROW	FC9h (w)	Row start address				Row end address			
W4COL	FCAh (w)	Column start address					WEN	-	WSHD
W4COL	FCBh (w)	Column end address					R	G	B
VERTD	FCCh (w)	Vertical delay							
HORD	FCDh (w)	Horizontal delay							
CH	FCEh (w)	-	Character height						
RSPACE	FD0h (w)	-	-	-	Row to row spacing				
OSDCON	FD1h (r/w)	OSDEN	BSEN	Shadow	FBEN	Blend	WENclr	RAMclr	FBKGC
OSDCON	FD2h (r/w)	-	-	-	DWE	HSP	VSP	-	-
CHSC	FD3h (w)						CSR	CSG	CSB
FSSTP	FD4h (w)	FSW	-	-	-	-	FSR	FSG	FSB
WINSW	FD5h (w)	WW41	WW40	WW31	WW30	WW21	WW20	WW11	WW10
WINSH	FD6h (w)	WH41	WH40	WH31	WH30	WH21	WH20	WH11	WH10
WINSC	FD7h (w)	-	R1	G1	B1	-	R2	G2	B2
WINSC	FD8h (w)	-	R3	G3	B3	-	R4	G4	B4
XDEL	FD9h (w)	-	-	-	-	D3	D2	D1	D0

Test Mode Condition

In normal application, users should avoid the MTV230M64 entering its test mode, outlined as follow:

Test Mode A: RESET=1 & P5.7=1 & P5.6=0 & P5.5=1 & P5.4=0
Test Mode B: RESET's falling edge & P5.7=0 & & P5.6=1 & P5.5=1 & P5.4=0
Writer Mode: RESET=1 & P5.5=0 & P5.4=1 & "special serial data on OSDVS"

ELECTRICAL PARAMETERS

1. Absolute Maximum Ratings

at: Ta= 0 to 70 °C, VSS=0V

Name	Symbol	Range	Unit
Maximum Supply Voltage	VDD	-0.3 to +4.0	V
Maximum Input Voltage	Vin	-0.3 to VDD+0.3	V
Maximum Output Voltage	Vout	-0.3 to VDD+0.3	V
Maximum Operating Temperature	Topg	0 to +70	°C
Maximum Storage Temperature	Tstg	-25 to +125	°C

2. Allowable Operating Conditions

at: Ta= 0 to 70 °C, VSS=0V

Name	Symbol	Min.	Max.	Unit
Supply Voltage	VDD	3.0	3.6	V
Input "H" Voltage	Vih1	0.7 x VDD	VDD +0.3	V
Input "L" Voltage	Vil1	-0.3	0.25 x VDD	V
Operating Freq.	Fopg	-	15	MHz

3. DC Characteristics

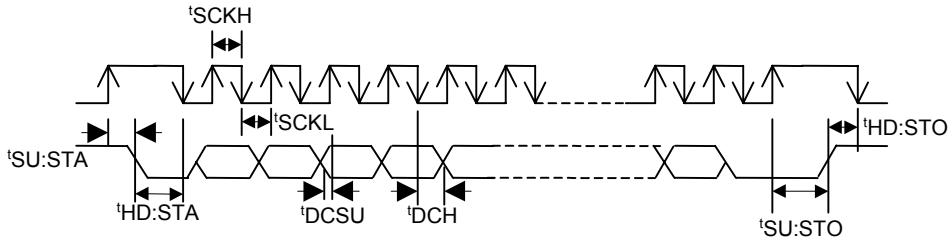
At: Ta=0 to 70℃, VDD=5.0V, VSS=0V

Name	Symbol	Condition	Min.	Typ.	Max.	Unit
Output “H” voltage, open drain pin	Voh1	Ioh=0uA	2.7			V
Output “H” voltage, 8051 I/O port pin	Voh2	Ioh2=-50uA	2.7			V
Output “H” voltage, CMOS	Voh3	Ioh=-5mA	2.7			V
Output “L” voltage	Vol	Iol=8mA			0.4	V
Power supply current	Idd	Active		18	4	mA
		Idle		1.3	4.0	mA
		Power-down		50	80	uA
RST pull-down resistor	Rrst	VDD=3.3V	100		250	Kohm
Pin capacitance	Cio				15	pF

4. AC Characteristics

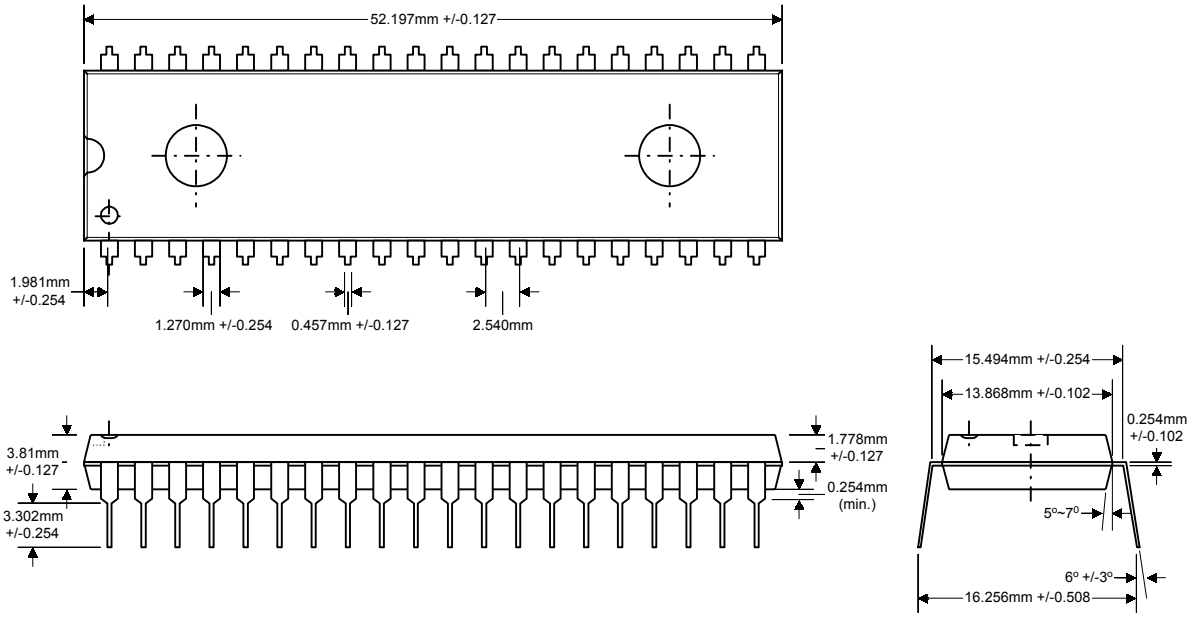
At: Ta=0 to 70℃, VDD=5.0V, VSS=0V

Name	Symbol	Condition	Min.	Typ.	Max.	Unit
Crystal frequency	fXtal			12		MHz
PWM DAC Frequency	fDA	fXtal=12MHz	46.875		94.86	KHz
HS input pulse Width	tHIPW	fXtal=12MHz	0.3		8	uS
VS input pulse Width	tVIPW	fXtal=12MHz	3			uS
H+V to Vblank Output Delay	tWBD	fXtal=12MHz		8		uS
VS pulse Width in H+V Signal	tVCPW	fXtal=12MHz	20			uS
SDA to SCL Setup Time	tDCSU		200			ns
SDA to SCL Hold Time	tDCH		100			ns
SCL High Time	tSCLH		500			ns
SCL Low Time	tSCLL		500			ns
START condition Setup Time	tSU:STA		500			ns
START condition Hold Time	tHD:STA		500			ns
STOP condition Setup Time	tSU:STO		500			ns
STOP condition Hold Time	tHD: STO		500			ns

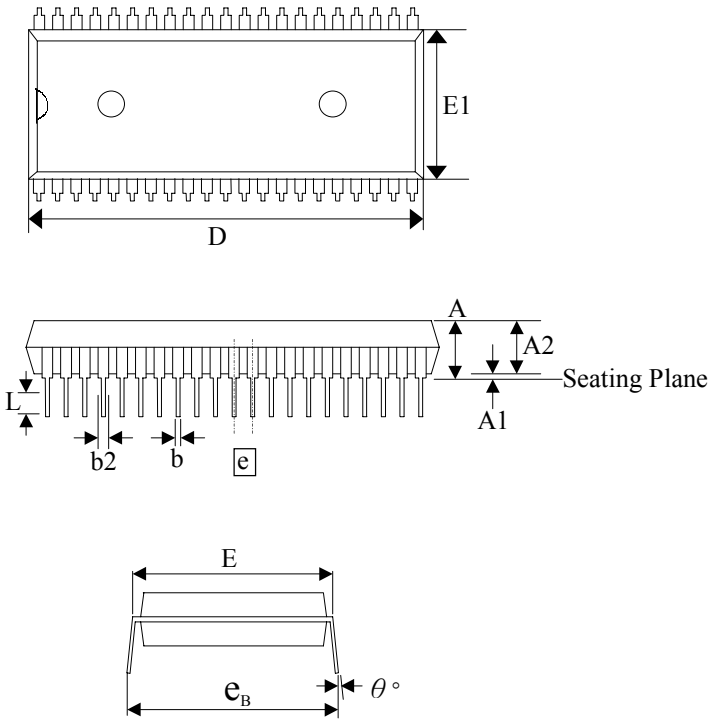

tSCKH
tSCKL
tHD:STO
tSU:STA
tHD:STA
tDCSU
tDCH
tSU:STO

PACKAGE DIMENSION

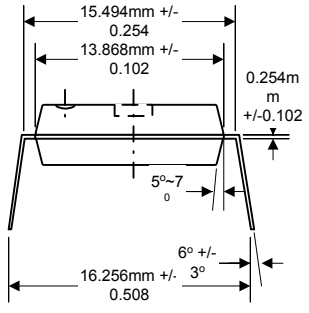
1. 40-pin PDIP 600 mil



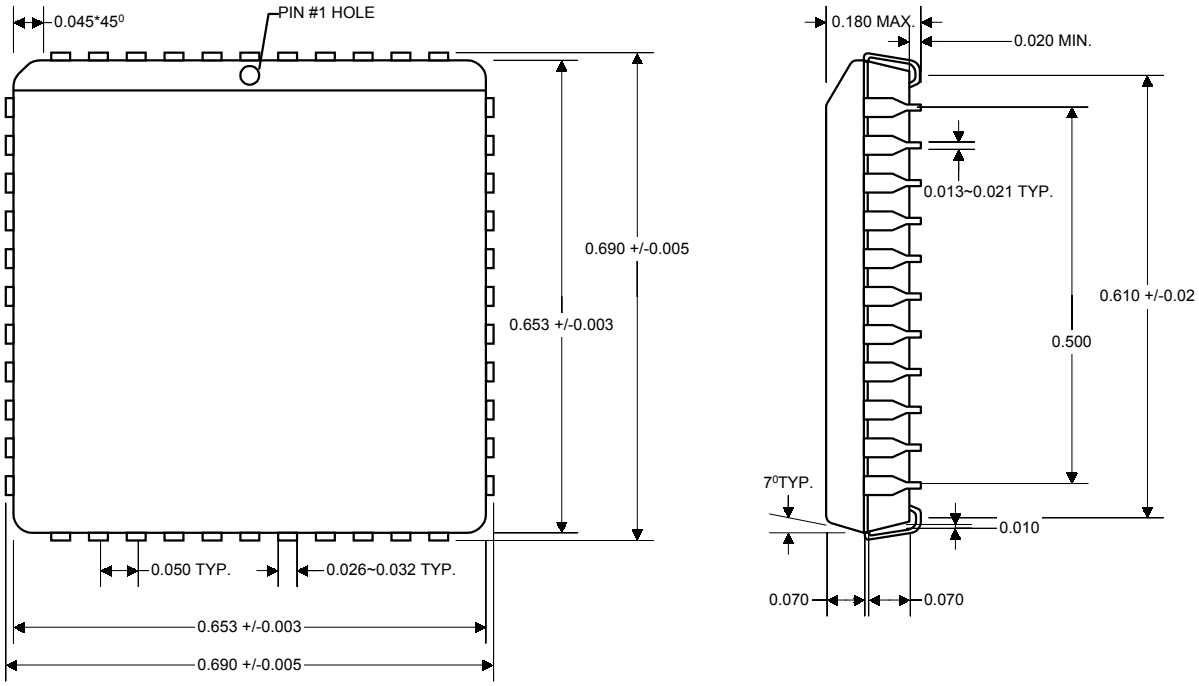
2. 42 pin SDIP



Symbol	Dimension in Inch		
	Min	Nor.	Max
A	--	--	0.200
A1	0.015	--	--
A2	0.120	0.150	0.180
D	1.44	1.45	1.46
E	0.600	--	0.630
E1	0.500	0.540	0.570
L	0.100	0.130	0.140
eB	--	--	0.730
e	0.070 BSC.		
b	0.014	0.018	0.022
b2	0.030	0.040	0.045
θ	0°	7.5°	15°



3. 44 pin PLCC Unit:



Ordering Information

Standard configurations:

Prefix	Part Type	Package Type	ROM Size (K)
MTV	230M64	S : SDIP V : PLCC F: QFP	64

Part Numbers:

Prefix	Part Type	Package Type	ROM Size (K)
MTV	230M64	S	64
MTV	230M64	V	64
MTV	230M64	F	64