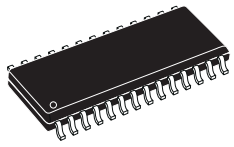
# STA003T

## MPEG 2.5 LAYER III AUDIO DECODER

- SINGLE CHIP MPEG2 LAYER 3 DECODER SUPPORTING:
  - All features specified for Layer III in ISO/IEC 11172-3 (MPEG 1 Audio) except 44.1KHz Audio
  - All features specified for Layer III 2 channels in ISO/IEC13818-3.2 (MPEG 2 Audio) except 22.05KHz Audio
  - Lower sampling frequencies syntax extension, (not specified by ISO) called MPEG 2.5 except 11.025KHz Audio
- DECODES LAYER III STEREO CHANNELS, DUAL CHANNEL, SINGLE CHANNEL (MONO)
- SUPPORTING THE MPEG 1 & 2 SAMPLING FREQUENCIES AND THE EXTENSION TO MPEG 2.5:
  48, 32, 24, 16, 12, 8 KHz
- ACCEPTS MPEG 2.5 LAYER III ELEMENTARY COMPRESSED BITSTREAM WITH DATA RATE FROM 8 Kbit/s UP TO 128 Kbit/s
- DIGITAL VOLUME CONTROL
- DIGITAL BASS & TREBLE CONTROL
- SERIAL BITSTREAM INPUT INTERFACE
- ANCILLARY DATA EXTRACTION VIA I2C INTERFACE.
- SERIAL PCM OUTPUT INTERFACE ($I^2S$ AND OTHER FORMATS)
- PLL FOR INTERNAL CLOCK AND FOR OUTPUT PCM CLOCK GENERATION
- LOW POWER DATA ELABORATION FOR POWER CONSUMPTION OPTIMISATION
- CRC CHECK AND SYNCHRONISATION ERROR DETECTION WITH SOFTWARE INDICATORS
- $I^2C$ CONTROL BUS
- LOW POWER 3.3V CMOS TECHNOLOGY
- 14.72MHz EXTERNAL INPUT CLOCK OR BUILT-IN XTAL OSCILLATOR



**SO28**

### APPLICATIONS

- STARMAN SATELLITE RADIO RECEIVER

### DESCRIPTION

The STA003T is a fully integrated high flexibility MPEG Layer III Audio Decoder, capable of decoding Layer III compressed elementary streams, as specified in MPEG 1 and MPEG 2 ISO standards. The device decodes also elementary streams compressed by using low sampling rates, as specified by MPEG 2.5.

STA003T receives the input data through a Serial Input Interface. The decoded signal is a stereo, mono, or dual channel digital output that can be sent directly to a D/A converter, by the PCM Output Interface. This interface is software programmable to adapt the STA003T digital output to the most common DACs architectures used on the market.

The functional STA003T chip partitioning is described in Fig.1.

**Figure 1.** BLOCK DIAGRAM: MPEG 2.5 Layer III Decoder Hardware Partitioning.

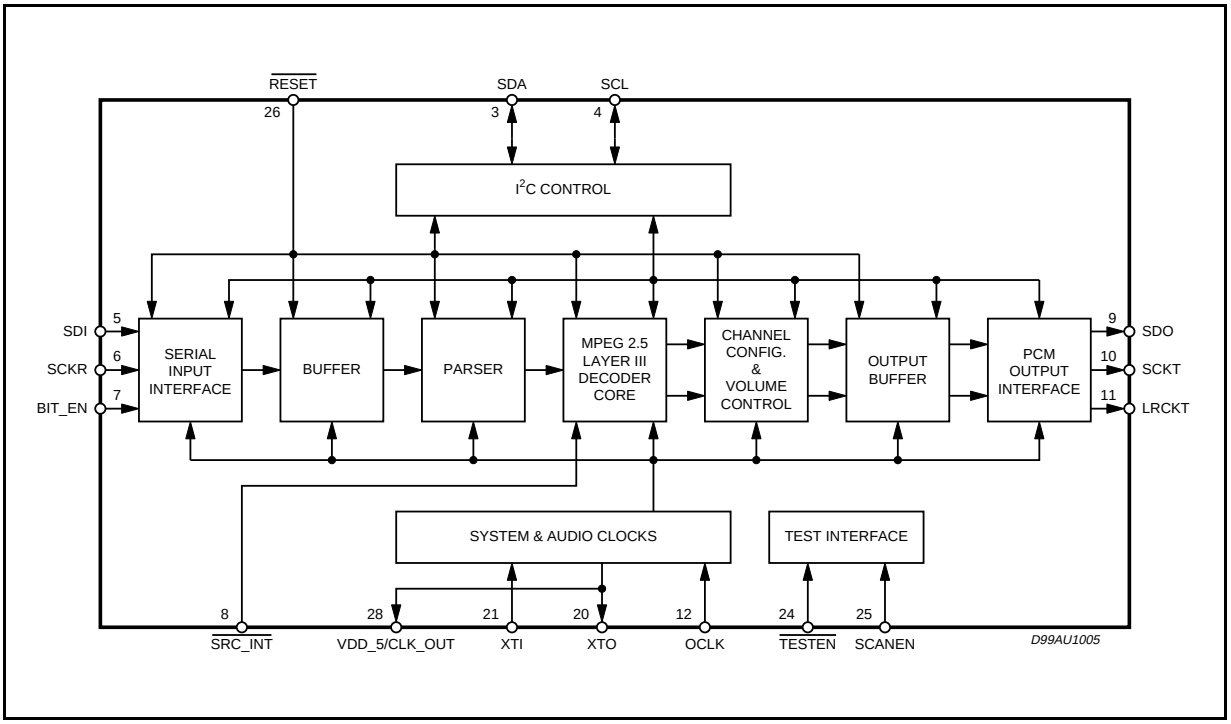



**Figure 2.** PIN CONNECTION

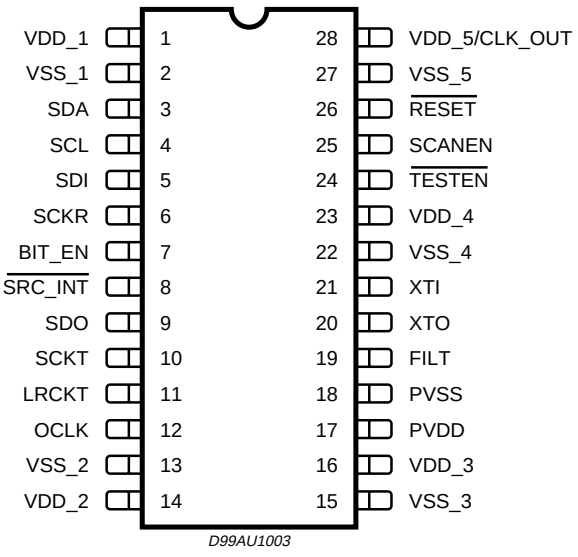



Fig. 2 describes the STA003T pinout in SO28 package

## THERMAL DATA

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $R_{th\ j\text{-}amb}$ | Thermal resistance Junction to Ambient | 85 | °C/W |

## PIN DESCRIPTION

| Type | Pin Name | Type | Function | PAD Description |
|---|---|---|---|---|
| 1 | VDD_1 | | Supply Voltage | |
| 2 | VSS_1 | | Ground | |
| 3 | SDA | I/O | $I^2C$ Serial Data + Acknowledge | CMOS Input Pad Buffer<br>CMOS 4mA Output Drive |
| 4 | SCL | I | $I^2C$ Serial Clock | CMOS Input Pad Buffer |
| 5 | SDI | I | Receiver Serial Data | CMOS Input Pad Buffer |
| 6 | SCKR | I | Receiver Serial Clock | CMOS Input Pad Buffer |
| 7 | BIT_EN | I | Bit Enable | CMOS Input Pad Buffer with pull up |
| 8 | SRC_INT | I | Interrupt Line For S.R. Control | CMOS Input Pad Buffer |
| 9 | SDO | O | Transmitter Serial Data (PCM Data) | CMOS 4mA Output Drive |
| 10 | SCKT | O | Transmitter Serial Clock | CMOS 4mA Output Drive |
| 11 | LRCLKT | O | Transmitter Left/Right Clock | CMOS 4mA Output Drive |
| 12 | OCLK | I/O | Oversampling Clock for DAC | CMOS Input Pad Buffer<br>CMOS 4mA Output Drive |
| 13 | VSS_2 | | Ground | |
| 14 | VDD_2 | | Supply Voltage | |
| 15 | VSS_3 | | Ground | |
| 16 | VDD_3 | | Supply Voltage | |
| 17 | PVDD | | PLL Power | |
| 18 | PVSS | | PLL Ground | |
| 19 | FILT | O | PLL Filter Ext. Capacitor Conn. | |
| 20 | XTO | O | Crystal Output | CMOS 4mA Output Drive |
| 21 | XTI | I | Crystal Input (Clock Input) | Specific Level Input Pad (see paragraph 2.1) |
| 22 | VSS_4 | | Ground | |
| 23 | VDD_4 | | Supply Voltage | |
| 24 | TESTEN | I | Test Enable | CMOS Input Pad Buffer with pull up |
| 25 | SCANEN | I | Scan Enable | CMOS Input Pad Buffer |
| 26 | RESET | I | System Reset | CMOS Input Pad Buffer with pull up |
| 27 | VSS_5 | | Ground | |
| 28 | VDD_5/CLK_OUT | | Power/14.72MHz Buffered Output Clock | CMOS 4mA Output Drive |

**Note:** In functional mode TESTEN must be connected to VDD, SCANEN to ground.

## ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$ | Power Supply | -0.3 to 4 | V |
| $V_i$ | Voltage on Input pins | -0.3 to $V_{DD}$ +0.3 | V |
| $V_O$ | Voltage on output pins | -0.3 to $V_{DD}$ +0.3 | V |
| $T_{stg}$ | Storage Temperature | -40 to +150 | °C |
| $T_{oper}$ | Operative ambient temp | -20 to +85 | °C |

**1. ELECTRICAL CHARACTERISTICS:** $V_{DD}$ = 3.3V ±0.3V; $T_{amb}$ = 0 to 70°C; Rg = 50Ω unless otherwise specified

## DC OPERATING CONDITIONS

| Symbol | Parameter | Value |
|---|---|---|
| $V_{DD}$ | Power Supply Voltage | 2.7 to 3.6V |
| $T_j$ | Operating Junction Temperature | -20 to 125°C |

## GENERAL INTERFACE ELECTRICAL CHARACTERISTICS

| Symbol | Parameter | Test Condition | Min. | Typ. | Max. | Unit | Note |
|---|---|---|---|---|---|---|---|
| $I_{IL}$ | Low Level Input Current Without pull-up device | $V_i$ = 0V | -10 | | 10 | µA | 1 |
| $I_{IH}$ | High Level Input Current Without pull-up device | $V_i = V_{DD}$ | -10 | | 10 | µA | 1 |
| $V_{esd}$ | Electrostatic Protection | Leakage < 1µA | 2000 | | | V | 2 |

**Note 1:** The leakage currents are generally very small, < 1nA. The value given here is a maximum that can occur after an electrostatic stress on the pin.
**Note 2:** Human Body Model.

## DC ELECTRICAL CHARACTERISTICS

| Symbol | Parameter | Test Condition | Min. | Typ. | Max. | Unit | Note |
|---|---|---|---|---|---|---|---|
| $V_{IL}$ | Low Level Input Voltage | | | | $0.2*V_{DD}$ | V | |
| $V_{IH}$ | High Level Input Voltage | | $0.8*V_{DD}$ | | | V | |
| $V_{ol}$ | Low Level Output Voltage | $I_{ol}$ = Xma | | | 0.4V | V | 1, 2 |
| $V_{oh}$ | High Level Output Voltage | | $0.85*V_{DD}$ | | | V | 1, 2 |

**Note 1:** Takes into account 200mV voltage drop in both supply lines.
**Note 2:** X is the source/sink current under worst case conditions and is reflected in the name of the I/O cell according to the drive capability.

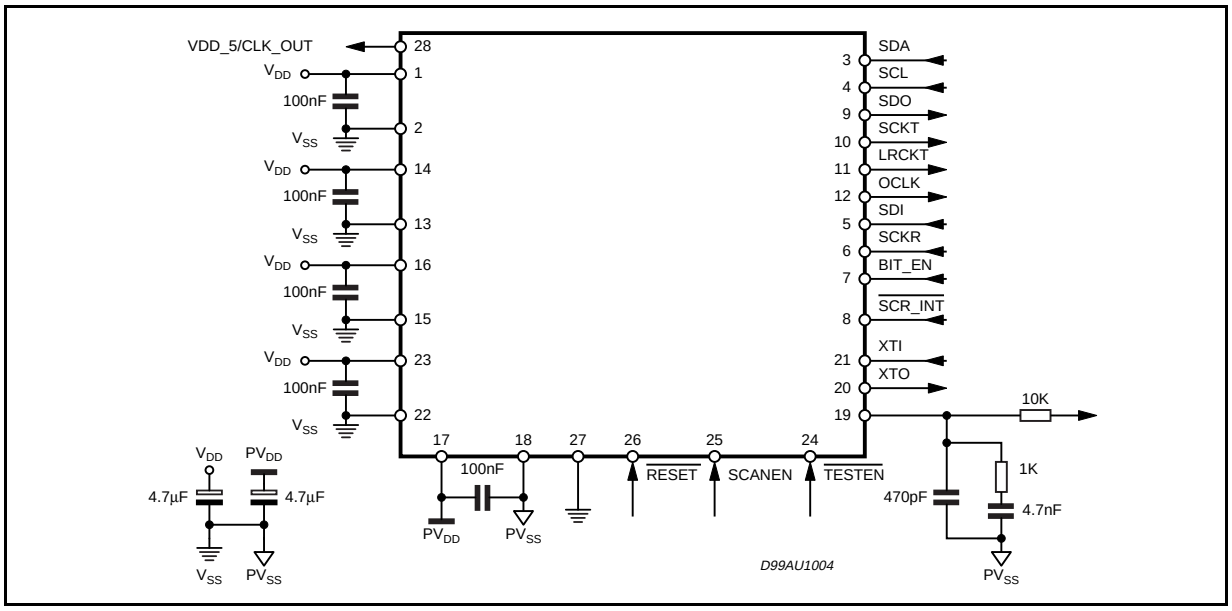
| Symbol | Parameter | Test Condition | Min. | Typ. | Max. | Unit | Note |
|---|---|---|---|---|---|---|---|
| $I_{pu}$ | Pull-up current | $V_i$ = 0V; pin numbers 7, 24 and 26 | -25 | -66 | -125 | µA | 1 |
| $R_{pu}$ | Equivalent Pull-up Resistance | | | 50 | | kΩ | |

**Note 1:** Min. condition: $V_{DD}$ = 2.7V, 125°C Min process
Max. condition: $V_{DD}$ = 3.6V, -20°C Max.

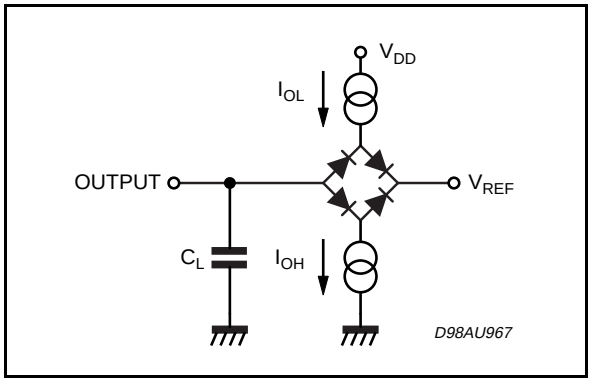
## POWER DISSIPATION

| Symbol | Parameter | Test Condition | Min. | Typ. | Max. | Unit | Note |
|---|---|---|---|---|---|---|---|
| PD | Power Dissipation @ $V_{DD}$ = 3V | Sampling_freq ≤24 kHz | | 120 | | mW | |
| | | Sampling_freq ≤32 kHz | | 125 | | mW | |
| | | Sampling_freq ≤48 kHz | | 135 | | mW | |

**Figure 3.** Test Circuit




**Test Load Circuit**




**Test Load**

| Output | $I_{OL}$ | $I_{OH}$ | $C_L$ | $V_{REF}$ |
|---|---|---|---|---|
| SDA | 1mA | | 100pF | 3.6V |
| Other Outputs | 100µA | 100µA | 100pF | 1.5V |
| | | | | |

## 2. FUNCTIONAL DESCRIPTION

### 2.1 - Clock Signal

The STA003T input clock is derivated from an external source or from a 14.72 MHz crystal.

XTI is an input Pad with specific levels.

| Symbol | Parameter | Test Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{IL}$ | Low Level Input Voltage | | | | $V_{DD}$-1.8 | V |
| $V_{IH}$ | High Level Input Voltage | | $V_{DD}$-0.8 | | | V |

CMOS compatibility

The XTI pad low and high levels are CMOS compatible; XTI pad noise margin is better than typical CMOS pads.

TTL compatibility

The XTI pad low level is compatible with TTL while the high level is not compatible (for example if $V_{DD}$ = 3V TTL min high level = 2.0V while XTI min high level = 2.2V)

**Figure 4.** MPEG Decoder Interfaces.

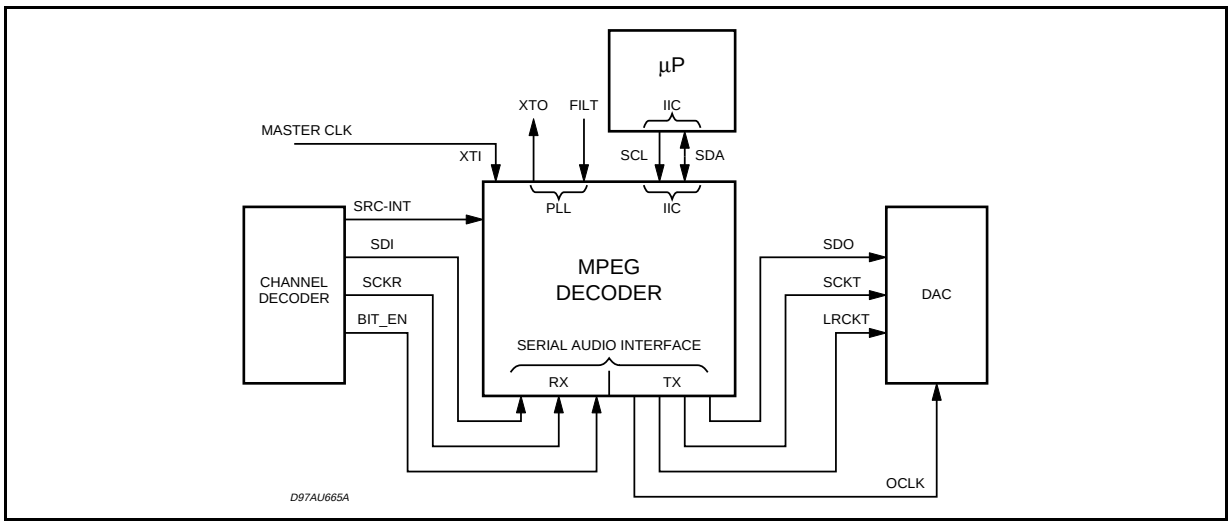
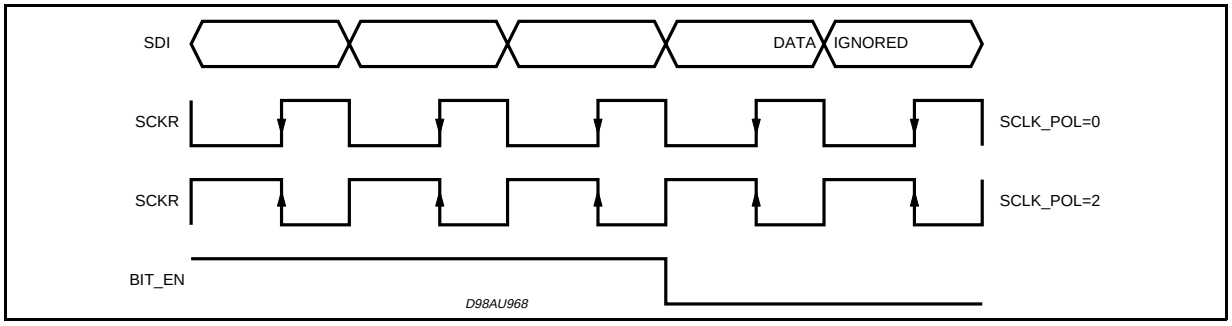



**Figure 5.** Serial Input Interface Clocks




### 2.2 - Serial Input Interface

STA003T receives the input data thought the Serial Input Interface (Fig.4). It is a serial communication interface connected to the SDI (Serial Data Input) and SCKR (Receiver Serial Clock).

The interface can be configured to receive data sampled on both rising and falling edge of the SCKR clock.The BIT_EN pin, when set to low, forces the bitstream input interface to ignore the incoming data. The possible configurations are described in Fig. 5.
The bitstream must be sent MSB first to STA003T.

### 2.3 - PLL & Clocks Generation System

The STA003T has a clock generation system that is used by the device core to adjust the core speed, for power saving, adapting the processing speed to the needs of the decoded audio program. The clocks generation system is even used to generate all the PCM output interface clocks: SCKT, LRCKT, and OCLK.

The block diagram in Fig. 6 is a description of STA003T clocks generation system. The input of STA003T clocks system is a 14.72MHz input clock.

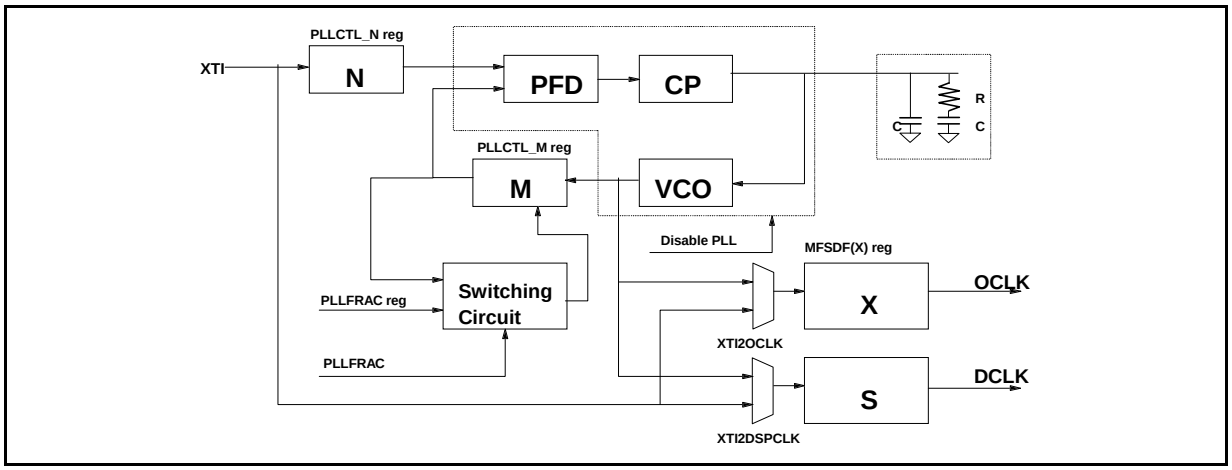
Internally it is composed by a PLL loop, and the VCO output is fed into a divider stage, used to program the Core speed and the PCM interface clocks. Several registers are programmed by the Layer III decoder core, and by the user, when a specific interface configuration is required.

The PLL can be programmed by a set of registers, as described in the I2C Registers section, The particularity of the STA003T clocks generation system is the possibility to modify the Audio Sampling Frequency (LRCKT) in steps of few ppm to compensate dynamically the audio sampling rate offset between the receiver and the broadcasting station.

The compensation is done by the STA003T core without requiring interaction with the application controller and the sampling rate compensation produces a jittering effect outside the audible range.

The device implements a sampling rate offset control receiving by STA002 (WorldSpace Channel Decoder) a dedicated signal every decoded Broadcast Channel Frame (432ms).

**Figure 6.** PLL and Clocks Generation System

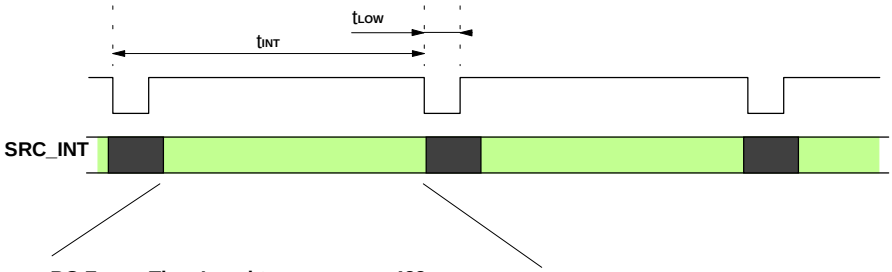



This signal is used as interrupt signal inside STA003T.

Within a WorldSpace Broadcast Frame, there are a fixed number of PCM samples, depending on the nominal audio sampling rate (Fig. 7).
Using this information, with the SRC_INT signal as external timer source, STA003T performs the compensation of the audio sampling rate.

The sampling rate control is done by the STA003T core, by setting PLLFRAC internal register. The PLLFRAC value is updated, in steps of few ppms, by Update PLLFRAC signal.

**Figure 7.** WorldSpace BC Framing




**BC Frame Time Lenght:** **432 ms**

**MPEG Frames into 1 BC Frame:**
**18 for 48 & 24 KHz**
**12 for 32 & 16 KHz**
**9 for 12 KHz**
**6 for 8 KHz**

**PCM Samples into 1 BC Frame:**
**20736 for 48 KHz**
**10368 for 24 KHz**
**13824 for 32 KHz**
**6912 for 16 KHz**
**5184 for 12 KHz**
**3456 for 8 KHz**

### 2.4 - PCM Output Interface

The decoded audio data are output in serial PCM format. The interface consists of the following signals:

SDO PCM Serial Data Output

SCKT PCM Serial Clock Output

LRCLK Left/Right Channel Selection Clock

The output samples precision is selectable from 16 to 24 bits/word, by setting the output precision (16, 18, 20 and 24 bits) with PCMCONF register. Data can be output either with the most significant bit first (MS) or least significant bit first (LS), selected by writing into a flag of the PCMCONF register.
Figure 8 gives a description of the STA003T PCM Output Formats.

The sample rates set decoded by STA003T is described in Table 1.

**Figure 8.** PCM Output Formats

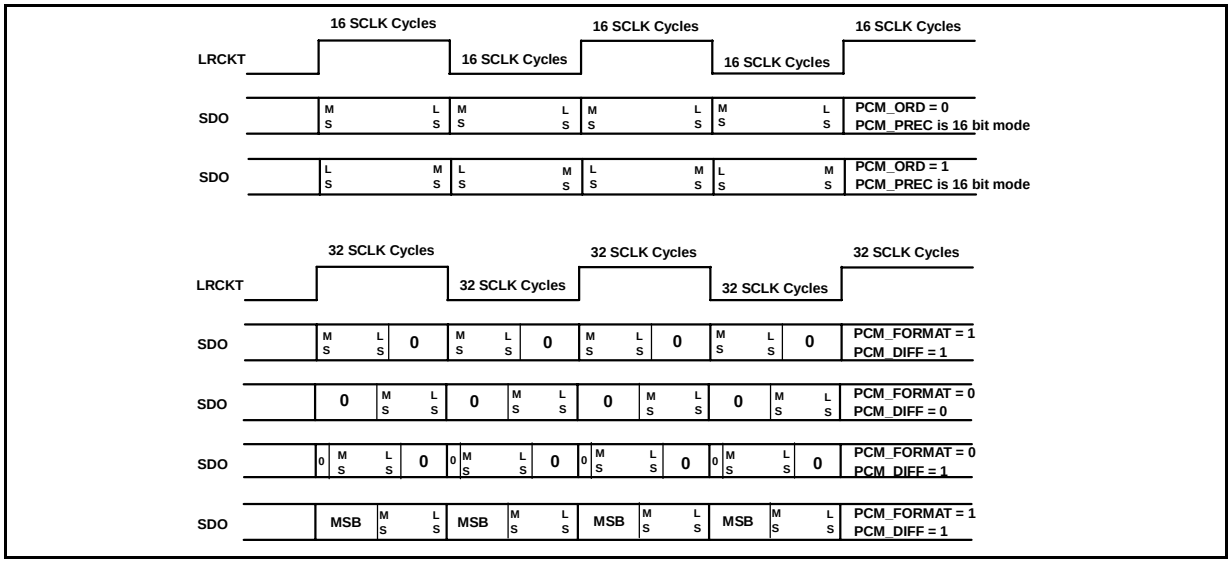



**Table 1: MPEG Sampling Rates (KHz)**

| MPEG 1 | MPEG 2 | MPEG 2.5 |
|---|---|---|
| 48 | 24 | 12 |
| 32 | 16 | 8 |

### 2.5 - STA003T Decoding States

There are three different decoder states: **Idle, Init,** and **Decode.** Commands to change the decoding states are described in the STA003T $I^2C$ registers description.

#### Idle Mode

In this mode the decoder is waiting for the RUN command. This mode should be used to initialise the configuration register of the device. The DAC connected to STA003T can be initialised during this mode (set MUTE to 1).

| PLAY | MUTE | Clock State | PCM Output |
|---|---|---|---|
| X | 0 | Not Running | 0 |
| X | 1 | Running | 0 |

#### Init Mode

"PLAY" and "MUTE" changes are ignored in this mode. The internal state of the decoder will be updated only when the decoder changes from the state "init" to the state "decode". The "init" phase ends when the first decoded samples are at the output stage of the device.

#### Decode Mode

This mode is completely described by the following table:

| PLAY | MUTE | Clock State | PCM Output | Decoding |
|---|---|---|---|---|
| 0 | 0 | Not Running | 0 | No |
| 0 | 1 | Running | 0 | No |
| 1 | 0 | Running | Decoded Samples | Yes |
| 1 | 1 | Running | 0 | Yes |

## 3 - I²C BUS SPECIFICATION

The STA003T supports the I²C protocol. This protocol defines any device that sends data on to the bus as a transmitter and any device that reads the data as a receiver. The device that controls the data transfer is known as the master and the others as the slave. The master always starts the transfer and provides the serial clock for synchronisation. The STA003T is always a slave device in all its communications.

### 3. 1 - COMMUNICATION PROTOCOL

#### 3.1.0 - Data transition or change

Data changes on the SDA line must only occur when the SCL clock is low. SDA transition while the clock is high are used to identify START or STOP condition.

#### 3.1.1 - Start condition

START is identified by a high to low transition of the data bus SDA signal while the clock signal SCL is stable in the high state. A START condition must precede any command for data transfer.

#### 3.1.2 - Stop condition

STOP is identified by low to high transition of the data bus SDA signal while the clock signal SCL is stable in the high state. A STOP condition terminates communications between STA003T and the bus master.

#### 3.1.3 - Acknowledge bit

An acknowledge bit is used to indicate a successful data transfer. The bus transmitter, either master or slave, releases the SDA bus after sending 8 bit of data.

During the 9th clock pulse the receiver pulls the SDA bus low to acknowledge the receipt of 8 bits of data.

#### 3.1.4 - Data input

During the data input the STA003T samples the SDA signal on the rising edge of the clock SCL.

For correct device operation the SDA signal has to be stable during the rising edge of the clock and the data can change only when the SCL line is low.

### 3.2 - DEVICE ADDRESSING

To start communication between the master and the STA003T, the master must initiate with a start condition. Following this, the master sends onto the SDA line 8 bits (MSB first) corresponding to the device select address and read or write mode.

The 7 most significant bits are the device address identifier, corresponding to the I²C bus definition. For the STA003T these are fixed as 1000011.

The 8th bit (LSB) is the read or write operation RW, this bit is set to 1 in read mode and 0 for write mode. After a START condition the STA003T identifies on the bus the device address and, if a match is found, it acknowledges the identification on SDA bus during the 9th bit time. The following byte after the device identification byte is the internal space address.

### 3.3 - WRITE OPERATION (see fig. 9)

Following a START condition the master sends a device select code with the RW bit set to 0.

The STA003T acknowledges this and waits for the byte of internal address.

After receiving the internal bytes address the STA003T again responds with an acknowledge.

#### 3.3.1 - Byte write

In the byte write mode the master sends one data byte, this is acknowledged by STA003T. The master then terminates the transfer by generating a STOP condition.

#### 3.3.2 - Multibyte write

The multibyte write mode can start from any internal address. The transfer is terminated by the master generating a STOP condition.

**Figure 9.** Write Mode Sequence

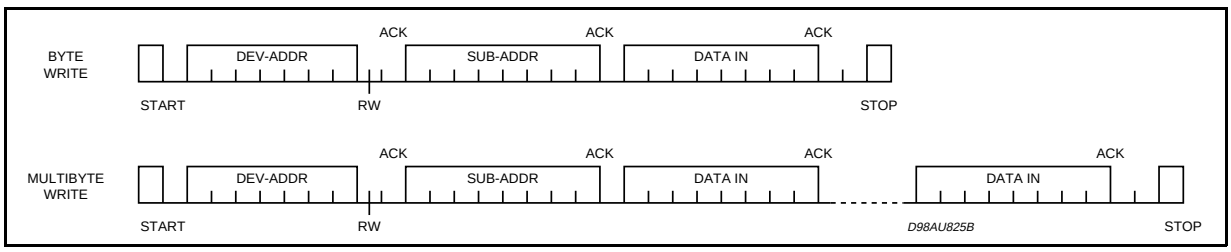
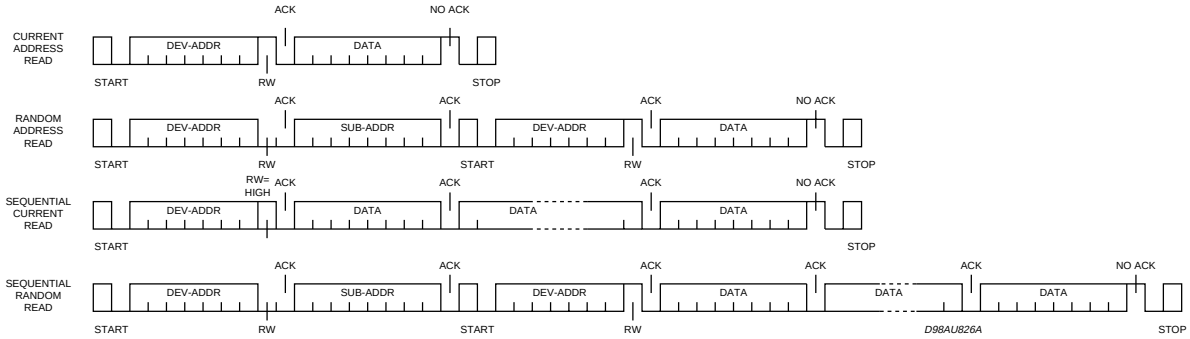


**Figure 10.** Read Mode Sequence




### 3.4 - READ OPERATION (see Fig. 10)

#### 3.4.1 - Current byte address read

The STA003T has an internal byte address counter. Each time a byte is written or read, this counter is incremented.

For the current byte address read mode, following a START condition the master sends the device address with the RW bit set to 1.

The STA003T acknowledges this and outputs the byte addressed by the internal byte address counter. The master does not acknowledge the received byte, but terminates the transfer with a STOP condition.

#### 3.4.2 - Sequential address read

This mode can be initiated with either a current address read or a random address read. However in this case the master does acknowledge the data byte output and the STA003T continues to output the next byte in sequence.

To terminate the streams of bytes the master does not acknowledge the last received byte, but terminates the transfer with a STOP condition.
The output data stream is from consecutive byte addresses, with the internal byte address counter automatically incremented after one byte output.

### 4 - I²C REGISTERS

The following table gives a description of the MPEG Source Decoder (STA003T) register list.

The first column (HEX_COD) is the hexadecimal code for the sub-address.
The second column (DEC_COD) is the decimal code.
The third column (DESCRIPTION) is the description of the information contained in the register.

The fourth column (RESET) inidicate the reset value if any. When no reset value is specifyed, the default is "undefined".

The fifth column (R/W) is the flag to distinguish register "read only" and "read and write", and the useful size of the register itself.

Each register is 8 bit wide. The master shall operate reading or writing on 8 bits only.

**I²C REGISTERS**

| HEX_COD | DEC_COD | DESCRIPTION | RESET | R/W |
|---|---|---|---|---|
| 0x00 | 0 | VERSION | | R (8) |
| 0x01 | 1 | IDENT | 0xAC | R (8) |
| 0x05 | 5 | PLLCTL [7:0] | 0x21 | R/W (8) |
| 0x06 | 6 | PLLCTL_M | 0x0C | R/W (8) |
| 0x07 | 7 | PLLCTL_N | 0x00 | R/W (8) |
| 0x0B | 11 | reserved | | |
| 0x0C | 12 | reserved | | |
| 0x0D | 13 | SCLK_POL | 0x04 | R/W (8) |
| 0x0F | 15 | ERROR_CODE | 0x00 | R (8) |

## I²C REGISTERS (continued)

| HEX_COD | DEC_COD | DESCRIPTION | RESET | R/W |
|---|---|---|---|---|
| 0x10 | 16 | SOFT_RESET | 0x00 | W (8) |
| 0x13 | 19 | PLAY | 0x01 | R/W(8) |
| 0x14 | 20 | MUTE | 0x00 | R/W(8) |
| 0x16 | 22 | CMD_INTERRUPT | 0x00 | R/W(8) |
| 0x18 | 24 | reserved | | |
| 0x40 | 64 | SYNCSTATUS | 0x00 | R (8) |
| 0x41 | 65 | ANCCOUNT_L | 0x00 | R (8) |
| 0x42 | 66 | ANCCOUNT_H | 0x00 | R (8) |
| 0x43 | 67 | HEAD_H[23:16] | 0x00 | R(8) |
| 0x44 | 68 | HEAD_M[15:8] | 0x00 | R(8) |
| 0x45 | 69 | HEAD_L[7:0] | 0x00 | R(8) |
| 0x46 | 70 | DLA | 0x00 | R/W (8) |
| 0x47 | 71 | DLB | 0xFF | R/W (8) |
| 0x48 | 72 | DRA | 0x00 | R/W (8) |
| 0x49 | 73 | DRB | 0xFF | R/W (8) |
| 0x54 | 84 | PCMDIVIDER | 0x01 | R/W (8) |
| 0x55 | 85 | PCMCONF | 0x21 | R/W (8) |
| 0x56 | 86 | PCMCROSS | 0x00 | R/W (8) |
| 0x59 | 89 | ANC_DATA_1 [7:0] | 0x00 | R (8) |
| 0x5A | 90 | ANC_DATA_2 [15:8] | 0x00 | R (8) |
| 0x5B | 91 | ANC_DATA_3 [23:16] | 0x00 | R (8) |
| 0x5C | 92 | ANC_DATA_4 [31:24] | 0x00 | R (8) |
| 0x5D | 93 | ANC_DATA_5 [39:32] | 0x00 | R (8) |
| 0x61 | 97 | MFSDF (X) | 0x0F | R/W (8) |
| 0x63 | 99 | DAC_CLK_MODE | 0x00 | R/W (8) |
| 0x64 | 100 | PLLFRAC_L | 0xC8 | R/W (8) |
| 0x65 | 101 | PLLFRAC_H | 0x59 | R/W (8) |
| 0x67 | 103 | FRAME_CNT_L | 0x00 | R (8) |
| 0x68 | 104 | FRAME_CNT_M | 0x00 | R (8) |
| 0x69 | 105 | FRAME_CNT_H | 0x00 | R (8) |
| 0x6A | 106 | AVERAGE_BITRATE | 0x00 | R (8) |
| 0x71 | 113 | SOFTVERSION | | R (8) |
| 0x72 | 114 | RUN | 0x00 | R/W (8) |
| 0x77 | 119 | TREBLE_FREQUENCY_LOW | 0x00 | R/W (8) |
| 0x78 | 120 | TREBLE_FREQUENCY_HIGH | 0x00 | R/W (8) |
| 0x79 | 121 | BASS_FREQUENCY_LOW | 0x00 | R/W (8) |
| 0x7A | 122 | BASS_FREQUENCY_HIGH | 0x00 | R/W (8) |
| 0x7B | 123 | TREBLE_ENHANCE | 0x00 | R/W (8) |
| 0x7C | 124 | BASS_ENHANCE | 0x00 | R/W (8) |
| 0x7D | 125 | TONE_ATTEN | 0x00 | R/W (8) |

Note:

1) The HEX_COD is the hexadecimal adress that the microcontroller has to generate to access the information.
2) RESERVED: register used for production test only, or for future use.

### 4.1 - STA003T REGISTERS DESCRIPTION

The STA003T device includes 128 $I^2C$ registers. In this document, only the user-oriented registers are described. The undocumented registers are reserved. These registers must never be accessed (in Read or in Write mode). The Read-Only registers must never be written.

The following table describes the meaning of the abbreviations used in the I2C registers description:

| Symbol | Comment |
|---|---|
| NA | Not Applicable |
| UND | Undefined |
| NC | No Charge |
| RO | Read Only |
| WO | Write Only |
| R/W | Read and Write |
| R/WS | Read, Write in specific mode |

**VERSION**

**Address: 0x00**

Type: RO

| MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|
| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
| V8 | V7 | V6 | V5 | V4 | V3 | V2 | V1 |

The VERSION register is read-only and it is used to identify the IC on the application board.

**IDENT**

**Address: 0x01**

Type: RO

Software Reset: 0xAC

Hardware Reset: 0xAC

| MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|
| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
| 1 | 0 | 1 | 0 | 1 | 1 | 0 | 0 |

IDENT is a read-only register and is used to identify the IC on an application board. IDENT always has the value "0xAC"

**PLLCTL**

**Address: 0x05**

Type: R/W

Software Reset: 0x21

Hardware Reset: 0x21

| MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|
| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
| XTO_BUF | XTODIS | OCLKEN | SYS2OCLK | PPLDIS | XTI2DSPCLK | XTI2OCLK | UPD_FRAC |

*UPD_FRAC:* when is set to 1, updates FRAC in the switching circuit. It is set to 1 after autoboot.

*XTI2OCLK:* when is set to 1, uses the XTI as input of the divider X instead of VCO output. It is set to 0 on HW reset.

*XTI2DSPCLK:* when is set to 1, uses the XTI as input of the divider S instead of VCO output. It is set to 0 on HW reset.

*PLLDIS:* when set to 1, the VCO output is disabled. It is set to 0 on HW reset.

*SYS2OCLK:* when is set to 1, the OCLK frequency is equal to the system frequency. It is useful for testing. It is set to 0 on HW reset.

*OCLKEN:* when is set to 1, the OCLK pad is enable as output pad. It is set to 1 on HW reset.

*XTODIS:* when is set to 1, the XTO pad is disabled. It is set to 0 on HW reset.

*XTO_BUF:* when this bit is set, the pin nr. 28 (VDD_5/CLK_OUT) is enabled as buffered (4mA) master clock output (CLK_OUT). It is set to 0 after autoboot.

**PLLCTL_M**

**Address: 0x06**

Type: R/W

Software Reset: 0x0C

Hardware Reset: 0x0C

**PLLCTL_N**

**Address: 0x07**

Type: R/W

Software Reset: 0x00

Hardware Reset: 0x00

The M and N registers are used to configure the STA003T PLL by DSP embedded software.

M and N registers are R/W type but they are completely controlled, on STA003T, by DSP software.

**SCKL_POL**

**Address: 0x0D**

Type: R/W

Software Reset: 0x04

Hardware Reset: 0x04

| MSB | | | | | | | LSB | |
|---|---|---|---|---|---|---|---|---|
| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 | |
| X | X | X | X | X | 0 | 0 | 0 | (1) |
| | | | | | 1 | 0 | 0 | (2) |

X = don't care

SCKL_POL is used to select the working polarity of the Input Serial Clock (SCKR).

(1) If SCKL_POL is set to 0x00, the data (SDI) are sent with the falling edge of SCKR and sampled on the rising edge.

(2) If SCKL_POL is set to 0x04, the data (SDI) are sent with the rising edge of SCKR and sampled on the falling edge.

**ERROR_CODE**

**Address: 0x0F**

Type: RO

Software Reset: 0x00

Hardware Reset: 0x00

| MSB | | | | | | | LSB | |
|---|---|---|---|---|---|---|---|---|
| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 | |
| X | X | X | X | 0 | 0 | 0 | 0 | (1) |
| | | | | 0 | 0 | 0 | 1 | (2) |
| | | | | 0 | 0 | 1 | 0 | (3) |

X = don't care

ERROR_CODE register contains the last error occourred if any. The codes can be as follows:

| Code | | Description |
|---|---|---|
| (1) | 0x00 | No error since the last SW or HW Reset |
| (2) | 0x01 | CRC Failure |
| (3) | 0x02 | DATA not available |

**SOFT_RESET**

**Address: 0x10**

Type: WO

Software Reset: 0x00

Hardware Reset: 0x00

| MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|
| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
| X | X | X | X | X | X | X | 0 |
| | | | | | | | 1 |

X = don't care; 0 = normal operation; 1 = reset

When this register is written, a soft reset occours. The STA003T core command register and the interrupt register are cleared. The decoder goes in to idle mode.

**PLAY**

**Address: 0x13**

Type: R/W

Software Reset: 0x00

Hardware Reset: 0x00

| MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|
| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
| X | X | X | X | X | X | X | 0 |
| | | | | | | | 1 |

X = don't care; 0 = normal operation; 1 = play

The PLAY command is handled according to the state of the decoder, as described in section 2.5. PLAY only becomes active when the decoder is in DECODE mode.

**MUTE**

**Address: 0x14**

Type: R/W

Software Reset: 0x00

Hardware Reset: 0x00

| MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|
| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
| X | X | X | X | X | X | X | 0 |
| | | | | | | | 1 |

X = don't care; 0 = normal operation; 1 = mute

The MUTE command is handled according to the state of the decoder, as described in section 2.5.

MUTE sets the clock running.

non-zero value.

**SYNCSTATUS**

**Address: 0x40**

Type: RO

Software Reset: 0x00

Hardware Reset: 0x00

| MSB | | | | | | LSB | | |
|---|---|---|---|---|---|---|---|---|
| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 | Description |
| X | X | X | X | X | X | SS1 | SS0 | |
| | | | | | | 0 | 0 | Research of sync word |
| | | | | | | 0 | 1 | Wait for Confirmation |
| | | | | | | 1 | 0 | Synchronised |
| | | | | | | 1 | 1 | not used |

**CMD_INTERRUPT**

**Address: 0x16**

Type: R/W

Software Reset: 0x00

Hardware Reset: 0x00

| MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|
| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
| X | X | X | X | X | X | X | 0 |
| | | | | | | | 1 |

X = don't care;
0 = normal operation;
1 = write into $I^2C$/Ancillary Data

The INTERRUPT is used to give STA003T the command to write into the I2C/Ancillary Data Buffer (Registers: 0x59 ... 0x5D). Every time the Master has to extract the new buffer content (5 bytes) it writes into this register, setting it to a

**ANCCOUNT_L**

**Address: 0x41**

Type: RO

Software Reset: 0x00

Hardware Reset: 0x00

MSB LSB

| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|
| AC7 | AC6 | AC5 | AC4 | AC3 | AC2 | AC1 | AC0 |

**ANCCOUNT_H**

**Address: 0x42**

Type: RO

Software Reset: 0x00

Hardware Reset: 0x00

ANCCOUNT_H

MSB LSB

| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|
| AC15 | AC14 | AC13 | AC12 | AC11 | AC10 | AC9 | AC8 |

ANCCOUNT registers are logically concatenated and indicate the number of Ancillary Data bits available at every correctly decoded MPEG frame.

**HEAD_H[23:16]**

MSB LSB

| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|
| X | X | X | H20 | H19 | H18 | H17 | H16 |

x = don't care

**HEAD_M[15:8]**

MSB LSB

| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|
| H15 | H14 | H13 | H12 | H1'1 | H10 | H9 | H8 |

**HEAD_L[7:0]**

MSB LSB

| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|
| H7 | H6 | H5 | H4 | H3 | H2 | H1 | H0 |

**Address: 0x43, 0x44, 0x45**

Type: RO

Software Reset: 0x00

Hardware Reset: 0x00

Head[1:0] emphasis

Head[2] original/copy

Head[3] copyrightHead

[5:4] mode extension

Head[7:6] mode

Head[8] private bit

Head[9] padding bit

Head[11:10] sampling frequency index

Head[15:12] bitrate index

Head[16] protection bit

Head[18:17] layer

Head[19] ID

Head[20] ID_ex

The HEAD registers can be viewed as logically concatenated to store the MPEG Layer III Header content. The set of three registers is updated every time the synchronisation to the new MPEG frame is achieved .

The meaning of the flags are shown in the following tables:

**MPEG IDs**

| IDex | ID | |
|---|---|---|
| 0 | 0 | MPEG 2.5 |
| 0 | 1 | reserved |
| 1 | 0 | MPEG 2 |
| 1 | 1 | MPEG 1 |

***Layer***

in Layer III these two flags must be set always to "01".

***Protection_bit***

It equals "1" if no redundancy has been added and "0" if redundancy has been added.

***Bitrate_index***

indicates the bitrate (Kbit/sec) depending on the MPEG ID.

| bitrate index | ID = 1 | ID = 0 |
|---|---|---|
| '0000' | free | free |
| '0001' | 32 | 8 |
| '0010' | 40 | 16 |
| '0011' | 48 | 24 |
| '0100' | 56 | 32 |
| '0101' | 64 | 40 |
| '0110' | 80 | 48 |
| '0111' | 96 | 56 |
| '1000' | 112 | 64 |
| '1001' | 128 | 80 |
| '1010' | not supported | 96 |
| '1011' | not supported | 112 |
| '1100' | not supported | 128 |
| '1101' | not supported | not supported |
| '1110' | not supported | not supported |
| '1111' | forbidden | forbidden |

**Sampling Frequency**

indicates the sampling frequency of the encoded audio signal (KHz) depending on the MPEG ID

| Sampling Frequency | MPEG1 | MPEG2 | MPEG2.5 |
|---|---|---|---|
| '00' | not supported | not supported | not supported |
| '01' | 48 | 24 | 12 |
| '10' | 32 | 16 | 8 |
| '11' | reserved | reserved | reserved |

**Padding bit**

if this bit equals '1', the frame contains an additional slot to adjust the mean bitrate to the sampling frequency, otherwise this bit is set to '0'.

**Private bit**

Bit for private use. This bit will not be used in the future by ISO/IEC.

**Mode**

Indicates the mode according to the following table. The joint stereo mode is intensity_stereo and/or ms_stereo.

| mode | mode specified |
|---|---|
| '00' | stereo |
| '01' | joint stereo (intensity_stereo and/or ms_stereo) |
| '10' | dual_channel |
| '11' | single_channel (mono) |

**Mode extension**

These bits are used in joint stereo mode. They indicates which type of joint stereo coding method is applied. The frequency ranges, over which the intensity_stereo and ms_stereo modes are applied, are implicit in the algorithm.

**Copyright**

If this bit is equal to '0', there is no copyright on the bitstream, '1' means copyright protected.

**Original/Copy**

This bit equals '0' if the bitstream is a copy, '1' if it is original.

**Emphasis**

Indicates the type of de-emphasis that shall be used.

| emphasis | emphasis specified |
|---|---|
| '00' | none |
| '01' | 50/15 microseconds |
| '10' | reserved |
| '11' | CCITT J,17 |

**DLA**

**Address: 0x46**

Type: R/W

Software Reset: 0x00

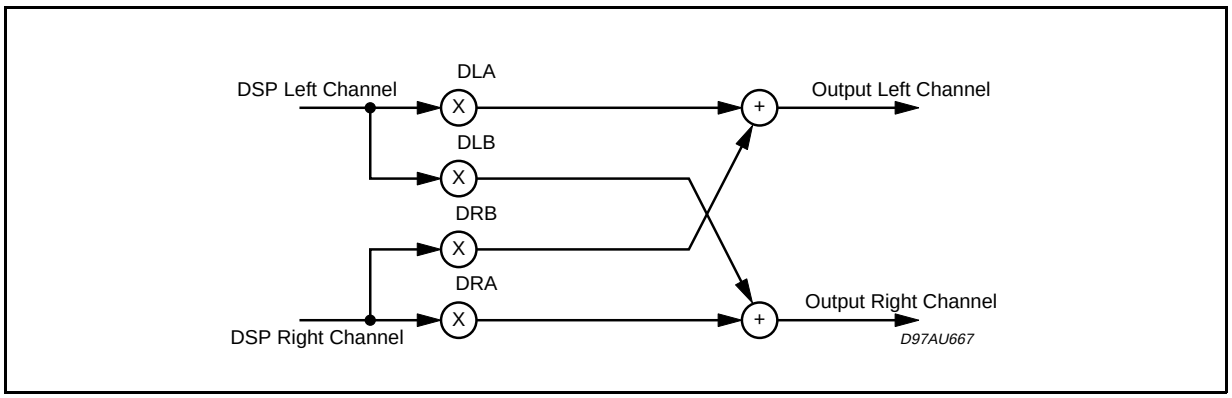
Hardware Reset: 0x00

MSB LSB

| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 | Description |
|---|---|---|---|---|---|---|---|---|
| DLA7 | DLA6 | DLA5 | DLA4 | DLA3 | DLA2 | DLA1 | DLA0 | OUTPUT ATTENUATION |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | NO ATTENUATION |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | -1dB |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | -2dB |
| : | : | : | : | : | : | : | : | : |
| 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | -96dB |

DLA register is used to attenuate the level of audio output at the Left Channel using the butterfly shown in Fig. 11. When the register is set to 255 (0xFF), the maximum attenuation is achieved.
A decimal unit correspond to an attenuation step of 1 dB.

**Figure 11.** Volume Control and Output Setup




**DLB**

**Address: 0x47**

Type: R/W

Software Reset: 0xFF

Hardware Reset: 0xFF

MSB LSB

| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 | Description |
|---|---|---|---|---|---|---|---|---|
| DLB7 | DLB6 | DLB5 | DLB4 | DLB3 | DLB2 | DLB1 | DLB0 | OUTPUT ATTENUATION |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | NO ATTENUATION |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | -1dB |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | -2dB |
| : | : | : | : | : | : | : | : | : |
| 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | -96dB |

DLB register is used to re-direct the Left Channel on the Right, or to mix both the Channels.

Default value is 0x00, corresponding at the maximum attenuation in the re-direction channel.

**DRA**

**Address: 0x48**

Type: R/W

Software Reset: 0X00

Hardware Reset: 0X00

MSB LSB

| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 | Description |
|---|---|---|---|---|---|---|---|---|
| DRA7 | DRA6 | DRA5 | DRA4 | DRA3 | DRA2 | DRA1 | DRA0 | OUTPUT ATTENUATION |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | NO ATTENUATION |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | -1dB |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | -2dB |
| : | : | : | : | : | : | : | : | : |
| 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | -96dB |

DRA register is used to attenuate the level of audio output at the Right Channel using the butterfly shown in Fig. 11. When the register is set to 255 (0xFF), the maximum attenuation is achieved.
A decimal unit correspond to an attenuation step of 1 dB.

**DRB**

**Address: 0x49**

Type: R/W

Software Reset: 0xFF

Hardware Reset: 0xFF

MSB LSB

| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 | Description |
|---|---|---|---|---|---|---|---|---|
| DRB7 | DRB6 | DRB5 | DRB4 | DRB3 | DRB2 | DRB1 | DRB0 | OUTPUT ATTENUATION |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | NO ATTENUATION |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | -1dB |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | -2dB |
| : | : | : | : | : | : | : | : | : |
| 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | -96dB |

DRB register is used to re-direct the Right Channel on the Left, or to mix both the Channels.

Default value is 0x00, corresponding at the maximum attenuation in the re-direction channel.

**PCMDIVIDER**

**Address: 0x54**

Type: RW

Software Reset: 0x01

Hardware Reset: 0x01

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| PD7 | PD6 | PD5 | PD4 | PD3 | PD2 | PD1 | PD0 |

PCMDIVIDER is used to set the frequency ratio between the OCLK (Oversampling Clock for DACs), and the SCKT (Serial Audio Transmitter Clock).

The relation is the following:

$$SCKT\_freq = \frac{OCLK\_freq}{2\,(1 + PCMDIVIDER)}$$

The Oversampling Factor (O_FAC) is related to OCLK and SCKT by the following expression:

**1)** OCLK_freq = O_FAC * LRCKT_ Freq
(DAC relation)

**2)** OCLK_ Freq = 2 * (1+PCMDIVIDER) * 32*
LRCKT_Freq (when 16 bit PCM mode is used)

**3)** OCLK_ Freq = 2 * (1+PCMDIVIDER) * 64*
LRCKT_Freq (when 32 bit PCM mode is used)

**4)** PCMDIVIDER = (O_FAC/64) - 1 in 16 bit mode

**5)** PCMDIVIDER = (O_FAC/128) - 1 in 32 bit mode

Example for setting:

MSB LSB

| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 | Description | |
|---|---|---|---|---|---|---|---|---|---|
| PD7 | PD6 | PD5 | PD4 | PD3 | PD2 | PD1 | PD0 | | |
| 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 16 bit mode | 512 x Fs |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 16 bit mode | 384 x Fs |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 16 bit mode | 256 x Fs |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 32 bit mode | 512 x Fs |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 32 bit mode | 384 x Fs |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 32 bit mode | 256 x Fs |

<u>for 16 bit PCM Mode</u>

O_FAC = 512 ; PCMDIVIDER = 7

O_FAC = 256 ; PCMDIVIDER = 3

O_FAC = 384 ; PCMDIVIDER = 5

<u>for 32 bit PCM Mode</u>

O_FAC = 512 ; PCMDIVIDER = 3

O_FAC = 256 ; PCMDIVIDER = 1

O_FAC = 384 ; PCMDIVIDER = 2

### PCMCONF

**Address: 0x55**

Type: R/W

Software Reset: 0x21

Hardware Reset: 0x21

| MSB | | | | | | | LSB | |
|---|---|---|---|---|---|---|---|---|
| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 | Description |
| X | ORD | DIF | INV | FOR | SCL | PREC [1] | PREC ([0] | |
| X | 1 | | | | | | | PCM order the LS bit is transmitted First |
| X | 0 | | | | | | | PCM order the MS bit is transmitted First |
| X | | 0 | | | | | | The word is right padded |
| X | | 1 | | | | | | The word is left padded |
| X | | | 1 | | | | | LRCKT Polarity compliant to I2S format |
| X | | | 0 | | | | | LRCKT Polarity inverted |
| X | | | | 0 | | | | I2S format |
| X | | | | 1 | | | | Different formats |
| X | | | | | 1 | | | Data are sent on the rising edge of SCKT |
| X | | | | | 0 | | | Data are sent on the falling edge of SCKT |
| X | | | | | | 0 | 0 | 16 bit mode (32 slots transmitted per LRCKT period) |
| X | | | | | | 0 | 1 | 18 bit mode (64 slots transmitted per LRCKT period) |
| X | | | | | | 1 | 0 | 20 bit mode (64 slots transmitted per LRCKT period) |
| X | | | | | | 1 | 1 | 24 bit mode (64 slots transmitted per LRCKT period) |

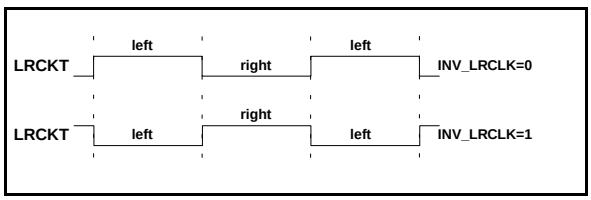
PCMCONF is used to set the PCM Output Interface configuration:

ORD: PCM order. If this bit is set to'1', the LS Bit is transmitted first, otherwise MS Bit is transmiited first.

DIF: PCM_DIFF. It is used to select the position of the valid data into the transmitted word. This setting is significant only in 18/20/24 bit/word mode.If it is set to '0' the word is right-padded, otherwise it is left-padded.

INV (fig.12): It is used to select the LRCKT clock polarity. If it is set to '1' the polarity is compliant to I2S format (low -> left , high -> right), otherwise the LRCKT is inverted. The default value is '0'. (if I2S have to be selected, must be set to '1' in the STA003T configuration phase).

**Figure 12.** LRCKT Polarity Selection

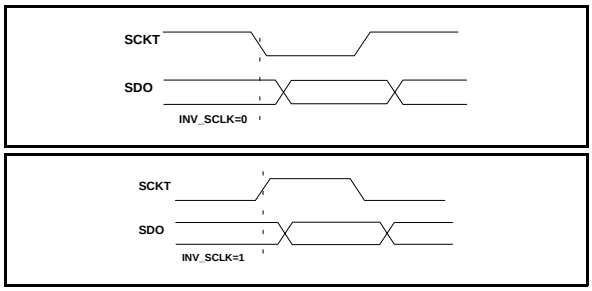



FOR: FORMAT is used to select the PCM Output Interface format.

After hw and sw reset the value is set to 0 corresponding to I2S format.

SCL (fig.13): used to select the Transmitter Serial Clock polarity. If set to '1' the data are sent on the rising edge of SCKT and sampled on the falling. If set to '0' , the data are sent on the falling edge and sampled on the rising. This last option is the most commonly used by the commercial DACs. The default configuration for this flag is '0'.

**Figure 13.** SCKT Polarity Selection




PREC [1:0]: PCM PRECISION

It is used to select the PCM samples precision, as follows:

'00': 16 bit (16 slots transmitted per LCKT period)

'01': 18 bit (32 slots transmitted per LCKT period)

'10': 20 bit (32 slots transmitted per LCKT period)

'11': 24 bit (32 slots transmitted per LCKT period)

The PCM samples precision in STA003T can be 16 or 18-20-24 bits.

When STA003T operates with a 16 (18-20-24) bits precision, the number of bits transmitted during a LRCKT period is 32 (64).

### PCMCROSS

**Address: 0x56**

Type: R/W

Software Reset: 0x00

Hardware Reset: 0x00

MSB LSB

| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 | Description |
|---|---|---|---|---|---|---|---|---|
| X | X | X | X | X | X | 0 | 0 | Left channel is mapped on the left output.<br>Right channel is mapped on the Right output |
| X | X | X | X | X | X | 0 | 1 | Left channel is duplicated on both Output channels. |
| X | X | X | X | X | X | 1 | 0 | Right channel is duplicated on both Output channels |
| X | X | X | X | X | X | 1 | 1 | Right and Left channels are toggled |

The default configuration for this register is '0x00'.

### ANCILLARY DATA BUFFER

**Address: 0x59 - 0x5D**

Type: RO

Software Reset: 0x00

Hardware Reset: 0x00

STA003T can extract max 56 bytes/MPEG frame. To know the number of A.D. bits available every MPEG frame, the ANCCOUNT_L and ANCCOUNT_H registers (0x41 and 0x42) have to be read.

The buffer dimension is 5 bytes, written by STA003T core in sequential order. The timing information to read the buffer can be obtained by reading the FRAME_CNT registers (0x67 - 0x69).

To fill up the buffer with a new 5-bytes slot, the STA003T waits until a CMD_INTERRUPT register is written by the master.

### MFSDF (X)

**Address: 0x61**

Type: R/W

Software Reset: 0x0F

Hardware Reset: 0x0F

MSB LSB

| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|
| X | X | X | M4 | M3 | M2 | M1 | M0 |

The register contains the values for PLL X divider (see Fig. 6).

The value is changed by the internal STA003T Core, to set the clock frequencies, according to the incoming bitstream. This value can be even set by the user to select the PCM interface configuration.

The VCO output frequency is divided by (X+1).

### DAC_CLK_MODE

**Address: 0x63**

Type: RW

Software Reset: 0x00

Hardware Reset: 0x00

MSB LSB

| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|
| X | X | X | X | X | X | X | MODE |

This register is used to select the operating mode for OCLK clock signal.

If it is set to '1', the OCLK frequency is fixed, and it is mantained to the value fixed by the user even if the sampling frequency of the incoming bitstream changes.

If the MODE flag is set to '0', the OCLK frequency changes, and can be set to (512, 384, 256) * Fs. The default configuration for this mode is 256 * Fs.

When this mode is selected, the default OCLK frequency is 12.288 MHz.

**PLLFRAC_L ([7:0])**

| MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|
| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
| PF7 | PF6 | PF5 | PF4 | PF3 | PF2 | PF1 | PF0 |

**PLLFRAC_H ([15:8])**

| MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|
| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
| PF15 | PF14 | PF13 | PF12 | PF11 | PF10 | PF9 | PF8 |

**Address: 0x64 - 0x65**

Type: R/W

Software Reset: 0xC8-0x59

Hardware Reset: 0xC8-0x59

The registers are considered logically concatenated and contain the fractional values for the PLL, used to select the internal configuration.

After Reset, the values are NA, and the operational setting are done when the MPEG synchronisation is achieved.

The following formula describes the relationships among all the STA003T fractional PLL parameters:

$$OCLK\_Freq = \left[\frac{1}{MFSDF(X)+1}\right] \cdot \left[\frac{MCLK\_freq}{PLLTL\_N+1}\right] \cdot$$

$$\cdot \left[PLLCTL\_M + 1 + \frac{PLLFRAC}{65536}\right]$$

where:

PLLFRAC=256 x FRAC_H + PLLFRAC_L (decimal)

**FRAME_CNT_L**

| MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|
| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
| FC7 | FC6 | FC5 | FC4 | FC3 | FC2 | FC1 | FC0 |

**FRAME_CNT_M**

| MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|
| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
| FC15 | FC14 | FC13 | FC12 | FC11 | FC10 | FC9 | FC8 |

**FRAME_CNT_H**

| MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|
| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
| FC23 | FC22 | FC21 | FC20 | FC19 | FC18 | FC17 | FC016 |

**Address: 0x67, 0x68, 0x69**

Type: RO

Software Reset: 0x00

Hardware Reset: 0x00

The three registers are considered logically concatenated and compose the Global Frame Counter.

They are updated at every decoded MPEG Frame. The registers are reset on both hardware and software reset.

**AVERAGE_BITRATE**

**Address: 0x6A**

Type: RO

Software Reset: 0x00

Hardware Reset: 0x00

| MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|
| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
| AB7 | AB6 | AB5 | AB4 | AB3 | AB2 | AB1 | AB0 |

AVERAGE_BITRATE is a read-only register and it contains the average bitrate of the incoming bitstream. The value is rounded with an accuracy of 1 Kbit/sec.

**SOFTVERSION**

**Address: 0x71**

Type: RO

| MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|
| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
| SV7 | SV6 | SV5 | SV4 | SV3 | SV2 | SV1 | SV0 |

After the STA003T boot, this register contains the version code of the embedded software.

**RUN**

**Address: 0x72**

Type: RW

Software Reset: 0x00

Hardware Reset: 0x00

| MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|
| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
| X | X | X | X | X | X | X | RUN |

Setting this register to 1, STA003T leaves the idle state, starting the decoding process.
The Microcontroller is allowed to set the RUN flag, once all the control registers have been initialized.

**TREBLE_FREQUENCY_LOW**

**Address: 0x77**

Type: RW

Software Reset: 0x00

Hardware Reset: 0x00

| MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|
| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
| TF7 | TF6 | TF5 | TF4 | TF3 | TF2 | TF1 | TF0 |

**TREBLE_FREQUENCY_HIGH**

**Address: 0x78**

Type: RW

Software Reset: 0x00

Hardware Reset: 0x00

| MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|
| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
| TF15 | TF14 | TF13 | TF12 | TF11 | TF10 | TF9 | TF8 |

The registers TREBLE_FREQUENCY_HIGH and TREBLE_FREQUENCY_LOW, logically concatenated as a 16 bit wide register, are used to select the frequency, in Hz, where the selected frequency is +12dB respect to the stop band.

By setting these registers, the following rule must be kept:

Treble_Freq < Fs/2

**BASS_FREQUENCY_LOW**

**Address: 0x79**

Software Reset: 0x00

Hardware Reset: 0x00

| MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|
| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
| BF7 | BF6 | BF5 | BF4 | BF3 | BF2 | BF1 | BF0 |

**BASS_FREQUENCY_HIGH**

**Address: 0x7A**

Software Reset: 0x00

Hardware Reset: 0x00

| MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|
| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
| BF15 | BF14 | BF13 | BF12 | BF11 | BF10 | BF9 | BF8 |

The registers BASS_FREQUENCY_HIGH and BASS_FREQUENCY_LOW, logically concatenated as a 16 bit wide register, are used to select the frequency, in Hz, where the selected frequency is -12dB respect to the pass-band. By setting the BASS_FREQUENCY registers, the following rules must be kept:

Bass_Freq <= Treble_Freq

Bass_Freq > 0

(suggested range: 20 Hz < Bass_Freq < 750 Hz)

Example:

Bass = 200Hz

Treble = 3kHz

**TFS**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 |

**BFS**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 |

**TREBLE_ENHANCE**

**Address: 0x7B**

Software Reset: 0x00

Hardware Reset: 0x00

| MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|
| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
| TE7 | TE6 | TE5 | TE4 | TE3 | TE2 | TE1 | TE0 |

Signed number (2 complement)
This register is used to select the enhancement or attenuation STA003T has to perform on Treble Frequency range at the digital signal.

A decrement (increment) of a decimal unit corresponds to a step of attenuation (enhancement) of 1.5dB.
The allowed Attenuation/Enhancement range is [-18dB, +18dB].

| MSB | | | | | | | LSB | ENHANCE/ATTENUATION |
|---|---|---|---|---|---|---|---|---|
| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 | 1.5dB step |
| 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | +18 |
| 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | +16.5 |
| 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | +15 |
| 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | +13.5 |
| | | | | | | | . | |
| | | | | | | | . | |
| | | | | | | | . | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | +1 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | -1 |
| | | | | | | | . | |
| | | | | | | | . | |
| | | | | | | | . | |
| 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | -13.5 |
| 1 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | -15 |
| 1 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | -16.5 |
| 1 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | -18 |

**BASS_ENHANCE**

**Address: 0x7C**

Software Reset: 0x00

Hardware Reset: 0x00

MSB LSB

| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|
| BE7 | BE6 | BE5 | BE4 | BE3 | BE2 | BE1 | BE0 |

Signed number (2 complement)

This register is used to select the enhancement or attenuation STA003T has to perform on Bass Frequency range at the digital signal.

A decrement (increment) of a decimal unit corresponds to a step of attenuation (enhancement) of 1.5dB.
The allowed Attenuation/Enhancement range is [-18dB, +18dB].

| MSB | | | | | | | LSB | ENHANCE/ATTENUATION |
|---|---|---|---|---|---|---|---|---|
| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 | 1.5dB step |
| 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | +18 |
| 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | +16.5 |
| 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | +15 |
| 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | +13.5 |
| | | | | | | | . | |
| | | | | | | | . | |
| | | | | | | | . | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | +1 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | -1 |
| | | | | | | | . | |
| | | | | | | | . | |
| | | | | | | | . | |
| 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | -13.5 |
| 1 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | -15 |
| 1 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | -16.5 |
| 1 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | -18 |

**TONE_ATTEN**

**Address: 0x7D**

Type: RW

Software Reset: 0x00

Hardware Reset: 0x00

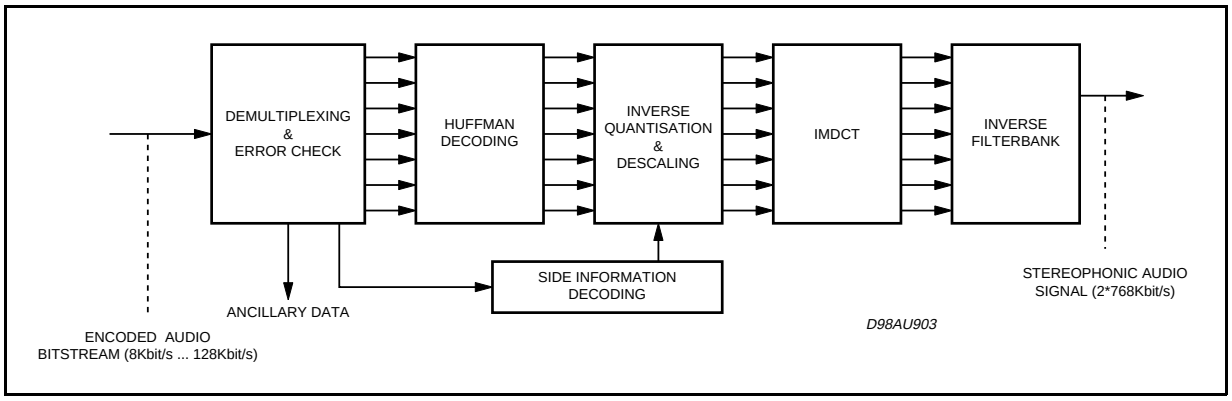
| MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|
| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
| TA7 | TA6 | TA5 | TA4 | TA3 | TA2 | TA1 | TA0 |

In the digital output audio, the full signal is achieved with 0 dB of attenuation. For this reason, before applying Bass & Treble Control, the user has to set the TONE_ATTEN register to the maximum value of enhancement is going to perform.
For example, in case of a 0 dB signal (max. level) only attenuation would be possible. If enhancement is desired, the signal has to be attenuated accordingly before in order to reserve a margin in dB.
An increment of a decimal unit corresponds to a Tone Attenuation step of 1.5dB.

| MSB | | | | | | | LSB | ATTENUATION |
|---|---|---|---|---|---|---|---|---|
| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 | -1.5dB step |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0dB |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | -1.5dB |
| 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | -3dB |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | -4.5dB |
| | | | | . | | | | |
| | | | | . | | | | |
| | | | | . | | | | |
| 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | -15dB |
| 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | -16.5dB |
| 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | -18dB |

## 5. GENERAL INFORMATION

### 5.1. MPEG 2.5 Layer III Algorithm.




### 5.2 - MPEG Ancillary Data Description:

As specifyed in the ISO standard, the MPEG Layer III frames have a variable bit lenght, and are constant in time depending on the audio sampling frequencies. The time duration of the Layer III frames is shown in Tab 2.

**Table2:** MPEG Layer III Frames Time Duration

| Sampling Frequency (KHz) | 48 | 32 | 24 | 16 | 12 | 8 |
|---|---|---|---|---|---|---|
| MPEG Frame Lenght (ms) | 24 | 36 | 24 | 36 | 48 | 72 |

The Ancillary Data extraction on STA003T can be described as follow:

STA003T has a specific 5 bytes Ancillary Data buffer, mapped into the I2C registers:

| | |
|---|---|
| 0x59 | ANC_DATA_1 |
| 0x5A | ANC_DATA_2 |
| 0x5B | ANC_DATA_3 |
| 0x5C | ANC_DATA_4 |
| 0x5D | ANC_DATA_5 |

Since the content of Ancillary Data into an MPEG Frame is max. 56 bytes, a specific register, to require new 5 bytes, is needed.

This register is:

| | |
|---|---|
| 0x16 | CMD_INTERRUPT |

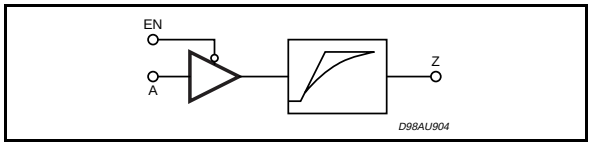
The interrupt register, is sensitive to any non-zero value written by the Microcontroller. When this register is updated the Ancillary Data buffer is filled up with new values and the registers

| | |
|---|---|
| 0x41 | ANCCOUNT_L |
| 0x42 | ANCCOUNT_H |

are updated (decremented) accordingly.

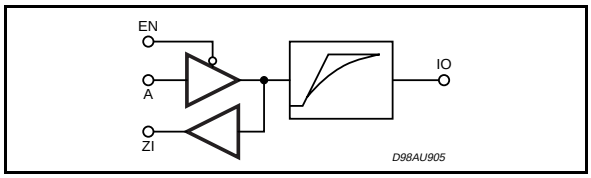
### 5.3. I/O CELL DESCRIPTION

**1) CMOS Tristate Output Pad Buffer**, 4mA, with Slew Rate Control / Pin numbers 9, 10, 11, 20, 28



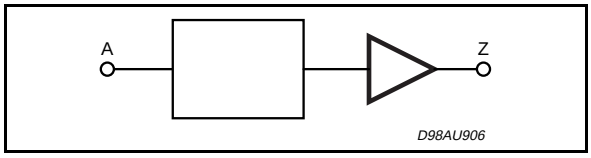

| OUTPUT PIN | MAX LOAD |
|---|---|
| Z | 100pF |

**2) CMOS Bidir Pad Buffer**, 4mA, with Slew Rate Control / Pin numbers 3, 12



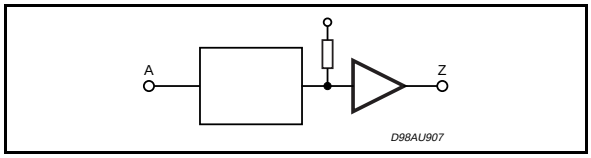

| OUTPUT PIN | CAPACITANCE | OUTPUT PIN | MAX LOAD |
|---|---|---|---|
| IO | 5pF | IO | 100pF |

**3) CMOS Inpud Pad Buffer** / Pin numbers 4, 5, 6, 8, 21, 25




| INPUT PIN | CAPACITANCE |
|---|---|
| A | 3.5pF |

**4) CMOS Inpud Pad Buffer with Active Pull-Up** / Pin numbers 7, 24, 26

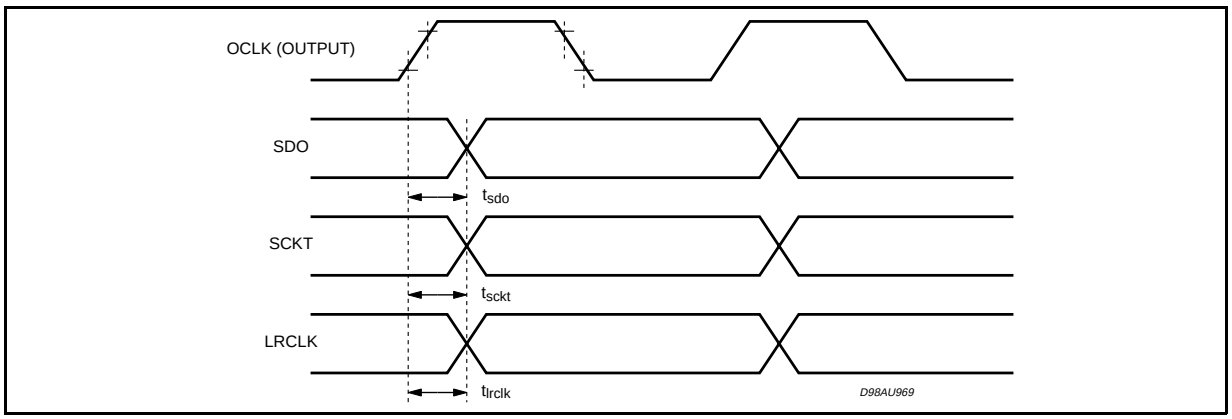



| INPUT PIN | CAPACITANCE |
|---|---|
| A | 3.5pF |

## 5.4. TIMING DIAGRAMS

### 5.4.1. Audio DAC Interface

a) OCLK in output. The audio PLL is used to clock the DAC




tsdo = 3.5 + pad_timing (Cload_SDO) - pad_timing (Cload_ OCLK)

tsckt = 4 + pad_timing (Cload_SCKT) - pad_timing (Cload_ OCLK)

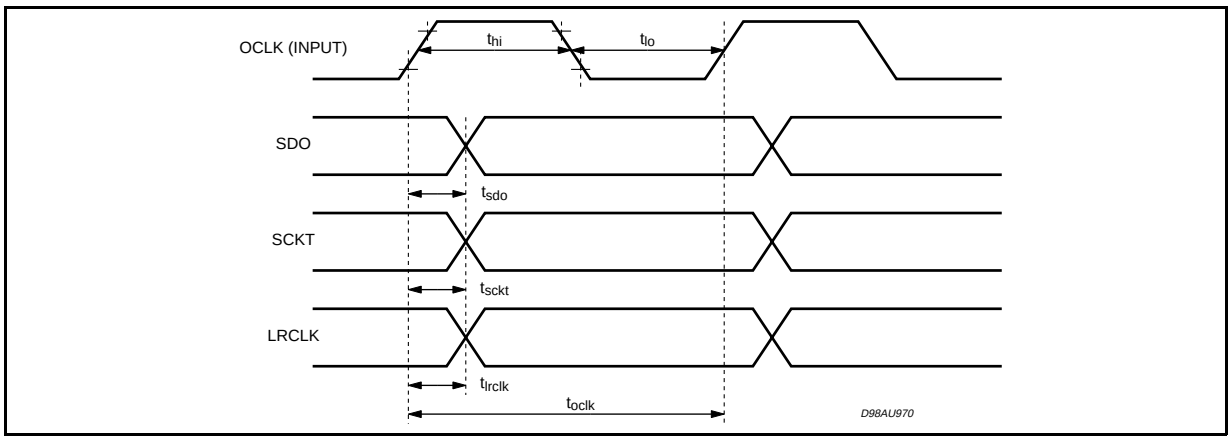
tlrckt = 3.5 + pad_timing (Cload_LRCCKT) - pad_timing (Cload_ OCLK)

**Pad-timing versus load**

| Load (pF) | Pad_timing |
|---|---|
| 25 | 2.90ns |
| 50 | 3.82ns |
| 75 | 4.68ns |
| 100 | 5.52ns |

Cload_XXX is the load in pF on the XXX output. pad_timing (Cload_XXX) is the propagation delay added to the XXX pad due to the load.

b) OCLK in input.




Thi min = 3ns

Tlo min = 3ns

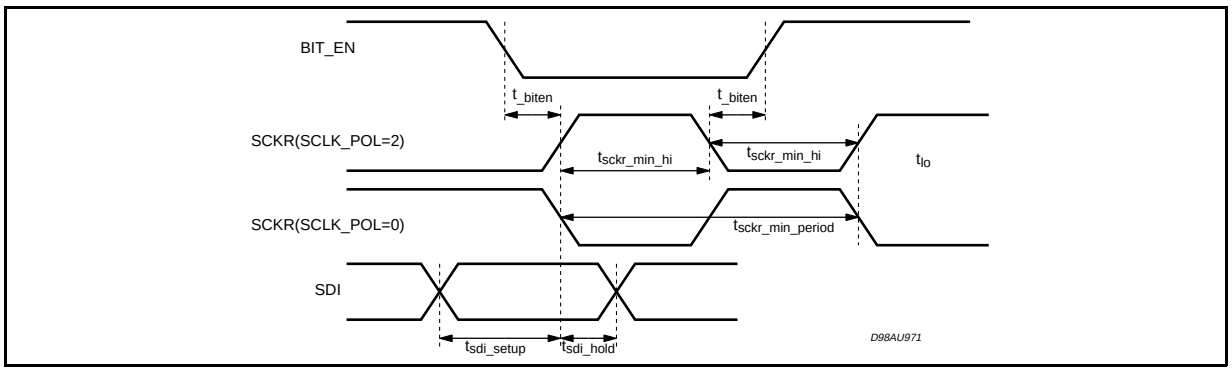
Toclk min = 25ns

tsdo = 5.5 + pad_timing (Cload_SDO) ns

tsckt = 6 + pad_timing (Cload_SCKT) ns

tlrckt = 5.5 + pad_timing (Cload_LRCKT) ns

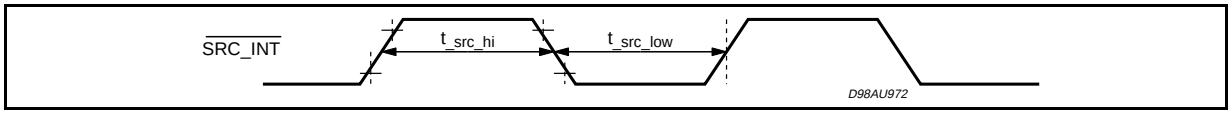
### 5.4.2. Bitstream input interface (SDI, SCKR, BIT_EN)




tsdi_setup_min = 2ns
tsdi_hold_min = 3ns
tsckr_min_hi = 10ns
tsckr_min_low = 10ns
tsckr_min_lperiod = 50ns
t_biten (min) = 2ns

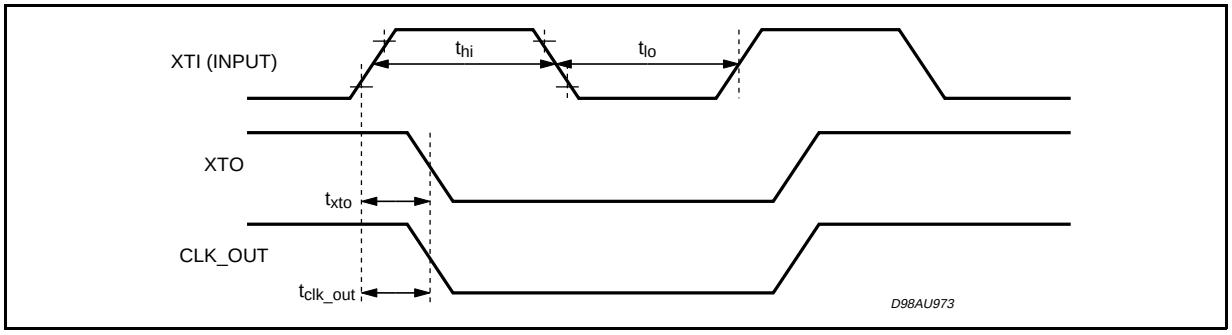
### 5.4.3. SRC_INT

This is an asynchronous input used in "broadcast' mode.
**SRC_INT is active low**




t_src_low min duration is 50ns (1DSP clock period)
t_src_high min duration is 50ns (1DSP clock period)

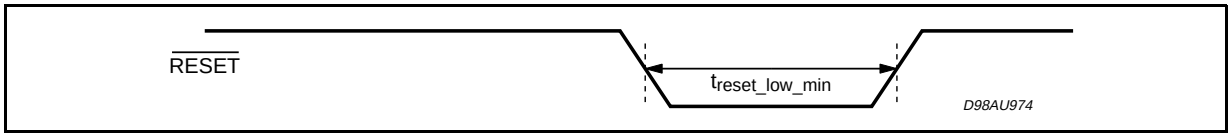
### 5.4.4. XTI,XTO and CLK_OUT timings




txto = 1.40 + pad_timing (Cload_XTO) ns

### 5.4.5. $\overline{\text{RESET}}$

The Reset min duration (t_reset_low_min) is 100ns



### 5.5 DAC RELATED REGISTERS CONFIGURATION

The different DAC registers must be configured for 48kHz audio frequency: this is the reference frequency. The STA003T will use these parameters to derivate the register configurations for the other audio frequencies (32, 24, 16, 12, 8 KHz) according to the bistream informations.

The STA003T DAC and PLL register must be configured according to the following steps:

1) OCLK_Freq determination from the DAC oversampling factor O_FAC.
   As all STA003T registers must be configured for 48KHz reference frequency, the OCLK frquency is:
   OCLK_Freq = O_FAC · 48KHz
   ex: O_FAC = 384, OCLK_Freq = 18.432MHz

2) PCMDIVIDER (0 x 54) register configuration.
   The PCMDIVIDER register is used to configure the frequency ratio between OCLK_Freq and SCKT_Freq:

$$SCKT\_Freq = \frac{OCLK\_Freq}{(2 \cdot (1 + PCMDIVIDER))}$$

   The SCKT signal is the bit clock for the DAC serial output. The SCKT frequency depends on the number of bits to be transmitted to the DAC during one LRCKT (Left/Right clock) clock period. These number of bit depends on the DAC precision (16, 18, 20 or 24bits) and on the mode that is used to transmit the data to the DAC (see figure 8). Once the PCMCONF register is set according to the DAC requirements, the number of SCKT clock periods per LRCKT clock period is 16x2 or 32x2.

   a) LRCKT_period = 16x2 SCKT_periods

   SCKT_Freq = LRCKT_Freq · 32 =

$$= \frac{OCLK\_Freq}{(2 \cdot (1+PCMDIVIDER))}$$

   As the reference audio frequency is 48 KHz, the previous relation becomes:
   48KHz · 32 = 48kHz · O_FAC (2 · (1+ PCMDIVIDER))

   Consequently:

   PCMDIVIDER = (O_FAC/64)-1
   ex: O_FAC = 384, PCMCONF[1:0] = 00, PCMDIVIDER = 5

   b) LRCKT_period = 32x2 SCKT_periods

   SCKT_Freq = LRCKT_Freq · 64 =

$$= \frac{OCLK\_Freq}{(2 \cdot (1+PCMDIVIDER))}$$

   Consequently:

   PCMDIVIDER = (O_FAC/128)-1

3) Configuration of the PLL registers to set OCLK_FREQ to the desired value computed in step 1.
   The PLL configuration in direct relation with the XTI input clock frequency (14.72 MHz).

$$OCLK\_freq = \left(\frac{1}{1 + MFSDF(X)}\right) \cdot \left(\frac{14.72MHz}{1 + PLLCTL\_N}\right) \cdot \left(PLLCTL\_M + 1 + \frac{PLLFRAC}{65536}\right)$$

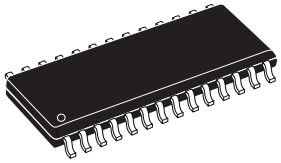
* MFSDF(X) is the value of the MFSDF(X)(0x61) register.
* PLLCTL_N is the value of the PLLCTL_N (0x07) register.
* PLLCTL_M is the value of the PLLCTL_N (0x07) register.
* PLLFRAC (decimal) is the value of the PLLFRAC_H and PLLFRAC_L registers as PLLFRAC = 256 · PLLFRAC_H + PLLFRAC_L.

The following table gives the possible values for these registers according to different OCLK_Freq values. Other values can be supported on request to STMicroelectronics.

| O_FAC | OCLK_Freq at 48KHz | PLLCTL_N | PLLCTL_M | PLLFRAC | MFSDF |
|---|---|---|---|---|---|
| 128 | 6.144MHz | 0 | 12 | 23365 | 31 |
| 256 | 12.288MHz | 0 | 12 | 23365 | 15 |
| 384 | 18.432MHz | 0 | 11 | 34193 | 9 |

| DIM. | mm | | | inch | | |
|---|---|---|---|---|---|---|
| | MIN. | TYP. | MAX. | MIN. | TYP. | MAX. |
| A | | | 2.65 | | | 0.104 |
| a1 | 0.1 | | 0.3 | 0.004 | | 0.012 |
| b | 0.35 | | 0.49 | 0.014 | | 0.019 |
| b1 | 0.23 | | 0.32 | 0.009 | | 0.013 |
| C | | 0.5 | | | 0.020 | |
| c1 | 45° (typ.) | | | | | |
| D | 17.7 | | 18.1 | 0.697 | | 0.713 |
| E | 10 | | 10.65 | 0.394 | | 0.419 |
| e | | 1.27 | | | 0.050 | |
| e3 | | 16.51 | | | 0.65 | |
| F | 7.4 | | 7.6 | 0.291 | | 0.299 |
| L | 0.4 | | 1.27 | 0.016 | | 0.050 |
| S | 8 ° (max.) | | | | | |

## OUTLINE AND MECHANICAL DATA



**SO28**