NOTIFICATION OF REVISIONS

ORIGINATOR: Samsung Electronics, SOC Development Group, Ki-Heung, South Korea

PRODUCT NAME: S3C2440A RISC Microcontroller

DOCUMENT NAME: S3C2440A User's Manual, Revision xx

DOCUMENT NUMBER:

EFFECTIVE DATE:

SUMMARY: As a result of additional product testing and evaluation, some specifications published in the S3C2440A User's Manual, Revision 0.01, have been changed. These changes are described in detail in the *Revision Descriptions* section below.

DIRECTIONS: Please note the changes in your copy (copies) of the S3C2440A User's Manual, Revision 0.01 or, simply attach the *Revision Descriptions* of the next page to S3C2440A User's Manual, Revision 0.01

REVISION HISTORY

Revision	Date	Remark
0.01	September xx, 2003	1st preliminary specification. This is the first edition.
0.08	October 21, 2003	Modified for S3C2440A
0.09	January 15, 2004	2nd update for S3C2440A
0.10	January 27, 2004	3rd update for S3C2440A
0.12	March 15, 2004	4th update for S3C2440A
0.13	June 3, 2004	5th update for S3C2440A
0.14	June 30, 2004	6th update for S3C2440A

REVISION DESCRIPTIONS

ERRATA FROM S3C2440A USER'S MANUAL

This document contains compilation of device and documentation errata, specification clarifications and changes. This document is intended for Hardware system manufacturers, Application software developers and Operating system analyst.

This document may also contain information that was not previously published.

[FORMAT]

<NO.> <CHAPTER> : <PAGE> : <CHANGED_ITEM> : <CHANGED_DATE>

<CHANGED DESCRIPTIONS>

✓ **CLOCK & POWER MANAGEMENT: <7-24> : CLOCK DIVIDER CONTROL (CLKDIVN) REGISTER : 10/21/2003**

Changed the following bit description

CLKDIVN	Bit	Description	Initial State
HDIVN	[2:1]	00: HCLK = FCLK/1. 01: HCLK = FCLK/2. 10: HCLK = FCLK/4 when CAMDIVN[9] = 0. HCLK= FCLK/8 when CAMDIVN[9] = 1. 11: HCLK = FCLK/3 when CAMDIVN[8] = 0. HCLK = FCLK/6 when CAMDIVN[8] = 1.	00

✓ **CLOCK & POWER MANAGEMENT: <7-25> : CAMERA CLOCK DIVIDER (CAMDIVN) REGISTER : 10/21/2003**

Added the following bit description

CAMDIVN	Bit	Description	Initial State
HCLK4_HALF	[9]	HDIVN division rate change bit, when CLKDIVN[2:1]=10b. 0: HCLK = FCLK/4 1: HCLK= FCLK/8 Refer CLKDIV Register.	0
HCLK3_HALF	[8]	HDIVN division rate change bit, when CLKDIVN[2:1]=11b. 0: HCLK = FCLK/3 1: HCLK= FCLK/6 Refer CLKDIV Register.	0

✓ **GPIO: <9-24/25> : MISCCR : 1/15/2004**

MISCCR	Bit	Description	Reset Value
CLKSEL1	[10:8]	000 = Select MPLL output clock with CLKOUT1 pad 001 = Select UPLL output with CLKOUT1 pad 010 = Select RTC clock output with CLKOUT1 pad 011 = Select HCLK with CLKOUT1 pad 100 = Select PCLK with CLKOUT1 pad 101 = Select DCLK1 with CLKOUT1 pad 11x = Reserved	000
Reserved	[7]	–	0
CLKSEL0	[6:4]	000 = Select MPLL INPUT Clock(XTAL) output with CLKOUT0 pad 001 = Select UPLL output with CLKOUT0 pad 010 = Select FCLK with CLKOUT0 pad 011 = Select HCLK with CLKOUT0 pad 100 = Select PCLK with CLKOUT0 pad 101 = Select DCLK0 with CLKOUT0 pad 11x = Reserved	010

✓ **GPIO: <9-35> : GSTATUS1 : 10/21/2003**

GSTATUS1	Bit	Description
CHIP ID	[0]	ID register = 0x32440001

✓ **GPIO: <9-4> : PORT E : 10/23/2003**

Added signal names on AC97 Interface as follows.

GPE4	Input/output	I2SSDO	AC_SDATA_OUT	–
GPE3	Input/output	I2SSDI	AC_SDATA_IN	–
GPE2	Input/output	CDCLK	AC_nRESET	–
GPE1	Input/output	I2SSCLK	AC_BIT_CLK	–
GPE0	Input/output	I2SLRCK	AC_SYNC	–

✓ **GPIO: <9-15> : PORT E CONTROL REGISTERS : 10/23/2003**

Added AC97 port setting as follows

GPE4	[9:8]	00 = Input 10 = I2SDO	01 = Output 11 = AC_SDATA_OUT
GPE3	[7:6]	00 = Input 10 = I2SDI	01 = Output 11 = AC_SDATA_IN
GPE2	[5:4]	00 = Input 10 = CDCLK	01 = Output 11 = AC_nRESET
GPE1	[3:2]	00 = Input 10 = I2SSCLK	01 = Output 11 = AC_BIT_CLK
GPE0	[1:0]	00 = Input 10 = I2SLRCK	01 = Output 11 = AC_SYNC

✓ **INTERRUPT: <14-XX> : INTERRUPT SOURCE NUMBERS : 10/23/2003**

The interrupt source numbers are changed from 59 to 60.

✓ **INTERRUPT: <14-XX> : INT_WDT REGISTER NAME : 10/23/2003**

The INT_WDT bit name is changed as INT_WDT_AC97.

✓ **INTERRUPT: <14-16> : SUBSRCPND: 10/23/2003**

Changed the following bit description

SUBSRCPND	Bit	Description	Initial State
Reserved	[31:15]	Not used	0
INT_AC97	[14]	0 = Not requested, 1 = Requested	0
INT_WDT	[13]	0 = Not requested, 1 = Requested	0

✓ **INTERRUPT: <14-17> : INTSUBMSK: 10/23/2003**

Changed the following bit description

INTSUBMSK	Bit	Description	Initial State
Reserved	[31:15]	Not used	0
INT_AC97	[14]	0 = Service available, 1 = Masked	1
INT_WDT	[13]	0 = Service available, 1 = Masked	1

✓ **OVERVIEW: <1-4> : FEATURES : 10/23/2003**

Features on AC97 Audio-CODEC Interface were added as follows.

AC97 Audio-CODEC Interface

- Support 16-bit samples
- 1-ch stereo PCM inputs/ 1-ch stereo PCM outputs
  1-ch MIC input

✓ **OVERVIEW: <1-5> : Block Diagram : 10/23/2003**

AC97 block was added to the Figure 1-1.

✓ **OVERVIEW: <1-8> : Block Diagram : 10/23/2003**

Changed a word as follows

L8	I2SSDI/AC_SDATA_IN

✓ **OVERVIEW: <1-9> : Block Diagram : 10/23/2003**

Changed words as follows

U6	I2SSDO/AC_SDATA_OUT
R7	I2SSCLK/AC_BIT_CLK
P7	I2SLRCK/AC_SYNC
T7	CDCLK/AC_nRESET

✓ **OVERVIEW: <1-15> : S3C2440A 289-Pin FBGA Pin Assignments : 10/23/2003**

Added signal names on AC97 Interface as follows.

I2SLRCK/AC_SYNC	GPE0	–/–	Hi-z/–	I	t8
I2SSCLK/AC_BIT_CLK	GPE1	–/–	Hi-z/–	I	t8
CDCLK/AC_nRESET	GPE2	–/–	Hi-z/–	I	t8
I2SSDI/AC_SDATA_IN	GPE3	–/–/–	Hi-z/Hi-z/–	I	t8
I2SSDO/AC_SDATA_OUT	GPE4	–/–/–	O(L)/Hi-z/–	I	t8

✓ **OVERVIEW: <1-41> : S3C2440A Special Registers : 10/23/2003**

Added the following Register description

Register Name	Address (B. Endian)	Address (L. Endian)	Acc. Unit	Read/ Write	Function
AC97 Audio-CODEC Interface					
AC_GLBCTRL	0x5B000000	←	W	R/W	AC97 Global Control Register
AC_GLBSTAT	0x5B000004			R	AC97 Global Status Register
AC_CODEC_CMD	0x5B000008			R/W	AC97 Codec Command Register
AC_CODEC_STAT	0x5B00000C			R	AC97 Codec Status Register
AC_PCMADDR	0x5B000010				AC97 PCM Out/In Channel FIFO Address Register
AC_MICADDR	0x5B000014				AC97 Mic In Channel FIFO Address Register
AC_PCMDATA	0x5B000018			R/W	AC97 PCM Out/In Channel FIFO Data Register
AC_MICDATA	0x5B00001C				AC97 MIC In Channel FIFO Data Register

✓ **OVERVIEW : <1-23> : S3C2440A SIGNAL DESCRIPTIONS : 11/10/2003**

Table 1-3. S3C2440A Signal Descriptions (Sheet 3 of 6)

Signal	I/O	Descriptions
AC'97		
AC_SYNC	O	48 kHz fixed rate sample sync
AC_BIT_CLK	IO	12.288 MHz serial data clock
AC_nRESET	O	AC'97 Master H/W Reset
AC_SDATA_IN	I	Serial, time division multiplexed, AC'97 input stream
AC_SDATA_OUT	O	Serial, time division multiplexed, AC'97 output stream

✓ **OVERVIEW: <1-26>: TABLE 1-3. S3C2440A SIGNAL DESCRIPTIONS (SHEET 6 OF 6) : 1/13/2004**

Table 1-3. S3C2440A Signal Descriptions (Sheet 6 of 6)

Signal	I/O	Description
Power		
VDDalive	P	S3C2440A reset block and port status register VDD (1.2V). It should be always supplied whether in normal mode or in Sleep mode.
VDDiarm	P	S3C2440A core logic VDD(1.2V) for ARM core.
VDDi	P	S3C2440A core logic VDD(1.2V) for Internal block.

✓ **OVERVIEW : <1-32> : S3C2440A SPECIAL REGISTERS : 11/10/2003**

Changed all Special Function Registers of CAMIF

There were two pages of special function register. But, in revision specification there is only one page.

1-32, 33 → 1-32

✓ **CHAPTER NUMBERING: <24, 25, 26> : CH24, CH25, CH26 : 1/12/2004**

The chapters are changed as follows

Chapter 24 is added for AC97
Chapter 25: Bus Priority
Chapter 26: Mechanical Data
Chapter 27: Electrical Data

✓ **INTERRUPT : <14-3> : INTERRUPT SOURCES : 11/10/2003**

INTERRUPT SOURCES

Sources	Descriptions	Arbiter Group
INT_ADC	ADC EOC and Touch interrupt (INT_ADC_S/INT_TC)	ARB5
INT_WDT_AC97	Watch-Dog timer interrupt(INT_WDT, INT_AC97)	ARB1
INT_CAM	Camera Interface (INT_CAM_C, INT_CAM_P)	ARB1

✓ **INTERRUPT : <14-17> : SUB SOURCE PENDING (SUBSRCPND) REGISTER : 11/10/2003**

SUBSRCPND	Bit	Description	Initial State
INT_CAM_P	[12]	0 = Not requested, 1 = Requested	0
INT_CAM_C	[11]	0 = Not requested, 1 = Requested	0
INT_ADC_S	[10]	0 = Not requested, 1 = Requested	0

SRCPND	SUBSRCPND	Remark
INT_ADC	INT_ADC_S, INT_TC	
INT_CAM	INT_CAM_C, INT_CAM_P	
INT_WDT_AC97	INT_WDT, INT_AC97	

✓ **INTERRUPT : <14-17> : SUB SOURCE MASK (INTSUBMSK) REGISTER : 11/10/2003**

INTSUBMSK	Bit	Description	Initial State
INT_CAM_P	[12]	0 = Service available, 1 = Masked	1
INT_CAM_C	[11]	0 = Service available, 1 = Masked	1
INT_ADC_S	[10]	0 = Service available, 1 = Masked	1

✓ **INTERRUPT : <14-4> : INTERRUPT SUB SOURCES : 11/10/2003**

Added a page of interrupt sub sources description

✓ **CLOCK & POWER MANAGEMENT: <7-10> : CLOCK DISTRIBUTION BLOCK DIAGRAM : 11/10/2003**

POWER MANAGEMENT

The Power Management block controls the system clocks by software for reducing the power consumption in S3C2440A. These schemes are related to PLL, clock control logics (FCLK, HCLK, and PCLK) and wakeup signals. Figure 7-7 shows the clock distribution of the S3C2440A.

The S3C2440A has four power modes. The following section describes all the power management modes. The transition between the modes is not allowed freely. Refer Figure 7-8 for available transitions among the modes.

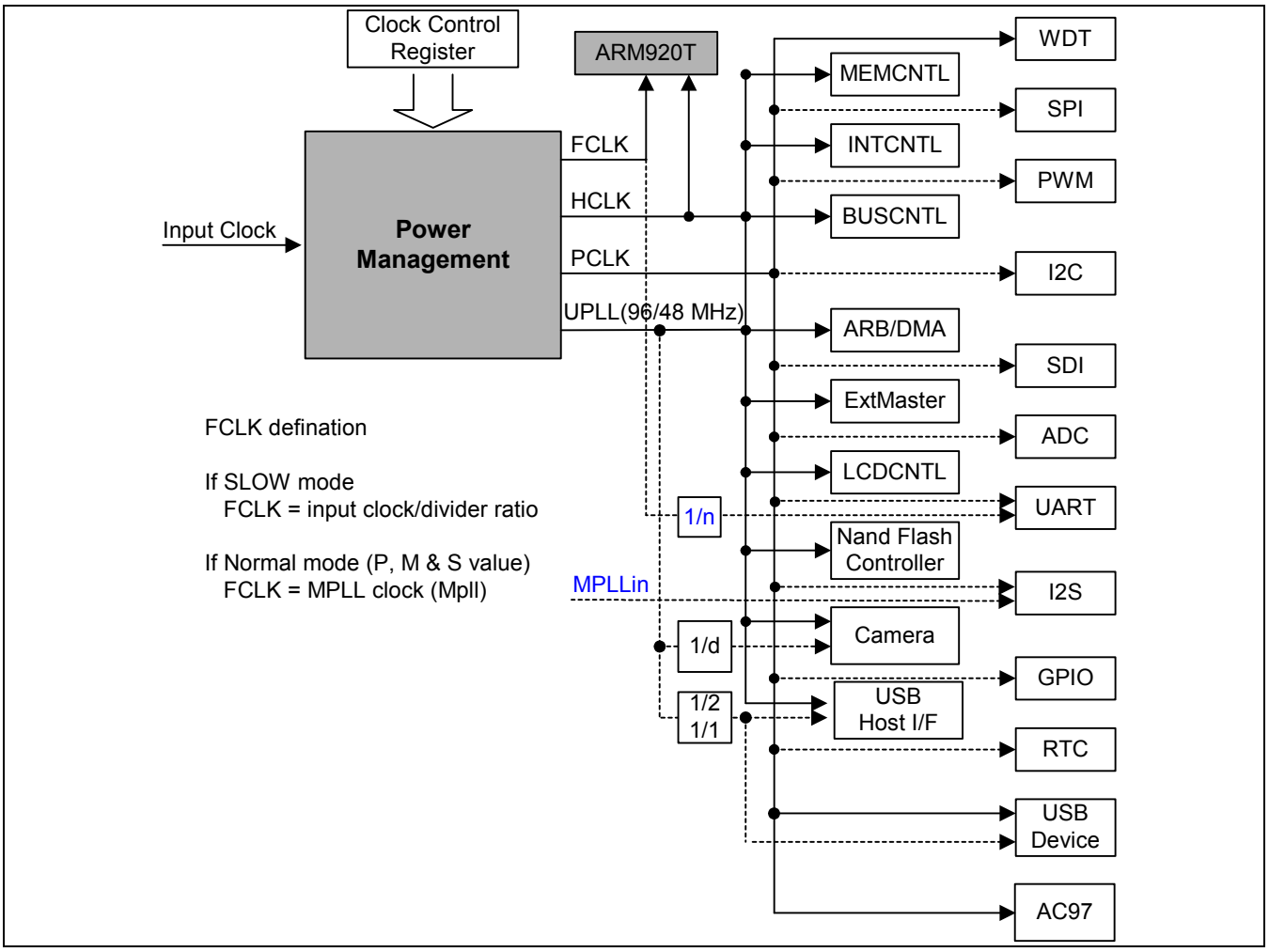

Figure 7-7 Clock Distribution Block Diagram

✓ **ELECTRICAL DATA: <27-1>: TABLE 27-1. ABSOLUTE MAXIMUM RATING: 12/12/2003**

Changed as follows

Table 27-1 Absolute Maximum Rating

Parameter	Symbol	Rating		Unit
DC Supply Voltage	V_{DDi}	1.2V V_{DD}	1.8	V
	V_{DDOP}	3.3V V_{DD}	4.8	
	V_{DDMOP}	1.8V/2.5V/3.0V/3.3V V_{DD}	4.8	
	V_{DDRTC}	1.8V/2.5V/3.0V/3.3V V_{DD}	4.5	
	V_{DDADC}	3.3V V_{DD}	4.8	
DC Input Voltage	V_{IN}	3.3V Input buffer	4.8	
		3.3V Interface / 5V Tolerant input buffer	6.5	
DC Output Voltage	V_{OUT}	3.3V Output buffer	4.8	
DC Input (Latch-up) Current	I_{IN}	± 200		mA
Storage Temperature	T_{STG}	– 65 to 150		°C

✓ **CLOCK&POWER: <7-16> : ITEM 7 : 12/16/2003**

The following sentence in italics is removed.

7. – For EINT[3:0], check the SRCPND register.
   – For EINT[15:4], check the EINTPEND instead of SRCPND (SRCPND will not be set although some bits of EINTPEND are set.).
   – *For alarm wake-up, check the RTC time because the RTC bit of SRCPND isn't set at the alarm wake-up.*
   – If there was nBATT_FLT assertion during SLEEP mode, then corresponding bit of SRCPND has been set.

✓ **CLOCK&POWER: <7-20> : PLL Control Register / Selection guide : 12/16/2003**

Changed as follows

MPLL Control Register

Mpll = (2*m * Fin) / (p * 2^s)
m = (MDIV + 8), p = (PDIV + 2), s = SDIV

UPLL Control Register

Upll = (m * Fin) / (p * 2^s)
m = (MDIV + 8), p = (PDIV + 2), s = SDIV

PLL Value Selection Guide (MPLLCON)

1. F_{out} = 2 * m * Fin / (p*2^s), F_{vco} = m * Fin / p where : m=MDIV+8, p=PDIV+2, s=SDIV
2. 600MHz ≤ F_{VCO} ≤ 1.2GHz
3. 200MHz ≤ $FCLK_{OUT}$ ≤ 600MHz
4. Do not set the P or M value as zero, i.e. P=000000, M=00000000 can cause malfunction of the PLL.
5. The proper range of P and M: 1 ≤ P ≤ 62, 1 ≤ M ≤ 248

✓ **I/O Port: <9-26> : DCLK CONTROL REGISTERS(DCLKCON) : 12/16/2003**

Changed as follows

DCLKCON	Bit	Description
DCLK1CMP	[27:24]	DCLK1 Compare value clock toggle value.(< DCLK1DIV) If the DCLK1CMP is n, Low level duration is(n + 1), High level duration is((DCLK1DIV + 1) –(n +1))
DCLK0CMP	[11:8]	DCLK0 Compare value clock toggle value.(< DCLK0DIV) If the DCLK0CMP is n, Low level duration is(n + 1), High level duration is((DCLK0DIV + 1) –(n +1))

✓ **I/O Port: <9-24> : MISCELLANEOUS CONTROL REGISTER (MISCCR) : 12/16/2003**

Changed as follows

MISCELLANEOUS CONTROL REGISTER (MISCCR)

MISCCR	Bit	Description	Reset Value
Reserved	[24]	Reserve to 0.	0
Reserved	[23]	Reserve to 0.	0
BATT_FUNC	[22:20]	Battery fault function selection 0XX: In nBATT_FLT=0, system will be in reset status 10X: In sleep mode, when nBATT_FLT=0, system will wake-up. 110: In sleep mode, when nBATT_FLT=0, system will ignore all the wake-up events. 111: nBATT_FLT function disable.	000

✓ **CLOCK & POWER MANAGEMENT: <7-21> : PLL Value Selection Table : 12/16/2003**

Changed the following table

PLL VALUE SELECTION TABLE

It is not easy to find a proper PLL value. So we recommend you to refer the following table.

Input Frequency	Output Frequency	MDIV	PDIV	SDIV
12.0000 MHz	**48.00 MHz** (Note)	56 (0X38)	2	2
12.0000 MHz	**96.00 MHz** (Note)	56 (0x38)	2	1
12.0000 MHz	**271.50 MHz**	173 (0xad)	2	2
12.0000 MHz	**304.00 MHz**	68 (0x44)	1	1
12.0000 MHz	**405.00 MHz**	127 (0x7f)	2	1
12.0000 MHz	**532.00 MHz**	125 (0x7d)	1	1
16.9344 MHz	**47.98 MHz** (Note)	60 (0x3c)	4	2
16.9344 MHz	**95.96 MHz** (Note)	60 (0x3c)	4	1
16.9344 MHz	**266.72 MHZ**	118 (0x76)	2	2

16.9344 MHz	**296.35 MHZ**	97 (0x61)	1	2
16.9344 MHz	**399.65 MHz**	110 (0x6e)	3	1
16.9344 MHz	**530.61 MHz**	86 (0x56)	1	1

✓ **Overviw: <1-9> : Table 1-1. 289-Pin FBGA Pin Assignments – Pin Number Order (Sheet 3 of 3) : 12/19/2003**

Changed the table as follows

Table 1-1. 289-Pin FBGA Pin Assignments – Pin Number Order (Sheet 3 of 3)

Pin Number	Pin Name	Pin Number	Pin Name	Pin Number	Pin Name

…

N7	VD22/nSS1/GPD14	R7	I2SSCLK/AC_BIT_CLK	U7	VSSiarm
N8	SDCLK/GPE5	R8	SDDAT0/GPE7	U8	IICSCL/GPE14
N9	EINT8/GPG0	R9	CLKOUT0/GPH9	U9	VSSOP
N10	EINT18/nCTS1/GPG10	R10	EINT11/nSS1/GPG3	U10	VSSiarm
N11	DP0	R11	EINT14/SPIMOSI1/GPG6	U11	VDDi
N12	DN1/PDN0	R12	NCON	U12	EINT19/TCLK1/GPG11

✓ **MEMORY CONTROLLER: <5-17> : REFRESH CONTROL REGISTER : 01/05/2004**

Changed the table as follows

REFRESH CONTROL REGISTER

Register	Address	R/W	Description	Reset Value
REFRESH	0x48000024	R/W	SDRAM Refresh Control Register	0xAC0000

REFRESH	Bit	Description	Initial State
REFEN	[23]	SDRAM Refresh Enable 0 = Disable 1 = Enable (self or CBR/auto refresh)	1
TREFMD	[22]	SDRAM Refresh Mode 0 = CBR/Auto Refresh 1 = Self Refresh In self-refresh time, the SDRAM control signals are driven to the appropriate level.	0
Trp	[21:20]	SDRAM RAS pre-charge Time 00 = 2 clocks 01 = 3 clocks 10 = 4 clocks 11 = Not support	10
Tsrc	[19:18]	SDRAM Semi Row cycle time 00 = 4 clocks 01 = 5 clocks 10 = 6 clocks 11 = 7 clocks SDRAM Row cycle time: Trc=Tsrc+Trp If Trp=3clocks & Tsrc=7clocks, Trc=3+7=10clocks.	11

✓ **CLOCK & POWER MANAGEMENT: <7-4> : USUAL CONDITIONS FOR PLL & CLOCK GENERATOR : 01/05/2004**

Changed the table as follows

Usual Conditions for PLL & Clock Generator

PLL & Clock Generator generally uses the following conditions.

Loop filter capacitance	C_{LF}	MPLLCAP: 1.3 nF
		UPLLCAP: 700 pF
External X-tal frequency	–	12 – 20 MHz (note)
External capacitance used for X-tal	C_{EXT}	15 – 22 pF

NOTES:
1. The value could be changed.
2. FCLK must be more than 200MHz.

✓ **CLOCK & POWER MANAGEMENT: <7-17> : POWER CONROL OF VDDI AND VDDIARM : 01/05/2004**

The following Note is added at the end of page.

NOTE: In Sleep mode, if you do not use the Touch Screen panel, then Touch ports (XP, XM, YP, and YM) must be floating, i.e. Touch ports (XP, XM, YP, and YM) should not be connected to other signal or power of external device.

✓ **CLOCK & POWER MANAGEMENT: <7-25> : CAMERA CLOCK DIVIDER(CAMDIVN) REGISTER : 01/05/2004**

Changed the table as follows

CAMERA CLOCK DIVIDER (CAMDIVN) REGISTER

Register	Address	R/W	Description	Reset Value
CAMDIVN	0x4C000018	R/W	Camera clock divider register	0x00000000

CAMDIVN	Bit	Description	Initial State
DVS_EN	[12]	DVS(Dynamic Voltage Scaling) enable register 0:DVS OFF (FCLK = MPLL clock) 1:DVS ON (FCLK = HCLK)	0
Reserved	[11:10]		0

✓ **CLOCK & POWER MANAGEMENT: <7-3> : CLOCK GENERATOR BLOCK DIAGRAM : 01/09/2004**

CLKOUT scheme part is changed in Block diagram (where is the figure?)

Figure 7-1. Clock Generator Block Diagram

✓ **CLOCK & POWER MANAGEMENT: <7-4> : PHASE LOCKED LOOP (PLL): 01/12/2004**

Mpll calculation equation is changed as follows.

PHASE LOCKED LOOP (PLL)

The MPLL within the clock generator, as a circuit, synchronizes an output signal with a reference input signal in frequency and phase. In this application, it includes the following basic blocks as shown in the Figure 7-2: the Voltage Controlled Oscillator (VCO) to generate the output frequency proportional to input DC voltage, the divider P to divide the input frequency (Fin) by p, the divider M to divide the VCO output frequency by m which is input to Phase Frequency Detector (PFD), the divider S to divide the VCO output frequency by s which is the Mpll (output frequency from MPLL block), the phase difference detector, the charge pump, and the loop filter. The output clock frequency Mpll is related to the reference input clock frequency Fin by the following equation:

Mpll = $(2*m * Fin) / (p * 2^s)$
m = M (the value for divider M)+ 8, p = P (the value for divider P) + 2

✓ **CLOCK & POWER MANAGEMENT: <7-8> : FCLK, HCLK, and PCLK : 01/12/2004**

The table is changed as follows

HDIVN	PDIVN	HCLK3_HALF/ HCLK4_HALF	FCLK	HCLK	PCLK	Divide Ratio
0	0	-	FCLK	FCLK	FCLK	1 : 1 : 1 (Default)
0	1	-	FCLK	FCLK	FCLK / 2	1 : 1 : 2
1	0	-	FCLK	FCLK / 2	FCLK / 2	1 : 2 : 2
1	1	-	FCLK	FCLK / 2	FCLK / 4	1 : 2 : 4
3	0	0 / 0	FCLK	FCLK / 3	FCLK / 3	1 : 3 : 3
3	1	0 / 0	FCLK	FCLK / 3	FCLK / 6	1 : 3 : 6
3	0	1 / 0	FCLK	FCLK / 6	FCLK / 6	1 : 6 : 6
3	1	1 / 0	FCLK	FCLK / 6	FCLK / 12	1 : 6 : 12
2	0	0 / 0	FCLK	FCLK / 4	FCLK / 4	1 : 4 : 4
2	1	0 / 0	FCLK	FCLK / 4	FCLK / 8	1 : 4 : 8
2	0	0 / 1	FCLK	FCLK / 8	FCLK / 8	1 : 8 : 8
2	1	0 / 1	FCLK	FCLK / 8	FCLK / 16	1 : 8 : 16

After setting PMS value, it is required to set the CLKDIVN register. The value set for CLKDIVN will be valid after the PLL lock time. The value is also available for reset and changing the Power Management Mode. The setting value can also be valid after 1.5 HCLK. Only, 1HCLK can validate the value of CLKDIVN register changed from Default (1:1:1) to other Divide Ratio (1:1:2, 1:2:2, 1:2:4)

✓ **CLOCK & POWER MANAGEMENT: <7-16> : Follow the Procedure to Wake-up from SLEEP mode : 01/12/2004**

One item in #7 is eliminated as follows.

7. – For EINT[3:0], check the SRCPND register.
   – For EINT[15:4], check the EINTPEND instead of SRCPND (SRCPND will not be set even though some bits of EINTPEND are set.).

✓ **CLOCK & POWER MANAGEMENT: <7-10>: Figure 7-7. The Clock Distribution Block Diagram : 01/12/2004**

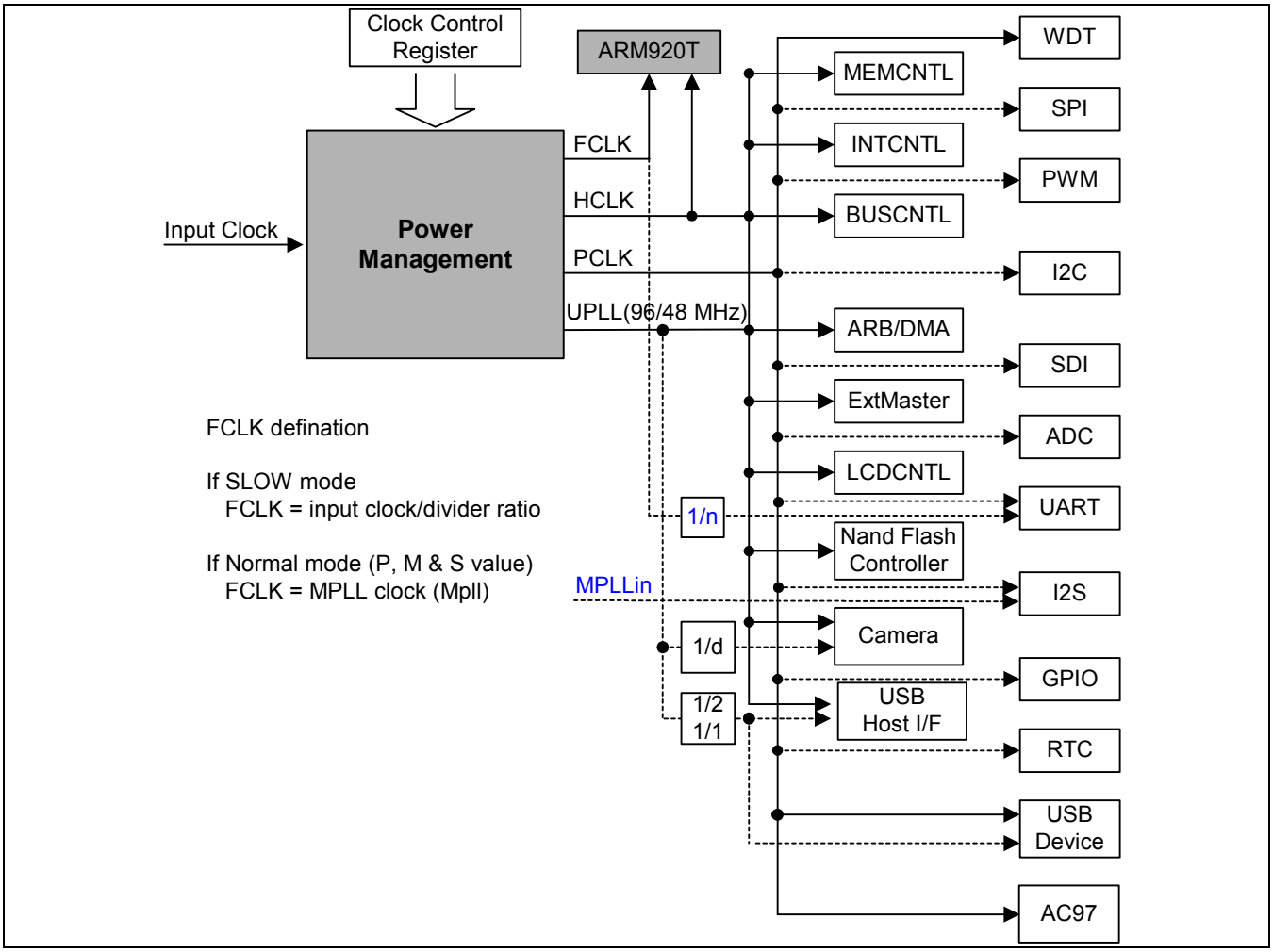

Figure 7-7. The Clock Distribution Block Diagram

✓ **IIS-BUS INTERFACE: <21-4> : Sampling Frequency And Master Clock : 01/13/2004**

The following sentence is changed.

Master clock frequency (PCLK or MPLLin) can be selected by sampling frequency as shown in Table 21-1. Because Master clock is made by IIS prescaler, the prescaler value and Master clock type (256 or 384fs) should be determined properly. Serial bit clock frequency type (16/32/48fs) can be selected by the serial bit per channel and Master clock as shown in Table 21-2.

✓ **IIS-BUS INTERFACE: <21-6> : IIS MODE REGISTER (IISMOD) REGISTER : 01/13/2004**

The following item is added

IISMOD	Bit	Description	Initial State
Master Clock Select	[9]	Master clock select 0 = PCLK, 1 = MPLLin	0

✓ **IIS-BUS INTERFACE: <21-2> : Block diagram : 01/16/2004**

The following block diagram is changed.

BLOCK DIAGRAM

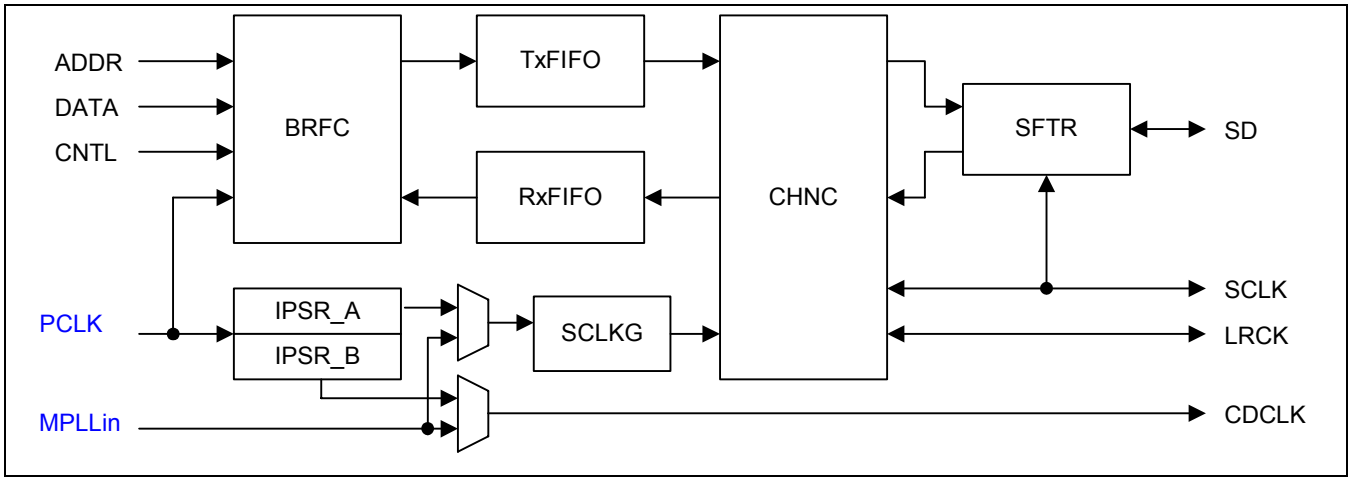

Figure 21-1. IIS-Bus Block Diagram

✓ **ELECTRICAL DATA : <27-31> : FIGURE 27-32 IIS INTERFACE TIMING : 1/15/2004**

The figure concerning IIS timing is changed as follows.

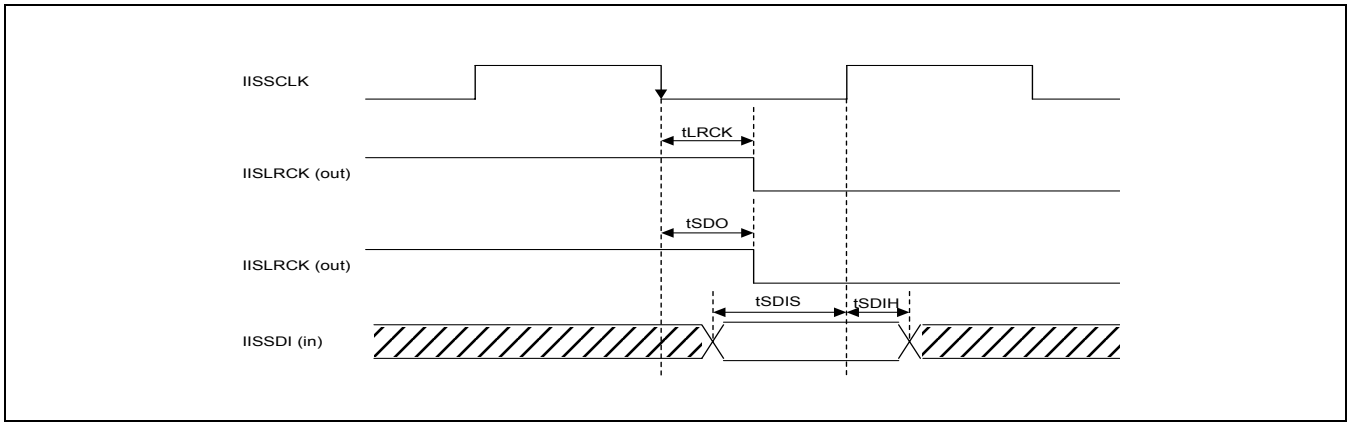

Figure 27-32. IIS Interface Timing

✓ **ELECTRICAL DATA : <27-34 ~ 27-39> : TABLE 27-7,8,9,10,11,13,15,16 : 1/15/2004**

The following table contents are changed.

Table 27-7. Clock Timing Constants
Table 27-8. ROM/SRAM Bus Timing Constants
Table 27-9. Memory Interface Timing Constants (3.3V)
Table 27-10. External Bus Request Timing Constants
Table 27-11. DMA Controller Module Signal Timing Constants
Table 27-13. IIS Controller Module Signal Timing Constants
Table 27-15. SD/MMC Interface Transmit/Receive Timing Constants
Table 27-16. SPI Interface Transmit/Receive Timing Constants

✓ **IIC: <20-9,10> : FIGURE 20-8,9 : 10/22/2003**

Figure 20-8 Operations for Slave/Transmitter Mode

Figure 20-9 Operations for Slave/Receiver Mode

Change return point after interrupt is pending.

✓ **SPI: <22-1> : FEATURES : 10/22/2003**

FEATURES

— 5V tolerant input except the nSS

✓ **UART: <11-3> : DATA RECEPTION : 10/22/2003**

Data Reception

Like transmission, data frame for reception is also programmable. It consists of a start bit, 5 to 8 data bits, an optional parity bit and 1 to 2 stop bits in the line control register (ULCONn). The receiver can detect overrun error, parity error, frame error and break condition, each of which can set an error flag.

— The overrun error indicates that new data has overwritten the old data before the old data has been read.

— The parity error indicates that the receiver has detected an unexpected parity condition.

— The frame error indicates that the received data does not have a valid stop bit.

— The break condition indicates that the RxDn input is held in logic 0 state for a duration longer than one frame transmission time.

Receive time-out condition occurs when it does not receive any data during the 3 word time (this interval follows the setting of Word Length bit) and the Rx FIFO is not empty in the FIFO mode.

✓ **UART: <11-5> : INTERRUPT/DMA REQUEST GENERATION, TABLE 11-1 : 10/22/2003**

Interrupt/DMA Request Generation

Each UART of the S3C2440A has seven status (Tx/Rx/Error) signals: Overrun error, Parity error, Frame error, Break, Receive buffer data ready, Transmit buffer empty, and Transmit shifter empty, all of which are indicated by the corresponding UART status register (UTRSTATn/UERSTATn).

The overrun error, parity error, frame error and break condition are referred to as the receive error status, each of which can cause the receive error status interrupt request, if the receive-error-status-interrupt-enable bit is set to one in the control register, UCONn. When a receive-error-status-interrupt-request is detected, the signal causing the request can be identified by reading the value of UERSTSTn.

Table 11-1 Interrupts in Connection with FIFO

Type	FIFO Mode	Non-FIFO Mode
Error Interrupt	Generated when frame error, parity error, or break signal are detected. Generated when it gets to the top of the receive FIFO without reading the data in it (overrun error).	Generated by all errors. However if another error occurs at the same time, only one interrupt is generated.

✓ **UART: <11-6> : UART ERROR STATUS FIFO : 10/22/2003**

Inserted this page

✓ **UART : <11-7> : UART BAUD-RATE GENERATOR ERROR TOLERANCE : 10/27/2003**

Added a section at the middle of this page as follows

Baud-Rate Error Tolerance

UART Frame error should be less than 1.87%(3/160).

tUPCLK = (UBRDIVn + 1) x 16 x 10 / PCLK tUPCLK : Real UART clock time

tUEXACT = 10 / baud-rate tUEXACT : Ideal UART clock time

UART error = (tUPCLK – tUEXACT) / tUEXACT x 100%

NOTE.

1. 1Frame = 1start bit + 8 data bit + 1 stop bit.
2. In specific condition, we can support bit rates up to 921.6K bps. For example, when PCLK is 60MHz, you can use bit rates of 921.6K bps under UART error of 1.69%.

✓ **UART: <11-11> : UCONN REGISTER: 10/22/2003**

UCONn	Bit	Description	Initial State
Clock Selection	[11:10]	Select PCLK, UARTCLK or UCLK for the UART baud rate. UBRDIVn = (int)(selected clock / (baudrate x 16)) –1 00, 10 = PCLK 01 = UARTCLK 11 = UCLK	0
Rx Error Status Interrupt Enable	[6]	Enable UART to generate an interrupt upon an exception, such as a break, frame error, parity error, or overrun error during a receive operation. 0 = Do not generate receive error status interrupt. 1 = Generate receive error status interrupt.	0
Send Break Signal	[4]	Setting this bit causes the UART to send a break during 1 frame time. This bit is automatically cleared after sending the break signal. 0 = Normal transmit 1 = Send break signal	0

✓ **UART: <11-16> : UERSTATN REGISTER: 10/22/2003**

UERSTATn	Bit	Description	Initial State
Break Detect	[3]	Set to 1 automatically to indicate that a break signal has been received. 0 = No break receive 1 = Break receive (Interrupt is requested.)	0
Frame Error	[2]	Set to 1 automatically whenever a frame error occurs during receive operation. 0 = No frame error during receive 1 = Frame error (Interrupt is requested.)	0
Parity Error	[1]	Set to 1 automatically whenever a parity error occurs during receive operation. 0 = No parity error during receive 1 = Parity error (Interrupt is requested.)	0

Note: These bits (UERSATn[3:0]) are automatically cleared to 0 when the UART error status register is read.

✓ **UART: <11-18> : UMSTAT0 REGISTER : 10/22/2003**

UMSTAT0	Bit	Description	Initial State
Delta CTS	[4]	Indicate that nCTS input to S3C2440A has changed state since the last time it was read by CPU. (Refer Figure 11-8.) 0 = Has not changed 1 = Has changed	0
Reserved	[3:1]		0

✓ **LCD : <15-10,11> : MEMORY DATA FORMAT (STN, BSWP=0) : 10/30/2003**

Added a section at the middle of this page as follows

In 4096 level color mode:

Packed 12 BPP Color mode

12 bits (4 bits of red, 4 bits of green, 4 bits of blue) of video data correspond to 1 pixel. The following table shows the color data format in words: (Video data must reside at 3 word boundaries (8 pixels), as follows)

RGB order

DATA	[31:28]	[27:24]	[23:20]	[19:16]	[15:12]	[11:8]	[7:4]	[3:0]
Word #1	Red(1)	Green(1)	Blue(1)	Red(2)	Green(2)	Blue(2)	Red(3)	Green(3)
Word #2	Blue(3)	Red(4)	Green(4)	Blue(4)	Red(5)	Green(5)	Blue(5)	Red(6)
Word #3	Green(6)	Blue(6)	Red(7)	Green(7)	Blue(7)	Red(8)	Green(8)	Blue(8)

Unpacked 12 BPP Color mode

12 bits (4 bits of red, 4 bits of green, 4 bits of blue) of video data correspond to 1 pixel. The following table shows the color data format in words:

RGB order

DATA	[31:28]	[27:24]	[23:20]	[19:16]	[15:12]	[11:8]	[7:4]	[3:0]
Word #1		Red(1)	Green(1)	Blue(1)		Red(2)	Green(2)	Blue(2)
Word #2		Red(3)	Green(3)	Blue(3)		Red(4)	Green(4)	Blue(4)
Word #3		Red(5)	Green(5)	Blue(5)		Red(6)	Green(6)	Blue(6)

16 BPP Color mode

16 bits (5 bits of red, 6 bits of green, 5 bits of blue) of video data correspond to 1 pixel. But, stn controller will use only 12 bit color data. It means that only upper 4 bit color data will be used as pixel data (R[15:12], G[10:7], B[4:1]). The following table shows the color data format in words:

RGB order

DATA	[31:28]	[27:21]	[20:16]	[15:11]	[10:5]	[4:0]
Word #1	Red(1)	Green(1)	Blue(1)	Red(2)	Green(2)	Blue(2)
Word #2	Red(3)	Green(3)	Blue(3)	Red(4)	Green(4)	Blue(4)
Word #3	Red(5)	Green(5)	Blue(5)	Red(6)	Green(6)	Blue(6)

✓ **LCD : <15-27> : LCD Control 1 Register : 10/30/2003**

LCDCON1	Bit	Description	Initial State
BPPMODE	[4:1]	Select the BPP (Bits Per Pixel) mode. 0000 = 1 bpp for STN, Monochrome mode 0001 = 2 bpp for STN, 4-level gray mode 0010 = 4 bpp for STN, 16-level gray mode 0011 = 8 bpp for STN, color mode (256 color) 0100 = packed 12 bpp for STN, color mode (4096 color) 0101 = unpacked 12 bpp for STN, color mode (4096 color) 0110 = 16 bpp for STN, color mode (4096 color) 1000 = 1 bpp for TFT 1001 = 2 bpp for TFT 1010 = 4 bpp for TFT 1011 = 8 bpp for TFT 1100 = 16 bpp for TFT 1101 = 24 bpp for TFT	0000

✓ **SPI : <22-8> : SPI PIN CONTROL REGISTER : 01/09/2004**

Register	Address	R/W	Description	Reset Value
SPPIN0	0x59000008	R/W	SPI channel 0 pin control register	0x00
SPPIN1	0x59000028	R/W	SPI channel 1 pin control register	0x00

SPPINn	Bit	Description	Initial State
Reserved	[7:3]		
Multi Master error detect Enable (ENMUL)	[2]	The /SS pin is used as an input to detect multi master error when the SPI system is a master. 0 = disable (general purpose) 1 = multi master error detect enable	0
Reserved	[1]	Reserved	0

✓ **SPI : <22-9> : SPI RX DATA REGISTER : 01/09/2004**

Register	Address	R/W	Description	Reset Value
SPRDAT0	0x59000014	R	SPI channel 0 Rx data register	0xFF
SPRDAT1	0x59000034	R	SPI channel 1 Rx data register	0xFF

SPRDATn	Bit	Description	Initial State
Rx Data Register	[7:0]	This field contains the data to be received over the SPI channel.	0xFF

✓ **RTC : <17-2,3,5> : EDIT INTERRUPT NAME : 01/14/2004**

Changed an interrupt name from “ALMINT” to “INT_RTC”

✓ **AC97 CONTROLLER: <24> : : 10/21/2003**

AC97 has been added into 2440A Manual.

✓ **AC97 CONTROLLER: <24-9> : WARM AC97 RESET : 01/12/2004**

The following sentence is deleted.

"When the AC97 Controller receives a wake-up from the Codec"

✓ **UART : <11-1> : OVERVIEW : 01/14/2004**

Changed the signal name of external input clock from "UARTCLK" to "UEXTCLK" and added the "FCLK/n" clock for UART input clock.

The baud-rate generator can be clocked by PCLK, FCLK/n or UEXTCLK (external input clock).

✓ **UART : <11-11> : UART CONTROL REGISTER : 01/14/2004**

Added tables as follows

UCONn	Bit	Description	Initial State
FCLK divider	[15:12]	Divider value when the Uart clock source is selected as FCLK/n. 'n' is determined by UCON0[15:12], UCON1[15:12], UCON2[14:12]. **UCON2[15] is FCLK/n Clock Enable/Disable bit.** For setting 'n' from 7 to 21, use UCON0[15:12], For setting 'n' from 22 to 36, use UCON1[15:12], For setting 'n' from 37 to 43, use UCON2[14:12], **UCON2[15]: 0 = Disable FCLK/n clock. 1 = Enable FCLK/n clock.** In case of UCON0, UART clock = FCLK / (divider+6), where divider>0. UCON1, UCON2 must be zero. ex) 1: UART clock = FCLK/7, 2: UART clock = FCLK/8 3: UART clock = FCLK/9, … , 15: UART clock = FCLK/21 In case of UCON1, UART clock = FCLK / (divider+21), where divider>0. UCON0, UCON2 must be zero. ex) 1: UART clock = FCLK/22, 2: UART clock = FCLK/23 3: UART clock = FCLK/24, … , 15: UART clock = FCLK/36 In case of UCON2, UART clock = FCLK / (divider+36), where divider>0. UCON0, UCON1 must be zero. ex) 1: UART clock = FCLK/37, 2: UART clock = FCLK/38 3: UART clock = FCLK/39, … **, 7: UART clock = FCLK/43** If UCON00/1[15:12] and UCON2[14:12] are all '0', the divider will be 44, that is UART clock = FCLK/44 Total division range is from 7 to 44.	0000
Clock Selection	[11:10]	Select PCLK, UEXTCLK or FCLK/n for the UART baud rate. UBRDIVn = (int)(selected clock / (baudrate x 16)) –1 00, 10 = PCLK 01 = UEXTCLK 11 = FCLK/n	0

✓ **UART : <11-7> : BAUD-RATE GENERATION : 01/14/2004**

Each UART's baud-rate generator provides serial clock for transmitter and receiver. The source clock for the baud-rate generator can be selected with the S3C2440A's internal system clock or UEXTCLK. In other words, dividend is selectable by setting Clock Selection of UCONn. The baud-rate clock is generated by dividing the source clock (PCLK, FCLK/n or UEXTCLK) by 16 and a 16-bit divisor specified in the UART baud-rate divisor register (UBRDIVn). The UBRDIVn can be determined by the following expression:

UBRDIVn = (int)(UART clock / (baud-rate x 16)) –1

(UART clock: PCLK, FCLK/n or UEXTCLK)

Where, UBRDIVn should be from 1 to (2^{16}-1), but can be set to 0 (bypass mode) only using the UEXTCLK which should be smaller than PCLK.

For example, if the baud-rate is 115200 bps and UART clock is 40 MHz, UBRDIVn is:

UBRDIVn = (int)(40000000 / (115200 x 16)) -1
= (int)(21.7) -1 [round to the nearest whole number]
= 22 -1 = 21

✓ **UART : <11-21> : UART BAUD RATE DIVISOR REGISTER : 01/14/2004**

There are three UART baud rate divisor registers including UBRDIV0, UBRDIV1 and UBRDIV2 in the UART block. The value stored in the baud rate divisor register (UBRDIVn), is used to determine the serial Tx/Rx clock rate (baud rate) as follows:

UBRDIVn = (int)(UART clock / (buad rate x 16)) –1

(UART clock : PCLK, FCLK/n or UEXTCLK)

Where, UBRDIVn should be from 1 to (2^{16}-1), but can be set to zero only using the UEXTCLK which should be smaller than PCLK.

For example, if the baud-rate is 115200 bps and UART clock is 40 MHz, UBRDIVn is:

UBRDIVn = (int)(40000000 / (115200 x 16)) -1
= (int)(21.7) -1 [round to the nearest whole number]
= 22 -1 = 21

Register	Address	R/W	Description	Reset Value
UBRDIV0	0x50000028	R/W	Baud rate divisior register 0	–
UBRDIV1	0x50004028	R/W	Baud rate divisior register 1	–
UBRDIV2	0x50008028	R/W	Baud rate divisior register 2	–

UBRDIV n	Bit	Description	Initial State
UBRDIV	[15:0]	Baud rate division value UBRDIVn > 0 Using the UEXTCLK as input clock, UBRDIVn can be set to ‘0’.	–

✓ **NAND FLASH CONTROLLER : <6-3> : PIN CONFIGURATION : 01/09/2004**

The note is added as follows.

PIN CONFIGURATION

- OM[1:0] = 00: Enable NAND flash memory boot
- NCON : NAND flash memory selection(Normal / Advance)
  0: Normal NAND flash (256Words/512Bytes page size, 3/4 address cycle)
  1: Advance NAND flash (1KWords/2KBytes page size, 4/5 address cycle)
- GPG13 : NAND flash memory page capacitance selection
  0: Page=256 Words (NCON = 0) or Page=1KWords (NCON = 1)
  1: Page=512 Bytes (NCON = 0) or Page=2Kbytes (NCON = 1)
- GPG14: NAND flash memory address cycle selection
  0: 3 address cycle (NCON = 0) or 4 address cycle (NCON = 1)
  1: 4 address cycle (NCON = 0) or 5 address cycle (NCON = 1)
- GPG15 : NAND flash memory bus width selection
  0: 8-bit bus width
  1: 16-bit bus width

NOTE: The configuration pin – NCON, GPG[15:13] – will be fetched during reset.
In normal status, these pins must be set as input so that the pin status is not changed, when enters Sleep mode by software or unexpected cause. (Explanation is not clear)

✓ **MMC/SD/SDIO CONTROLLER: <19-1> : FEATURES : 10/21/2003**

Features were added and modified as follows.

- Normal, and DMA data transfer mode(byte, halfword, word transfer)
- DMA burst4 access support(only word transfer)

✓ **MMC/SD/SDIO CONTROLLER: <19-4> : SDICON REGISTER : 10/21/2003**

SDICON Register's bits were added as follows.

SDICON	Bit	Description	Initial Value
SDMMC Reset (SDreset)	[8]	Reset whole sdmmc block. This bit is automatically cleared. 0 = normal mode, 1 = SDMMC reset	0
Hold Margin (HoldMgn)	[7:6]	Determines how much you can delay CMD, DAT lines for hold margin in the MMC clock type 00 = 1/2 PCLK cycle, 01 = 1 PCLK cycle 10 = 3/2 PCLK cycles, 11 = 2 PCLK cycles	0
Reserved	[1]		

* Byte Order Type

- Type A : (Access by Word) D[7:0] → D[15:8] → D[23:16] → D[31:24]
  (Access by Halfword) D[7:0] → D[15:8]
- Type B : (Access by Word) D[31:24] → D[23:16] → D[15:8] → D[7:0]
  (Access by Halfword) D[15:8] → D[7:0]

✓ **MMC/SD/SDIO CONTROLLER: <19-5> : SDICMDCON REGISTER : 10/21/2003**

Description of Command Start (CMST) bit was modified as follows.

Command Start(CMST)	[8]	Determines whether the command operation starts or not. This bit is automatically cleared. 0 = command ready, 1 = command start	0

✓ **MMC/SD/SDIO CONTROLLER: <19-8> : SDI DATA CONTROL REGISTER : 10/21/2003**

SDIDatCon Register's bits were added as follows.

SDIDatCon	Bit	Description	Initial Value
Burst4 enable (Burst4)	[24]	Enable Burst4 mode in DMA mode. This bit should be set only when the Data Size is word. 0 = disable, 1 = Burst4 enable	0
Data Size (DataSize)	[23:22]	Indicates the size of the transfer with FIFO, which is typically byte, halfword or word. 00 = Byte transfer, 01 = Halfword transfer 10 = Word transfer, 11 = reserved	0
Data Transfer Start(DTST)	[14]	Determines whether the data transfer start or not. This bit is automatically cleared. 0 = data ready, 1 = data start	0
Data Transfer Mode (DatMode)	[13:12]	Determines the direction of data transfer 00 = no operation, 01 = only busy check start 10 = data receive start, 11 = data transmit start	00

✓ **MC/SD/SDIO CONTROLLER: <19-9> : SDI DATA STATUS REGISTER : 10/21/2003**

SDIDatSta Register's bits were added and changed as follows.

SDIDatSta	Bit	Description	Initial Value
Reserved	[31:12]		
No Busy(NoBusy)	[11] R/C	Busy is not active during 16cycle after the cmd packet transmitted only in busy check mode. This flag is cleared by setting 1 in this bit. 0 = not detect, 1 = no busy signal	0
Reserved	[8]		

✓ **MMC/SD/SDIO CONTROLLER: <19-11> : SDI INTERRUPT MASK REGISTER : 10/21/2003**

SDIIntMsk Register's address and bits were added as follows.

Register	Address	R/W	Description	Reset Value
SDIIntMsk	0x000B_003C	R/W	SDI Interrupt Mask Register	0x0

SDICON	Bit	Description	Initial Value
NoBusy Interrupt Enable (NoBusyInt)	[18]	Determines whether SDI generates an interrupt if the busy signal is not active. 0 = disable, 1 = interrupt enable	0

✓ **MMC/SD/SDIO CONTROLLER: <19-10> : SDI FIFO STATUS REGISTER : 10/21/2003**

SDIFSTA Register's bits were added and changed as follows.

SDIFSTA	Bit	Description	Initial State
FIFO Reset(FRST)	[16] C	Reset FIFO value. This bit is automatically cleared. 0 = normal mode, 1 = FIFO reset	0
FIFO Fail error (FFfail)	[15:14] R/C	FIFO fail error when FIFO overrun/underrun data saving. This flag is cleared by setting one to these bits. 00 = not detect, 01 = FIFO fail 10 = FIFO fail in the last transfer(only FIFO reset need) 11 = reserved	0
Rx FIFO Last Data Ready (RFLast)	[9] R/C	This bit is set to 1 when Rx FIFO receives the last data block. This flag is cleared by setting one to this bit. 0 = not received yet, 1 = Rx FIFO gets Last data	0

*** Although the last Rx data size is lager than remained count of FIFO data, you could read this data. If this event happens, you should clear FFfail field, and FIFO reset field**

✓ **MMC/SD/SDIO CONTROLLER: <19-12> : SDI DATA REGISTER : 10/21/2003**

SDIDAT Register's address and notes were added as follows.

Register	Address	R/W	Description	Reset Value
SDIDAT	0x000b_0040, 44, 48, 4c(Li/W, Li/HW, Li/B, Bi/W) 0x000b_0041(Bi/HW), 0x000b_0043(Bi/B)	R/W	SDI Data Register	0x0

SDIDAT	Bit	Description	Initial State
Data Register	[31:0]	This field contains the data to be transmitted or received over the SDI channel	0x00000000

* (Li/W, Li/HW, Li/B): Access by Word/HalfWord//Byte unit in Little-endian mode
* (Bi/W): Access by Word unit in Big-endian mode
* (Bi/HW): Access by HalfWord unit in Big-endian mode
* (Bi/B): Access by Byte unit in Big-endian mode

✓ **DMA : <8-2> : DMA REQUEST SOURCES : 10/21/2003**

Table 8-1 was changed as follows.

Table 8-1. DMA Request Sources for Each Channel

	Source0	Source1	Source2	Source3	Source4	Source5	Source6
Ch-0	nXDREQ0	UART0	SDI	Timer	USB device EP1	I2SSDO	PCMIN
Ch-1	nXDREQ1	UART1	I2SSDI	SPI0	USB device EP2	PCMOUT	SDI
Ch-2	I2SSDO	I2SSDI	SDI	Timer	USB device EP3	PCMIN	MICIN
Ch-3	UART2	SDI	SPI1	Timer	USB device EP4	MICIN	PCMOUT

✓ **DMA : <8-10> : DCONN REGISTER : 10/21/2003**

Description of HWSRCSEL bit was modified as follows.

HWSRCSEL	[26:24]	Select DMA request source for each DMA. DCON0: 000:nXDREQ0 001:UART0 010:SDI 011:Timer 100:USB device EP1 DCON1: 000:nXDREQ1 001:UART1 010:I2SSDI 011:SPI 100:USB device EP2 DCON2: 000:I2SSDO 001:I2SSDI 010:SDI 011:Timer 100:USB device EP3 DCON3: 000:UART2 001:SDI 010:SPI 011:Timer 100:USB device EP4 DCON0: 101:I2SSDO 110:PCMIN DCON1: 101:PCMOUT 110:SDI DCON2: 101:PCMIN 110:MICIN DCON3: 101:MICIN 110:PCMOUT These bits control the 4-1 MUX to select the DMA request source of each DMA. These bits have meanings only if H/W request mode is selected by DCONn[23].	00

✓ **CLOCK & POWER MANAGEMENT : <7-16> : PIN CONFIGURATION TABLE IN SLEEP MODE: 1/15/2004**

Table 7-4 was changed as follows.

Table 7-4. Pin configuration table in Sleep mode

Pin Condition			Configuration
GPIO Pin		which are configured as Input	Pull-up Enable
		which are configured as Output	Pull-up Disable and Output Low
Input Pin, which does not have internal Pull-up control		If External Device doesn't always drive Pin's level.	Pull-up Enable by external Pull-up Resistor
Output pin, which are connected to external device		If External Device's Power is Off	Drive Low
		If External Device's Power is On	High or Low(It depends on External device's status)
Data Bus	If Memory Power is Off		Pull-up Disable & External Pull-down
	If Memory Power is On	and has External Buffer exist	Pull-up Disable, Control signal has previous value
		and has no External Buffer	Pull-up Enable, Control signal has Previous value (Recommended)

NOTE:
1. **ADC** should be set as **Standby** mode.
2. **USB** pads should be **Suspend** mode.

- This table is just for informational use only. User should consider his own Board condition and application.

✓ **ADC & TOUCH : <16-6> : ADC TOUCH SCREEN CONTROL REGISTER (ADCTSC): 03/05/2004**

Note 3) was added as follows

NOTE: 1) While waiting for Touch screen Interrupt, XP_SEN bit should be set to '1' (XP Output disable) and PULL_UP bit should be set to '0' (XP Pull-up enable).
2) AUTO_PST bit should be set '1' only in Automatic & Sequential X/Y Position conversion.
3) XP, YP should be disconnected from GND source during sleep mode to avoid leakage current. Because XP, YP will be maintained as 'H' states in sleep mode.

✓ **ADC & TOUCH : <16-9> : ADC TOUCH SCREEN UP-DOWN REGISTER (ADCUPDN): 1/15/2004**

The following register is added.

ADC TOUCH SCREEN UP-DOWN REGISTER (ADCUPDN)

Register	Address	R/W	Description	Reset Value
ADCUPDN	0x5800014	R/W	Stylus Up or Down Interrpt status register	0x0

ADCUPDN	Bit	Description	Initial State
TSC_UP	[1]	Stylus Up Interrupt. 0 = No stylus up status. 1 = Stylus up status.	0
TSC_DN	[0]	Stylus Down Interrupt. 0 = No stylus down status. 1 = Stylus down status.	0

✓ **CLOCK&POWER: <7-20> : PLL control register / Selection guide : 1/26/2004**

The following Note is changed.

Register	Address	R/W	Description	Reset Value
MPLLCON	0x4C000004	R/W	MPLL configuration register	0x00096030
UPLLCON	0x4C000008	R/W	UPLL configuration register	0x0004D030

PLLCON	Bit	Description	Initial State
MDIV	[19:12]	Main divider control	0x96 / 0x4D
PDIV	[9:4]	Pre-divider control	0x03 / 0x03
SDIV	[1:0]	Post divider control	0x0 / 0x0

NOTE: When you set MPLL&UPLL values, set UPLL value first and then MPLL value. (Needs intervals approximately 7 NOP)

✓ **RTC: <17-3> : REAL TIME CLOCK : 01/27/2004**

The round reset function was eliminated.

The table is modified as follows.

RESERVED REGISTER

Register	Address	R/W	Description	Reset Value
Reserved	0x5700006C(L) 0x5700006F(B)	-	Reserved	0x0

Reserved	Bit	Description	Initial State
Reserved	[3]	Reserved	0
Reserved	[2:0]	Reserved	000

✓ **I/O PORT: <9-24> : MISCELLANEOUS CONTROL REGISTER : 02/13/2004**

The table is modified as follows.

MISCCR	Bit	Description	Reset Value
nRSTCON	[16]	nRSTOUT signal manual control 0 = nRSTOUT signal level will be low (‘0’) 1 = nRSTOUT singal level will be high (‘1’)	1

✓ **CLOCK & POWER MANAGEMENT: <7-16> : TABLE 7-4: 03/04/2004**

Table description was changed in red.

Table 7-4 Pin configuration table in Sleep mode

Pin Condition			Pin Configuration
GPIO Pin		which are configured as Input	Pull-up Enable
		which are configured as Output	Pull-up Disable and Output Low
Input Pin, which does not have internal Pull-up control.		If External Device doesn't always drive Pin's level.	Pull-up Enable by external Pull-up Resistor
Output pin, which are connected to External device		If External Device's Power is Off	Output Low
		If External Device's Power is On	High or Low (It depends on External device's status)
Data Bus	If Memory Power is Off		Output Low
	If Memory Power is On	and External Buffer does exist	Pull-up Disable, Control signals are Previous values
		and no External Buffer	Pull-up Enable, Control signal has Previous value (Recommended)

✓ **UART: <11-11> : UART CONTROL REGISTER : 03/04/2004**

Added the following lines

UCONn	Bit	Description	Initial State
Clock Selection	[11:10]	Select PCLK, UEXTCLK or FCLK/n for the UART baud rate. UBRDIVn = (int)(selected clock / (baudrate x 16)) –1 00, 10 = PCLK 01 = UEXTCLK 11 = FCLK/n (If you would select FCLK/n, you should add the code in “NOTE” after selecting or deselecting the FCLK/n.)	0

Note: You should add the following codes after selecting or deselecting the FCLK/n.

```
rGPHCON = rGPHCON & ~(3<<16); //GPH8(UEXTCLK) input
Delay(1); // about 100us
rGPHCON = rGPHCON & ~(3<<16) | (1<<17); //GPH8(UEXTCLK) UEXTCLK
```

✓ **Electrical data: <27-3>: Table 27-3. Normal I/O PAD DC Electrical Characteristics : 1/27/2004**

The tables are changed as follows.

Table 27-3 Normal I/O PAD DC Electrical Characteristics

Normal I/O PAD DC Electrical Characteristics for Memory (V_{DDMOP} = 2.5V±0.2V, T_A = 0 to 70 °C)

Symbol	Parameters	Condition	Min	Type	Max	Unit
V_{IH}	High level input voltage					
	LVCMOS interface		1.7			V
V_{IL}	Low level input voltage					
	LVCMOS interface				0.7	V
VT	Switching threshold			$0.5V_{DD}$		V
VT+	Schmitt trigger, positive-going threshold	CMOS			2.0	V
VT-	Schmitt trigger, negative-going threshold	CMOS	0.8			V
I_{IH}	High level input current					
	Input buffer	$V_{IN} = V_{DD}$	-10		10	µA
I_{IL}	Low level input current					
	Input buffer	$V_{IN} = V_{SS}$	-10		10	µA
	Input buffer with pull-up		-60	-33	-10	
V_{OH}	High level output voltage					
	Type B4 to B12	I_{OH}= - 1 µA	V_{DD} -0.05			
	Type B4	I_{OH}= - 4 mA	2.0			V
	Type B6	I_{OH}= - 6 mA				
	Type B8	I_{OH}= - 8 mA				
	Type B10	I_{OH}= -10 mA				
	Type B12	I_{OH} = -12 mA				
V_{OL}	Low level output voltage					
	Type B4 to B12	I_{OL}= 1 µA			0.05	
	Type B4	I_{OL} = 4 mA			0.4	V
	Type B6	I_{OL} = 6 mA				
	Type B8	I_{OL} = 8 mA				
	Type B10	I_{OL} = 10 mA				
	Type B12	I_{OL} = 12 mA				

Normal I/O PAD DC Electrical Characteristics for Memory (V_{DDMOP} = 3.0V±0.3V, 3.3V ± 0.3V, T_A = 0 to 70 °C)

Symbol	Parameters	Condition	Min	Type	Max	Unit
V_{IH}	High level input voltage					
	LVCMOS interface		2.0			V
V_{IL}	Low level input voltage					
	LVCMOS interface				0.8	V
VT	Switching threshold			$0.5V_{DD}$		V
VT+	Schmitt trigger, positive-going threshold	CMOS			2.0	V
VT-	Schmitt trigger, negative-going threshold	CMOS	0.8			V
I_{IH}	High level input current					
	Input buffer	$V_{IN} = V_{DD}$	-10		10	µA
I_{IL}	Low level input current					
	Input buffer	$V_{IN} = V_{SS}$	-10		10	µA
	Input buffer with pull-up		-60	-33	-10	
V_{OH}	High level output voltage					
	Type B4 to B12	I_{OH}= - 1 µA	V_{DD} -0.05			
	Type B4	I_{OH}= - 4 mA	2.4			V
	Type B6	I_{OH}= - 6 mA				
	Type B8	I_{OH}= - 8 mA				
	Type B10	I_{OH}= -10 mA				
	Type B12	I_{OH} = -12 mA				
V_{OL}	Low level output voltage					
	Type B4 to B12	I_{OL}= 1 µA			0.05	
	Type B4	I_{OL} = 4 mA			0.4	V
	Type B6	I_{OL} = 6 mA				
	Type B8	I_{OL} = 8 mA				
	Type B10	I_{OL} = 10 mA				
	Type B12	I_{OL} = 12 mA				

✓ **Electrical data: <27-35> : Table 27-8. ROM/SRAM Bus Timing Constants : 1/27/2004**

The table is changed as follows.

Table 27-8 ROM/SRAM Bus Timing Constants

($V_{DDi,}$ $V_{DDalive,}$ V_{DDiarm} = 1.2 V ± 0.1 V, T_A = 0 to 70 °C, V_{DDMOP} = 3.3V ± 0.3V / 3.0V ± 0.3V / 2.5.0V ± 0.2V)

Parameter	Symbol	Min (V_{DDMOP} = 3.3V/3.0V/2.5V)	Typ	Max (V_{DDMOP} = 3.3V/3.0V/2.5V)	Unit
ROM/SRAM Address Delay	t_{RAD}	2 / 2 / 2	–	6 / 6 / 7	ns
ROM/SRAM Chip select Delay	t_{RCD}	2 / 2 / 3	–	6 / 6 / 6	ns
ROM/SRAM Output enable Delay	t_{ROD}	2 / 2 / 2	–	5 / 5 / 5	ns
ROM/SRAM read Data Setup time.	t_{RDS}	1 / 1 / 1	–	– / – / –	ns
ROM/SRAM read Data Hold time.	t_{RDH}	0 / 0 / 0	–	– / – / –	ns
ROM/SRAM Byte Enable Delay	t_{RBED}	2 / 2 / 2	–	5 / 5 / 5	ns
ROM/SRAM Write Byte Enable Delay	t_{RWBED}	2 / 2 / 2	–	5 / 5 / 6	ns
ROM/SRAM output Data Delay	t_{RDD}	2 / 2 / 2	–	6 / 6 / 6	ns
ROM/SRAM external Wait Setup time	t_{WS}	3 / 3 / 4	–	– / – / –	ns
ROM/SRAM external Wait Hold time	t_{WH}	0 / 0 / 0	–	– / – / –	ns
ROM/SRAM Write enable Delay	t_{RWD}	2 / 2 / 2	–	5 / 5 / 6	ns

✓ **Electrical data: <27-35> : Table 27-9. Memory Interface Timing Constants : 1/27/2004**

The table is changed as follows.

Table 27-9. Memory Interface Timing Constants

($V_{DDi,}$ $V_{DDalive,}$ V_{DDiarm} = 1.2 V ± 0.1 V, T_A = 0 to 70 °C, V_{DDMOP} = 3.3V ± 0.3V / 3.0V ± 0.3V / 2.5.0V ± 0.2V)

Parameter	Symbol	Min	Typ	Max	Unit
SDRAM Address Delay	t_{SAD}	1	–	4	ns
SDRAM Chip Select Delay	t_{SCSD}	1	–	3	ns
SDRAM Row active Delay	t_{SRD}	1	–	3	ns
SDRAM Column active Delay	t_{SCD}	1	–	3	ns
SDRAM Byte Enable Delay	t_{SBED}	1	–	3	ns
SDRAM Write enable Delay	t_{SWD}	1	–	2	ns
SDRAM read Data Setup time	t_{SDS}	2 / 3 / 3 *	–	–	ns
SDRAM read Data Hold time	t_{SDH}	0	–	–	ns
SDRAM output Data Delay	t_{SDD}	1	–	4	ns
SDRAM Clock Enable Delay	T_{cked}	2	–	3	ns

NOTE: Minimum t_{SDS} = 2ns / 3ns / 3ns, when V_{DDMOP} = 3.3V / 3.0V / 2.5V for each.

✓ **Electrical data: <27-3>: Table 27-3. Normal I/O PAD DC Electrical Characteristics : 2/13/2004**

The following table is added.

Normal I/O PAD DC Electrical Characteristics for I/O (V_{DDOP} = 3.3V ± 0.3V, T_A = 0 to 70 °C)

Symbol	Parameters	Condition	Min	Type	Max	Unit
V_{IH}	High level input voltage					
	LVCMOS interface		2.0			V
V_{IL}	Low level input voltage					
	LVCMOS interface				0.8	V
VT	Switching threshold			$0.5V_{DD}$		V
VT+	Schmitt trigger, positive-going threshold	CMOS			2.0	V
VT-	Schmitt trigger, negative-going threshold	CMOS	0.8			V
I_{IH}	High level input current					
	Input buffer	$V_{IN} = V_{DD}$	-10		10	µA
I_{IL}	Low level input current					
	Input buffer	$V_{IN} = V_{SS}$	-10		10	µA
	Input buffer with pull-up		-60	-33	-10	
V_{OH}	High level output voltage					
	Type B4 to B12	I_{OH}= - 1 µA	V_{DD} -0.05			
	Type B4	I_{OH}= - 4 mA	2.4			V
	Type B6	I_{OH}= - 6 mA				
	Type B8	I_{OH}= - 8 mA				
	Type B10	I_{OH}= -10 mA				
	Type B12	I_{OH} = -12 mA				
V_{OL}	Low level output voltage					
	Type B4 to B12	I_{OL}= 1 µA			0.05	
	Type B4	I_{OL} = 4 mA			0.4	V
	Type B6	I_{OL} = 6 mA				
	Type B8	I_{OL} = 8 mA				
	Type B10	I_{OL} = 10 mA				
	Type B12	I_{OL} = 12 mA				

NOTES:

1. Type B6 means 6mA output driver cell.
2. Type B8 means 8mA output driver cell.
3. Type B12 means 12mA output driver cells.

✓ **Electrical data: <27> : Temperature Range : 2/17/2004**

Temperature range T_A = 0 to 70 °C is changed to **T_A = -40 to 85 °C**

✓ **I/O Port: <9-24> : MISCELLANEOUS control register (MISCCR) : 02/23/2004**

Changed the following table

MISCELLANEOUS CONTROL REGISTER (MISCCR)

BATT_FUNC	[22:20]	Battery fault function selection. 0XX: In nBATT_FLT=0, the system will be in reset status. After reset, Change this bit to some other value, this bit is used only to prevent from booting in Battery fault status. 10X: In sleep mode status, when nBATT_FLT=0, the system will wake-up. In normal mode, when nBATT_FLT=0, the Battery fault interrupt will occur. 110: In sleep mode status, during nBATT_FLT=0, the system will ignore all the wake-up events (the system will not wake-up by wake-up source). In normal mode, nBATT_FLT signal does not affect the system. 111: nBATT_FLT function disable	000

✓ **CLOCK & POWER MANAGEMENT: <7-19> : Battery Fault signal (nBATT_FLT): 02/25/2004**

Changed the following sentences

Battery Fault Signal(nBATT_FLT)

The two functions in nBATT_FLT pin are as follows;

— When CPU is not in SLEEP mode, nBATT_FLT pin will cause the interrupt request by setting BATT_FUNC (MISCCR[22:20]) as 10x'b. The interrupt attribute of the nBATT_FLT is L-level triggered.

— While CPU is in SLEEP mode, assertion of the nBATT_FLT will prohibit the wake up from the power-down mode, which is achieved by setting BATT_FUNC(MISCCR[22:20]) as 11x'b. So, any wake-up source will be masked if nBATT_FLT is asserted, which is protecting the system malfunction of the low battery capacity

✓ **ELECTRICAL DATA: <27-2> : TABLE 27-2. RECOMMENDED OPERATING CONDITIONS : 03/04/2004**

Changed a sentence as follows

Table 27-2. Recommended Operating Conditions

Parameter	Symbol	Rating			Unit
		Typ.	Min	Max	
DC Supply Voltage for Alive Block	$V_{DDalive}$	300MHz: 1.2V V_{DD} 400MHz: 1.3V V_{DD} 533MHz: TBD	1.0 1.0 TBD	1.25 1.35 TBD	V
DC Supply Voltage for Internal	V_{DDi} V_{DDiarm} V_{DDMPLL} V_{DDUPLL}	300MHz: 1.2V V_{DD} 400MHz: 1.3V V_{DD} 533MHz: TBD	1.15 1.25 TBD	1.25 1.35 TBD	
DC Supply Voltage for I/O Block	V_{DDOP}	3.3V V_{DD}	3.0	3.6	
DC Supply Voltage for Memory interface	V_{DDMOP}	1.8V/2.5V/3.0V/3.3V V_{DD}	1.7	3.6	
DC Supply Voltage for Analog Core	V_{DD}	3.3V V_{DD}	3.0	3.6	
DC Supply Voltage for RTC	V_{DDRTC}	1.8V/2.5V/3.0V/3.3V V_{DD}	1.8	3.6	
DC Input Voltage	V_{IN}	3.3V Input buffer	– 0.3	V_{DDOP}+0.3	
		3.3V Interface / 5V Tolerant input buffer	– 0.3	5.25	
DC Output Voltage	V_{OUT}	3.3V Output buffer	– 0.3	V_{DDOP}+0.3	
Operating Temperature	T_{OPR}	Industrial	-40 to 85		°C

✓ **OVERVIEW: <1-4> : FEATURES : 03/04/2004**

Frequency limit is added as follows.

Operating Voltage Range

- Core : 1.20V for 300MHz
  1.30V for 400MHz
  1.35V for 533MHz

Operating Frequency

- Fclk Up to 533MHz
- Hclk Up to 136MHz
- Pclk Up to 68MHz

✓ **ADC & TOUCH : <16-6> : ADC TOUCH SCREEN CONTROL REGISTER (ADCTSC): 03/05/2004**

Note 3) was added as follows

NOTE: 1) While waiting for Touch screen Interrupt, XP_SEN bit should be set to '1'(XP Output disable) and PULL_UP bit should be set to '0'(XP Pull-up enable).
2) AUTO_PST bit should be set '1' only in Automatic & Sequential X/Y Position conversion.
3) XP, YP should be disconnected with GND source during sleep mode to avoid leakage current. Because XP, YP will be maintained as 'H' states in sleep mode.

✓ **MMC&SD&SDIO : <19-9> : SDI DATA STATUS REGISTER (SDIDATSTA): 03/09/2004**

SDIDatSta[2] bit was reserved.

SDIDatSta	Bit	Description	Initial Value
Reserved	[2]		0

✓ **MMC&SD&SDIO : <19-11> : SDI INTERRUPT MASK REGISTER (SDIINTMSK): 03/09/2004**

SDIIntMsk[5] bit was reserved.

SDIIntMsk	Bit	Description	Initial Value
Reserved	[5]		0

✓ **I/O PORT : <9-38> : MSLCON(MEMORY SLEEP CONTROL REGISTER): 03/13/2004**

The following two registers are corrected which were misprinted.

Select memory interface status when in SLEEP mode.

Register	Address	R/W	Description	Reset Value
MSLCON	0x560000cc	R/W	Memory Sleep Control Register	0x0

MSLCON	Bit	Description	Reset Value
PSC_DATA	[11]	DATA[31:0] pin status in Sleep mode. 0: Hi-Z 1: Output "0".	0
PSC_WAIT	[10]	nWAIT pin status in Sleep mode. 0: Input 1: Output "0"	0
PSC_RnB	[9]	RnB pin status in Sleep mode. 0: Input 1: Output "0"	0

✓ **ADC & TOUCH : <16-5> : ADCCON(ADC CONTROL REGISTER): 03/13/2004**

NOTE was changed as follow in the description of ADCCON[13:6]=PRSCVL.

ADC Freqeuncy should be set less than PCLK by 5times.

Register	Address	R/W	Description	Reset Value
ADCCON	0x5800000	R/W	ADC Control Register	0x3FC4

ADCCON	Bit	Description	Initial State
PRSCVL	[13:6]	A/D converter prescaler value Data value: 0 ~ 255 NOTE: ADC Freqeuncy should be set less than PCLK by 5times. (Ex. PCLK=10MHZ, ADC Freq.< 2MHz)	0xFF

✓ **RTC : <17-2,3,5> : REAL TIME CLOCK : 03/15/2004**

Changed name of alarm interrupt from ALMINT to INT_RTC.

✓ **UART : <11-11,12> : UART CONTROL REGISTER : 03/15/2004**

Changed the following table

UCONn	Bit	Description	Initial State
Clock Selection	[11:10]	Select PCLK, UEXTCLK or FCLK/n for the UART baud rate. UBRDIVn = (int)(selected clock / (baudrate x 16)) –1 00, 10 = PCLK 01 = UEXTCLK 11 = FCLK/n (If you would select FCLK/n, you should add the code of “NOTE” after selecting or deselecting the FCLK/n.)	0

Note

You should add following codes after selecting or deselecting the FCLK/n.

```
rGPHCON = rGPHCON & ~(3<<16); //GPH8(UEXTCLK) input
Delay(1); // about 100us
rGPHCON = rGPHCON & ~(3<<16) | (1<<17); //GPH8(UEXTCLK) UEXTCLK
```

✓ **CAMERA INTERFACE : <23-ALLPAGES> : CAMERA INTERFACE : 03/15/2004**

Changed the following signal Names.

Table 23-1. Camera interface signal description

Name	I/O	Active	Description
CAMPCLK	I	–	Pixel Clock, driven by the Camera processor
CAMVSYNC	I	H/L	Frame Sync, driven by the Camera processor
CAMHREF	I	H/L	Horizontal Sync, driven by the Camera processor
CAMDATA[7:0]	I	–	Pixel Data driven by the Camera processor
CAMCLKOUT	O	–	Master Clock to the Camera processor
CAMRESET	O	H/L	Software Reset or Power down to the Camera processor

✓ **CAMERA INTERFACE : <23-17> : CODEC MAIN-SCALER CONTROL REGISTER: 03/15/2004**

Changed the following signal Names.

CICOSCCTRL	Bit	Description	Initial State
ScaleUpDown_Co	[30:29]	Scale up/down flag for codec scaler (In 1:1 scale ratio, this bit should be “1”) 00 = down 11 = up	00

✓ **CAMERA INTERFACE : <23-21> : PREVIEW MAIN-SCALER CONTROL REGISTER: 03/15/2004**

Changed the following signal Names.

CIPRSCCTRL	Bit	Description	Initial State
ScaleUpDown_Pr	[29:28]	Scale up/down flag for preview scaler (In 1:1 scale ratio, this bit should be “1”) 00 = down 11 = up	00

✓ **CAMERA INTERFACE : <23-7> : TIMING DIAGRAM FOR REGISTER SETTING : 03/15/2004**

Added sentences and modified figure 23-8 as follows

Especially, capture operation should be disabled when related information for target size are changed.

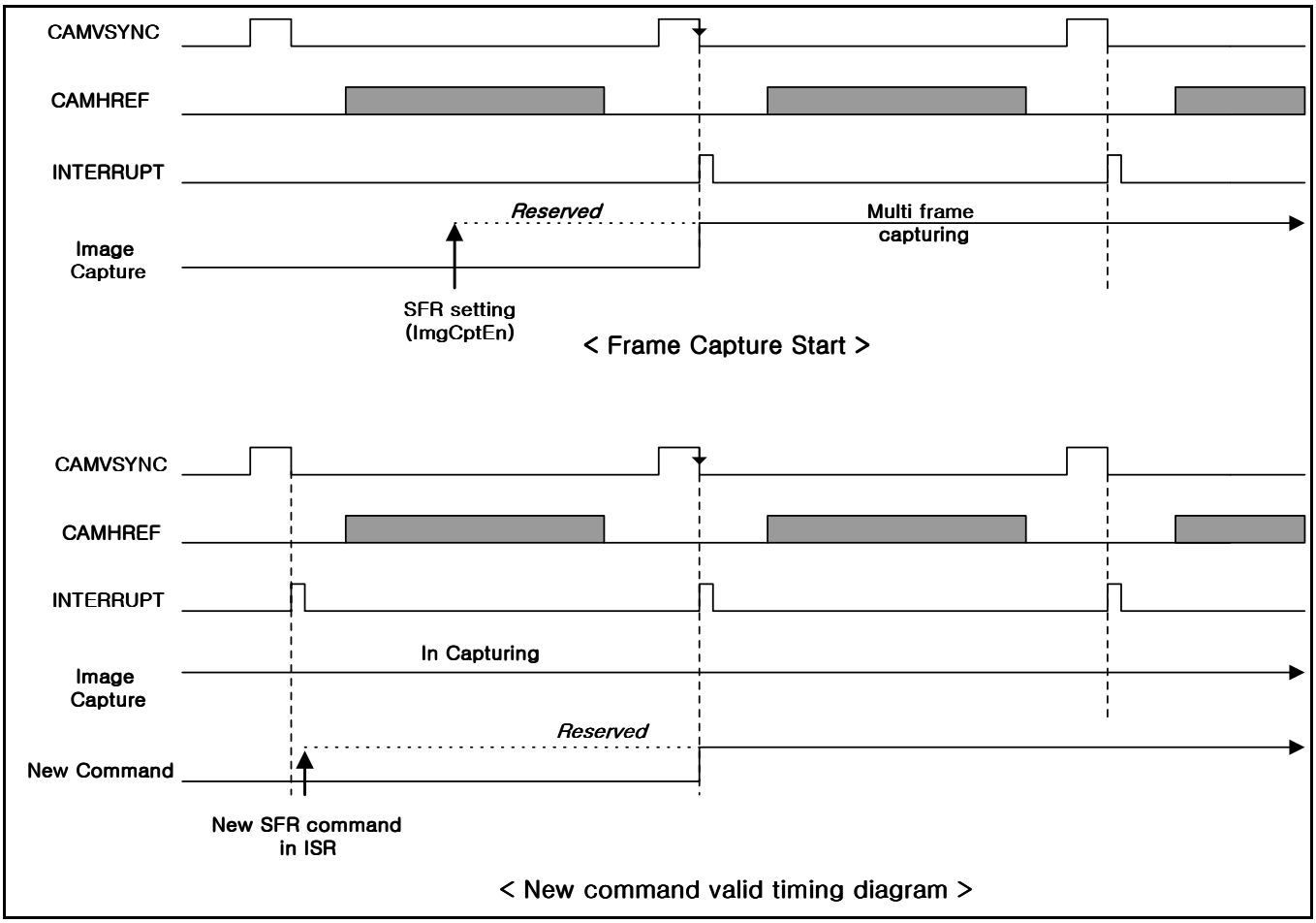

Figure 23-8 Timing Diagram for Register Setting

NOTE :

FIFO overflow of codec port will be occurred if codec port is not operating when preview port is operated. If you want to use codec port under this case, you should stop preview port and reset CAMIF using SwRst bit of CIGCTRL register. Then clear overflow of codec port and set special function registers that you want.

✓ **BUS PRIORITY : <25-1> : BUS PRIORITY MAP : 03/15/2004**

Changed sentences as follows.

BUS PRIORITY MAP

The S3C2440A holds 13 bus masters. They include DRAM refresh controller, LCD_DMA, CAMIF DMA, DMA0, DMA1, DMA2, DMA3, USB_HOST_DMA, EXT_BUS_MASTER, Test interface controller (TIC) and ARM920T. The following list shows the priorities among these bus masters after a reset:

1. DRAM refresh controller
2. LCD_DMA
3. CAMIF codec DMA
4. CAMIF preview DMA

✓ **CAMERA INTERFACE : <23-8> : TIMING DIAGRAM FOR LAST IRQ : 03/31/2004**

Added page as follows

TIMING DIAGRAM FOR LAST IRQ

IRQ except LastIRQ is generated before image capturing. Last IRQ which means capture-end can be set by following timing diagram. LastIRQEn is auto-cleared and ,as mentioned, SFR setting in ISR is for next frame command. So, for adequate last IRQ, you should follow next sequence between LastIRQEn and ImgCptEn/ImgCptEn_CoSc/ImgCptEnPrSC. It is recommended that ImgCptEn/ImgCptEn_CoSc/ImgCptEnPrSC are set at same time and at last of SFR setting in ISR. FrameCnt which is read in ISR, means next frame count. On following diagram, last captured frame count is “1”. That is, Frame 1 is the last-captured frame among frame 0~3. FrameCnt is increased by 1 at IRQ rising.

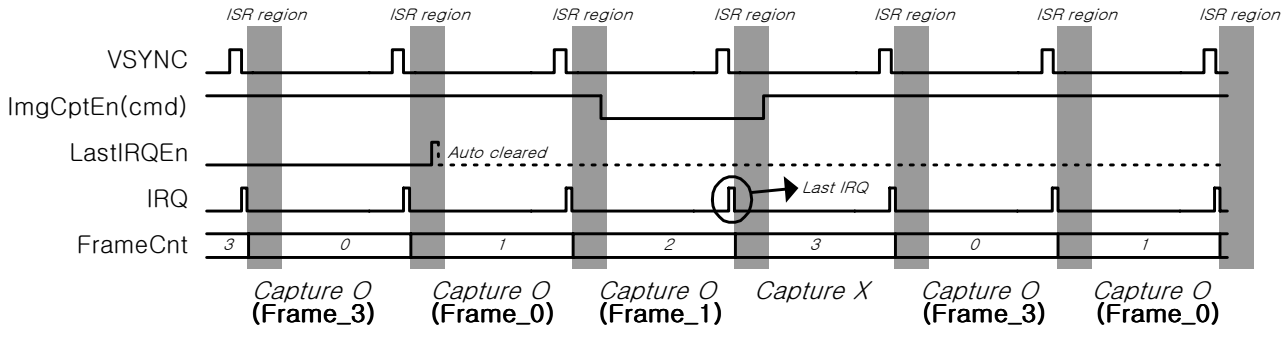

Figure 23-9 Timing diagram for last IRQ

✓ **CAMERA INTERFACE : <23-8> : REGISTER SETTING GUIDE FOR CODEC SCALER AND PREVIEW SCALER : 03/31/2004**

Added a sentence and changed figure 23-12 as follows

TargetHsize should not be larger than SourceHsize. Similarly, TargetVsize should not be larger than SourceVsize.

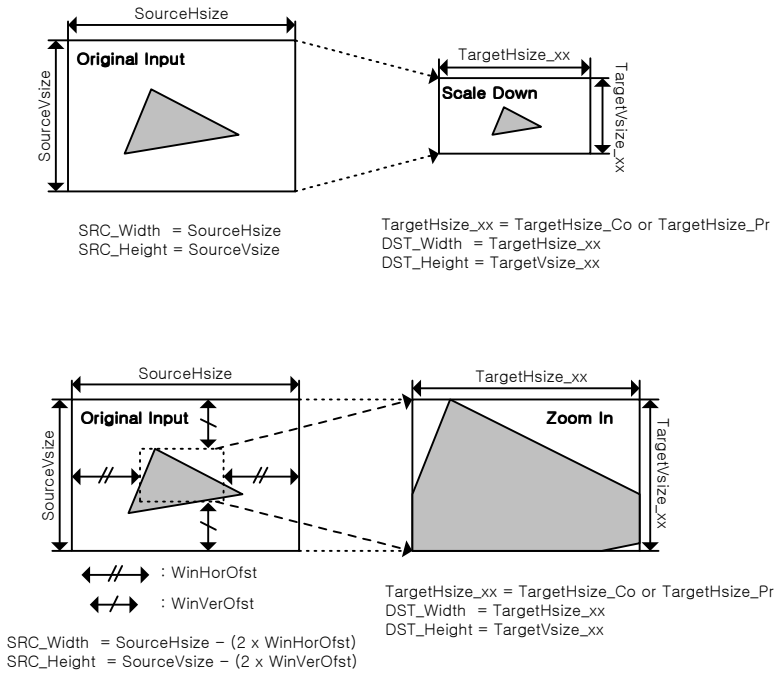

Figure 23-12 Scaling Scheme

✓ **OVERVIEW : <1-1> : INTRODUCTION : 03/31/2004**

Changed sentences as follows

- IIC bus interface (multi-master support)
- IIS Audio CODEC interface
- AC'97 CODEC interface
- SD Host interface version 1.0 & MMC Protocol version 2.11 compatible
- 2-ch USB Host controller / 1-ch USB Device controller (ver 1.1)
- 4-ch PWM timers / 1-ch Internal timer / Watch Dog Timer
- 8-ch 10-bit ADC and Touch screen interface
- RTC with calendar function
- Camera interface (Max. 4096 x 4096 pixels input support. 2048 x 2048 pixel input support for scaling)
- 130 General Purpose I/O ports / 24-ch external interrupt source

✓ **OVERVIEW : <1-1> : INTRODUCTION : 05/31/2004**

The tt8 I/O type is changed to t8.

→ 5V tolerant I/O is not supported anymore.

✓ **ELECTRICAL DATA : <27-2> : TABLE 27-2 RECOMMENDED OPERATING CONDITIONS : 05/31/2004**

Changed sentences as follows

Parameter	Symbol	Rating			Unit
		Typ.	Min	Max	
DC Supply Voltage for Alive Block	$V_{DDalive}$	300MHz: 1.2V V_{DD} 400MHz: 1.3V V_{DD} 533MHz: TBD	1.15 1.15 TBD	1.25 1.35 TBD	V

✓ **ELECTRICAL DATA : <27-36> : TABLE 27-8 ROM/SRAM BUS TIMING CONSTANTS : 06/01/2004**

The Table is changed as follows

Table 27-8 ROM/SRAM Bus Timing Constants

(V_{DDi}, $V_{DDalive}$, V_{DDiarm} = 1.2 V ± 0.1 V, T_A = -40 to 85 °C, V_{DDMOP} = 3.3V ± 0.3V / 3.0V ± 0.3V / 2.5V ± 0.2V / 1.8V ± 0.1V)

Parameter	Symbol	Min (V_{DDMOP} = 3.3V/3.0V/2.5V/1.8V)	Typ	Max (V_{DDMOP} = 3.3V/3.0V/2.5V/1.8V)	Unit
ROM/SRAM Address Delay	t_{RAD}	2 / 2 / 2 / 3	–	6 / 6 / 7 / 8	ns
ROM/SRAM Chip Select Delay	t_{RCD}	2 / 2 / 3 / 3	–	6 / 6 / 6 / 7	ns
ROM/SRAM Output Enable Delay	t_{ROD}	2 / 2 / 2 / 3	–	5 / 5 / 5 / 6	ns
ROM/SRAM Read Data Setup Time.	t_{RDS}	1 / 1 / 1 / 2	–	– / – / – / –	ns
ROM/SRAM Read Data Hold Time.	t_{RDH}	0 / 0 / 0 / 0	–	– / – / – / –	ns
ROM/SRAM Byte Enable Delay	t_{RBED}	2 / 2 / 2 / 3	–	5 / 5 / 5 / 7	ns
ROM/SRAM Write Byte Enable Delay	t_{RWBED}	2 / 2 / 2 / 3	–	5 / 5 / 6 / 7	ns
ROM/SRAM Output Data Delay	t_{RDD}	2 / 2 / 2 / 2	–	6 / 6 / 6 / 7	ns
ROM/SRAM External Wait Setup Time	t_{WS}	3 / 3 / 4 / 4	–	– / – / – / –	ns
ROM/SRAM External Wait Hold Time	t_{WH}	0 / 0 / 0 / 0	–	– / – / – / –	ns
ROM/SRAM Write Enable Delay	t_{RWD}	2 / 2 / 2 / 3	–	5 / 5 / 6 / 7	ns

✓ **ELECTRICAL DATA : <27-36> : TABLE 27-9 MEMORY INTERFACE TIMING CONSTANTS : 06/01/2004**

The Table is changed as follows

Table 27-9 Memory Interface Timing Constants

(V_{DDi}, $V_{DDalive}$, V_{DDiarm} = 1.2 V ± 0.1 V, T_A = -40 to 85 °C, V_{DDMOP} = 3.3V ± 0.3V / 3.0V ± 0.3V / 2.5V ± 0.2V / 1.8V ± 0.1V)

Parameter	Symbol	Min	Typ	Max	Unit
SDRAM Read Data Setup Time	t_{SDS}	2 / 3 / 3 / 5 *	–	–	ns

NOTE: Minimum t_{SDS} = 2ns / 3ns / 3ns, when V_{DDMOP} = 3.3V / 3.0V / 2.5V / 1.8V respectively.

✓ **ELECTRICAL DATA : <27-42> : TABLE 27-20 NAND FLASH INTERFACE TIMING CONSTANTS : 06/01/2004**

The Table is changed as follows

Table 27-20 NAND Flash Interface Timing Constants

(V_{DDi}, $V_{DDalive}$, V_{DDiarm} = 1.2 V ± 0.1 V, T_A = -40 to 85 °C, V_{DDMOP} = 3.3V ± 0.3V / 3.0V ± 0.3V / 2.5V ± 0.2V / 1.8V ± 0.1V)

Parameter	Symbol	Min (V_{DDMOP} = 3.3V/3.0V/2.5V/1.8V)	Max (V_{DDMOP} = 3.3V/3.0V/2.5V/1.8V)	Unit
NFCON Chip Enable Delay	t_{CED}	2.1/2.1/2.3/2.7	5.4/5.6/5.9/7.1	ns
NFCON CLE Delay	t_{CLED}	2.3/2.3/2.5/2.9	5.3/5.5/5.8/7.0	ns
NFCON ALE Delay	t_{ALED}	2.3/2.3/2.5/2.9	5.4/5.6/5.9/7.1	ns
NFCON Write Enable Delay	t_{WED}	2.1/2.1/2.3/2.7	5.0/5.2/5.5/6.7	ns
NFCON Read Enable Delay	t_{RED}	2.1/2.1/2.3/2.7	5.0/5.2/5.5/6.7	ns
NFCON Write Data Setup Time	t_{WDS}	2.1/2.2/2.3/2.7	5.8/6.0/6.3/7.5	ns
NFCON Write Data Hold Time	t_{WDH}	1.9/1.9/2.1/2.5	4.6/4.8/5.1/6.3	ns
NFCON Read Data Setup Requirement Time	t_{RDS}	3/3.1/3.3/4	– / – / – / –	ns
NFCON Read Data Hold Requirement Time	t_{RDH}	0.3/0.3/0.3/0.3	– / – / – / –	ns

✓ **CAMERA INTERFACE : <23-1> : FEATURE : 06/03/2004**

FEATURES

- ITU-R BT. 601/656 8-bit mode external interface support
- Max. 4096 x 4096 pixel input support without scaling (2048 x 2048 pixel input support with scaling)
- Max. 4096 x 4096 pixel output support for CODEC path
- Max. 640 x 480 pixel output support for PREVIEW path

✓ **CAMERA INTERFACE : <23-10> : SOURCE FORMAT REGISTER : 06/03/2004**

Note : We recommend a following sequence for preventing FIFO overflow at first frame of capture operation in CODEC path
<ITU 601 Format>
1. CISRCFMT[31] <- '1'
2. S/W reset
3. Initialize the Camera I/F
4. Start Capturing
<ITU 656 Format>
1. CISRCFMT[31] <- '1'
2. S/W reset
3. Initialize the Camera I/F
4. CISRCFMT[31] <- '0' //for ITU 656 foramt
6. Start Capturing
7. Clear Overflow of codec on First ISR

✓ **CAMERA INTERFACE : <23-12> : WINDOW OPTION REGISTER : 06/03/2004**

CIWDOFST	Bit	Description	Initial State
WinHorOfst	[26:16]	Window Horizontal Offset (the number which is the horizontal pixels except WinHorOfst * 2, must be multiple of 8) * WinHorOfst >= (SourceHsize-640*PreHorRatio_Pr)/2	0

✓ **CAMERA INTERFACE : <23-13> : Y1 START ADDRESS REGISTER : 06/03/2004**

Note : Address of buffers must be multiple of 1024.

✓ **CAMERA INTERFACE : <23-19> : REGISTER SETTING GUIDE : 06/03/2004**

NOTE : Preview path contains 640 pixel line buffer. (Codec path contains 2048 pixel line buffer) So, upper 1280 pixels, input images must be pre-scaled by over 1/2 for capturing valid preview image.
((SourceHsize-2*WinHorOfst)/PreHorRatio_Pr) <= 640

✓ **SPI : <22-1> : FEATURE : 06/03/2004**

Deleted 5V tolerant feature.

✓ **NAND FLASH CONTROLLER : <6-3> : NAND FLASH CONFIGURATION REGISTER : 06/03/2004**

NFCONF	Bit	Description	Initial State
Reserved	[15:14]	Reserved	-
TACLS	[13:12]	CLE & ALE duration setting value (0~3) Duration = HCLK x TACLS	01

✓ **OVERVIEW: <1-4> : FEATURES : 06/30/2004**

Frequency limit is added as follows.

Operating Voltage Range

- Core : 1.20V for 300MHz
  1.30V for 400MHz

Operating Frequency

- Fclk Up to 400MHz
- Hclk Up to 136MHz
- Pclk Up to 68MHz

✓ **OVERVIEW: <1-4> : FEATURES : 06/30/2004**

The following item is added.

System Manager

- Little/Big Endian support.
- Support Fast bus mode and Asynchronous bus mode.
- …
-

✓ **DSCN (DRIVE STRENGTH CONTROL) : <9-36> : DSCN0/1 REGISTER : 06/30/2004**

DSC0/1 regisger I/O strength level setting values are changed as follows.

Register	Address	R/W	Description	Reset Value
DSC0	0x560000c4	R/W	strength control register 0	0x0
DSC1	0x560000c8	R/W	strength control register 1	0x0

DSC0	Bit	Description	Reset Value
nEN_DSC	[31]	enable Drive Strength Control 0: enable 1: Disable	0

Reserved	[30:10]	-	0
DSC_ADR	[9:8]	Address Bus Drive strength. 00: 12mA 10: 10mA 01: 8mA 11: 6mA	00

…

DSC1	Bit	Description	Reset Value
DSC_SCK1	[29:28]	SCLK1 Drive strength. 00: 12mA 10: 10mA 01: 8mA 11: 6mA	00