Offset and CMRR : Random and systematic

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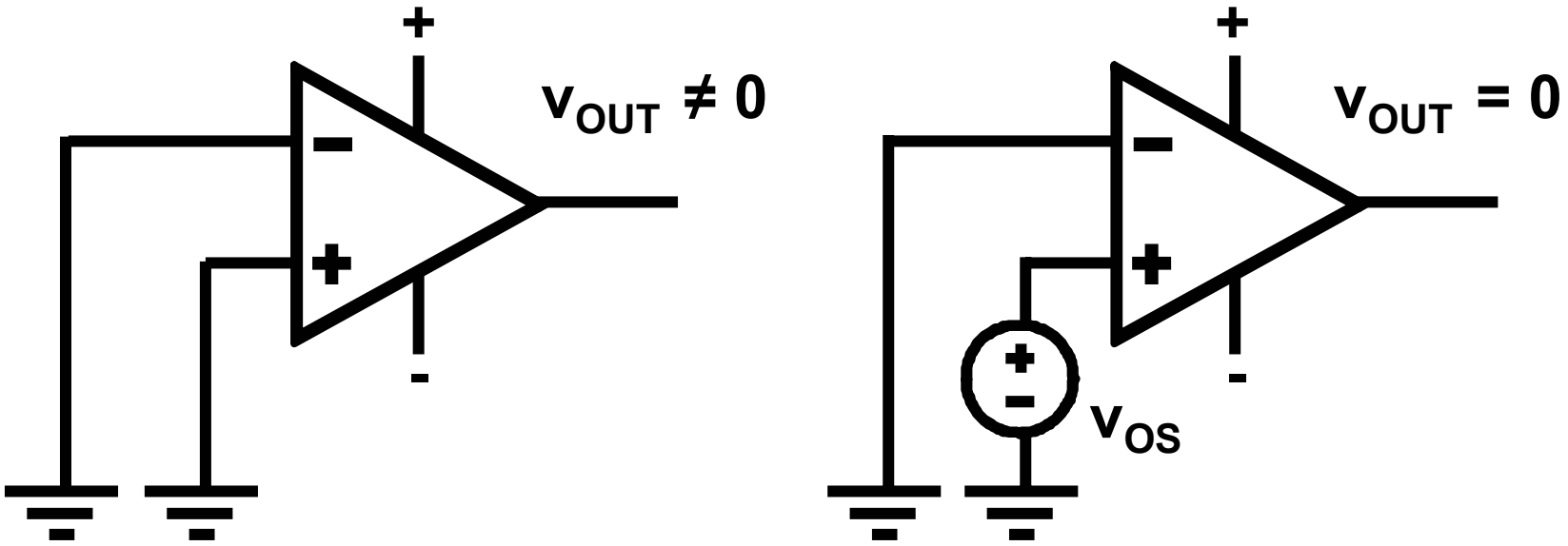
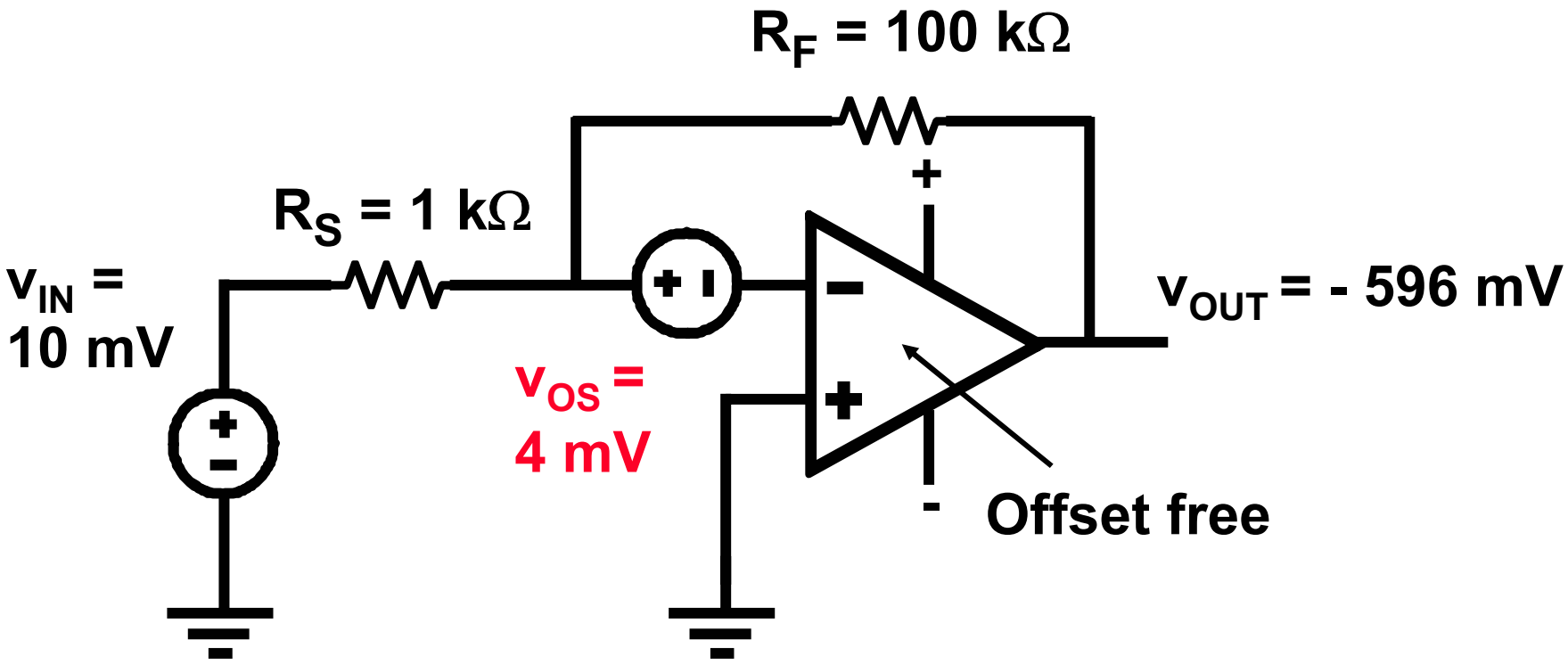
Ref: Pelgrom, JSSC Oct.1989, 1433-1439
Croon, JSSC Aug.02, 1056-1064
Croon, Springer, 2005

Definition of offset



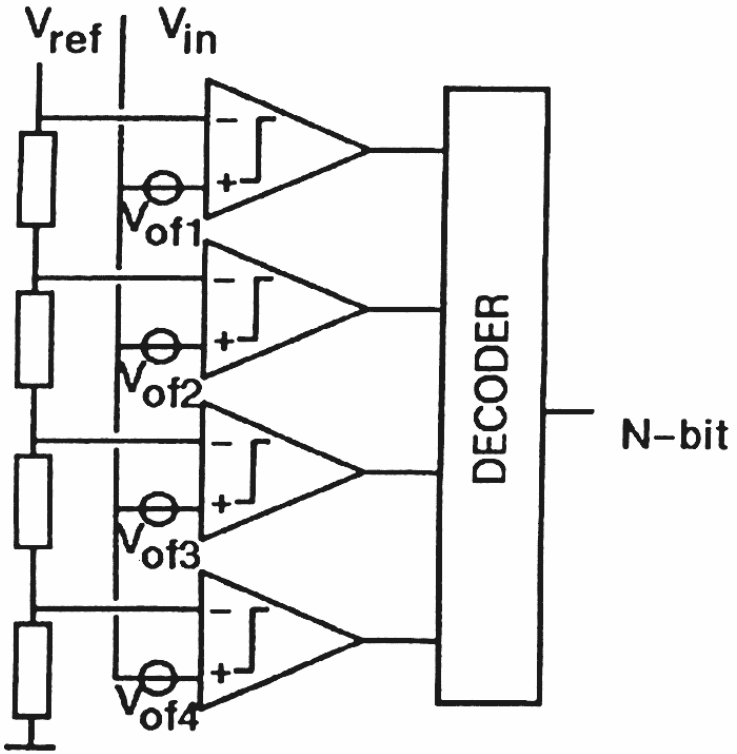
Offset voltage v_{os}

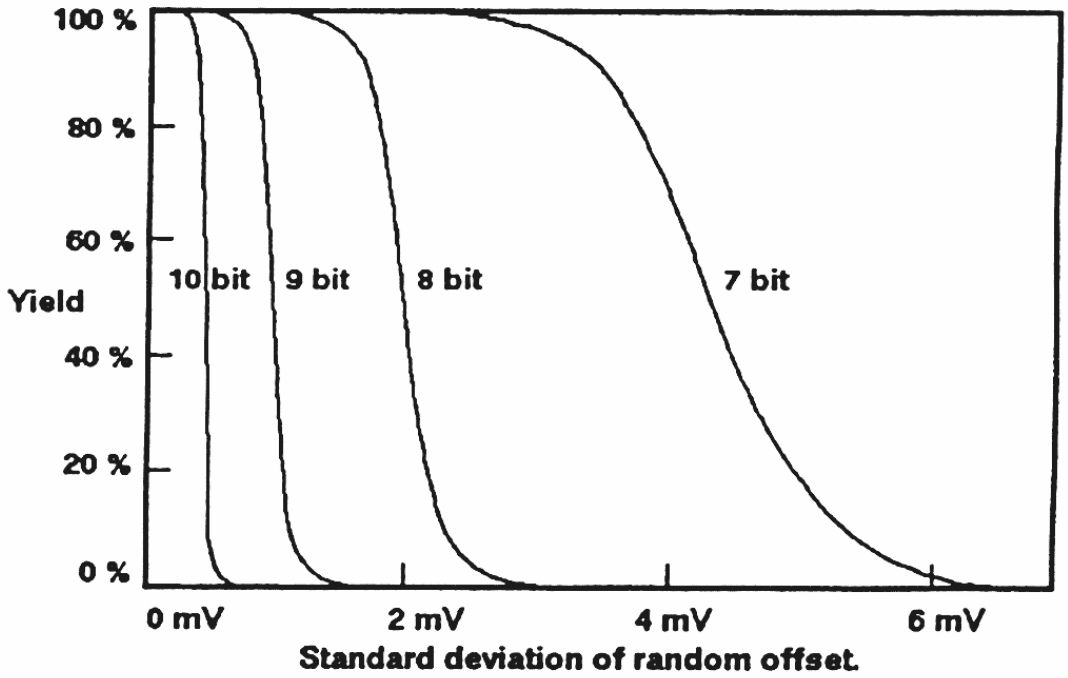
Gain error with offset



The gain is 59 instead of 100 !

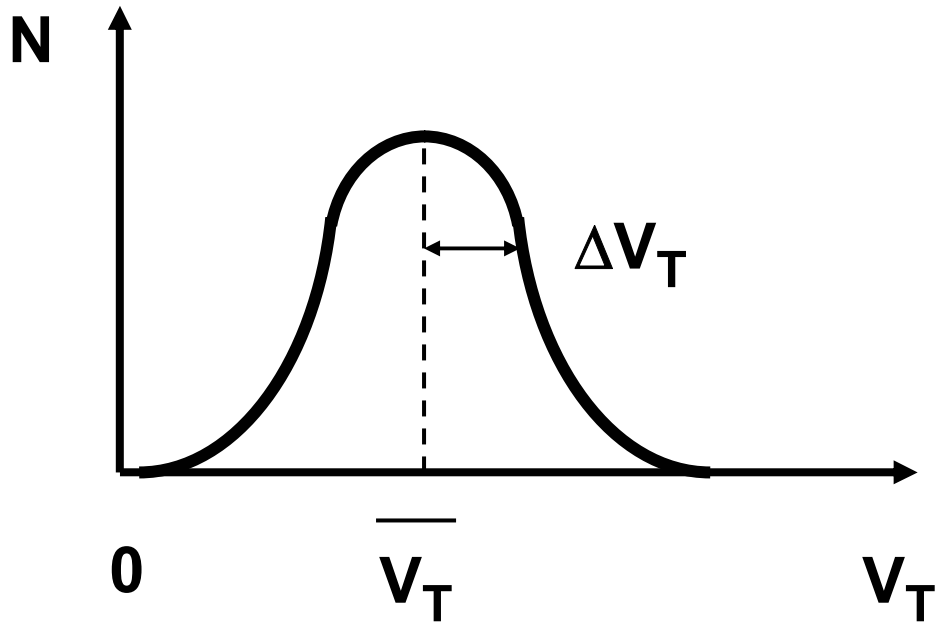
Yield of n-bit flash-ADC with offset





Ref: Pelgrom, IEDM 1998, pp.789.

Random offset : mismatches



$$I_{DS} = K' \frac{W}{L} (V_{GS} - V_T)^2$$

$$\sigma_{\Delta VT} = \frac{A_{VT}}{\sqrt{WL}}$$

$$A_{VT} \sim t_{ox} \sqrt[4]{N_B}$$

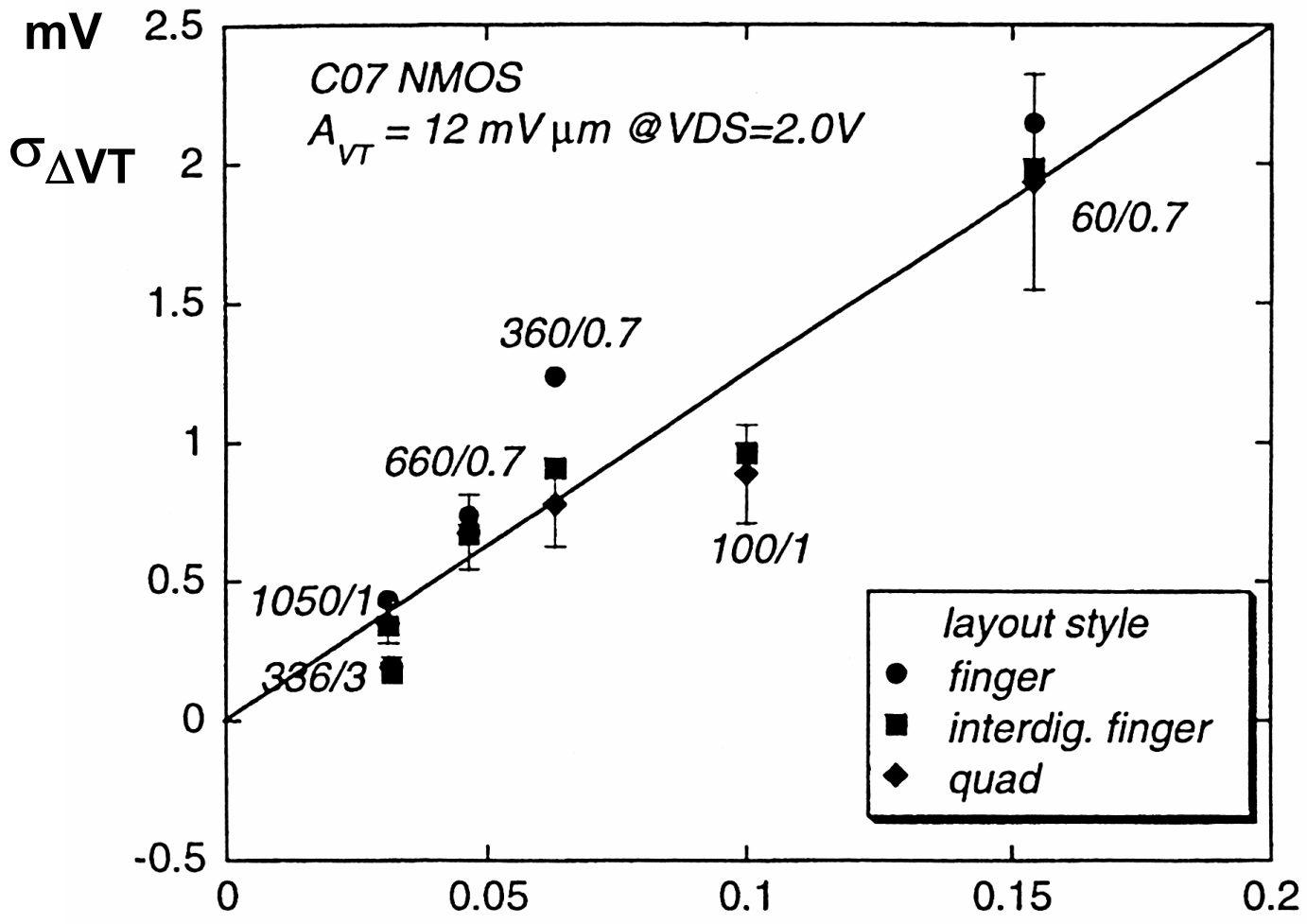
$A_{VT} \approx 5$ mVμm

for 0.25 μm nMOST

+50 % for pMOST

Ref: Keyes, JSSC Aug. 1975, 245-247
Shyu, JSSC Dec 1984, 948-955
Lakshmikumar, JSSC Dec 1986, 1057-1066
Pelgrom, JSSC Oct.1989, 1433-1439
Croon, JSSC Aug. 2002, 1056-1064

Threshold voltage sigma $\sigma_{\Delta VT}$



$$\sigma_{\Delta VT} = \frac{A_{VT}}{\sqrt{WL}}$$

$\sigma(\Delta V_T) \approx 2$ mV

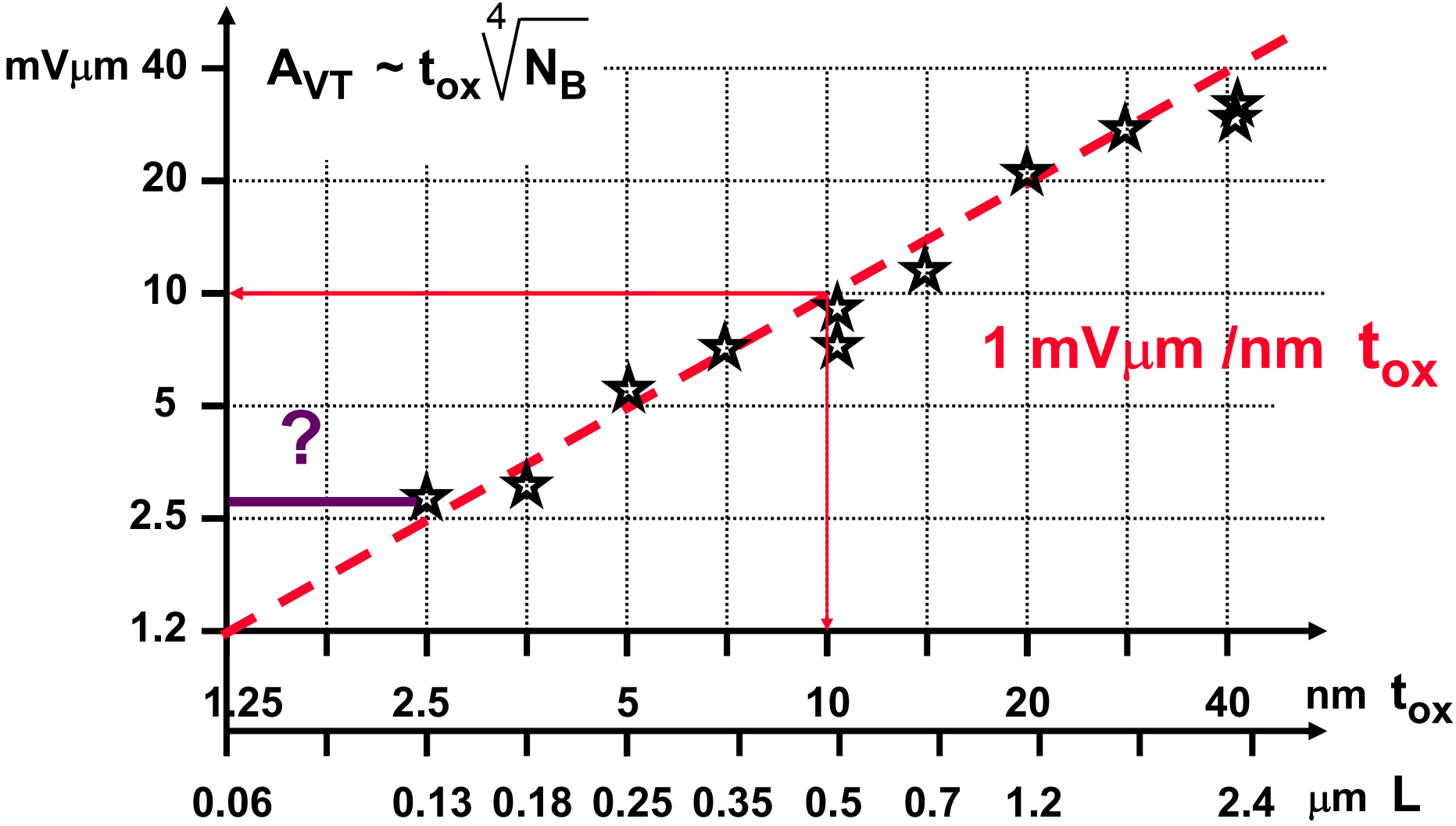
W/L = 60/0.7 µm

in 0.7 µm CMOS

$1/\sqrt{WL}$

1/µm

Threshold voltage mismatch A_{VT}



Random offset : mismatches

$$\frac{\Delta K'}{K'} = \frac{A_{K'}}{\sqrt{WL}}$$

$A_{K'} \approx 0.0056\ \mu m$ +50 % for pMOST

$$\frac{\Delta W/L}{W/L} = A_{WL}\sqrt{\frac{1}{W^2}+\frac{1}{L^2}}$$

$A_{WL} \approx 0.02\ \mu m$ +50 % for pMOST

$$\frac{\Delta \gamma}{\gamma} = \frac{A_{\gamma}}{\sqrt{WL}}$$

$A_{\gamma} \approx 0.016\ \mu m$ -25 % for pMOST

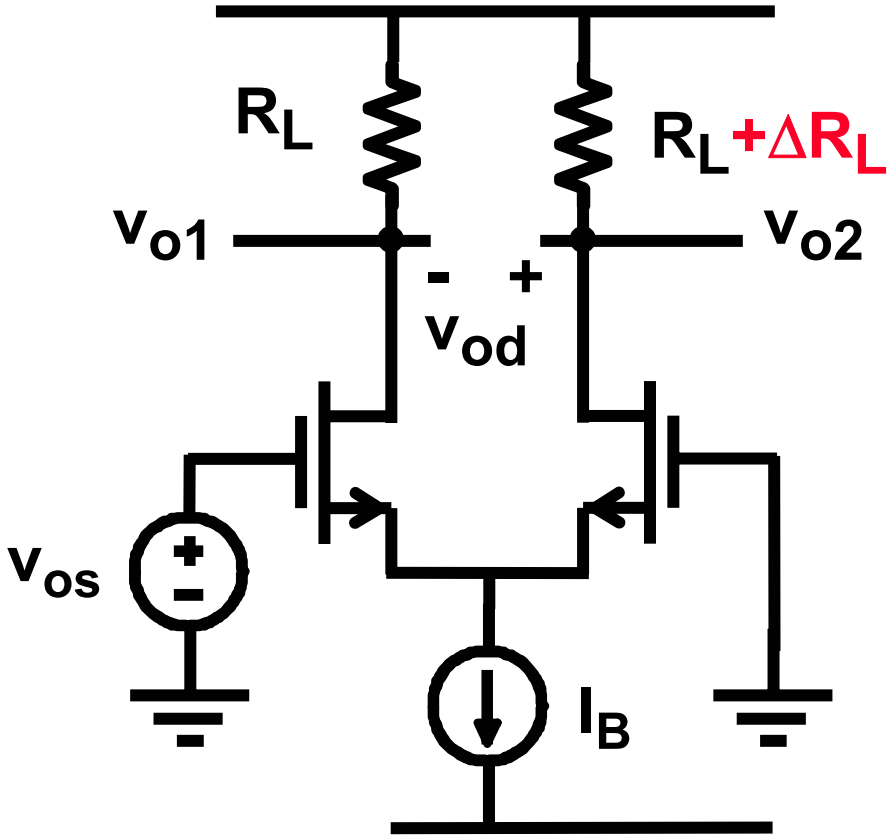
Negligible if B = S

Ref.: Pelgrom : JSSC Oct.1989, pp.1430-1440

Mismatch coefficients for nMOST

Techno L (μm)	2.5	1.2	0.7	0.5	0.35	0.25
t_{ox} (nm)	50	25	15	11	8	6
A_{VT} (mV μm)	30	21	13	7.1	6	⇨ 0
A_{WL} (% μm)	2.5	1.8	2.5	1.3	2	⇨ 1.8
S_{VT} (mV/mm)	0.3	0.3	0.4	0.2		
S_{WL} (%/mm)	0.3		0.2	0.2		

Random offset in differential pair



$$v_{od} = \Delta R_L \frac{I_B}{2}$$

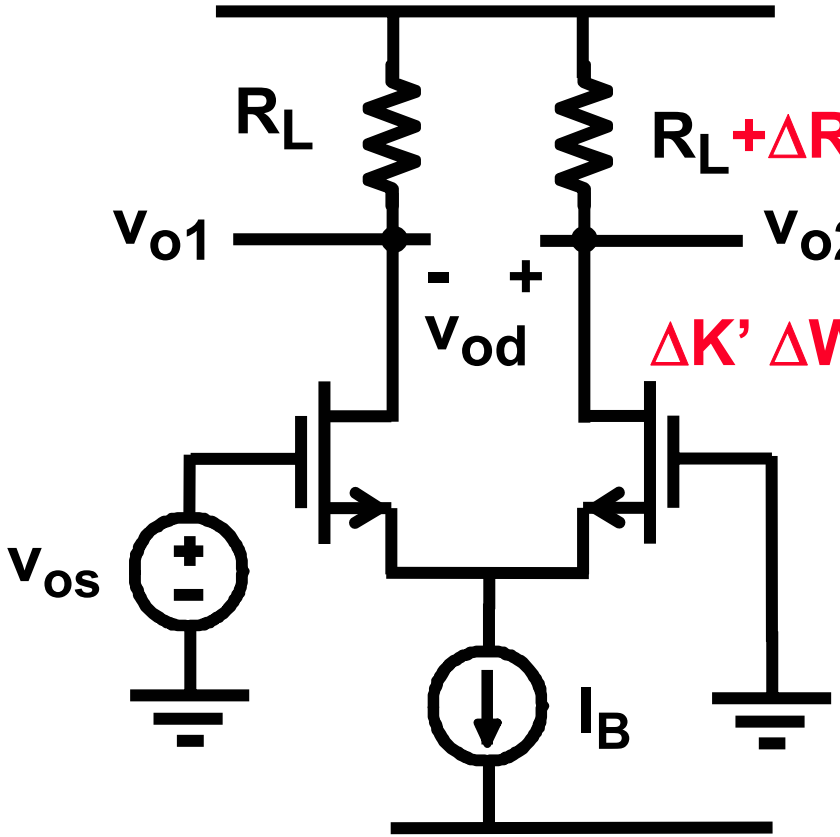
$$v_{os} = \frac{v_{od}}{g_m R_L}$$

$$v_{os} = \frac{\Delta R_L}{R_L} \frac{I_B}{2g_m}$$

$$v_{os} = \frac{\Delta R_L}{R_L} \frac{V_{GS} - V_T}{2}$$

Ref.: Laker, Sansen : Design of analog …, MacGrawHill 1994

Random offset in differential pair

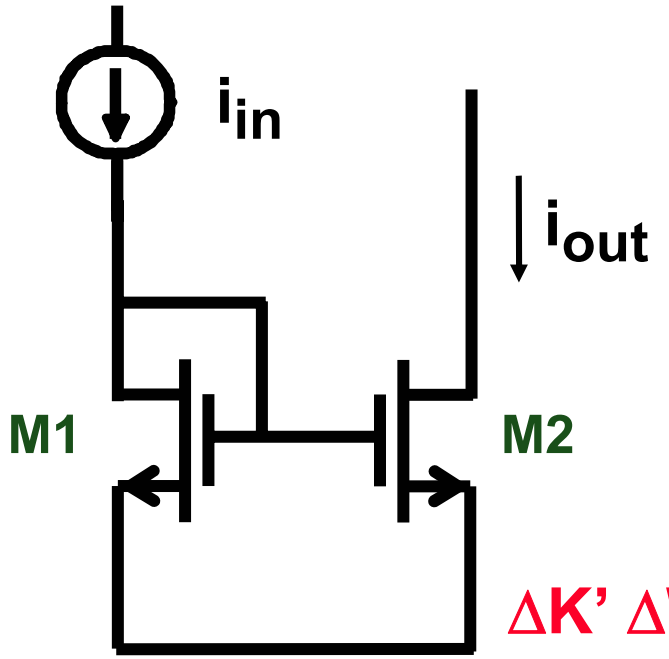


$$v_{OS} = \Delta V_T + \frac{V_{GS} - V_T}{2} \left(\frac{\Delta R_L}{R_L} + \frac{\Delta K'}{K'} + \frac{\Delta W/L}{W/L} \right)$$

$\Longrightarrow$ small $V_{GS} - V_T$

Ref.: Laker, Sansen : Design of analog …, MacGrawHill 1994

Random offset in current mirror



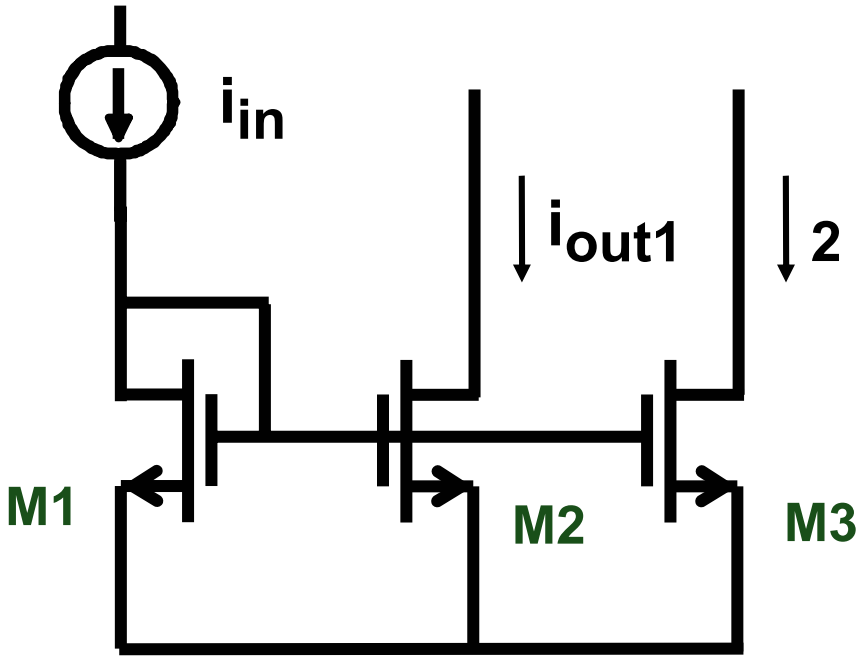
$\Delta K' \; \Delta W/L \; \Delta V_T$

$$\frac{\Delta I_{out}}{I_{out}} = \frac{\Delta V_T}{(V_{GS} - V_T)/2} + \frac{\Delta K'}{K'} + \frac{\Delta W/L}{W/L}$$

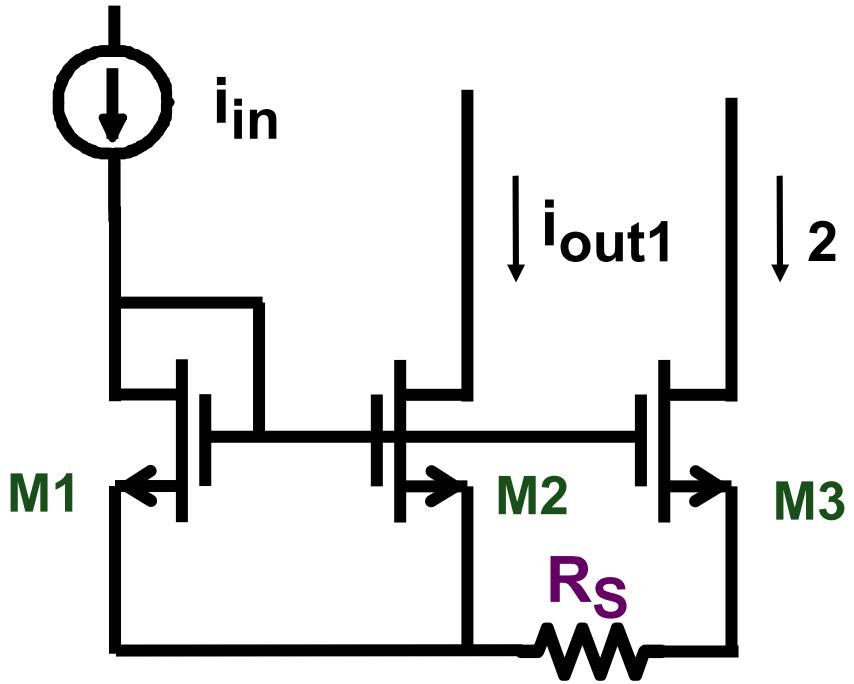
$\Rightarrow$ large $V_{GS} - V_T$

Ref.: Laker, Sansen : Design of analog …, MacGrawHill 1994

More offset in current mirror



$\Delta K' \; \Delta W/L \; \Delta V_T$



$\Delta K' \; \Delta W/L \; \Delta V_T \; R_S$

Mismatch in drain current

$$I_{DS} = \frac{\beta}{2}(V_{GS} - V_T)^2 \qquad \beta = \frac{K'}{n}\frac{W}{L}$$

$$\frac{\Delta I_{DS}}{I_{DS}} = \frac{\Delta\beta}{\beta} - \Delta V_T \frac{2}{V_{GS} - V_T}$$

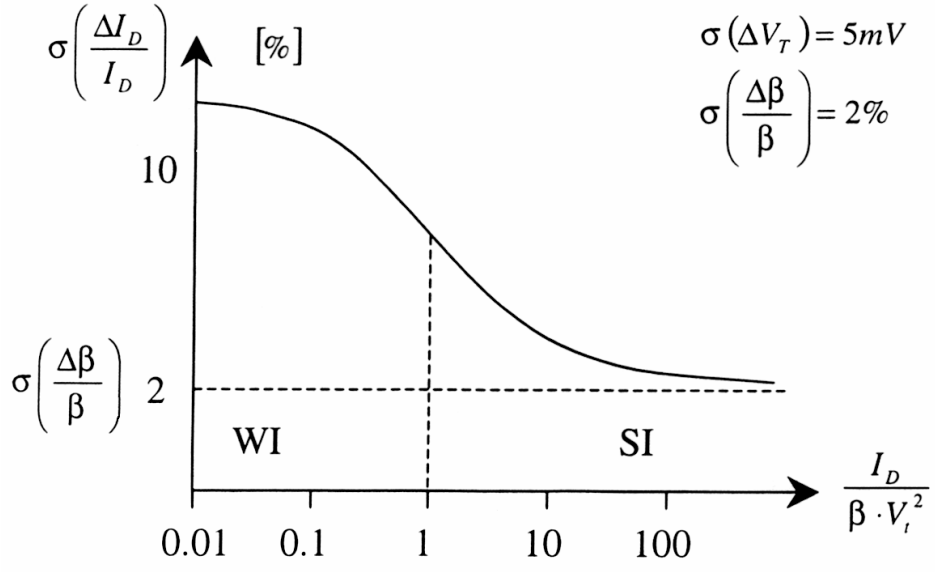
$$\sigma^2\left(\frac{\Delta I_{DS}}{I_{DS}}\right) = \sigma^2\left(\frac{\Delta\beta}{\beta}\right) + \sigma^2(\Delta V_T)\ \underbrace{\frac{4}{(V_{GS} - V_T)^2}}$$

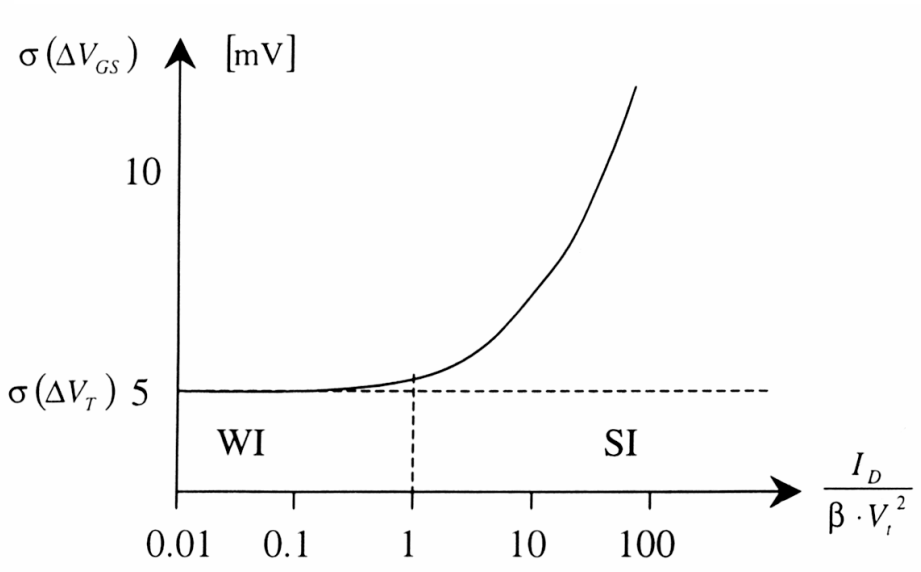
$$\frac{1}{(nkT/q)^2} \quad \text{in wi}$$

$$\left(\frac{g_m}{I_{DS}}\right)^2 \quad \text{in general}$$

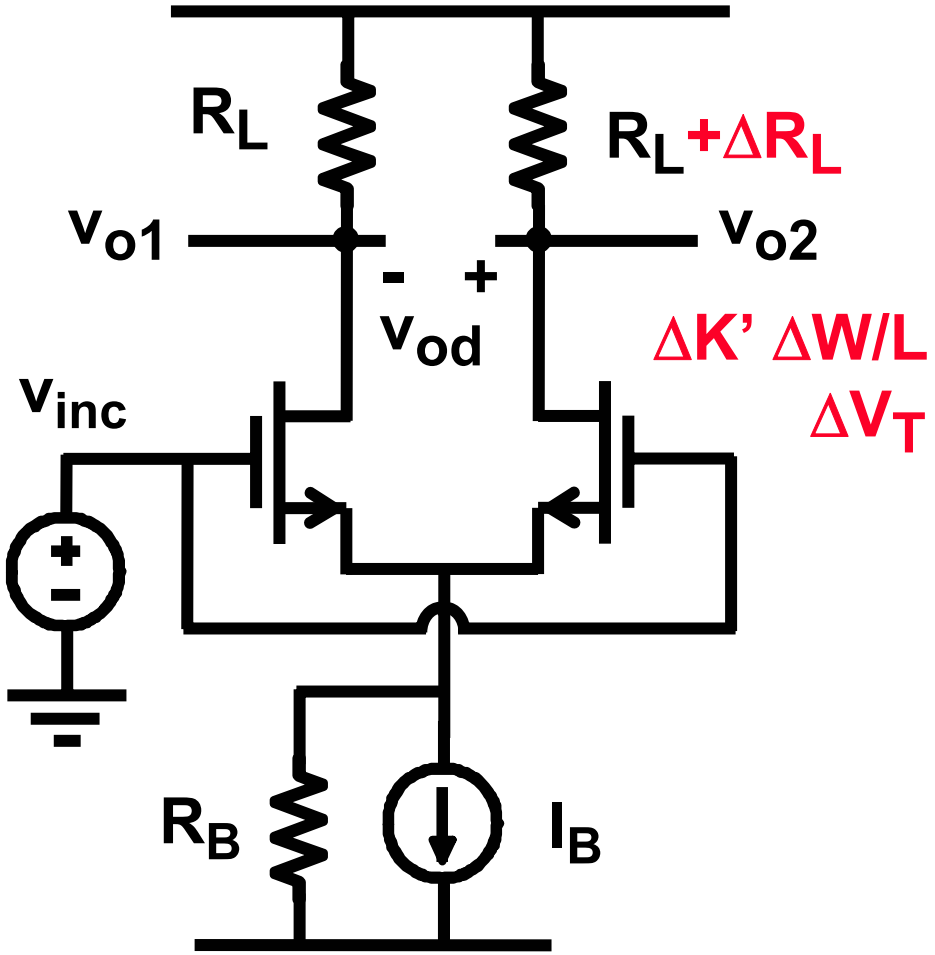
Mismatch in drain current for wi and si

$$\sigma^2\left(\frac{\Delta I_{DS}}{I_{DS}}\right) = \sigma^2\left(\frac{\Delta\beta}{\beta}\right) + \sigma^2(\Delta V_T)\ \underbrace{\frac{4}{(V_{GS}-V_T)^2}}_{\text{in si}}\ \text{or}\ \underbrace{\frac{1}{(nkT/q)^2}}_{\text{in wi}}$$





Random CMRR in differential pair -1



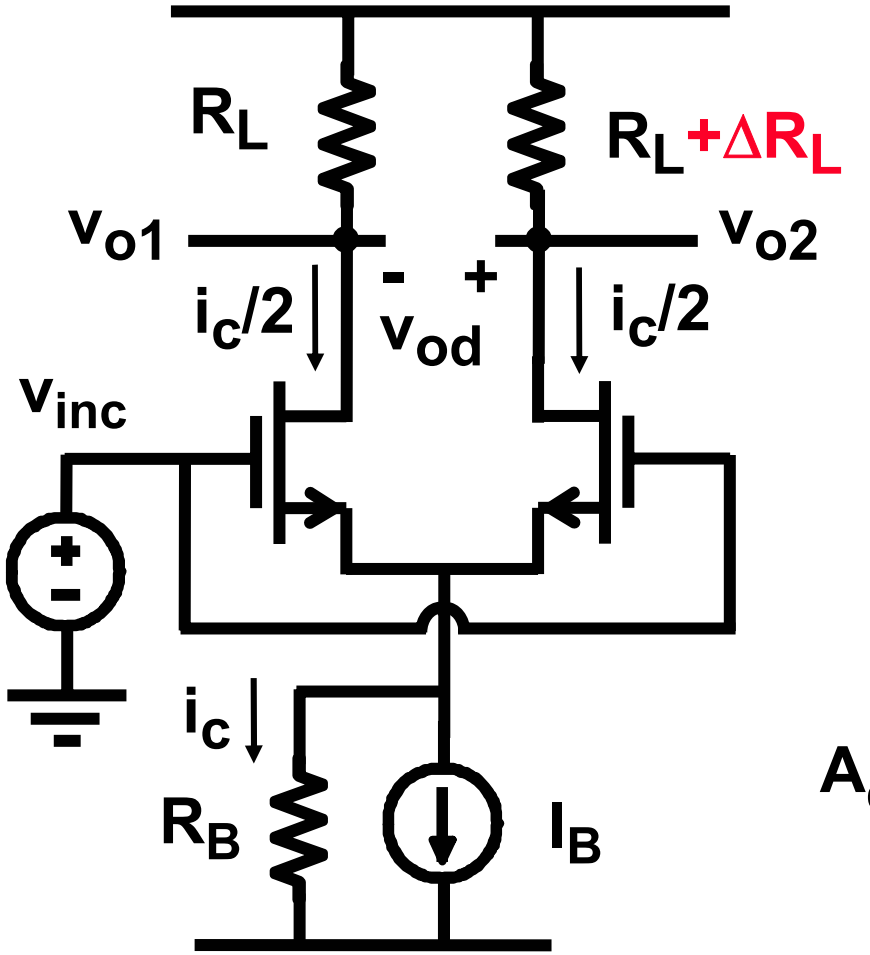
$$v_{od} = A_{dd}\, v_{id} + A_{dc}\, v_{ic}$$
$$v_{oc} = A_{cd}\, v_{id} + A_{cc}\, v_{ic}$$

$$A_{dd} = \left.\frac{v_{od}}{v_{id}}\right|_{v_{ic}=0} = g_m R_L$$

$$A_{dc} = \left.\frac{v_{od}}{v_{ic}}\right|_{v_{id}=0} \approx 0$$

$$CMRR = \frac{A_{dd}}{A_{dc}} \approx \infty$$

Random CMRR in differential pair -2



$$A_{dc} = \left.\frac{v_{od}}{v_{ic}}\right|_{v_{id}=0} \neq 0$$

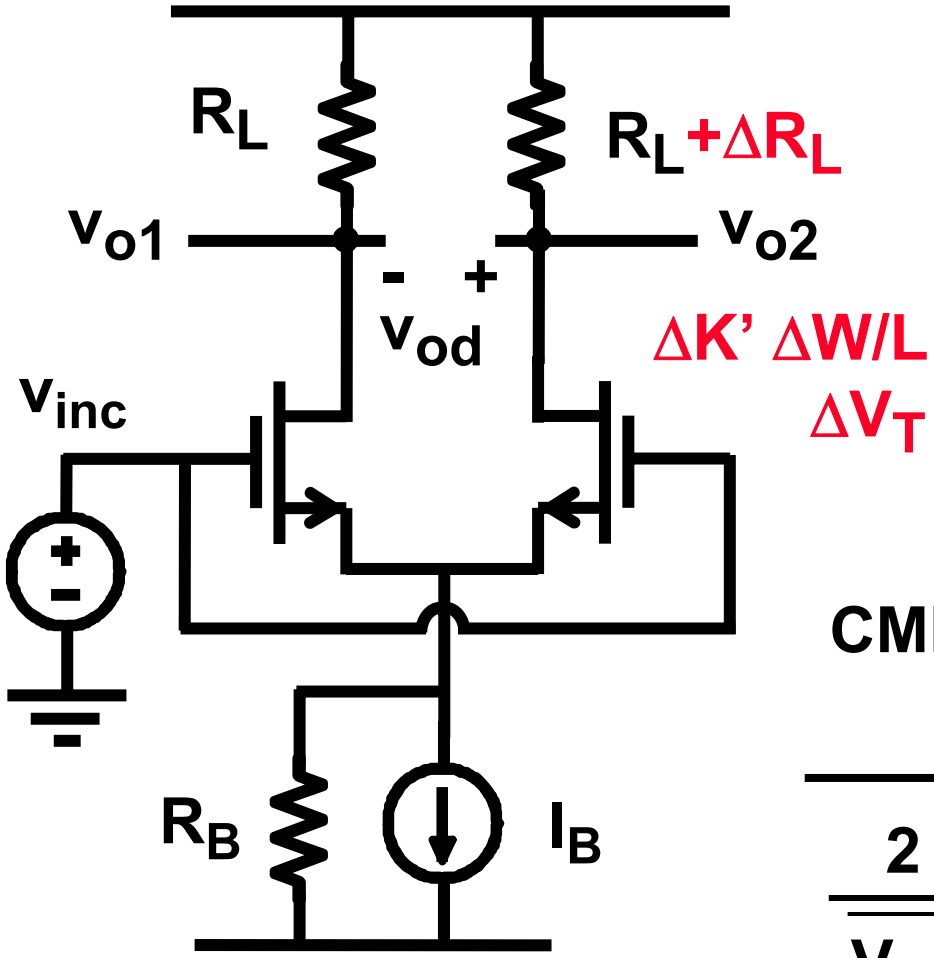
$$v_{ic} = v_{inc} \Rightarrow i_c = \frac{v_{inc}}{R_B}$$

$$v_{od} = \Delta R_L \, i_c/2$$

$$A_{dc} = \frac{\Delta R_L}{2 R_B}$$

$$\text{CMRR} = \frac{2 g_m R_B}{\Delta R_L/R_L}$$

Random CMRR in differential pair -3



$$CMRR = \frac{2\, g_m R_B}{\frac{2\,\Delta V_T}{V_{GS} - V_T} + \frac{\Delta R_L}{R_L} + \frac{\Delta K'}{K'} + \frac{\Delta W/L}{W/L}}$$

Relation random offset and CMRR

$$v_{OSr} = \Delta V_T + \frac{V_{GS} - V_T}{2}\left(\frac{\Delta R_L}{R_L} + \frac{\Delta K'}{K'} + \frac{\Delta W/L}{W/L}\right)$$

$$CMRR_r = \frac{2\, g_m R_B}{\frac{2\,\Delta V_T}{V_{GS} - V_T} + \frac{\Delta R_L}{R_L} + \frac{\Delta K'}{K'} + \frac{\Delta W/L}{W/L}}$$

$$v_{OSr}\, CMRR_r = \frac{V_{GS} - V_T}{2}\, 2\, g_m R_B = I_B R_B = V_E L_B = 5 \ldots 15\ V$$

$$v_{OSr}\, CMRR_r = 10\ V$$

Relation random offset and CMRR

$v_{OSr}\ CMRR_r \approx V_E L_B \approx 10\ V \quad (\sim L_B)$

10 mV 60 dB ≈ 10 V as for MOSTs

1 mV 80 dB ≈ 10 V as for Bipolar transistors

10 μV 120 dB ≈ 10 V with trimming : with laser
with Zener zap
with fusible links

Low offset = High CMRR

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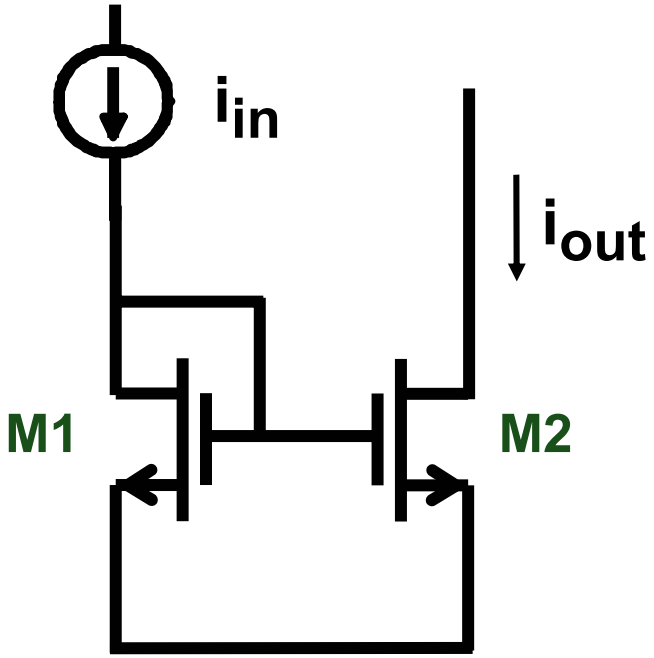
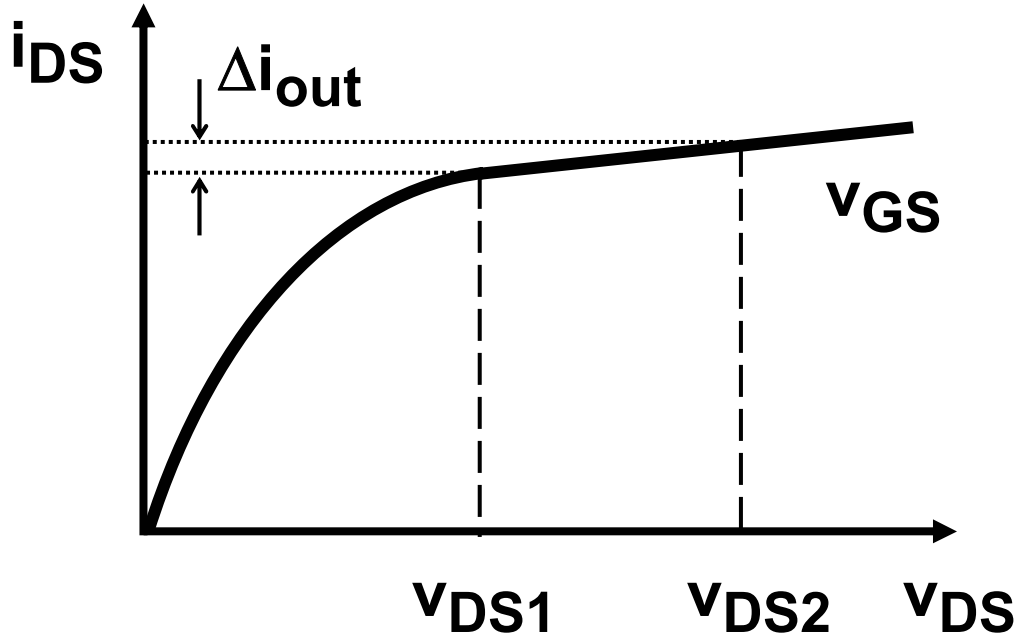
Systematic offset in current mirror

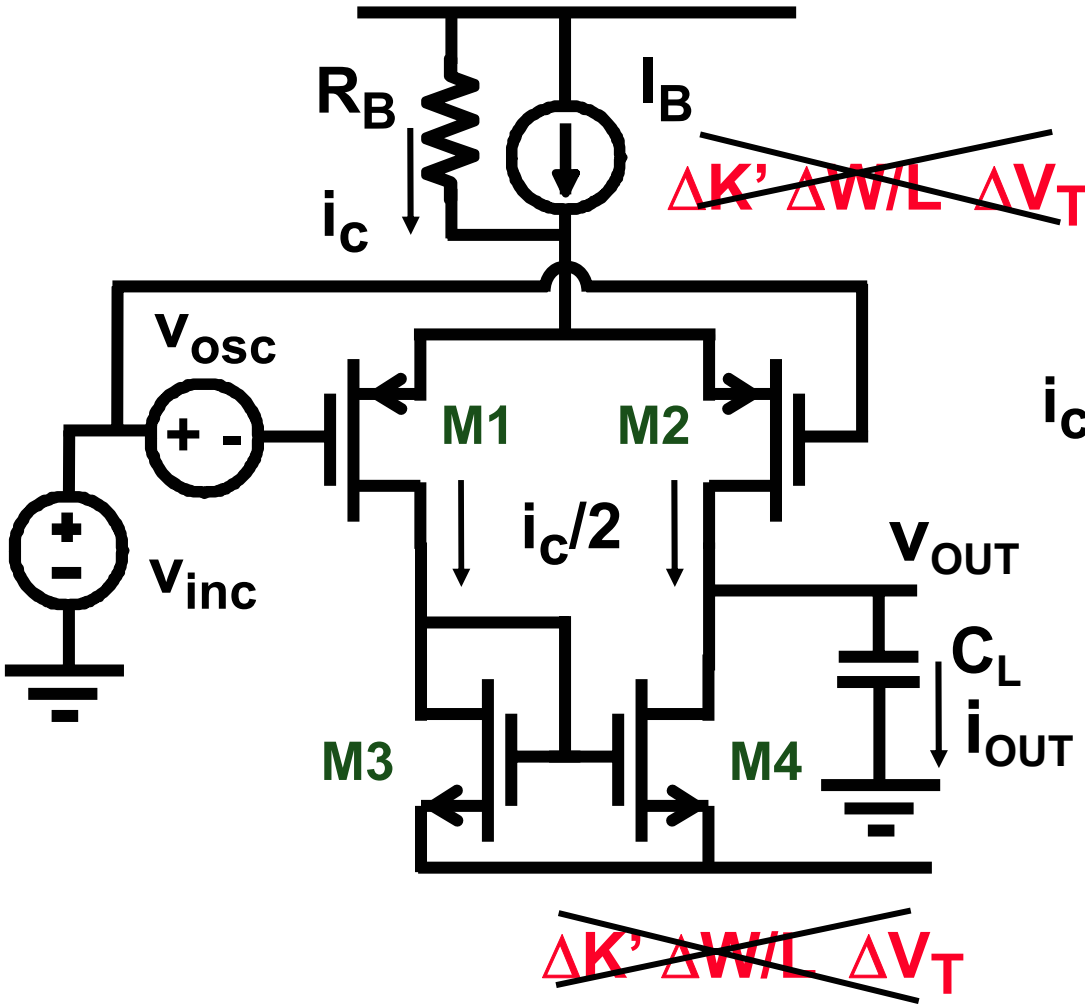




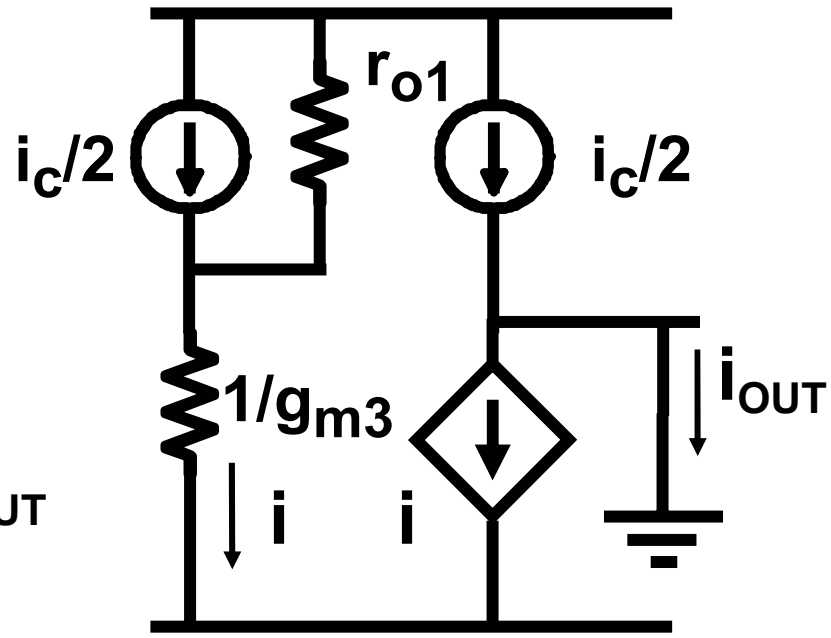
~~$\Delta K' \; \Delta W/L \; \Delta V_T$~~

$$\frac{\Delta i_{out}}{i_{out}} = \frac{v_{DS2} - v_{DS1}}{V_E L_2}$$

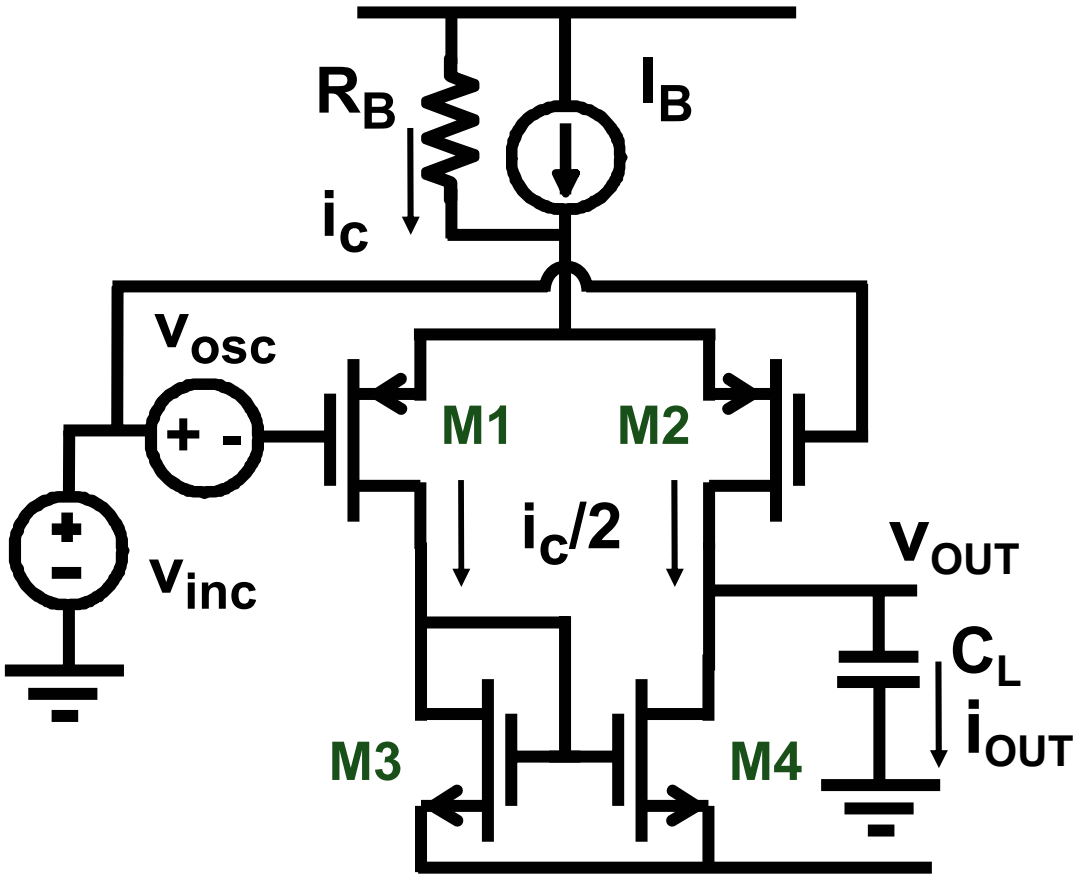
Systematic CMRR in differential Pair - 1



$$i_c = \frac{v_{inc}}{R_B} \qquad \frac{i_{out}}{i_c} = \frac{2}{g_{m3}r_{o1}}$$



Systematic CMRR in differential Pair - 2



$$\frac{i_{out}}{v_{inc}} = \frac{1}{R_B}\,\frac{2}{g_{m3}r_{o1}}$$

$$\frac{i_{out}}{v_{osc}} = g_{m1}$$

v_{ind}

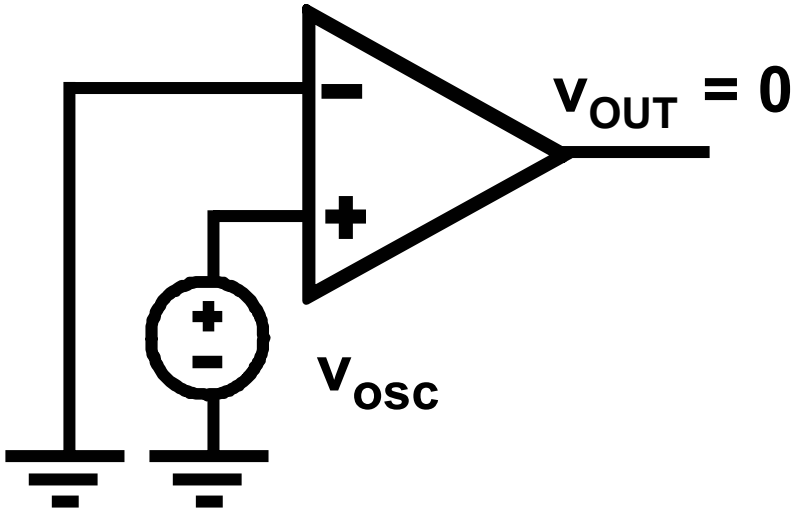
$$\frac{\dfrac{i_{out}}{v_{inc}}}{\dfrac{i_{out}}{v_{osc}}} = \frac{A_{dc}}{A_{dd}} = \frac{1}{CMRR_s}$$

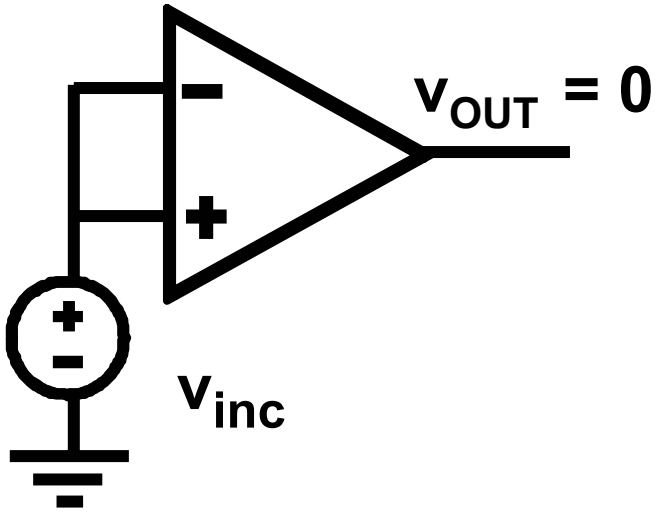
Systematic CMRR in differential Pair - 3

$$\frac{\frac{i_{out}}{v_{inc}}}{\frac{i_{out}}{v_{osc}}} = \frac{v_{osc}}{v_{inc}} = \frac{A_{dc}}{A_{dd}} = \frac{1}{CMRR_s}$$

$$CMRR_s = \frac{1}{2} g_{m1} R_B g_{m3} r_{o1}$$

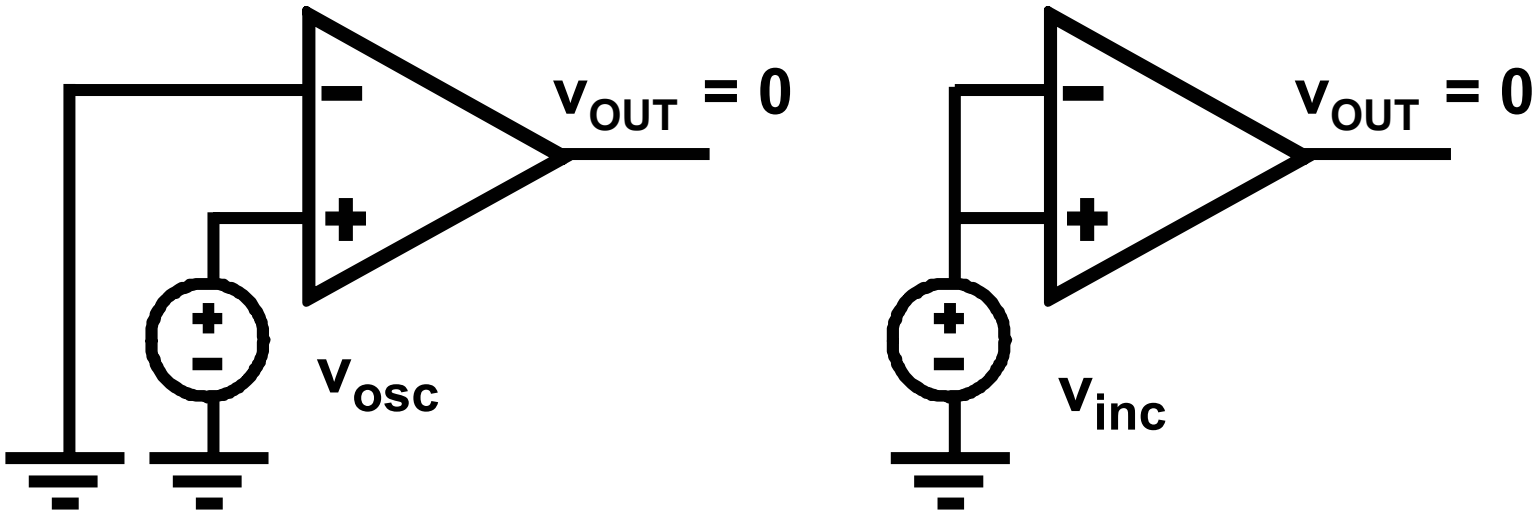
$$CMRR_s \, v_{osc} = v_{inc}$$



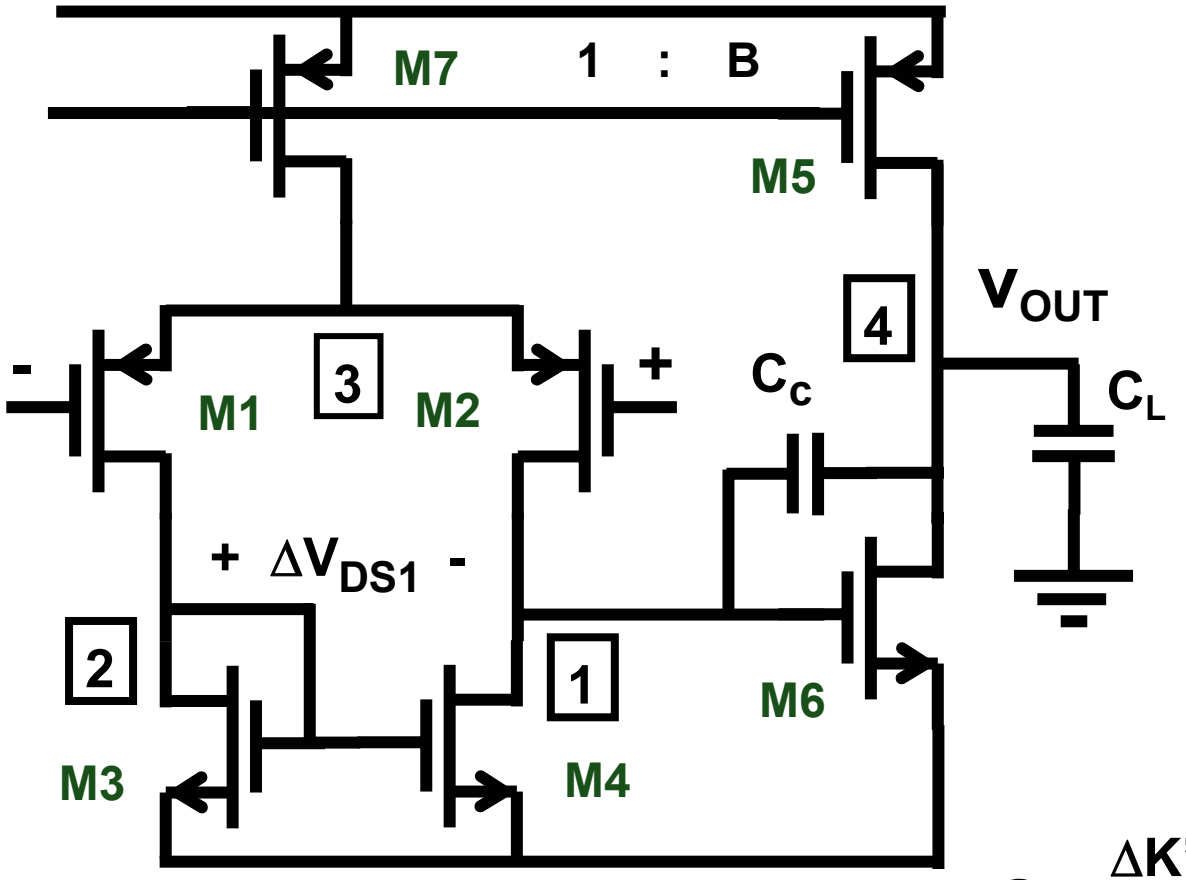


Total CMRR

$$\frac{1}{CMRR} = \frac{1}{CMRR_r} + \frac{1}{CMRR_s}$$



Offset Miller CMOS OTA

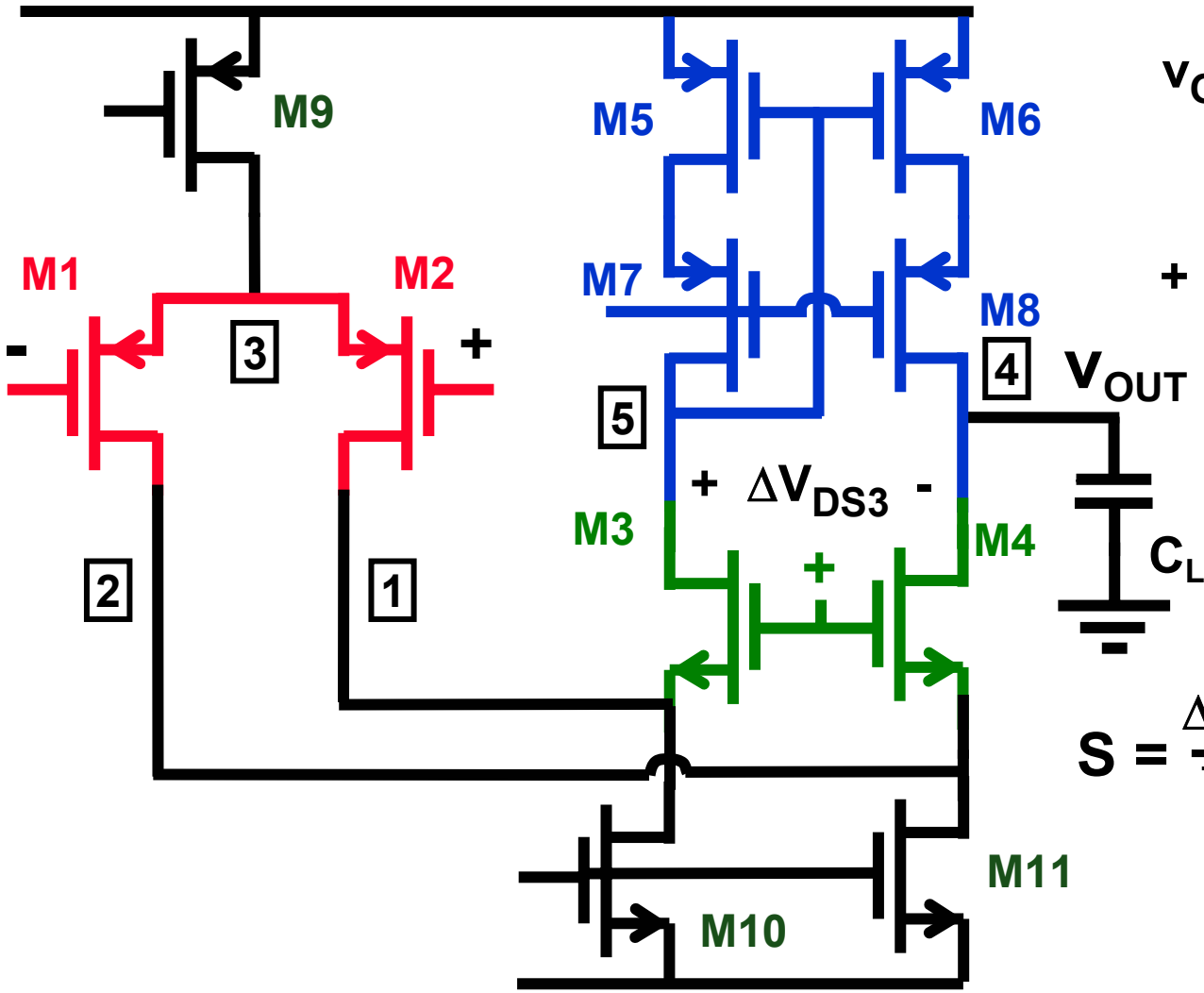


$$A_{v1} = g_{m1}\, r_{02} // r_{04}$$

$$v_{OS} = \frac{\Delta V_{DS1}}{A_{v1}} + \Delta V_{T1} + \frac{g_{m3}}{g_{m1}} \Delta V_{T3}^{*} + \frac{V_{GS1} - V_T}{2} S$$

$$S = \frac{\Delta K'_n}{K'_n} + \frac{\Delta K'_p}{K'_p} + \frac{\Delta W/L_1}{W/L_1} + \frac{\Delta W/L_3}{W/L_3}$$

Offset Folded cascode CMOS OTA



$$v_{OS} = \frac{\Delta V_{DS3}}{A_v} + \Delta V_{T1} + \frac{g_{m6}}{g_{m1}}\Delta V_{T5} + \frac{g_{m11}}{g_{m1}}\Delta V_{T11}^{*} + \frac{V_{GS1} - V_T}{2} S$$

$$S = \frac{\Delta K'_n}{K'_n} + \frac{\Delta K'_p}{K'_p} + \frac{\Delta W/L_{1,6,11}}{W/L_{1,6,11}}$$

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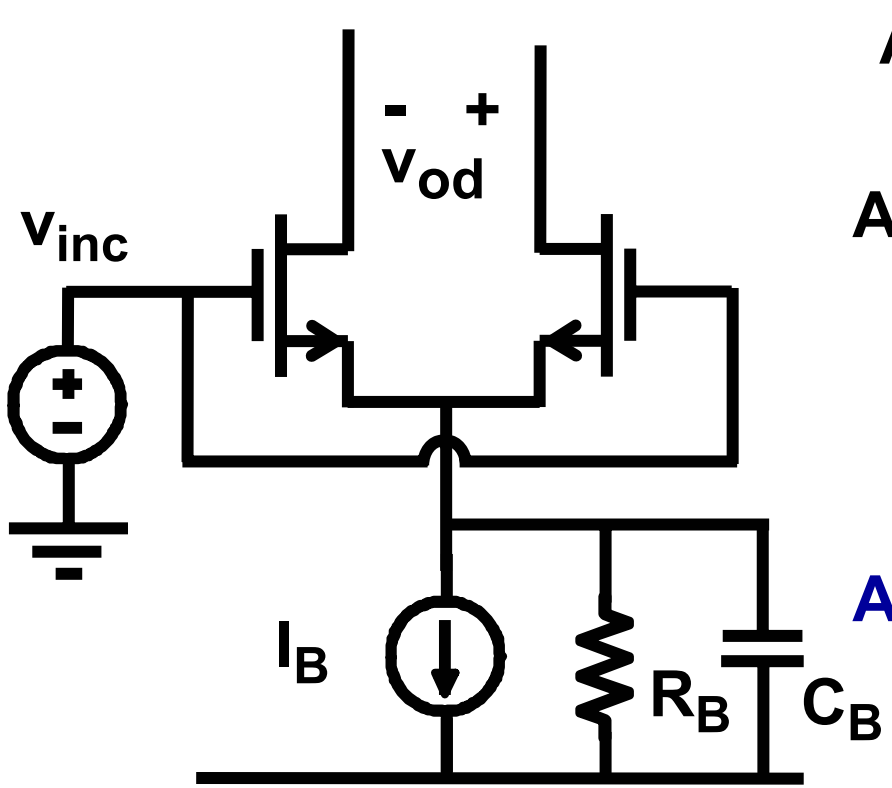
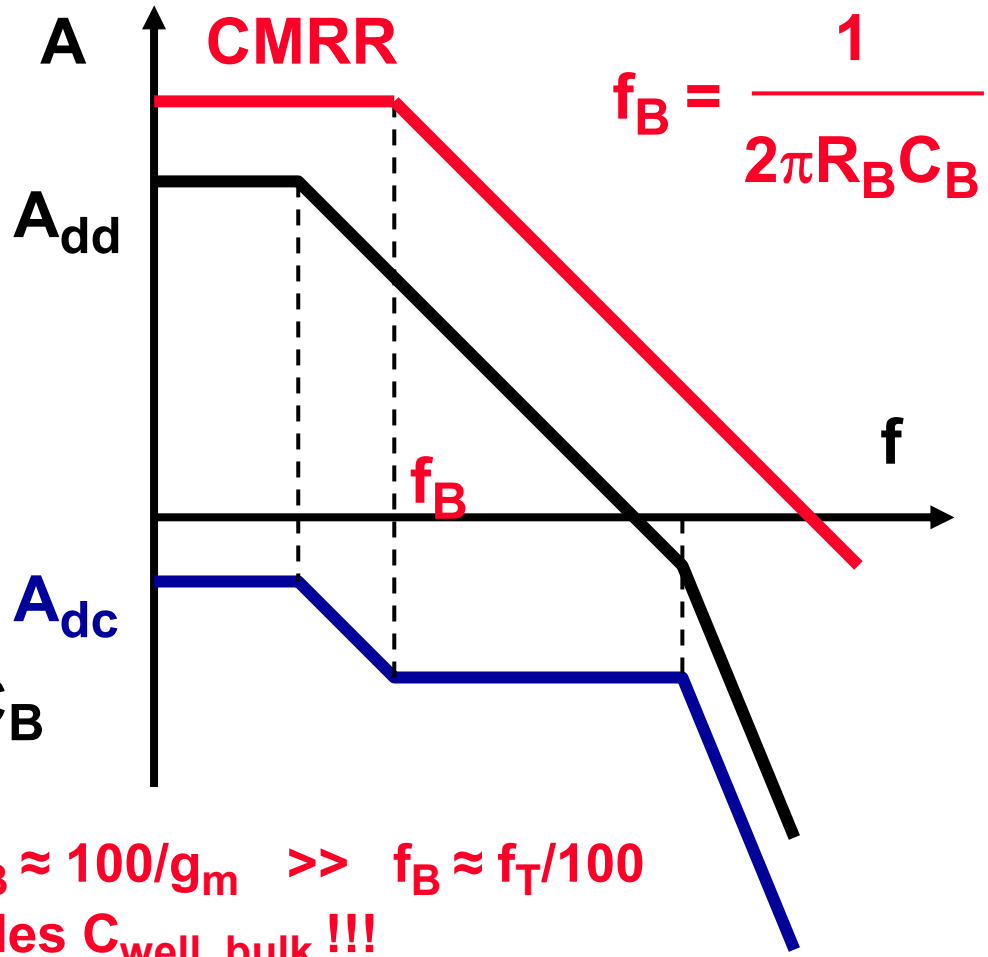
Ref.: Laker, Sansen : Design of analog …, MacGrawHill 1994

CMRR vs frequency





$C_B \approx C_{GS}$ $R_B \approx 100/g_m$ >> $f_B \approx f_T/100$

BUT C_B includes $C_{well,\ bulk}$!!!

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Layout rules for low offset

1. Equal nature
2. Same temperature
3. Increase size
4. Minimum distance
5. Same orientation
6. Same area/perimeter ratio
7. Round shape
8. Centroide layout
9. End dummies
10. Bipolar always better !

Hastings,
"The Art of Analog Layout"
Prentice Hall 2001
R. Soin, .."A-D Asics, .. "
Peregrinus, 1991

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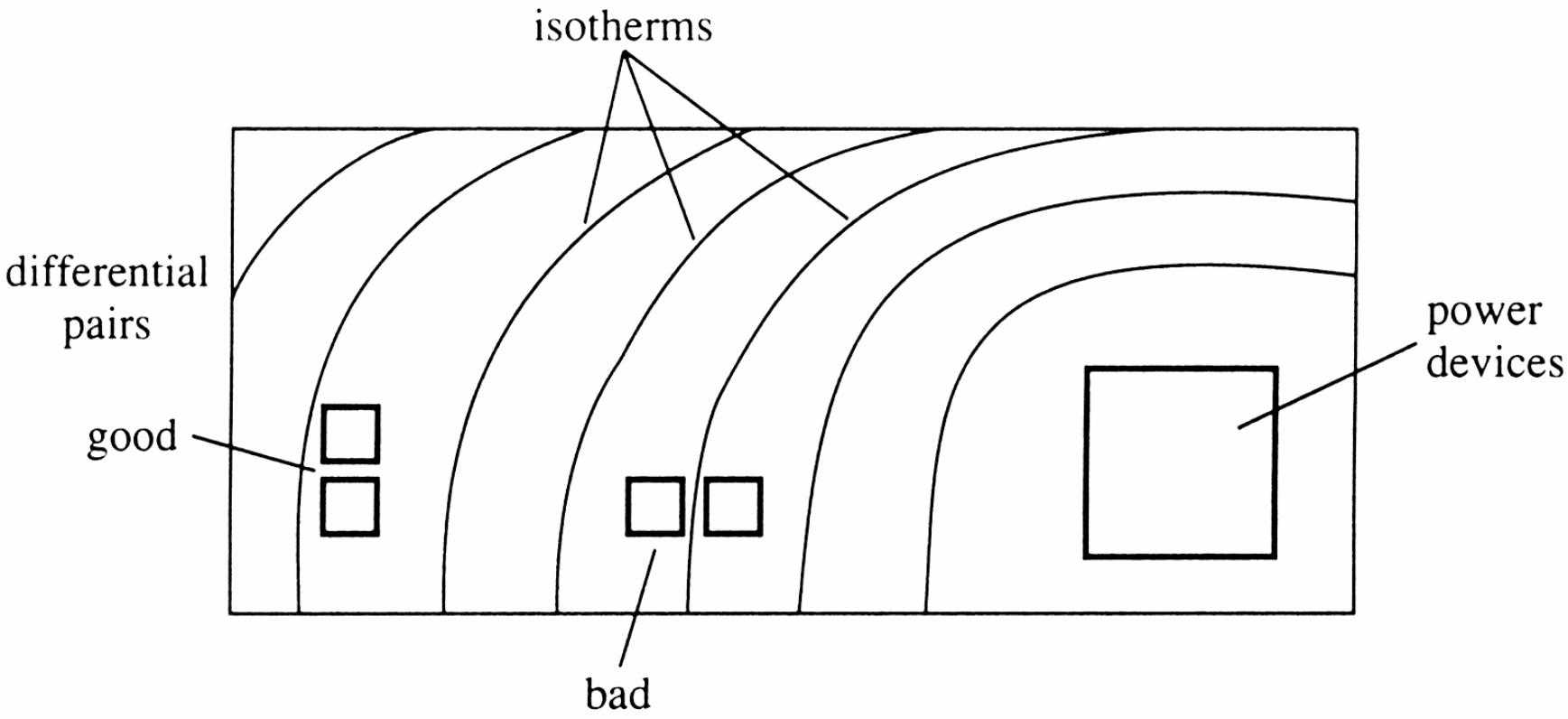
On same isotherm



Solomon, JSSC Dec 74, 314-332

Layout rules for low offset

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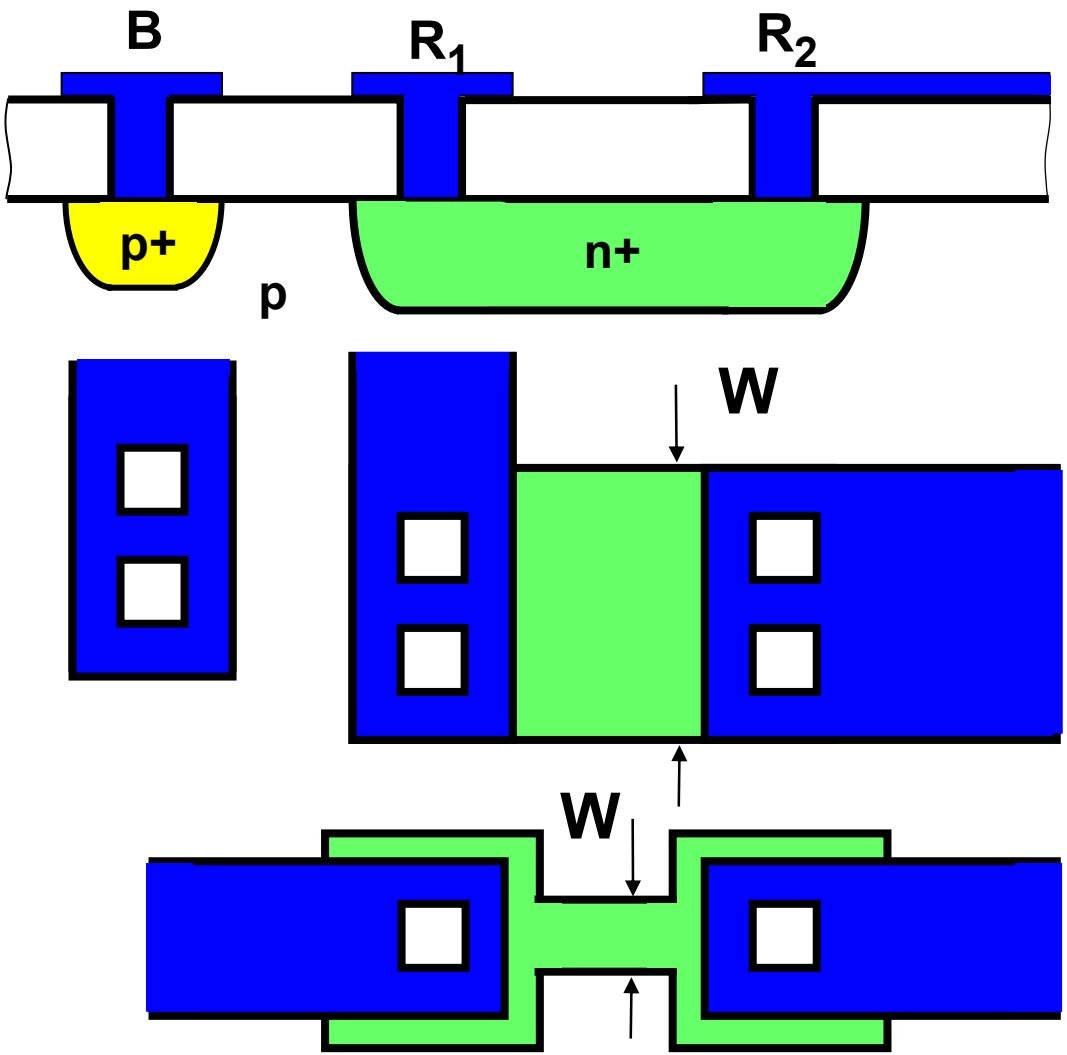
Layout resistor



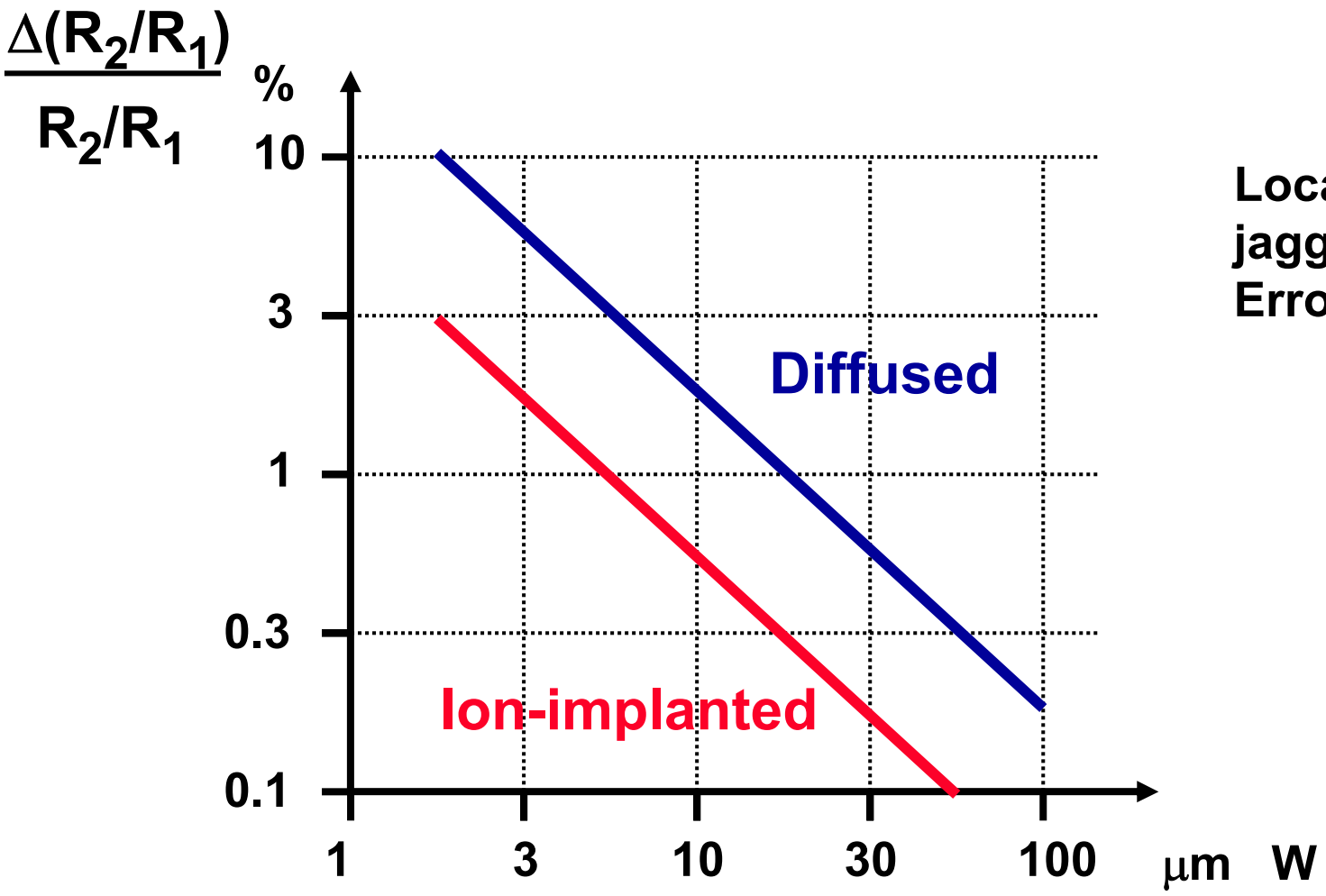
Source/drain diffusion resistor in CMOS

Ref.: Laker, Sansen : Design of analog …, MacGrawHill 1994 Table 2-6

Table resistors

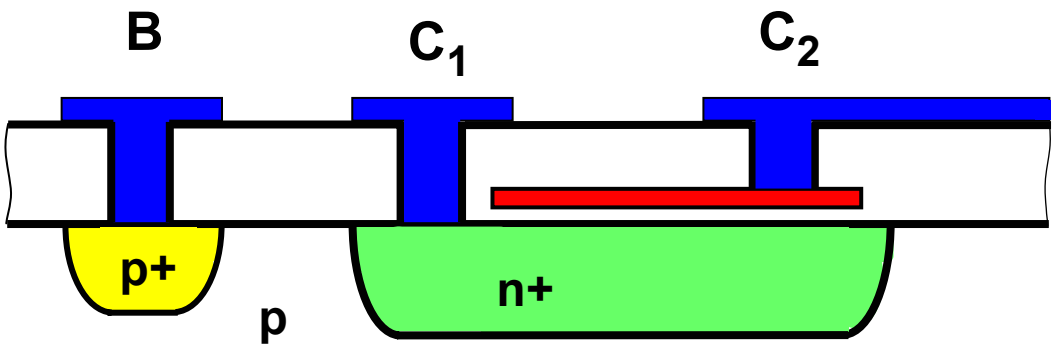
Process	Type	$\rho\square$ $\Omega/\square$	absolute accuracy percent	temperature coefficient percent/°C	voltage coefficient percent/V	breakdown voltage V
Bipolar	base diffusion	150	10	0.12	2	50
	emitter diffusion	10	20	0.02	0.5	7
	pinch resistance	5 k	40	0.33	5	7
	epi layer	1 k	10	0.3	1	60
	aluminum	50 m	20	0.01	0.02	90
	ion-implantation	2 k	1	0.02	0.2	20
	ion-implantation	200	0.3	0.02	0.05	20
CMOS	S/D diffusion	20-50	20	0.2	0.5	20
	well	2.5 k	10	0.3	1	20
	poly gate	50	20	0.2	0.05	40
	poly resistance	1.5 k	1	0.05	0.02	20
	aluminum	50 m	20	0.01	0.02	90
Thin film	NiCr(Ta)	200	1	0.005	0.005	90
	aluminum	50 m	20	0.01	0.02	90

Mismatch vs size for resistors

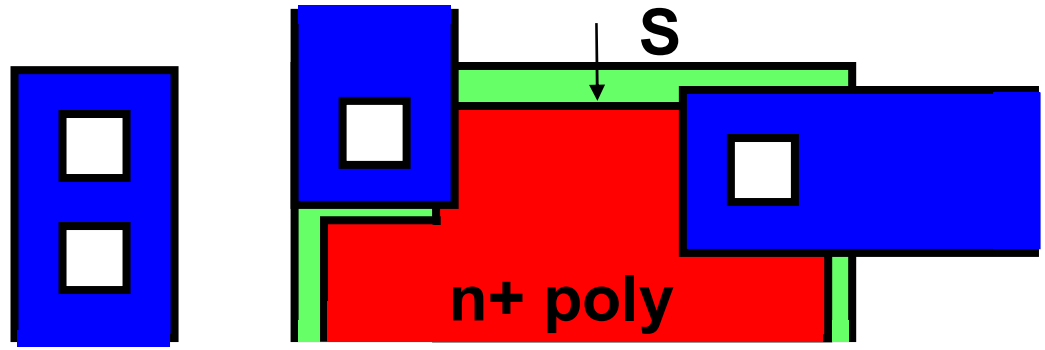


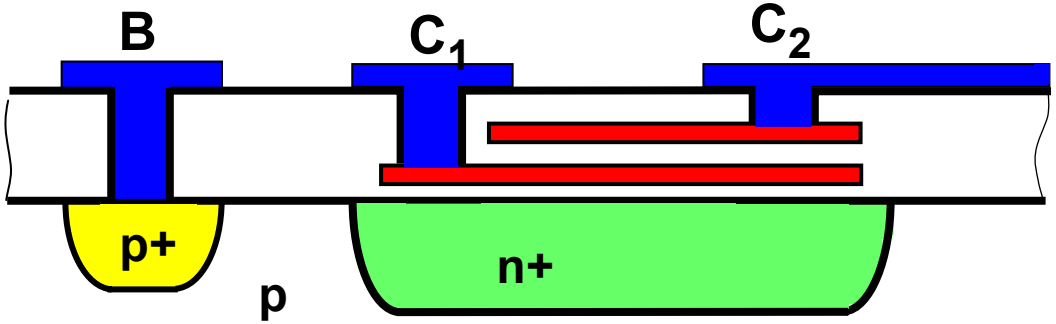
Local errors :
jagged edges, ..
Error ~ 1/size

Layout capacitors



Poly to S/D capacitor





Poly to poly capacitor

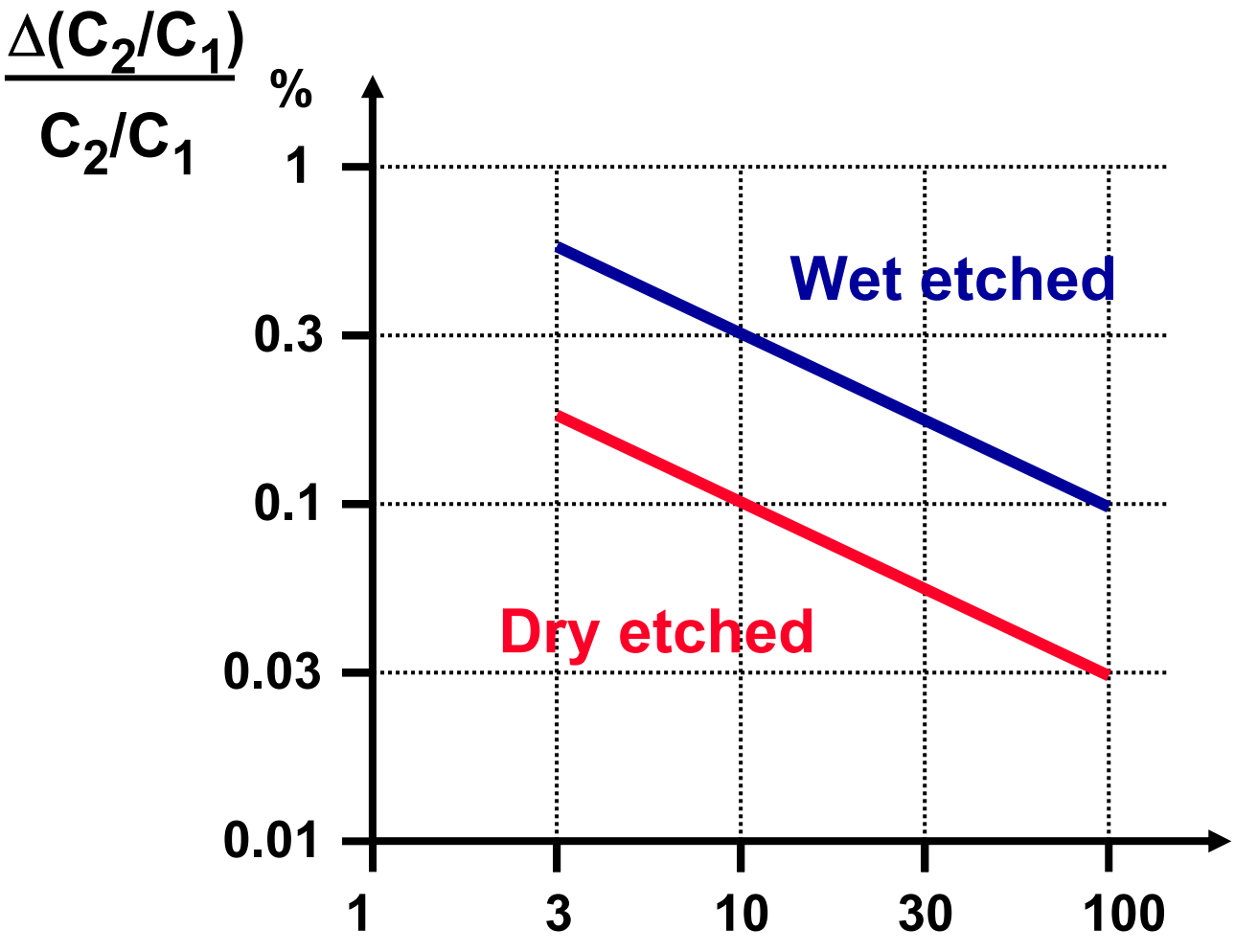
$$C_{par} \approx \frac{1}{6 \ldots 15} C_{pp}$$

Table capacitors

Process	Type	C nF/cm^2	absolute accuracy percent	temperature coefficient percent/°C	voltage coefficient percent V	breakdown voltage V
Bipolar	C_{CB}	16	10	0.02	2	50
	C_{EB}	50	10	0.02	1	7
	C_{CS}	8	20	0.01	0.5	60
CMOS	C_{ox}(50 nm)	70	5	0.002	0.005	40
	$C_{m,poly}$	12	10	0.002	0.005	40
	$C_{poly,poly}$	56	2	0.002	0.005	40
	$C_{poly,substrate}$	6.5	10	0.01	0.05	20
	$C_{m,substrate}$	5.2	10	0.01	0.05	20
	$C_{poly,substrate}$	6.5	10	0.01	0.05	20

Ref.: Laker, Sansen : Design of analog …, MacGrawHill 1994 Table 2-7

Mismatch vs size for capacitors



Local errors :
jagged edges, ..
Error ~ 1/size

Global errors :
oxide thickness,
bulk doping, ..

Layout rules for low offset

1. Equal nature
2. Same temperature
3. Increase size
4. Minimum distance
5. Same orientation
6. Same area/perimeter ratio
7. Round shape
8. Centroide layout
9. End dummies
10. Bipolar always better !

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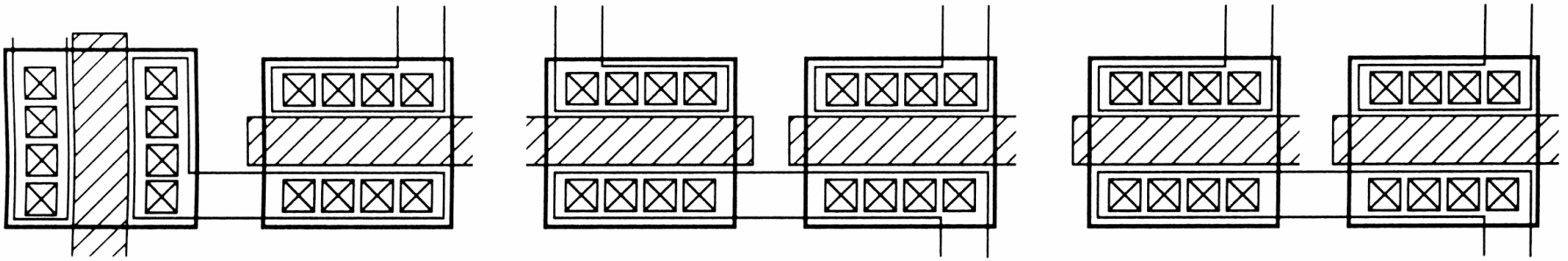
Matching of transistor pairs



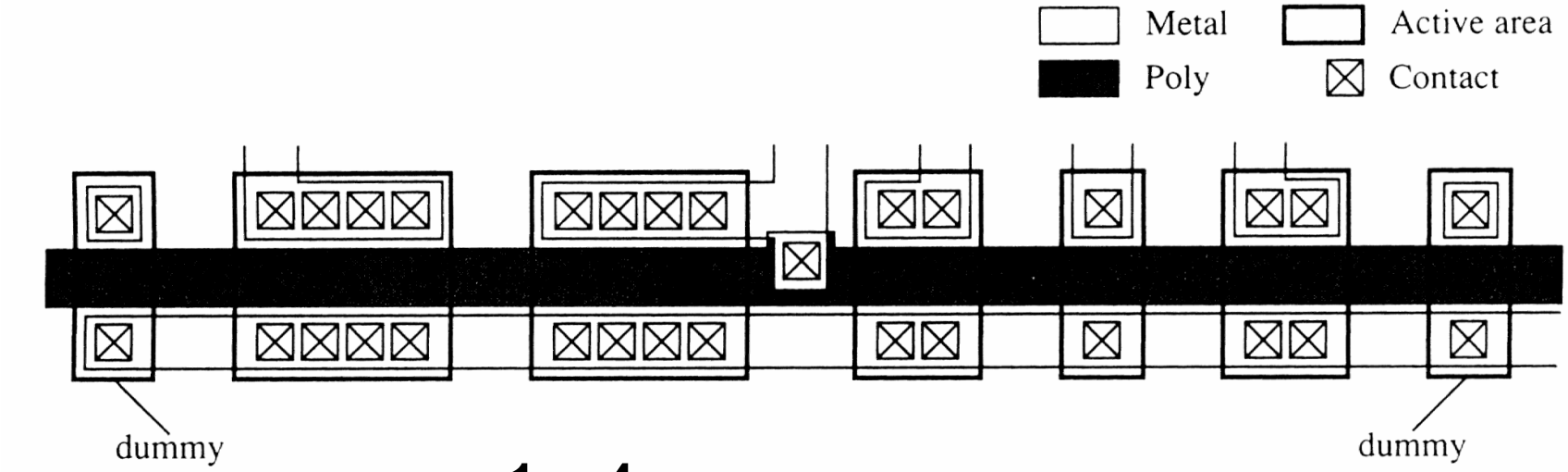
Bad **Better** **Better**

Layout rules for low offset

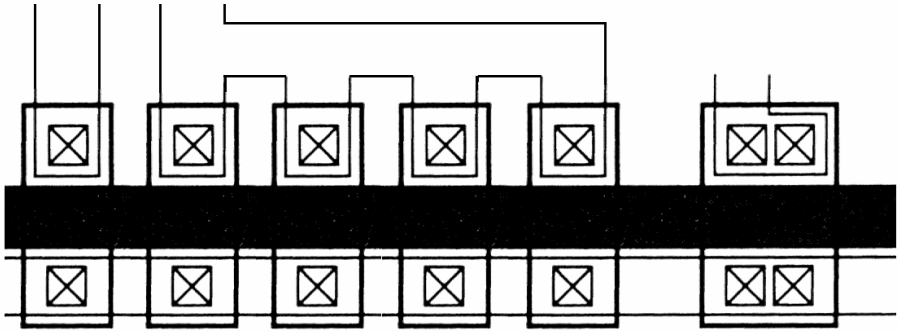
1. Equal nature
2. Same temperature
3. Increase size
4. Minimum distance
5. Same orientation
6. Same area/perimeter ratio
7. Round shape
8. Centroide layout
9. End dummies
10. Bipolar always better !

Matching of current mirrors

Current mirror 4:4:2:1:2 with end dummies.



1 : 4



Layout rules for low offset

1. Equal nature
2. Same temperature
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9. End dummies
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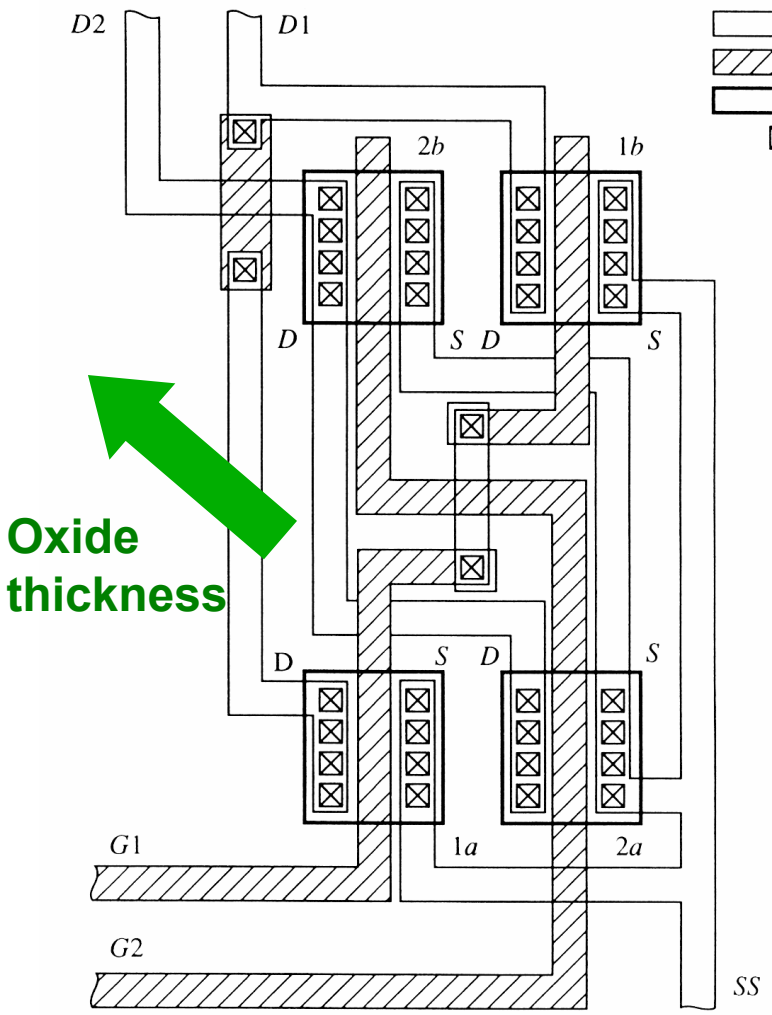
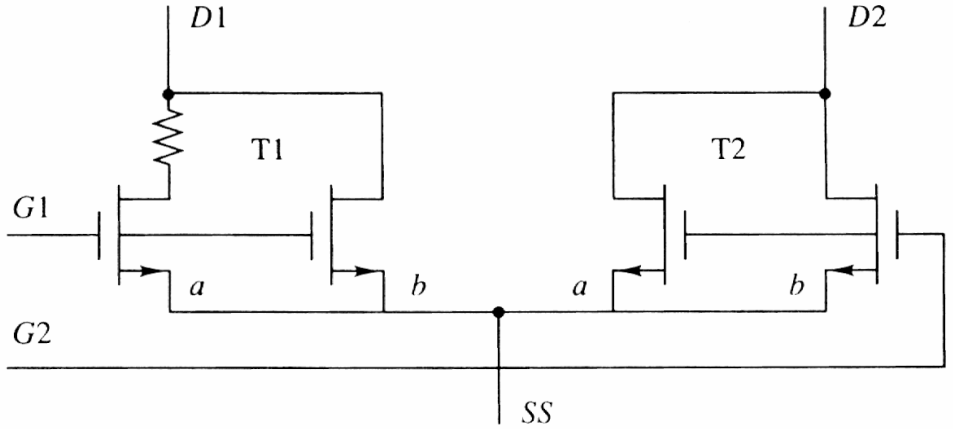
Cross-coupled differential pair

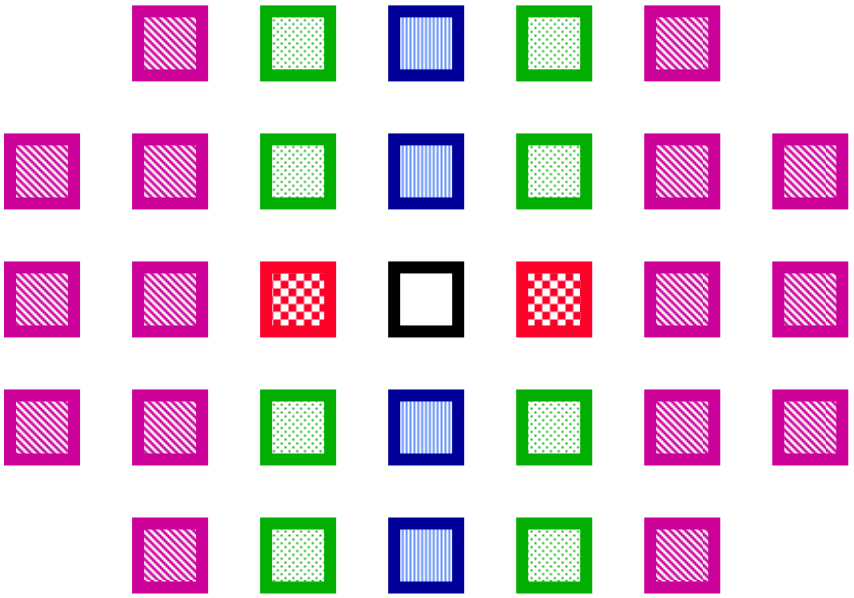


Oxide thickness



Less sensitive to global variations :
Oxide thickness
Substrate doping level
……..

Centroide layout of capacitors



Ratio:

1

2

4

8

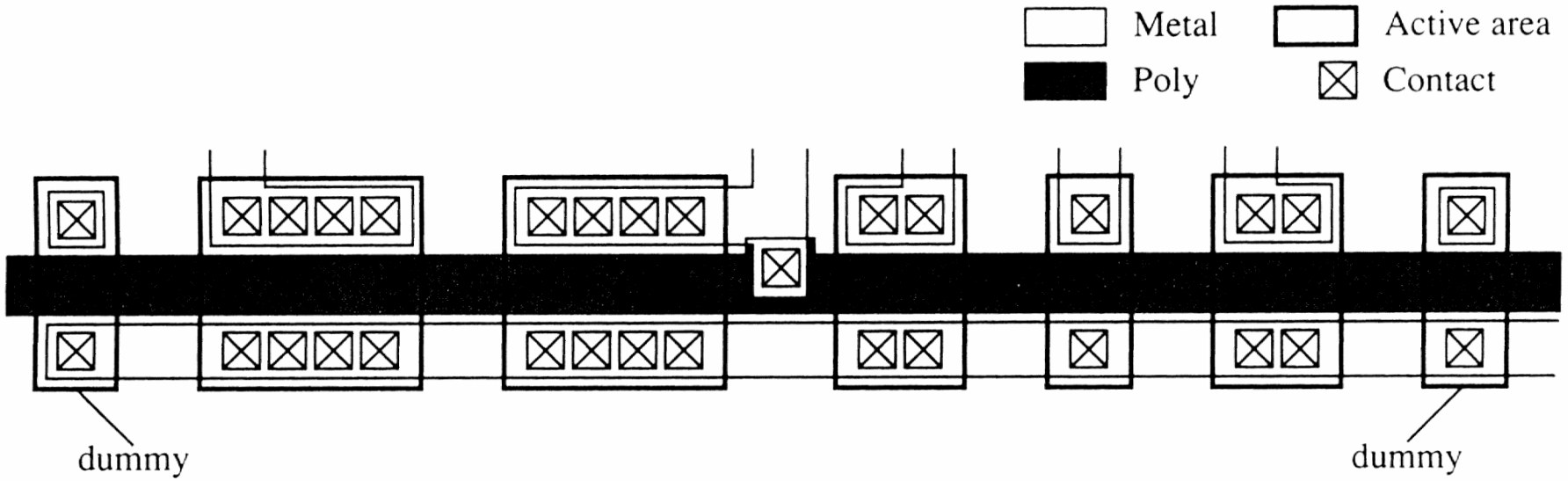
16

Layout rules for low offset

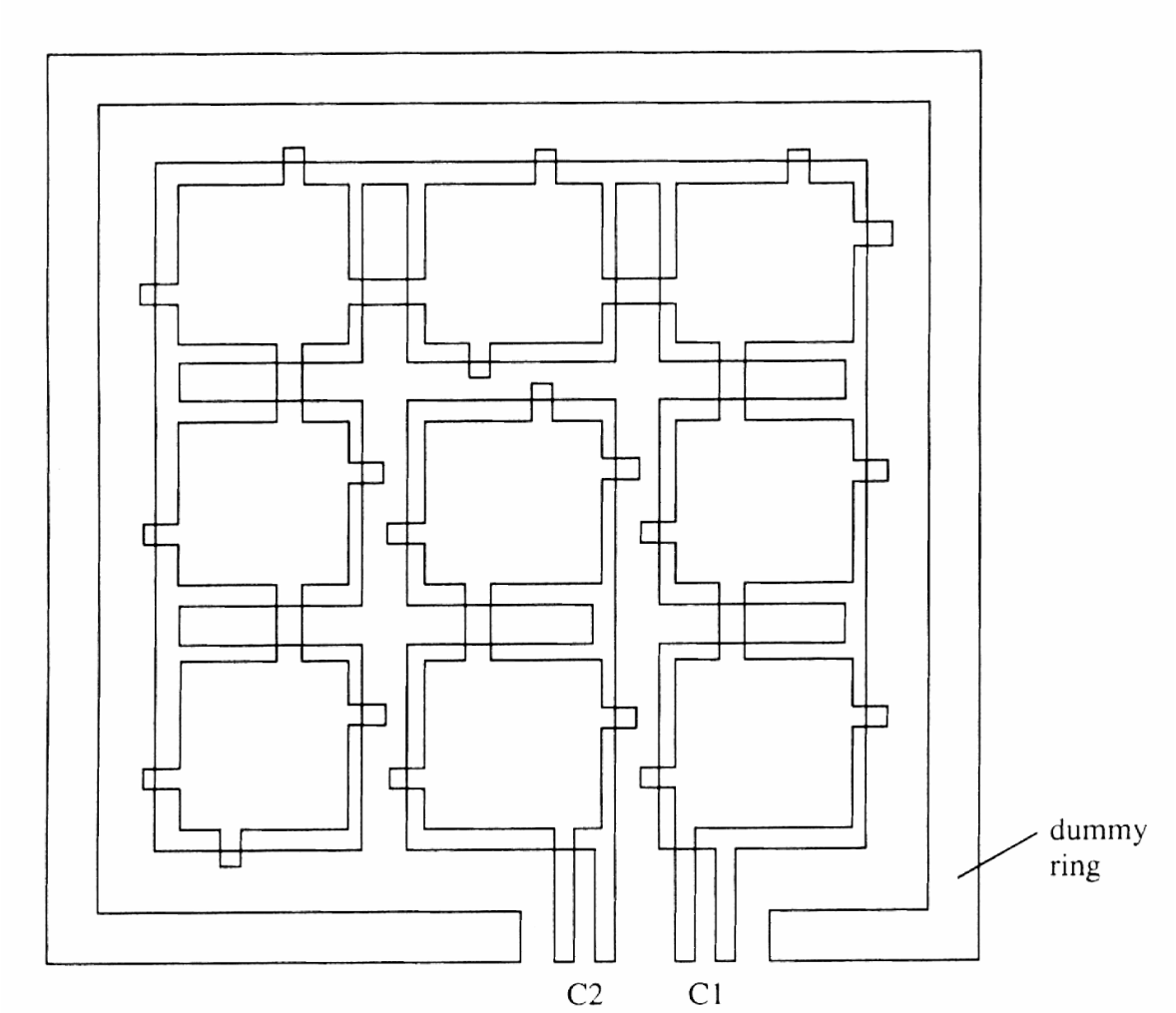
1. Equal nature
2. Same temperature
3. Increase size
4. Minimum distance
5. Same orientation
6. Same area/perimeter ratio
7. Round shape
8. Centroide layout
9. End dummies
10. Bipolar always better !

Matching of current mirrors

Current mirror 4:4:2:1:2 with end dummies.



Layout capacitance ratio



Ratio 7/2 = 3.5

Courtesy Vittoz

Layout rules for low offset

1. Equal nature
2. Same temperature
3. Increase size
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Offset of MOST and bipolar transistors

MOST : $$v_{OS} = \Delta V_T + \frac{V_{GS} - V_T}{2}\left(\frac{\Delta R_L}{R_L} + \frac{\Delta K'}{K'} + \frac{\Delta W/L}{W/L}\right)$$

Bipolar : $$v_{OS} = \frac{kT}{q}\left(\frac{\Delta R_L}{R_L} + \frac{\Delta I_S}{I_S}\right)$$ is much smaller !!

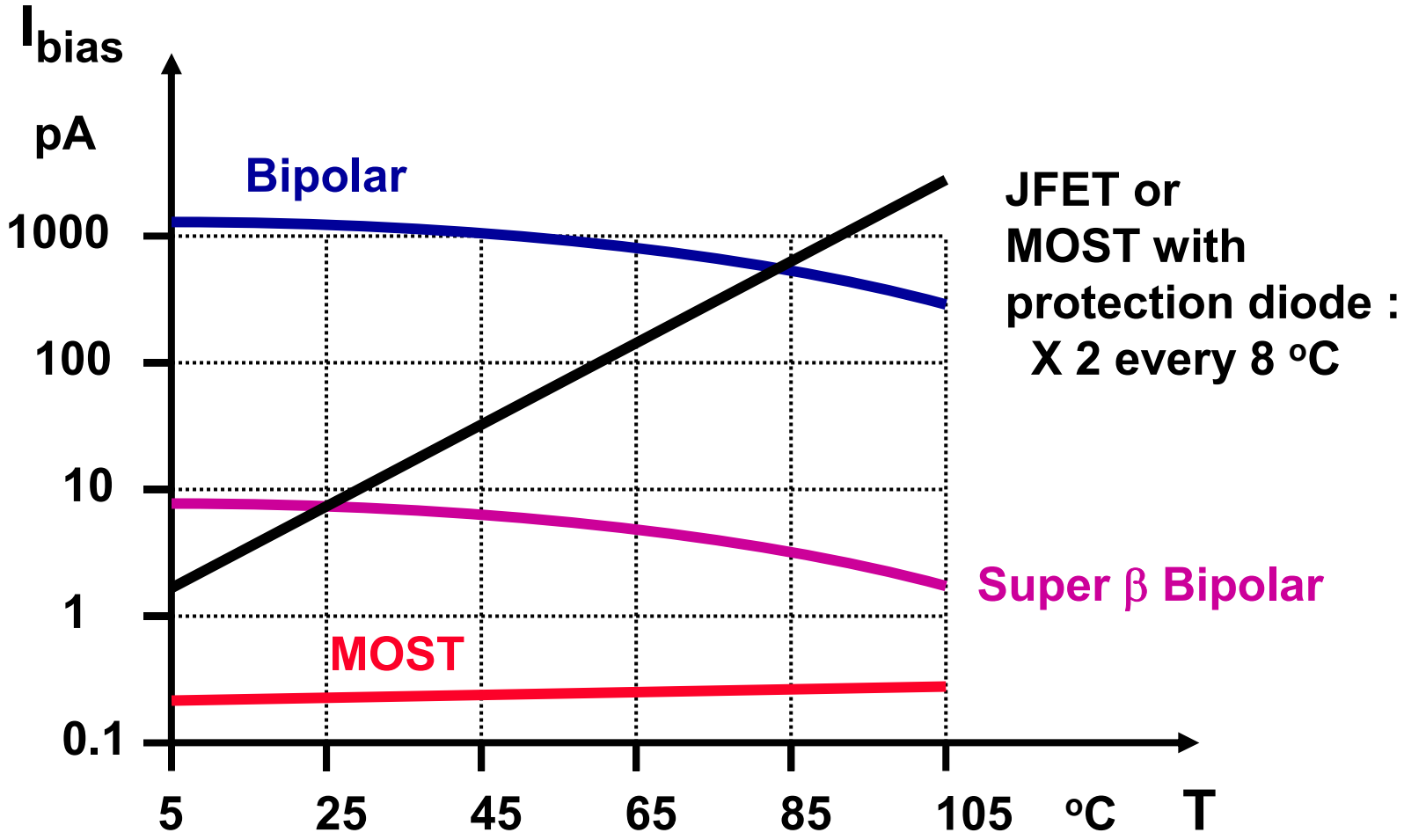
1) no V_T

2) $kT/q \ll (V_{GS}-V_T)/2$

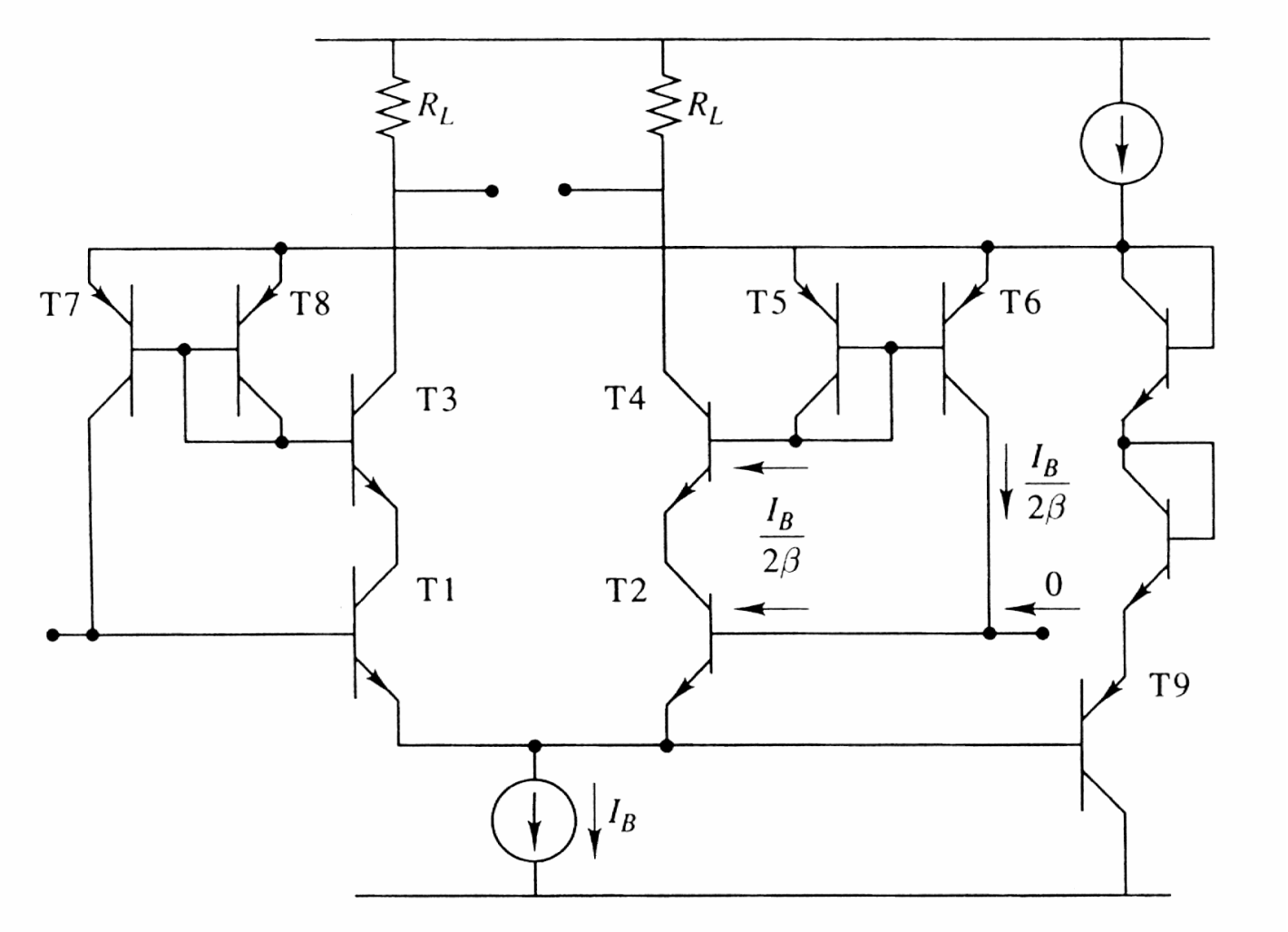
3) Drift decreases with v_{OS} : $$\frac{\Delta v_{OS}}{\Delta T} = \frac{v_{OS}}{T}$$

Bipolar : Base current !

Bias or base currents

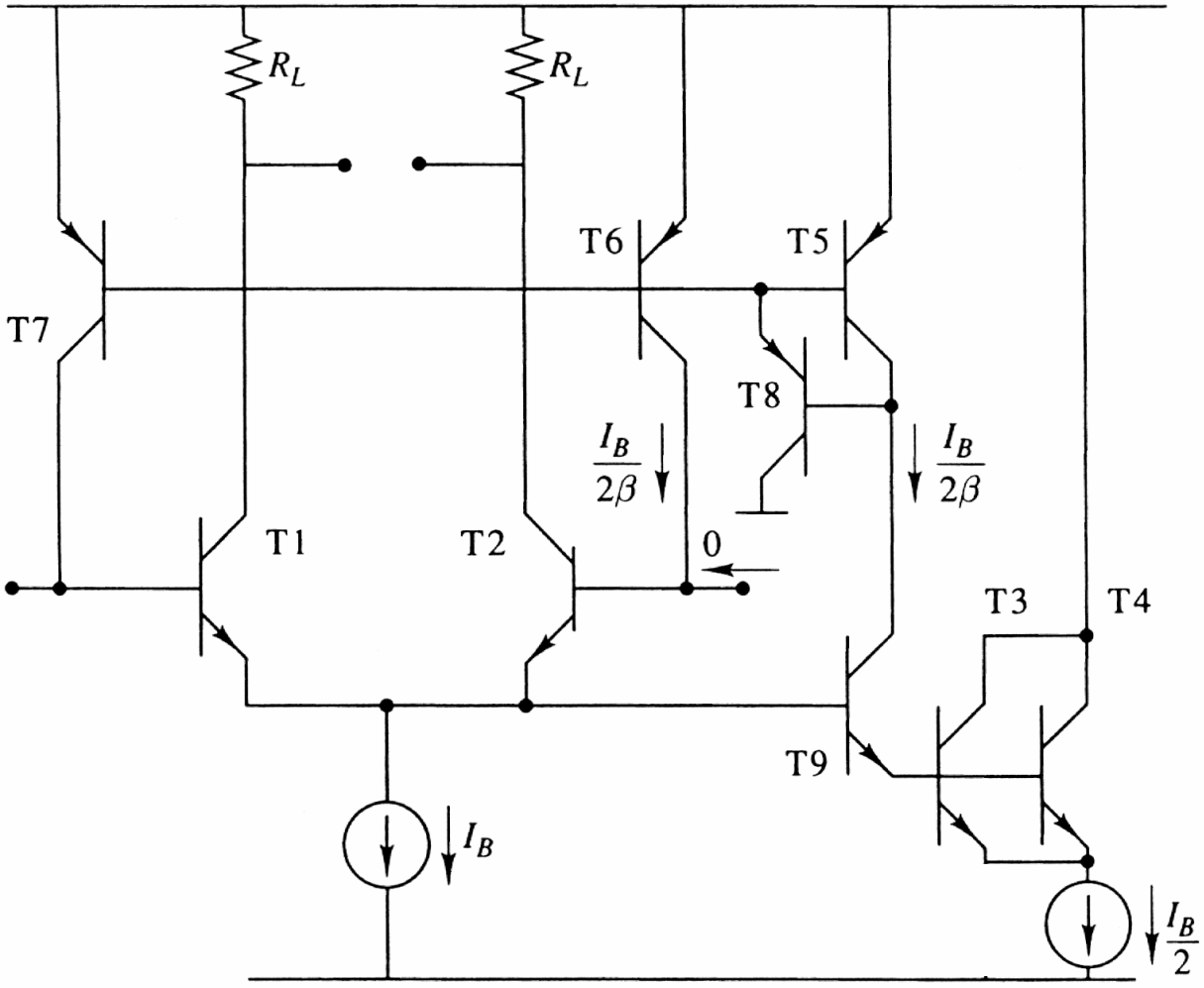


Base current compensation



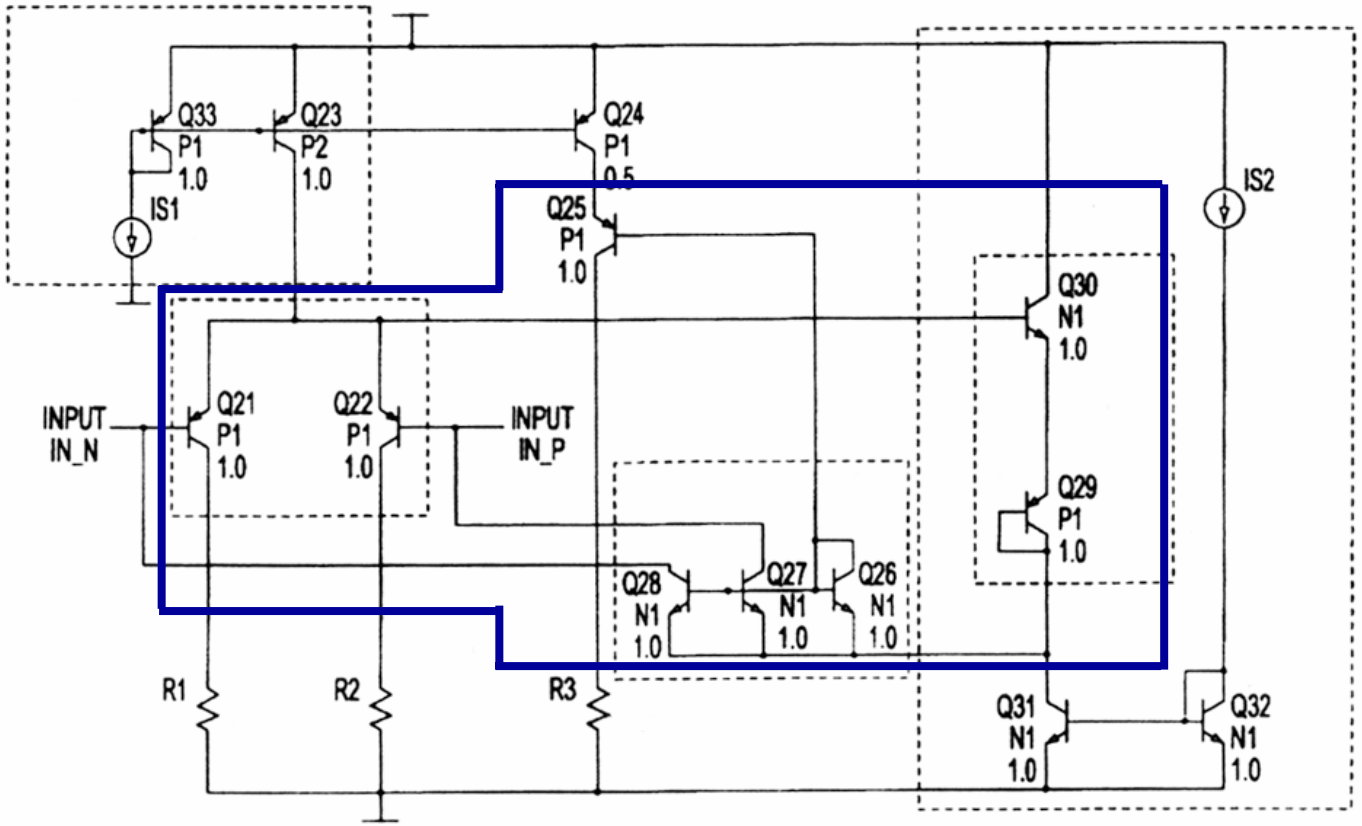
OP07

Common-mode base current compensation



OP27

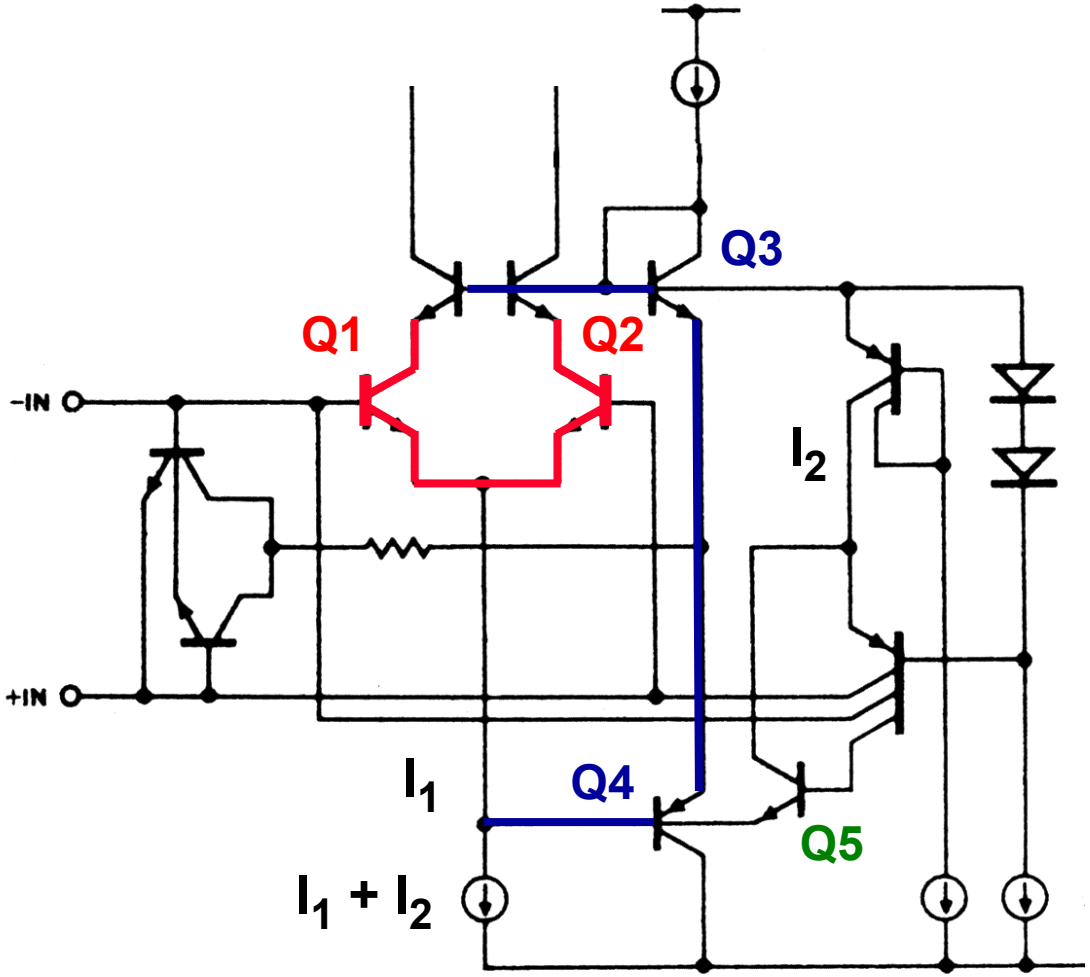
Tracking base current compensation



Q29 & Q30 provide a voltage clamp to track the input bias currents for changes in CM input voltage.

Ref. Gross, JSSC, Feb. 2004, 404.

OP-97 : input current compensation

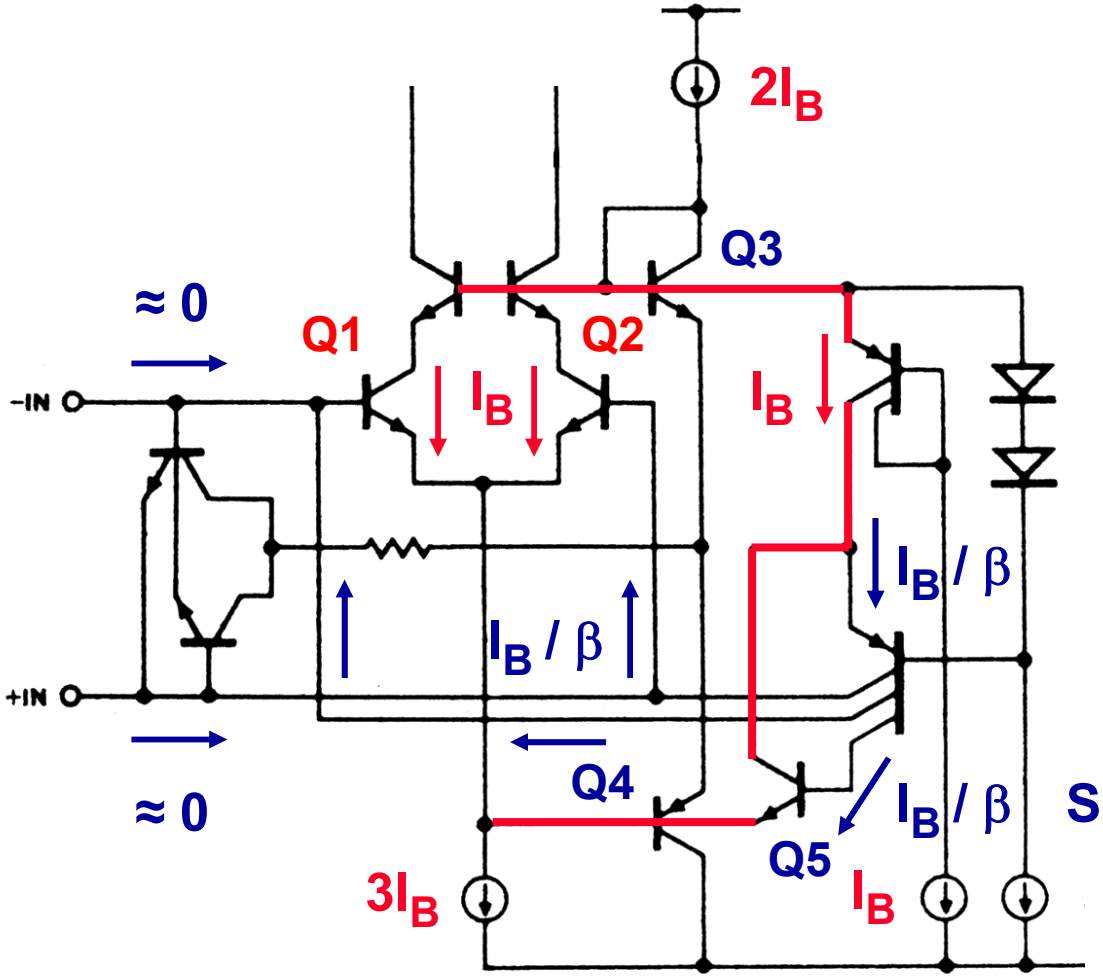


Low input currents because super- β transistors at the input !

Require low V_{CE} !

$V_{CE1,2} = V_{BEon} \approx 0.7$ V

OP-97 : input current compensation



Same β and V_{CE} as input transistors

Limits because of device mismatch

$$\frac{1}{(\text{Accuracy})^2} \approx \sigma^2\left(\frac{\Delta I_{DS}}{I_{DS}}\right) \approx \frac{4\,A_{VT}^{\,2}}{WL\,(V_{GS}-V_T)^2}$$

$$\text{Speed} \approx f_T = \frac{2\,I_{DS}}{2\pi\,WL\,2/3\,C_{ox}\,(V_{GS}-V_T)} \qquad \frac{V_{DD}}{2}$$

$$\frac{\text{Speed x (Accuracy)}^2}{\text{Power}} = \frac{1}{C_{ox}\,A_{VT}^{\,2}} \sim \frac{1}{t_{ox}}$$

= Technological constant

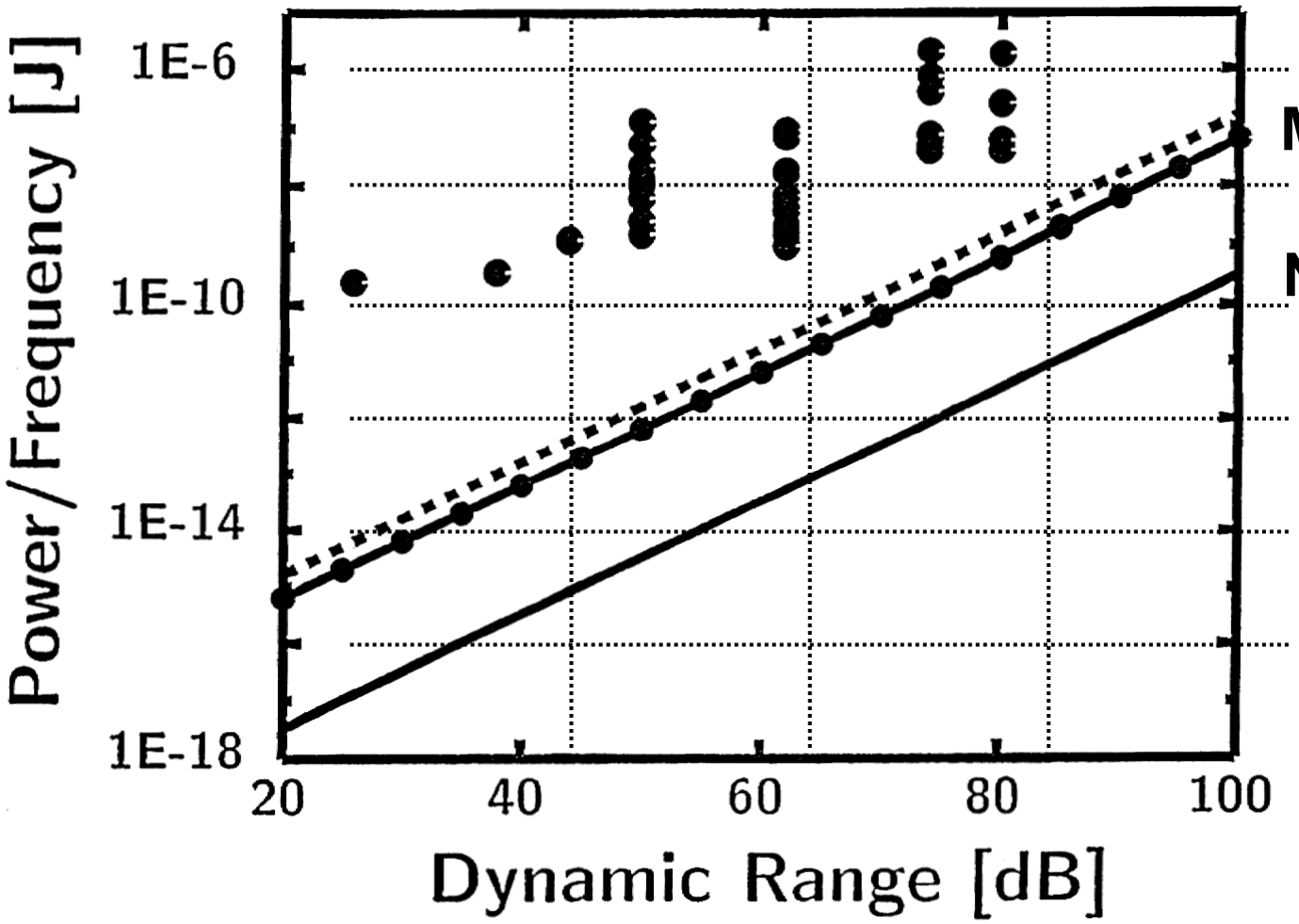
Limits because of device noise

$$S/N = \frac{V_{pp}^2 / 2}{4kT\ R\ BW} \qquad S/N = \frac{V_{pp}^2 / 8}{kT\ /\ C}$$

$$P_{min} = \frac{V_{pp}^2}{R} \qquad P_{min} = V_{DD}\ BW\ V_{pp}\ C$$

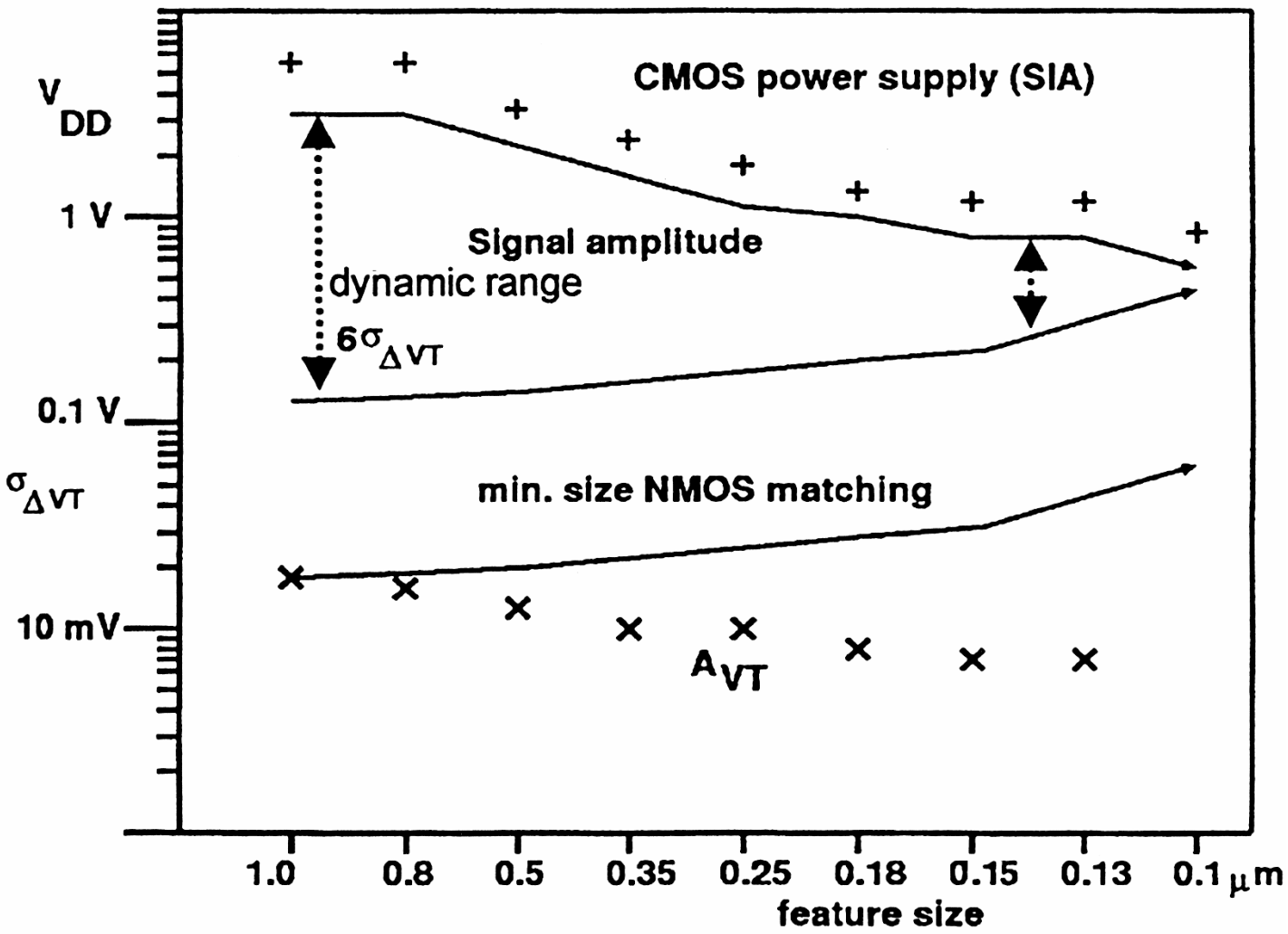
$$P_{min} \approx 8kT\ BW\ S/N$$

Noise versus mismatch for high DR



Ref. P.Kinget, ...
"Analog VLSI .."
page 67,
Kluwer 1997.

Reduced DR in deep submicron CMOS



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- Random offset and $CMRR_r$
- Systematic offset and $CMRR_s$
- CMRR versus frequency
- Design rules
- Comparison MOST and bipolar transistors

Ref: Pelgrom, JSSC Oct.1989, 1433-1439
Croon, JSSC Aug.02, 1056-1064
Croon, Springer, 2005