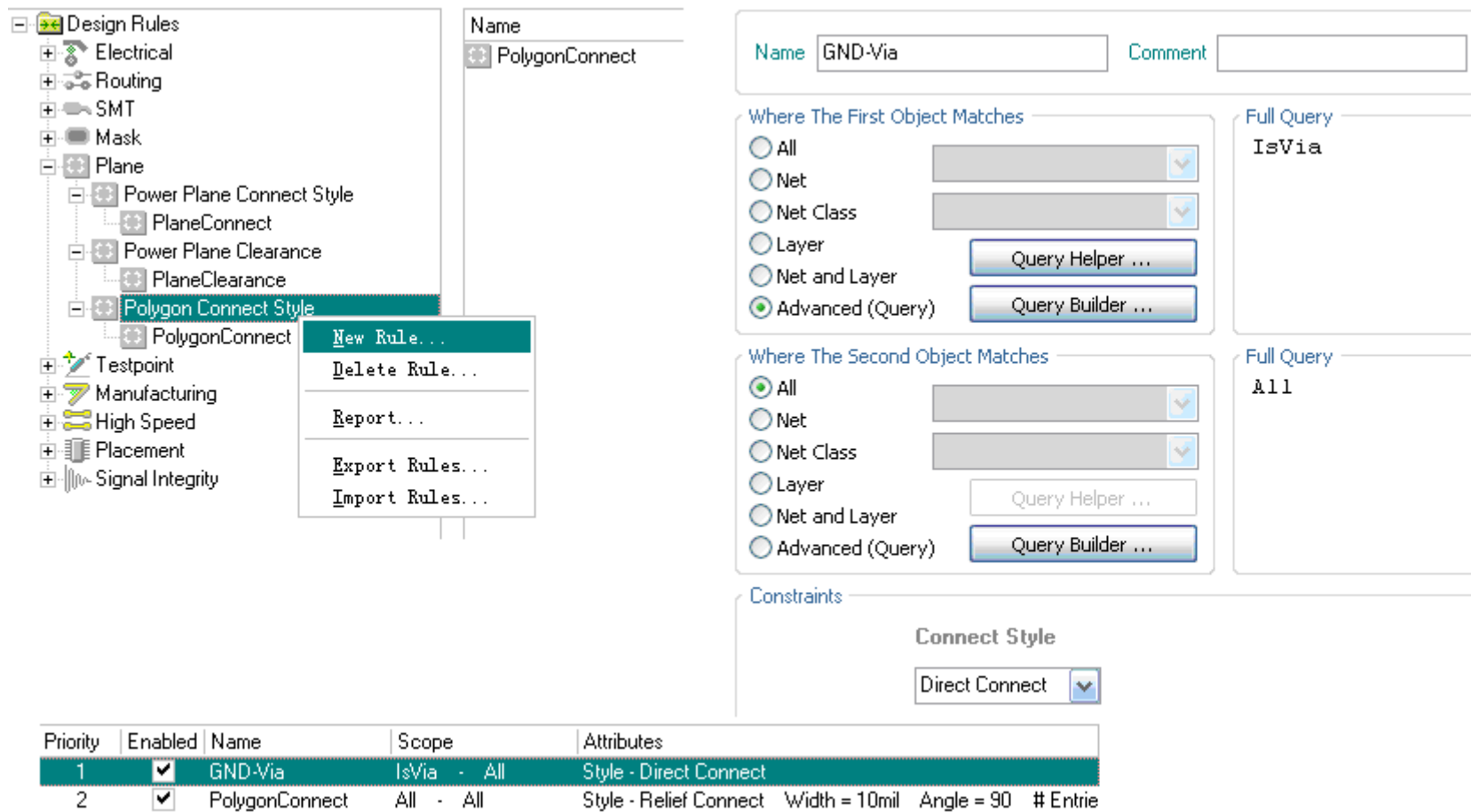


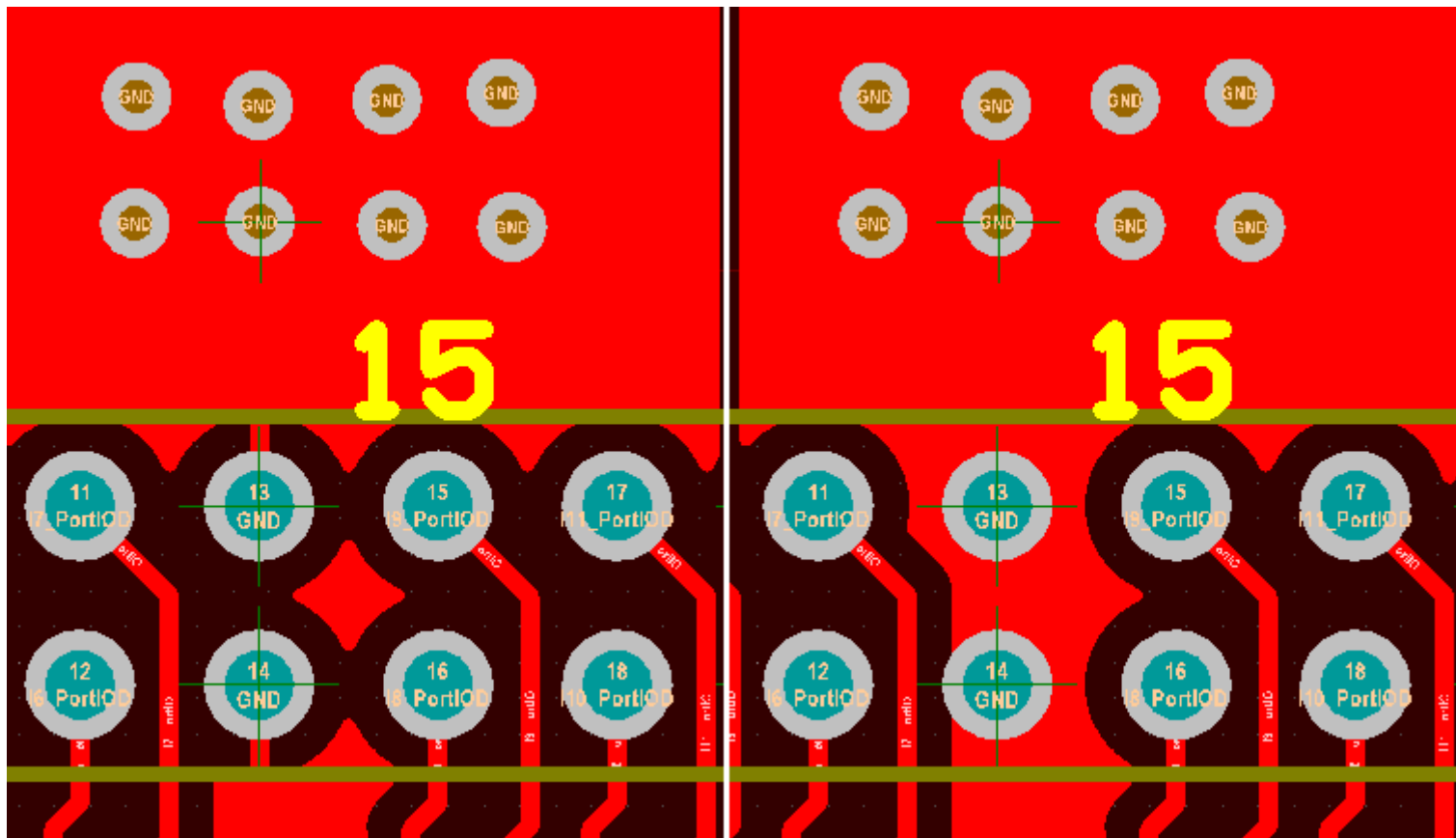
## 覆铜高级连接方式

如过孔全连接，焊盘热焊盘连接；顶层 GND 网络全连接，其他层热焊盘连接线宽 0.3mm

在 AD PCB 环境下，Design>Rules>Plane> Polygon Connect style ,点中 Polygon Connect style，右键点击 new rule -----新建一个规则 点击新建的规则既选中该规则，在 name 框中改变里面的内容即可修改该规则的名称，默认是 PolygonConnect\_1，现我们修改为 GND-Via，选项 Where The Frist Object Matches 选Advanced (Query)，Full Query 输入IsVia（大小写随意），Connect Style 选 Direct Connect，其他默认设置，点击下边的priorities 把GND-Via规则优先级置最高，（1 为最高，2 次之...）如下图：



回到 PCB 设计环境下进行覆铜，覆铜网络选 GND，覆好铜以后对于网络为 GND 的 Via（过孔）将为全覆铜的连接，而非默认的 relief connect 方式（热焊盘方式），由于规则是对过孔的全连接覆铜，所以对于焊盘的覆铜是热焊盘方式连接方式，见下图（左）：



如果想过孔和焊盘多用热焊盘方式，那在 Full Query 修改为 IsVia or Is pad，更新下刚才的覆铜，地焊盘也全连接了，如上图（右）同样也可以 Full Query 为 Is pad，InNet('GND')，InNet('GND') And OnLayer('TopLayer')，InComponent('U1')，InComponent('U1') OR InComponent('U2') OR InComponent('U3')，innetclass('Power')等等...

1. InNet('GND') 对于网络名为 GND 的网络进行覆铜连接，覆铜连接规则采用 InNet('GND') 的覆铜连接规则，注：InNet('X')，X 为 PCB 中的网络名，Connect Style 可全连接或热焊盘或无连接方式；热焊盘方式还可设置 2，4 连接，45 度，90 度和连接线宽，下面的也类同；

2. InNet('GND') And OnLayer('TopLayer')，对于位于 TopLayer 层的 GND 网络进行的覆铜采用该覆铜连接规则，OnLayer('X')，X 为层名，层名称修改可通过 Design>Layer Stack Manager，双击层名称修改。；

3. InComponent('U1')，对于元件 U1 的覆铜采用该覆铜连接规则，U1 上有个 x 网络，同时覆铜的网络也为 x，这样改规则才有效果，例如 U1 上有个管脚连接到 GND 网络，同时覆铜网络选 GND，此时改规则才有效果；否则等于没有这个规则，与不建立规则效果一样；

4. InComponent('U1') OR InComponent('U2') OR InComponent('U3') 对于元件 U1，U2，U3 采用该覆铜连接规则，即 U1，U2，U3

多采用改覆铜连接规则，关系是 OR ，而非 AND；

`innetclass('Power')`，Power 类网络的覆铜连接方式规则，Design>Classes 创建一个规则类，类的方式有多种，网络类，元件类，层类等。

网络类指向 PCB 中的网络名，层类指向 PCB 中的元件（焊位），层类指向 PCB 中的层；；；例：`innetclass('Power')`，在 net classes（网络类）下新建一个规则（new rule），同样是右键增加，并改名为 Power，选中这个网络类规，添加左边的的网络到右边去，比如添加 GND，VCCINT，

VCC3.3,VCC1.2,VCCA,GNDA 等...这样在多个多个网络的不同覆铜就不用分别建立 GND，VCCINT，VCC3.3，VCC1.2，VCCA，GNDA 的覆铜连接规则，自需要建立一个网络类覆铜连接规则即可，在覆铜的时候覆铜网络连接到相应的网络即可；

注意：所有上面的规则多要设置相应的优先级和新建规则，**新建规则的优先级设为高，默认规则的优先级最低**，其他优先级看实际排列。所有选项选 Where The Frist Object Matches 选 Advanced (Query)，Full Query 输入相应的数据命令，对于相对简单的类似只是网络和层的覆铜连接 `InNet('GND') And OnLayer('TopLayer')`---顶层地网络的覆铜连接方式，可选择 The Frist Object Matches---Net and Layer，在里面的下拉框中选择相应的 Net 和 Layer 后。Full Query 框软件会执行填充数据，完成后 Apply OK 回到 PCB 中（Full Query 框中语法错误，软件会提示错误，而填入一个不存在的层或网络名则不会），再在 PCB 进行覆铜选择相应的覆铜网络即可，覆铜间距默认是 10mil，如需特殊间距则需修改间距规则；

## 高级间距规则

比如覆铜间距 16mil，其他安全间距 8mil，过孔到过孔间距 100mil，焊盘到焊盘间距 100mil，焊盘到过孔间距 100mil，顶层地覆铜 0.8mm，顶层 VCC3.3 与 VCC1.8 覆铜间距 0.5mm 等

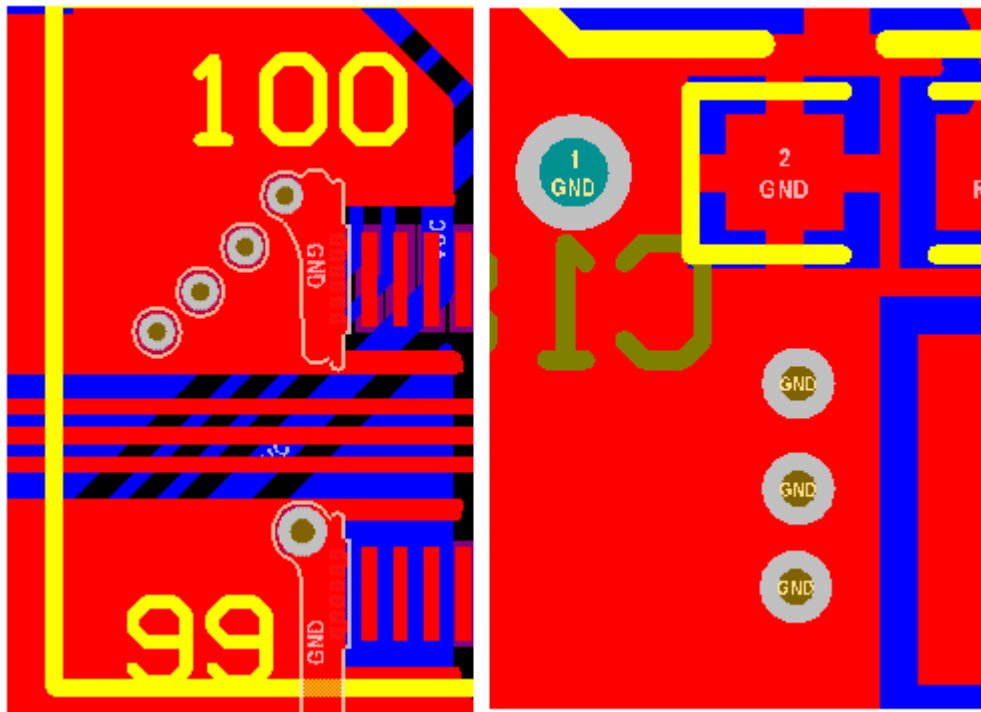
Altium Designer 的间距规则默认为一个 10mil 间距，没有区分焊盘到焊盘，过孔到过孔，走线到覆铜等的间距，想要高级规则，必须自己新建。

在 PCB 设计环境下 **Design>Rules>Electrical>Clearance**，同样右键新建一个间距规则并重命名为 Poly，Where The First Object Matches 选 Advanced (Query)，Full Query 输入 inpolygon，Constraints 把默认的 10mil 修改为 20mil，优先级 Poly 比默认的 Clearance 的 10mil 高，这 2 个间距规则共同构成覆铜间距为 20mil，其他间距例如走线到走线，走线到焊盘过孔间距为 10mil 的规则，如下图：

Priority	Enabled	Name	Scope	Attributes
1	<input checked="" type="checkbox"/>	Poly	inpolygon - All	Clearance = 20mil
2	<input checked="" type="checkbox"/>	Clearance	All - All	Clearance = 10mil

下 2 图是过孔覆铜全连接 viaconnect，默认安全间距 clearance 8mil，覆铜间距 16mil 规则的覆铜，inpolygon 是所有的覆铜，如果想要其他覆铜间距，则需要在新建覆铜规则，比如 VCC3.3 覆铜 0.5mm，VCC1.8 覆铜间距 0.6mm，其他覆铜 0.4mm；优先级 16mil 的最低；覆一片铜到 VCC3.3 网络同时起名该覆铜为 VCC3.3-ALL；覆一片铜到 VCC1.8 网络同时起名该覆铜为 VCC1.8-ALL；同样要兴建间距规则，见下面第 3-6 张图：

Priority	Enabled	Name	Scope	Attributes
1	<input checked="" type="checkbox"/>	viaconnect	isvia - All	Clearance = 16mil
2	<input checked="" type="checkbox"/>	Clearance	All - All	Clearance = 8mil



Design Rules

- Electrical
  - Clearance
    - VCC1.8-ALL**
    - VCC3.3-ALL
    - OtherPoly
    - Clearance
  - Short-Circuit
    - ShortCircuit
  - Un-Routed Net
    - UnRoutedNet
    - Un-Connected Pin

Different Nets Only

Minimum Clearance 0.6mm

Name: VCC1.8-ALL    Comment:    Unique ID: TVSKOS

Where The First Object Matches

- All
- Net
- Net Class
- Layer
- Net and Layer
- Advanced (Query)
  - Query Helper ...
  - Query Builder ...

Full Query: InNamedPolygon ('VCC1.8-ALL')

Where The Second Object Matches

- All
- Net
- Net Class
- Layer
- Net and Layer
- Advanced (Query)
  - Query Helper ...
  - Query Builder ...

Full Query: All

Constraints

Design Rules

- Electrical
  - Clearance
    - VCC1.8-ALL
    - VCC3.3-ALL**
    - OtherPoly
    - Clearance
  - Short-Circuit
    - ShortCircuit
  - Un-Routed Net
    - UnRoutedNet
    - Un-Connected Pin
- Routing
- SMT
- Mask
- Plane

Different Nets Only

Minimum Clearance 0.5mm

Name: VCC3.3-ALL    Comment:    Unique ID: GDOTGJI

Where The First Object Matches

- All
- Net
- Net Class
- Layer
- Net and Layer
- Advanced (Query)
  - Query Helper ...
  - Query Builder ...

Full Query: InNamedPolygon ('VCC3.3-ALL')

Where The Second Object Matches

- All
- Net
- Net Class
- Layer
- Net and Layer
- Advanced (Query)
  - Query Helper ...
  - Query Builder ...

Full Query: All

Constraints

**Design Rules**

- Electrical
  - Clearance
    - VCC1.8-ALL
    - VCC3.3-ALL
    - OtherPoly
    - Clearance
  - Short-Circuit
    - ShortCircuit
  - Un-Routed Net
    - UnRoutedNet
    - Un-Connected Pin
- Routing
- SMT
- Mask

Different Nets Only

Minimum Clearance 0.4mm

**Name:** OtherPoly **Comment:**

**Where The First Object Matches**

- All
- Net
- Net Class
- Layer
- Net and Layer
- Advanced (Query)

**Full Query:** inpolygon

**Where The Second Object Matches**

- All
- Net
- Net Class
- Layer
- Net and Layer
- Advanced (Query)

**Full Query:** All

**Constraints:**

**Design Rules**

- Electrical
  - Clearance
    - VCC1.8-ALL
    - VCC3.3-ALL
    - OtherPoly
    - Clearance
  - Short-Circuit
    - ShortCircuit
  - Un-Routed Net
    - UnRoutedNet
    - Un-Connected Pin
- Routing
- SMT
- Mask
- Plane

Different Nets Only

Minimum Clearance 0.254mm

**Name:** Clearance **Comment:**

**Where The First Object Matches**

- All
- Net
- Net Class
- Layer
- Net and Layer
- Advanced (Query)

**Full Query:** All

**Where The Second Object Matches**

- All
- Net
- Net Class
- Layer
- Net and Layer
- Advanced (Query)

**Full Query:** All

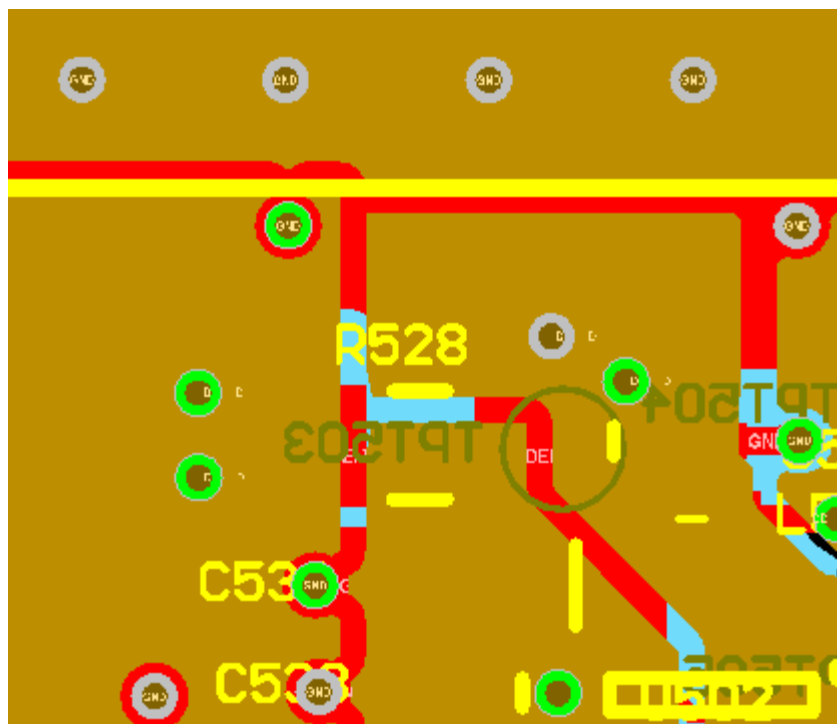
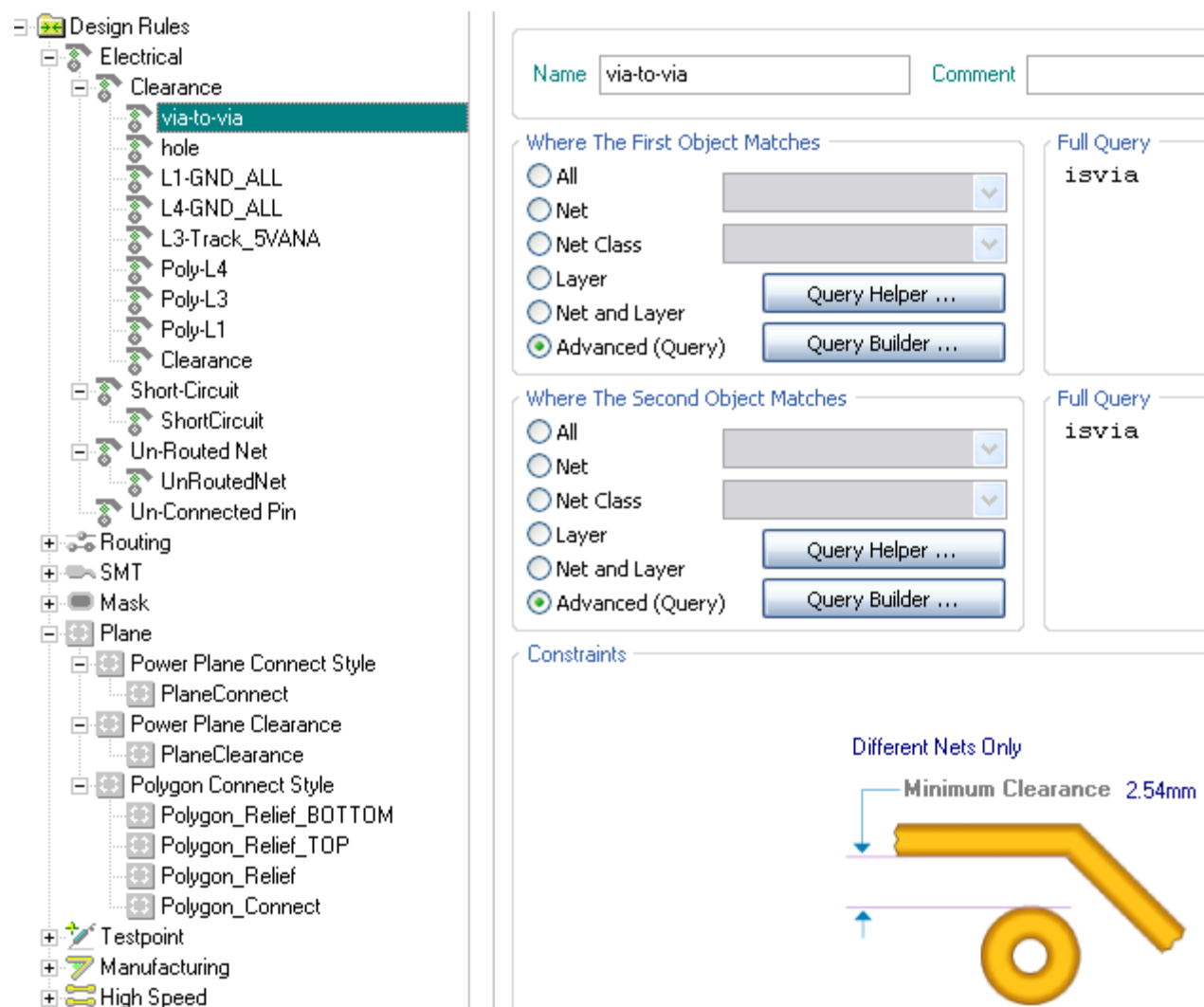
**Constraints:**

**Edit Rule Priorities**

Rule Type: Clearance

Priority	Enabled	Name	Scope	Attributes
1	<input checked="" type="checkbox"/>	VCC1.8-ALL	InNamedPolygon	(VC Clearance = 0.6mm
2	<input checked="" type="checkbox"/>	VCC3.3-ALL	InNamedPolygon	(VC Clearance = 0.5mm
3	<input checked="" type="checkbox"/>	OtherPoly	inpolygon	All - All Clearance = 0.4mm
4	<input checked="" type="checkbox"/>	Clearance	All	All - All Clearance = 0.254mm

下图是过孔到过孔的间距规则，Where The First Object Matches ,Where The Second Object Matches 的 FullQuery ,只有这2个参数一个是 isvia, 另一个是 ispad 即可； 如果一个 ispad 另一个 isvia, 那就是过孔到焊盘的间距； 如果一个 ispad 另一个 ispad, 那就是焊盘到焊盘的间距； 随后填入具体的间距即可， Where The Second Object Matches 默认是 ALL ， 修改他就是第一个和第二个间距规则， IsVia 和 ALL 就是 Via 到其他的间距规则， IsVia 和 IsVia 就是过孔到过孔的间距规则；



过孔到过孔间距没有到 2.54mm 的在线 DRC 检查出来绿色显示；

注：设置小间距管脚间距：一些FPGA芯片等很多焊盘间距多达到了0.2mm，默认的10mil（0.254mm）间距显然是冲突的，上述问题可以通过 `HasFootprint('PQ208') or IsPad and InComponent('U1') ; (IsPad and InComponent('JP4')) or (IsPad and InComponent('JP3'))` HasFootprint('PQ208')，封装为 PQ208 的元件；

`sPad and InComponent('U1')`，元件 U1 的管脚间的间距；

上面 2 个规则只是管脚间距，从上面拉出来的线的间距是其他的规则值，当然不能太大；比如上面的 PQ208 焊盘 0.3mm。焊盘间距 0.2mm，布线 0.2mm，那拉出来的线间距就是 0.4mm。如果把布线间距设为 0.5mm,1mm ，要么绿色，要么拉不出来；

`(IsPad and InComponent('JP4')) or (IsPad and InComponent('JP3'))`，元件 JP3,JP4 的间距规则；

见下面 3 张图：



Design Rules

- Electrical
  - Clearance
    - Clearance\_Polygon
    - Clearance\_FPGA
    - Clearance
  - Short-Circuit
  - Un-Routed Net
  - UnRoutedNet
  - Un-Connected Pin
- Routing
- SMT
- Mask
- Plane
  - Power Plane Connect Style
  - PlaneConnect
  - Power Plane Clearance
  - PlaneClearance
  - Polygon Connect Style
  - PolygonConnect
- Testpoint
- Manufacturing
- High Speed
- Placement
- Signal Integrity

Name: Clearance\_FPGA    Comment:    Unique ID: GYTV

Where The First Object Matches

- All
- Net
- Net Class
- Layer
- Net and Layer
- Advanced (Query)

Full Query: IsPad **and** InComponent ( ' U1 ' )

Where The Second Object Matches

- All
- Net
- Net Class
- Layer
- Net and Layer
- Advanced (Query)

Full Query: All

Constraints

Different Nets Only

Minimum Clearance 0.2mm

Design Rules

- Electrical
  - Clearance
    - Clearance\_PQ208
    - Clearance\_Polygon
    - Clearance\_FPGA
    - Clearance
  - Short-Circuit
  - Un-Routed Net
  - UnRoutedNet
  - Un-Connected Pin
- Routing
- SMT
- Mask
- Plane
  - Power Plane Connect Style
  - PlaneConnect
  - Power Plane Clearance
  - PlaneClearance
  - Polygon Connect Style
  - PolygonConnect
- Testpoint
- Manufacturing
- High Speed
- Placement
- Signal Integrity

Name: Clearance\_PQ208    Comment:    Unique:

Where The First Object Matches

- All
- Net
- Net Class
- Layer
- Net and Layer
- Advanced (Query)

Full Query: HasFootprint ( ' PQ208 ' )

Where The Second Object Matches

- All
- Net
- Net Class
- Layer
- Net and Layer
- Advanced (Query)

Full Query: All

Constraints

Different Nets Only

Minimum Clearance 0.2mm

Design Rules

- Electrical
  - Clearance
    - Clearance
    - 8mil

Different Nets Only

Minimum Clearance 5mil

Name: Clearance    Comment:    Unique ID: HPXAKJTM

Where The First Object Matches

- All
- Net
- Net Class
- Layer
- Net and Layer
- Advanced (Query)

Full Query: ( IsPad **and** InComponent ( ' JP4 ' ) ) **or** ( IsPad **and** InComponent ( ' JP3 ' ) ) **or** ( IsPad **and** InComponent ( ' u2 ' ) ) **or** ( IsPad **and** InComponent ( ' jp5 ' ) ) **or** ( IsPad **and** InComponent ( ' jp2 ' ) )

Where The Second Object Matches

- All

Full Query: All

下图是一个定位孔间距为 3mm 的间距规则：常用一个内孔=外孔的焊盘做定位孔。该孔不连接到任何网络（不进行电气连接），只拧螺丝用。我们在 PCB 上 4 个脚上放 4 个定位孔,不连接到任何网络，焊盘名称起为 HOLE, 内孔=外孔大小；free-hole 含义 free 不连接到任何网络，Hole 焊盘名称；可以是 free-0 ， free-1， free-2 等等；

The screenshot shows the 'Design Rules' tree on the left with 'pholeClearance' selected under 'Electrical' > 'Clearance'. The main panel displays the rule configuration for 'pholeClearance'. The 'Where The First Object Matches' section is set to 'Advanced (Query)' with the full query 'HasPad('free-HOLE')'. The 'Where The Second Object Matches' section is set to 'All' with the full query 'All'. The 'Constraints' section is set to 'Different Nets Only' with a 'Minimum Clearance' of 100mil. A preview image shows a PCB layout with a large circular pad labeled '0' and two smaller pads labeled 'R2'.

下图为一个在 toplayer 层覆铜名为 5VANA 的间距规则，当然 toplayer 可以换成其他层，5VANA 可以换成其他覆铜的名称；

The screenshot shows the 'Design Rules' tree on the left with 'top\_5VANA' selected under 'Electrical' > 'Clearance'. The main panel displays the rule configuration for 'top\_5VANA'. The 'Where The First Object Matches' section is set to 'Advanced (Query)' with the full query 'OnLayer('toplayer') AND InNamedPolygon('5VANA')'. The 'Where The Second Object Matches' section is set to 'All' with the full query 'All'. The 'Constraints' section is set to 'Different Nets Only' with a 'Minimum Clearance' of 0.4mm. A preview image shows a PCB layout with a large circular pad labeled '0' and two smaller pads labeled 'R2'.



下图为 DM 到 DP 网络间距为 20mil 的间距规则:

The screenshot shows the Design Rules Editor interface. On the left is a tree view of Design Rules, with 'Electrical' > 'Clearance' > 'DP-DM' selected. The main panel is configured as follows:

- Name:** DP-DM
- Where The First Object Matches:**
  - Net: DM
  - Full Query: InNet ('DM')
- Where The Second Object Matches:**
  - Net: DP
  - Full Query: InNet ('Dp')
- Constraints:**
  - Different Nets Only
  - Minimum Clearance 20mil

The constraints section includes a 3D visualization of a yellow L-shaped trace and a circular pad, with a dimension line indicating a 20mil clearance between them.

下图为 MSCLK1 网络到其他间距为 16mil 的间距规则

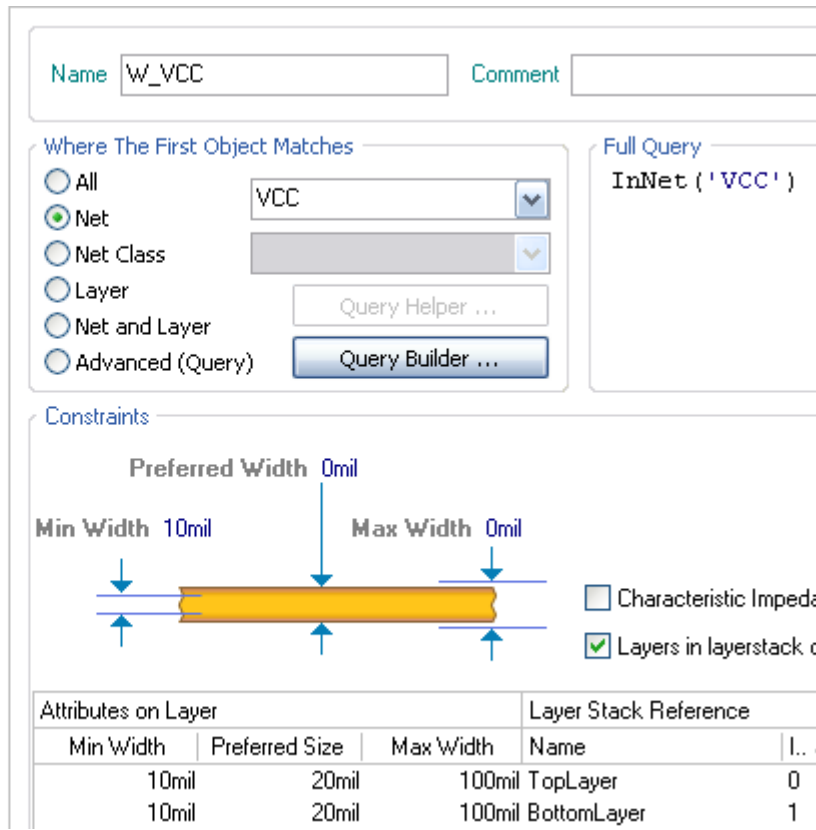
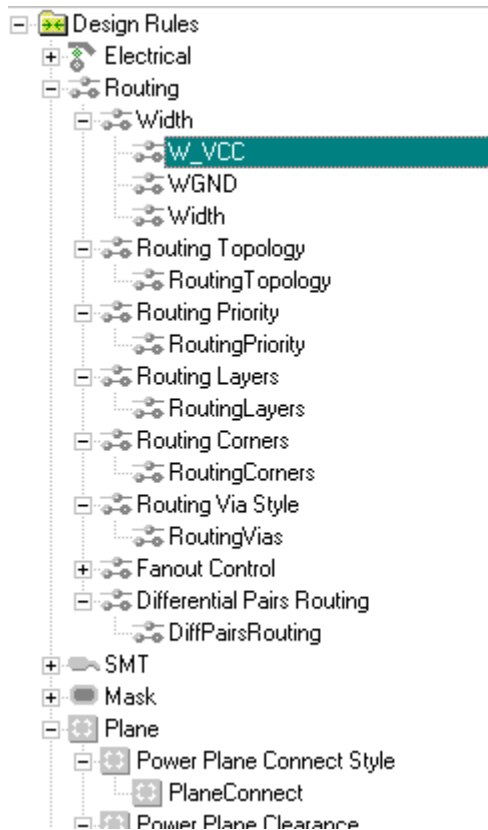
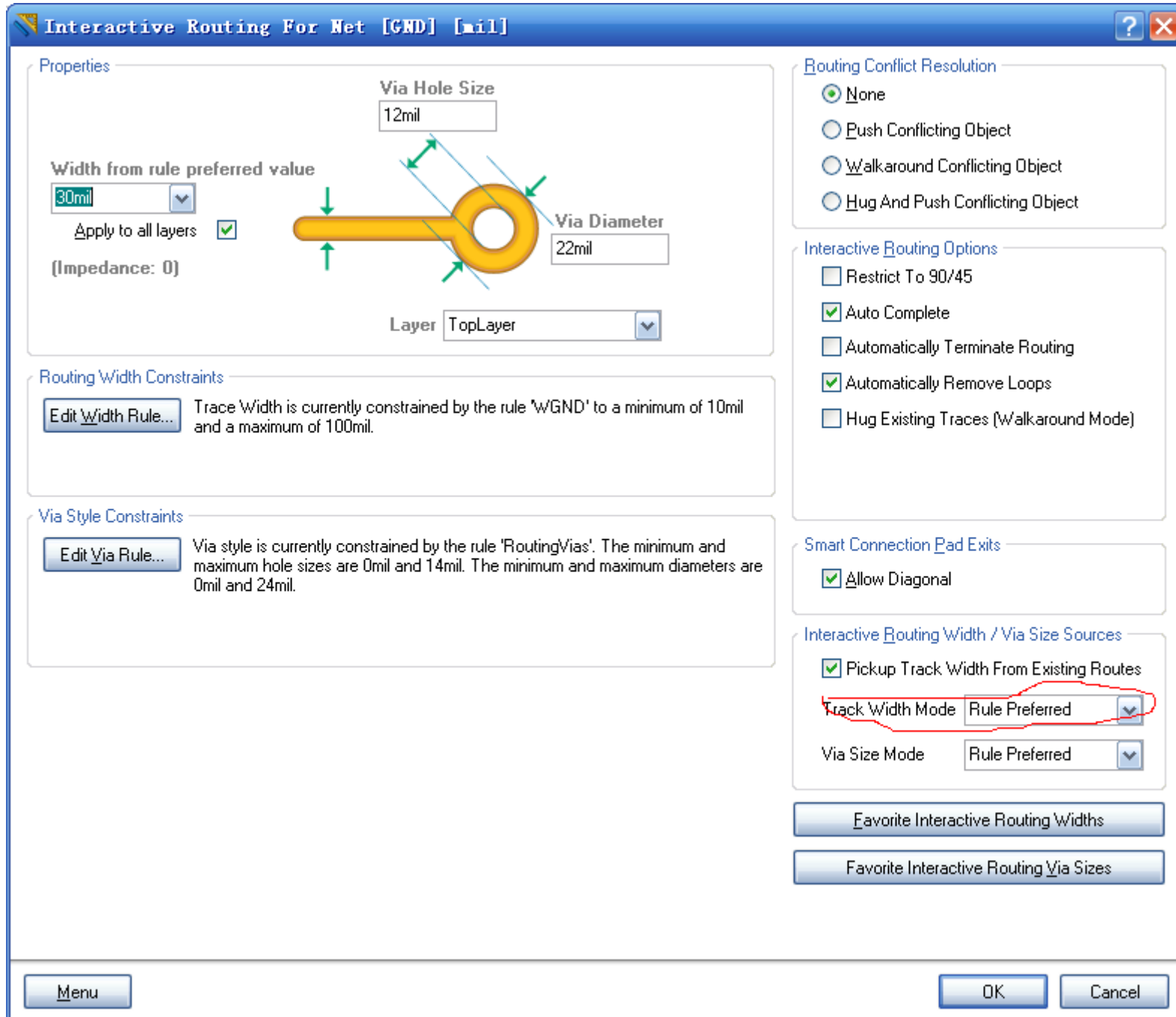
The screenshot shows the Design Rules Editor interface. On the left is a tree view of Design Rules, with 'Electrical' > 'Clearance' > 'DP-DM' selected. The main panel is configured as follows:

- Name:** DP-DM
- Where The First Object Matches:**
  - Net: MSCLK1
  - Full Query: InNet ('MSCLK1')
- Where The Second Object Matches:**
  - All: All
  - Full Query: All
- Constraints:**
  - Different Nets Only
  - Minimum Clearance 16mil

The constraints section includes a 3D visualization of a yellow L-shaped trace and a circular pad, with a dimension line indicating a 16mil clearance between them.

# 高级线宽规则

设置 GND 网络 30mil, VCC 网络线宽 20mil, 布线时按 TAB ,Track Width Mode 选 Rule Preferred;



Name: WGND

Where The First Object Matches: Net (GND)

Full Query: InNet ( ' GND ' )

Constraints:

Preferred Width 0mil

Min Width 10mil

Max Width 0mil

Attributes on Layer	Layer Stack Reference			
Min Width	Preferred Size	Max Width	Name	I..
10mil	30mil	100mil	TopLayer	0
10mil	30mil	100mil	BottomLayer	1

Name: Width

Where The First Object Matches: All

Full Query: All

Constraints:

Preferred Width 8mil

Min Width 8mil

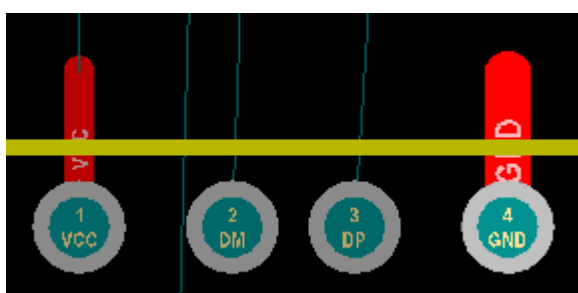
Max Width 30mil

Attributes on Layer	Layer Stack Reference			
Min Width	Preferred Size	Max Width	Name	I..
8mil	8mil	30mil	TopLayer	
8mil	8mil	30mil	BottomLayer	

Rule Type: Width

Priority	Enabled	Name	Scope	Attributes
1	<input checked="" type="checkbox"/>	W_VCC	InNet('VCC')	Pref Width = 10mil Min Width = 10mil Max Width = 100mil
2	<input checked="" type="checkbox"/>	WGND	InNet('GND')	Pref Width = 10mil Min Width = 10mil Max Width = 100mil
3	<input checked="" type="checkbox"/>	Width	All	Pref Width = 8mil Min Width = 8mil Max Width = 30mil

Buttons: Increase Priority, Decrease Priority, Close



另外还可以添加类来设置线宽规则，适合大批量线宽处理：