# Op amp stability and input capacitance

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## Introduction

Op amp instability is compensated out with the addition of an external RC network to the circuit. There are thousands of different op amps, but all of them fall into two categories: uncompensated and internally compensated. Uncompensated op amps always require external compensation components to achieve stability; while internally compensated op amps are stable, under limited conditions, with no additional external components.

Internally compensated op amps can be made unstable in several ways: by driving capacitive loads, by adding capacitance to the inverting input lead, and by adding in phase feedback with external components. Adding in phase feedback is a popular method of making an oscillator that is beyond the scope of this article. Input capacitance is hard to avoid because the op amp leads have stray capacitance and the printed circuit board contributes some stray capacitance, so many internally compensated op amp circuits require external compensation to restore stability. Output capacitance comes in the form of some kind of load—a cable, converter-input capacitance, or filter capacitance—and reduces stability in buffer configurations.

## Stability theory review

The theory for the op amp circuit shown in Figure 1 is taken from Reference 1, Chapter 6. The loop gain, $A\beta$, is critical because it solely determines stability; input circuits and sources have no effect on stability because inputs are grounded for the stability analysis. Equation 1 is the loop-gain equation for the resistive case where $Z = R$.

$$A\beta = \frac{aR_G}{R_F + R_G} \qquad (1)$$

Beware of Equation 1; its simplicity fools people because they make the assumption that $A = a$, which is not true for all cases. Stability can be determined easily from a plot of the loop gain versus frequency. The critical point is when the loop gain equals 0 dB (gain equals 1) because a circuit must have a gain $\geq 1$ to become unstable. The phase margin, which is the difference between the measured phase angle and 180º, is calculated at the 0-dB point. A typical open-loop-gain curve for the TLV278x family of op amps is used as a teaching example and is shown in Figure 2.

The op amp's open-loop gain and phase ($a$ in Equation 1) are represented in Figure 2 by the left and right vertical axes, respectively. Never assume that the op amp open-loop-gain curve is identical to the loop gain because external components have to be accounted for to get the loop-gain

**Figure 1. Equation 1 can be written from the op amp schematic by opening the feedback loop and calculating gain**
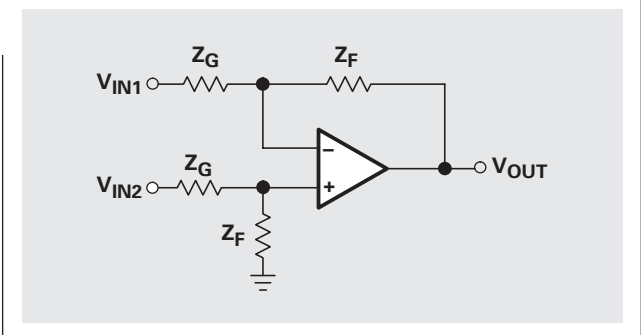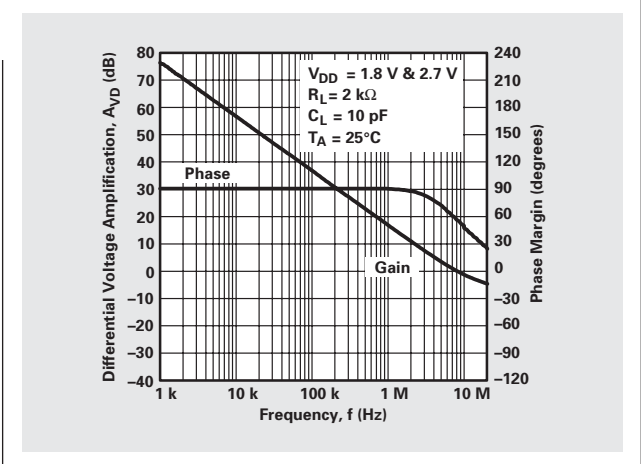


**Figure 2. Open-loop-gain/phase curves are critical stability-analysis tools**



curve. When $R_F = 0$ and $R_G = \infty$, the op amp reduces to a noninverting buffer amp (unity gain) and the loop gain becomes equal to the op amp open-loop gain. We can obtain the buffer phase margin directly from Figure 2 by tracing the gain line down from its vertical intercept (at approximately 78 dB) to where it crosses the 0-dB line at approximately 8 MHz. Then we can trace the 8-MHz line up until it intersects the phase curve, and read the phase margin as approximately 56º. This plot was made with phase margin, but many plots are made instead with phase shift. For plots made with phase shift, the phase shift must be subtracted from 180º to obtain the phase margin.

Now that we have the phase margin, what can we do with it other than to say that the circuit does not oscillate?

Figure 3 is a plot of phase margin and percent maximum overshoot versus a dummy variable, the damping ratio. Enter this plot at a phase margin of 56° and go up to the phase curve intersection. At this point, go horizontally (constant damping ratio) to the intersection of the over-shoot curve, and then drop down to read an overshoot of approximately 11%. This plot enables the designer to predict the transient step response from the phase margin, and transient response is a measure of relative stability.

### Figure 3. Phase margin/percent overshoot versus damping ratio



### Figure 4. Input capacitance includes IC internal, lead, and PCB capacitance
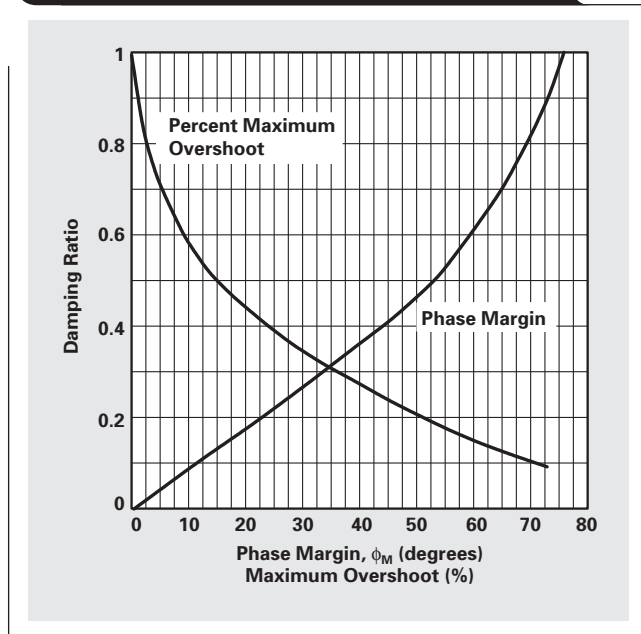


The external resistors come into play when the op amp is conFigured as an inverting, noninverting, or differential amplifier. When $R_F = R_G$, Equation 1 reduces to $A\beta = a/2$; and the vertical intercept for the amplifier reduces from that of the buffer by 6 dB. Although the vertical intercept has changed, the pole location remains constant because gain is not tied to phase. The 0-dB crossover frequency changes to approximately 3 MHz because of the gain drop; the phase margin increases to approximately 87°; and the percent overshoot is negligible. Notice that the buffer is less stable than any of the amplifier circuits and that, at the same phase margin, the inverting gain is –1 while the noninverting gain is 2.
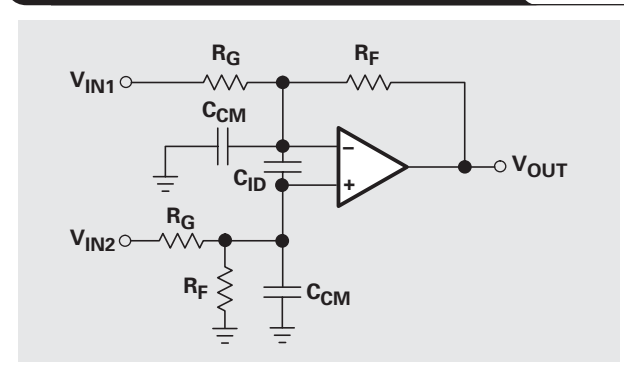
## Added input capacitance and its effect

When input capacitors are added to the circuit (see Figure 4), they cause a pole to occur in the loop gain, as shown in Equation 2.

$$A\beta = \frac{aZ_G}{Z_G + R_F} = \frac{aR_G}{R_G + R_F} \times \frac{1}{R_G \| R_F C_{IN} + 1} \qquad (2)$$

The input capacitor, $C_{IN}$, is the summation of all the inverting input capacitances, and it adds a pole to the loop

gain. Adding a pole to the loop gain does not always change the stability because the pole location and its added phase shift may not affect the phase margin. Consider the case where the pole is located at a very high frequency—say, 100 MHz—for the TLV278x. Notice from Figure 2 that the op amp open-loop gain is so low above 10 MHz that the overall gain can never equal 1, so the added pole is of no value. The case where the pole is located at a very low frequency—say, 0.001 Hz—is harder to calculate because the low-frequency response is not shown in Figure 2. However, we can be sure that the phase shift is close to zero at this frequency. A pole with a frequency intercept that low would cause the gain to be down 120 dB at 1 kHz, and again the loop gain would be less than 1 before the phase margin went to zero. An op amp open-loop gain/phase plot that shows low-frequency response is shown in Figure 5. Notice that the phase shift (not phase margin in this plot) approaches zero at low frequencies. In addition, notice that the phase shift approaches 180° at very high frequencies and that the gain is given in ratios rather than in decibels.

### Figure 5. Gain/phase plots of medium-frequency op amps show frequency extremes



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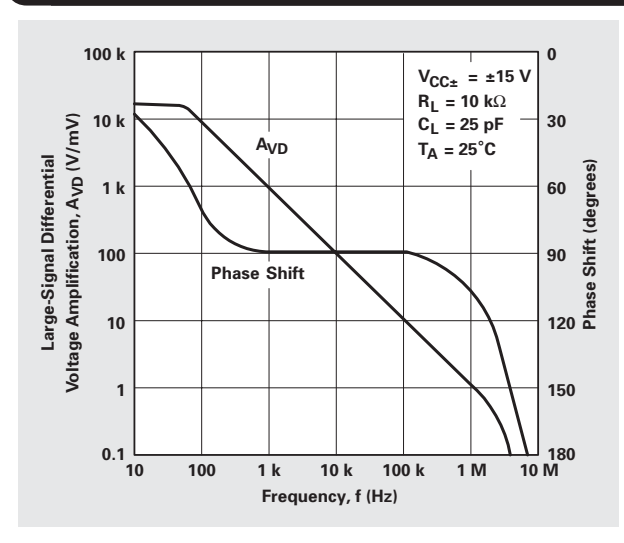
The DC gain in Equation 2 remains the same as it was without an input capacitor, but the pole is added at $f = 1/(2\pi R_F \| R_G C_{IN})$. If this pole occurs at approximately 3 MHz, it reduces the gain by 3 dB and adds a 45° phase shift at that frequency. Using $C_{IN} = 20$ pF and $R_G \| R_F = 2.7$ k$\Omega$ yields a 3-dB frequency of 2.94 MHz, so it is reasonable to assume a pole frequency of 3 MHz. The gain in Figure 4 must be moved down 9 dB to account for the resistors and the pole. The new 0-dB crossover frequency is 2 MHz, and the phase margin at 2 MHz (as shown in Figure 4) is 89°. The pole phase shift of 45° must be subtracted from the curve phase margin to obtain the final circuit phase margin; thus $\phi = 89° - 45° = 44°$. The percent overshoot corresponding to the 44° phase margin is 24.45%. Adding $C_{IN}$ reduces the phase margin from 87° in the purely resistive case to 44° with input capacitance. If the op amp initially had less than a 44° phase margin, the circuit would be unstable rather than just bouncy.

If the resistor values were larger than 5.4 k$\Omega$, the pole would move down in frequency. The exact pole location that does the most damage to stability is hard to calculate because the phase is a nonlinear tangent function. In this case, it is best to move the resistors down in value to about 1 k$\Omega$, thus moving the pole to 8 MHz and reducing the added phase shift to about 14°. A second problem crops up in the noninverting configuration because $C_{ID}$ couples a portion of the input signal to the inverting input. This action reduces the common-mode rejection capability and introduces high-frequency distortion.

The buffer circuit with an input capacitance is shown in Figure 6. Notice that the input capacitance includes the output capacitance and load capacitance in the absence of a feedback resistor, and that the output impedance, $Z_{OUT}$, comes into play.

**Figure 6. Input, output, and load capacitors are in parallel in the buffer circuit**
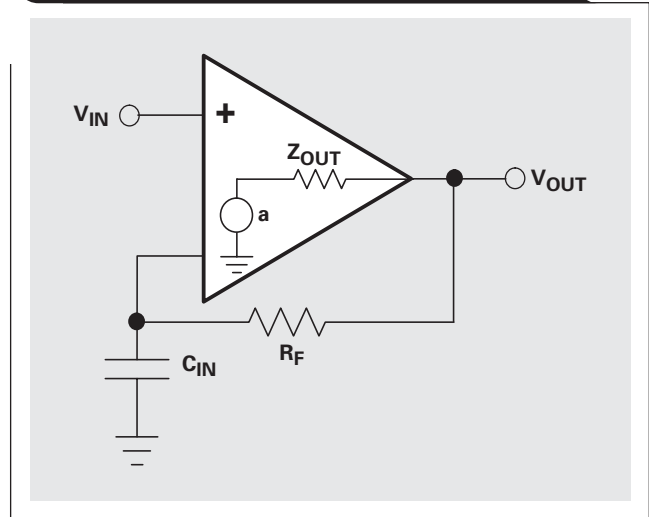


The buffer loop gain is given as

$$A\beta = \frac{a}{\left(R_F + Z_{OUT}\right)C_{IN} + 1}. \tag{3}$$

First, consider the case when $R_F = 0$; $Z_{OUT}$ is obtained from Figure 7 as 70 $\Omega$ at 8 MHz. Assuming that the input, output, and load capacitance is 100 pF, the pole frequency is located at 22.7 MHz; and this pole adds a 19.4° phase shift at the 0-dB crossover frequency. This added phase shift subtracts directly from the previously calculated phase margin of 56° because the pole attenuation doesn't

**Figure 7. Op amp output impedance increases with increasing frequency**
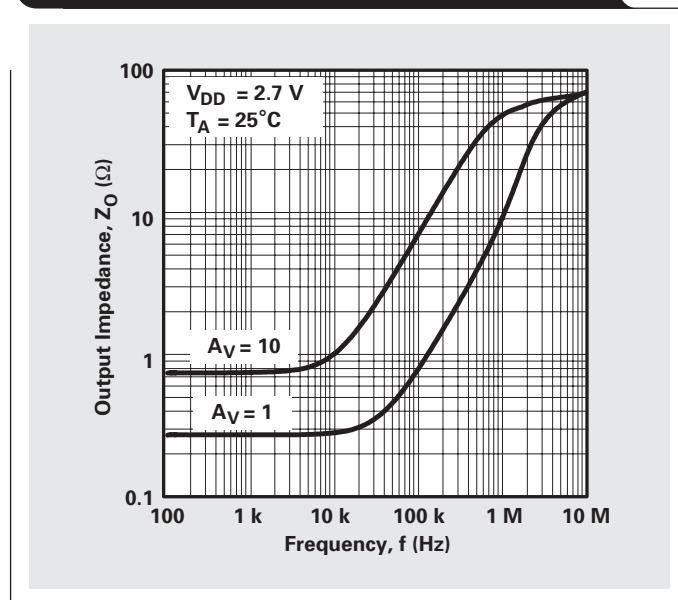
occur until after the 0-dB crossover frequency. This circuit has a phase margin of $56^\circ - 19.4^\circ = 36.6^\circ$, leading to an overshoot of 33%.

When $R_F = 1$ k$\Omega$, the $R_F C_{IN}$ pole is located at 8 MHz; so it becomes dominant. Under these conditions, the gain curve moves down 3 dB and the phase shift is increased $45^\circ$. Moving the gain curve down 3 dB yields an $80^\circ$ phase margin at f = 4 MHz. Subtracting $45^\circ$ plus $19.4^\circ$ from $80^\circ$ yields a phase margin of $15.6^\circ$, and the overshoot increases to approximately 50%. It is obvious that increasing the value of $R_F$ makes it dominant over $Z_{OUT}$ and will quickly make the circuit oscillate.

## $C_F$ increases stability

Input and output capacitors always decrease stability. Input capacitors are a pole in the open-loop transfer function, but they are a zero in the closed-loop transfer function. The closed-loop zero increases the circuit (not the op amp) bandwidth, so sometimes input capacitors are added to the circuit to improve high-frequency response.

A capacitor placed in parallel with the feedback resistor, $C_F$, introduces a zero into the loop gain:

$$A\beta = \frac{aR_G}{R_F + R_G} \times \frac{R_F C_F + 1}{R_F \| R_G (C_F + C_G) + 1} \qquad (4)$$

When the closed-loop gain is greater than 1 and $C_F$ is greater than $C_G$, the zero precedes the pole. In this case, which is not unusual, the zero contributes a positive phase shift to the loop-gain plot, causing an increase in stability. The more the zero leads the pole, the more stable the

circuit becomes; but the pole always ends up canceling the zero. The idea is to place the zero so that we achieve the required overshoot and then to accept the pole location. The open-loop zero translates to a closed-loop pole; thus $C_F$ always decreases high-frequency performance. Optimal performance is gained when the acceptable overshoot is obtained at an acceptable frequency response.

## Conclusion

The addition of input, output, or load capacitance to an op amp circuit decreases stability, which leads to overshoot in the time domain. The stability decrease is worse for a buffer than for other amplifier configurations. Reducing the resistance value that makes up the RC circuit reduces the effect of the capacitance; this effect leads to the rule of thumb that high frequencies and low resistance go together. Input capacitance is easily compensated by adding a feedback capacitor into the circuit. The value of the feedback capacitor should be just large enough to achieve the desired overshoot response, because larger values cause a loss of high-frequency performance.

## Reference

1. Ron Mancini, *Op Amps For Everyone* (Newnes Publishers, 2003). An earlier 2002 edition is available at www-s.ti.com/sc/techlit/slod006

## Related Web sites

**analog.ti.com**
**www.ti.com/sc/device/TLV278x**

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