CYUSB3KIT-001

EZ-USB FX3 Development Kit User Guide

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1. INTRODUCTION

The FX3 DVK is a combination of hardware, software and documentation that can be used by Cypress customers to evaluate the FX3 device. Customers can use this DVK to start hardware/software integration and then move to their final systems after the integration phase is complete.
This user guide only targets the hardware. The SDK documentation comes with the SDK installation. It will be placed in the folder: Cypress\FX3 SDK\doc; where 'FX3 SDK' is custom installation folder name.

1.1 Development Board

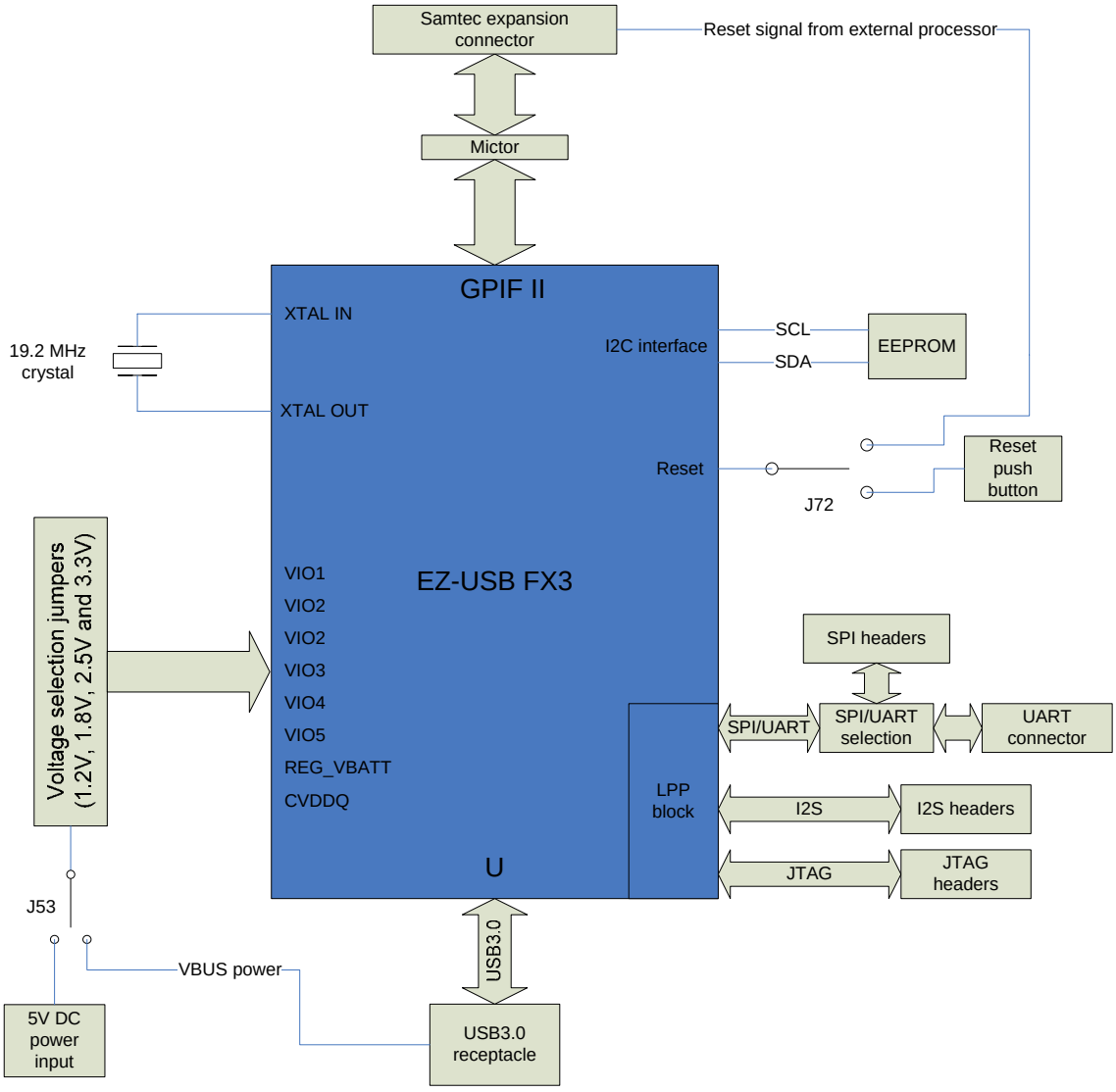

Figure 1-1: FX3 DVK board block diagram

1.1.1 Power Supply

The user has the option to power the board either from the 5V DC external power or from the USB host (VBUS line). This selection can be made on the board through the SW9 toggle switch. J53 should be populated with jumpers if VBUS is being used to power the board. The voltage for FX3 I/O power domains can be selected using on-board selection jumpers. These domains include VIO1, VIO2, VIO3, VIO4, VIO5, REG_VBATT and CVDDQ. All other power domains are tied to 1.2V.
The following table shows the power domain selection option through jumpers:

Table 1-1: Power Supply domains

Power Domain	Description	Headers	Voltage Levels
VIO1	IO1 domain	J136	1.8V, 2.5V, 3.3V
VIO2	IO2 domain	J144	1.8V, 2.5V, 3.3V
VIO3	IO3 domain	J145	1.8V, 2.5V, 3.3V
VIO4	IO4 domain	J146	1.8V, 2.5V, 3.3V
VIO5	IO5 domain	J134	1.2V, 1.8V, 2.5V, 3.3V
REG_VBATT	VBATT power domain	J143	2.5V, 3.3V, 5V
CVDDQ	Crystal power domain	J135	1.8V, 3.3V

1.1.2 USB Receptacle

A standard Micro B receptacle is used on the FX3 DVK board. VBUS power also comes from the host through this connector. The USB3.0 and USB2.0 lines go through an ESD protection device for additional ESD protection.

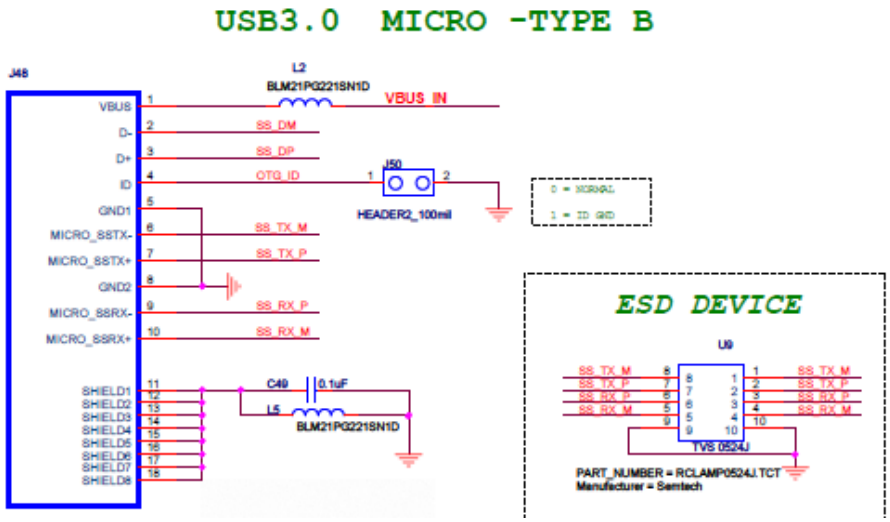

Figure 1-2: USB3.0 micro B connector and ESD device

1.1.3 Crystal Oscillator

The clock for the FX3 device is provided through an on-board 19.2 MHz crystal that is connected to the XTALIN and XTALOUT pins of FX3. The FSLC[2:0] lines of FX3 are tied to ground, which means that the device is configured to only use the 19.2 MHz crystal for clocking.

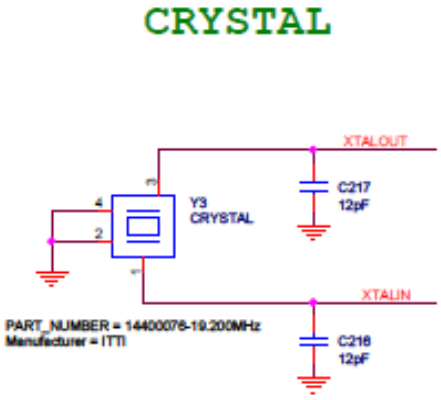

Figure 1-3: Crystal circuit

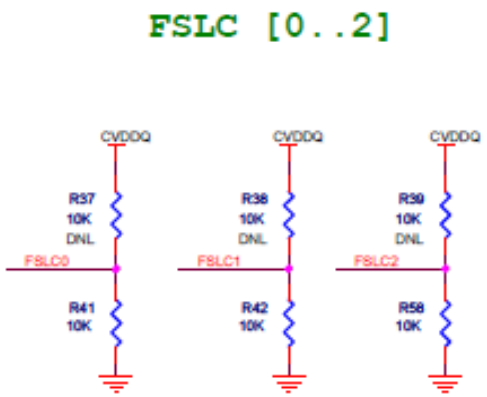

Figure 1-4: FSLC [2:0] lines pulled to ground. Pull up resistors are not loaded on the board.

1.1.4 GPIF II Connector

FX3 offers a high performance General Programmable Interface, GPIF II. This interface enables functionality similar to but more advanced than FX2LP's GPIF. The GPIF II is a programmable state machine that enables a flexible interface that may function either as a master or slave in industry standard or proprietary interfaces. Both parallel and serial interfaces may be implemented with GPIF II. The DVK board consists of a samtec expansion connector to interface with user's external processors, ASICs, DSPs or FPGAs. The GPIF II lines going out to the samtec connector also come out on a mictor for probing purposes.
The figure below shows the samtec expansion connector with the GPIF II signals coming out on it.

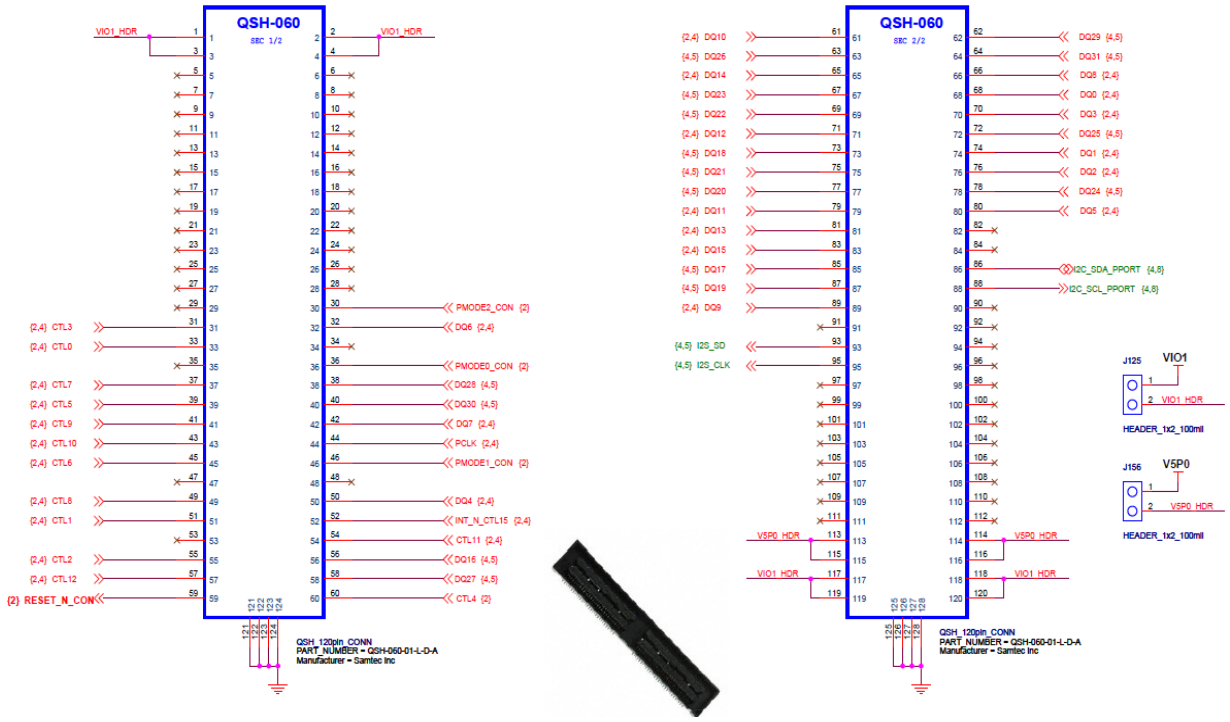

Figure 1-5: Samtec expansion connector circuit

The table below shows the pin out of the GPIF II interface coming out on the samtec expansion connector.

Table 1-2: FX3 GPIF II signal pin out on samtec connector

Connector Pin Number	FX3 signals	GPI/O
88	I2C-SCL	i2c_gpio[58]
86	I2C-SDA	i2c_gpio[59]
52	INT	int#
53	SPI-SCK_UART-RTS	L_gpio[53]
34	SPI-SSN_UART-CTS_I2S-CLK	L_gpio[54]
35	SPI-MISO_UART-TX_I2S-SD	L_gpio[55]
48	SPI-MOSI_UART-RX_I2S_WS	L_gpio[56]
90	I2S-MCLK	L_gpio[57]
68	D0	p_gpio[0]
74	D1	p_gpio[1]
61	D10	p_gpio[10]
79	D11	p_gpio[11]
71	D12	p_gpio[12]
81	D13	p_gpio[13]
65	D14	p_gpio[14]
83	D15	p_gpio[15]
44	CLK	p_gpio[16]

33	CTL0	p_gpio[17]
51	CTL1	p_gpio[18]
55	CTL2	p_gpio[19]
76	D2	p_gpio[2]
31	CTL3	p_gpio[20]
60	CTL4	p_gpio[21]
39	CTL5	p_gpio[22]
45	CTL6	p_gpio[23]
37	CTL7	p_gpio[24]
49	CTL8	p_gpio[25]
41	CTL9	p_gpio[26]
43	CTL10	p_gpio[27]
54	CTL11	p_gpio[28]
57	CTL12	p_gpio[29]
70	D3	p_gpio[3]
36	PMODE0	p_gpio[30]
46	PMODE1	p_gpio[31]
30	PMODE2	p_gpio[32]
50	D4	p_gpio[4]
80	D5	p_gpio[5]
32	D6	p_gpio[6]
42	D7	p_gpio[7]
66	D8	p_gpio[8]
89	D9	p_gpio[9]
59	RESET	reset#
56	D16	s0_gpio[33]
85	D17	s0_gpio[34]
73	D18	s0_gpio[35]
87	D19	s0_gpio[36]
77	D20	s0_gpio[37]
75	D21	s0_gpio[38]
69	D22	s0_gpio[39]
67	D23	s0_gpio[40]
78	D24	s0_gpio[41]
72	D25	s0_gpio[42]
63	D26	s0_gpio[43]
58	D27	s0_gpio[44]
38	D28_UART-RTS	s1_gpio[46]
62	D29_UART-CTS	s1_gpio[47]
40	D30_UART-TX	s1_gpio[48]
64	D31_UART-RX	s1_gpio[49]
95	I2S-CLK	s1_gpio[50]
93	I2S-SD	s1_gpio[51]
91	I2S-WS	s1_gpio[52]

As can be seen in Figure 1-5, J125 can be used to enable the VIO1 power going out on the samtec connector, if populated. Similarly, J156 can be used to enable the 5V power going out on the samtec connector, if populated.
The CTRL_4 line on the GPIF II interface is also used to enable/disable the on-board USB switch for OTG power. This selection can be made on J100. The figure below shows how the selection for CTRL_4 can be made.

Figure 1-6: CTRL_4 selection jumper

As can be seen in Figure 1-5, if 1 and 2 are connected on J100 through a jumper, the CTRL_4 line will go to the GPIF II interface on the samtec connector. If 2 and 3 are connected, the CTRL_4 line will route to the USB switch for OTG power control.

1.1.5 Reset Circuit

The FX3 device can either be reset from the external processor hooked up to the samtec connector or from an on-board push button. This selection can be made on J72, as seen in Figure 1-6 below:

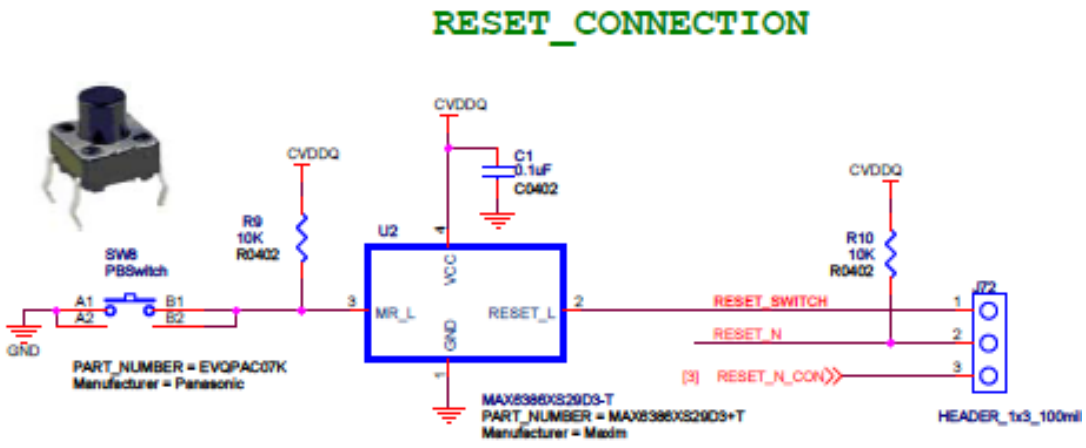

Figure 1-7: Reset circuit and selection headers

A de bounce IC detects the pressing of the button and generates a reset signal at it's output. Based on the selection made on J72, either this reset signal goes to the FX3 device (pins 1 and 2 connected on J72) or a signal from the external processor resets the FX3 device (pins 2 and 3 connected on J72).

1.1.6 I2C Interface

The I2C interface lines on the FX3 device come out to headers for probing and expansion, and also connect to an on board EEPROM device. The EEPROM address bits A2, A1 and A0 can be set using the on-board dip switches on SW40, as follows:

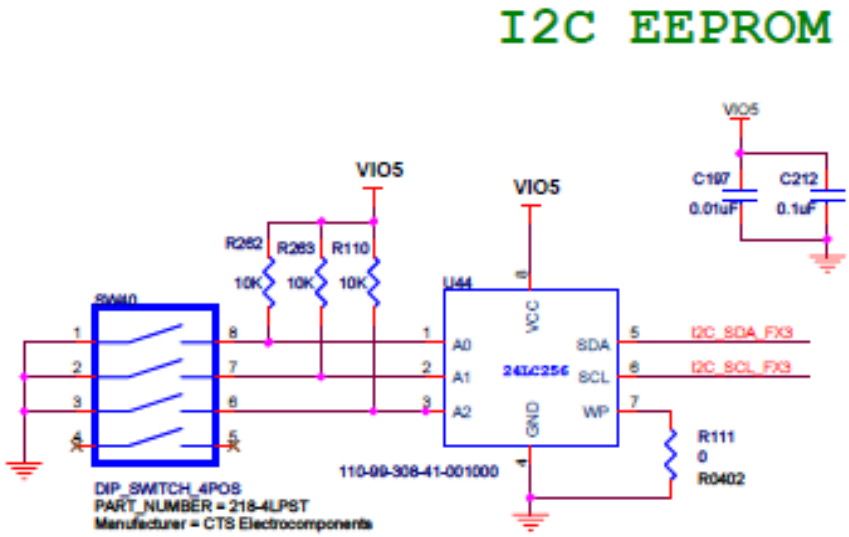

Figure 1-8: EEPROM and address selection switches

If the bit is set towards the ‘ON’ text on SW40, that particular line will be connected to ground, thus making the corresponding line to be grounded. If the bit is set towards the numeric text (away from the ‘ON’ text) on SW40, the corresponding line will be pulled high to VIO5.

1.1.6.1 Booting from the EEPROM

The FX3 device can boot from the EEPROM connected to its I2C interface. To enable I2C EEPROM boot, the PMODE [2:0] signals need to be set correctly. A brief description on how to set the PMODE [2:0] signals is presented below.

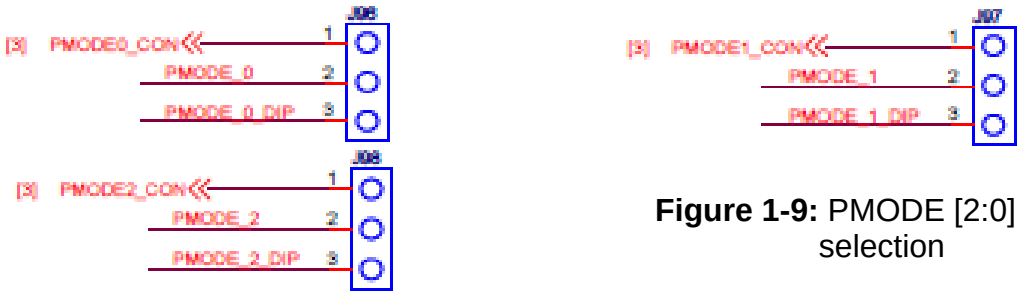

Figure 1-9: PMODE [2:0] signal selection

Headers J96, J97 and J98 are used to select whether the PMODE [2:0] signals are set externally (from the external processor) or on the board. PMODE_0, PMODE_1 and PMODE_2 on the FX3 device are connected to pin 2 of each header, J96, J97 and J98. The user can place a jumper on 1 and 2 to control the PMODE signals from the external processor, or on 2 and 3 to control the PMODE signals from the dip switch SW25 on the board.

The PMODE [2:0] signals can be set, either from the external processor or from the on-board dip switch, according to the table below:

Table 1-3: PMODE signal settings

PMODE [2:0]	Boot from
F11	USB boot
F1F	I2C; on failure, USB boot is enabled
1FF	I2C only

F = floating

If the PMODE [2:0] signals are set to F1F or 1FF, the FX3 device will boot from the EEPROM connected to the I2C interface. The EEPROM will have to contain the correct boot data for the FX3 device to boot from it.
The PMODE [2:0] signals can be set on the dip switch SW25 as follows:

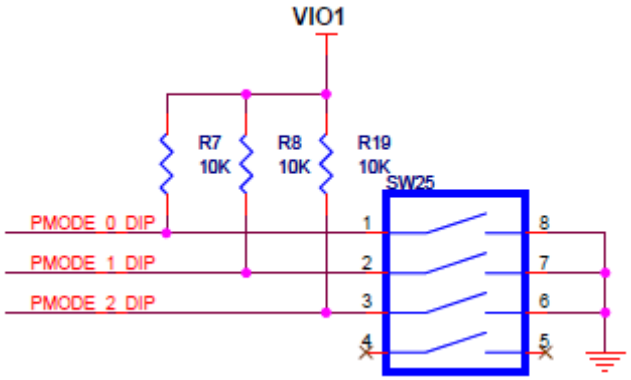

Figure 1-10: PMODE [2:0] selection dip switches

If the bit is set towards the ‘ON’ text, the corresponding signal line is connected to ground. If the bit is set towards the numeric text (away from the ‘ON’ text), the corresponding signal line is pulled high to VIO1.

1.1.7 Low Performance Peripherals (LPP)

EZ-USB FX3 consists of the following Low Performance Peripherals:

- JTAG
- I2S
- SPI and UART

1.1.7.1 JTAG

FX3's JTAG interface provides a standard five-pin interface for connecting to a JTAG debugger to debug the firmware through the CPU core's on-chip debug circuitry. Industry standard debugging tools for the ARM926E-J-S core can be used for FX3 application development. The JTAG pins of FX3 come out on J51. Please refer to the SDK documentation for details regarding the debugger.

1.1.7.2 I2S

EZ-USB FX3 has an I2S port to support external audio codec devices. FX3 functions as an I2S master (transmitter only). The I2S interface consists of four signals: clock line (I2S_CLK), serial data line (I2S_SD), word select line (I2S_WS) and master system clock (I2S_MCLK). FX3 can generate the system clock as an output on the I2S_MCLK line or accept an external system clock input on the same line. All four I2S lines come out on header J20.

1.1.7.3 SPI and UART

EZ-USB FX3 supports an SPI master interface on the serial peripherals port. The SPI lines are shared with the UART lines on the FX3 device. Selection is made on the board to be able to use either the SPI interface or the UART interface.

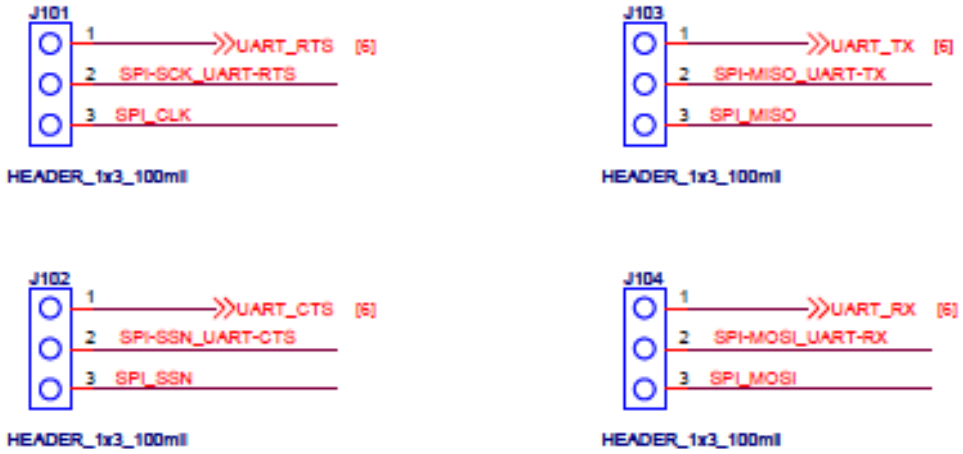

Figure 1-11: SPI/UART selection headers

If 1 and 2 are shorted on J101, J102, J103 and J104; FX3 device will be connected to an RS-232 connector for UART operation. If 2 and 3 are shorted on

these four jumpers, the SPI interface of FX3 will come out to J34 only. The RS-232 connector will be disconnected from the FX3 device in this case.