



NuMicro Mini51 Series Product Brief

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1 DESCRIPTION

The NuMicro Mini series is a single-chip low pin count 32-bit microcontroller designed for applications demanding high performance, high-integration low-cost requirements. The NuMicro MINI series is based on the latest ARM® Cortex™-M0 core that has a cost equivalent to a traditional 8-bit microcontroller.

The NuMicro Mini series can run up to 24MHz. Thus it can afford to support a variety of industrial control and applications which need high CPU performance. The NuMicro Mini series has 4K/8K/16K bytes of embedded Flash for program memory and up to 4K bytes data FLASH for user's non-volatile data which share with program memory.

Many system level peripheral functions, such as I/O Ports, RAM, Timers, UART, SPI, I2C, PWM, ADC, Watchdog Timer and low voltage detector, have been incorporated into the NuMicro Mini series in order to reduce component count, board space and system cost. These useful functions make the NuMicro Mini series powerful for a wide range of applications.

Additionally, the NuMicro Mini series is equipped with ISP (In-System Programming) and ICP (In-Circuit Programming) functions, which allow the user to update program memory and non-volatile data without removing the MCU chip from the actual end product.



2 FEATURES

- Built-in LDO for Wide Operating Voltage Range: 2.5V to 5.5V
- Core
 - ARM® Cortex™ -M0 core runs up to 24 MHz.
 - One 24-bit system timer.
 - Supports low power sleep-mode.
 - Single-cycle 32-bit hardware multiplier.
 - NVIC for the 32 interrupt inputs, each with 4-levels of priority.
 - Serial Wire Debug (SWD) supports with 4 breakpoints.
- Memory
 - APROM: 4KB/ 8KB/16KB Flash memory for program memory
 - Data FLASH: Configurable 0/1/2/4KB Flash memory for data memory (Share with APROM)
 - 2KB Flash memory for loader (LDRAM)
 - 2KB SRAM for internal scratch-pad RAM (SRAM)
- In-System Programming (ISP) & In-Circuit Programming (ICP)
- Clock Control
 - Programmable system clock source
 - 4 ~ 24 MHz crystal oscillator
 - 32.768K crystal oscillator for low power operating current and wake-up in sleep mode.
 - 10 kHz low-power oscillator for Watchdog Timer and wake-up in sleep mode
 - 22.1184MHz internal oscillator (trimmed to 1% accuracy)
 - ◆ 32.768K crystal calibration mode: Dynamic trim the 22.1184MHz RC OSC to 1% from -40°C to 85°C by external 32.768K crystal oscillator.
- I/O Port
 - Up to 29 general-purpose I/O (GPIO) pins for QFN33/LQFP33 package and up to 30 GPIO pins for LQFP48 package.
 - Software-configured I/O type (All I/O pins power on default as input tri-stated)
 - ◆ Quasi-bidirectional input/output
 - ◆ Push-pull output
 - ◆ Open-drain output
 - ◆ Input-only
 - Optional Schmitt trigger input
 - I/O pin can be configured as interrupt source with edge/level setting
- Timer
 - Two 24-bit Timers with 8-bit prescaler
 - ◆ Support event counter mode
 - ◆ Support pulse width capture mode

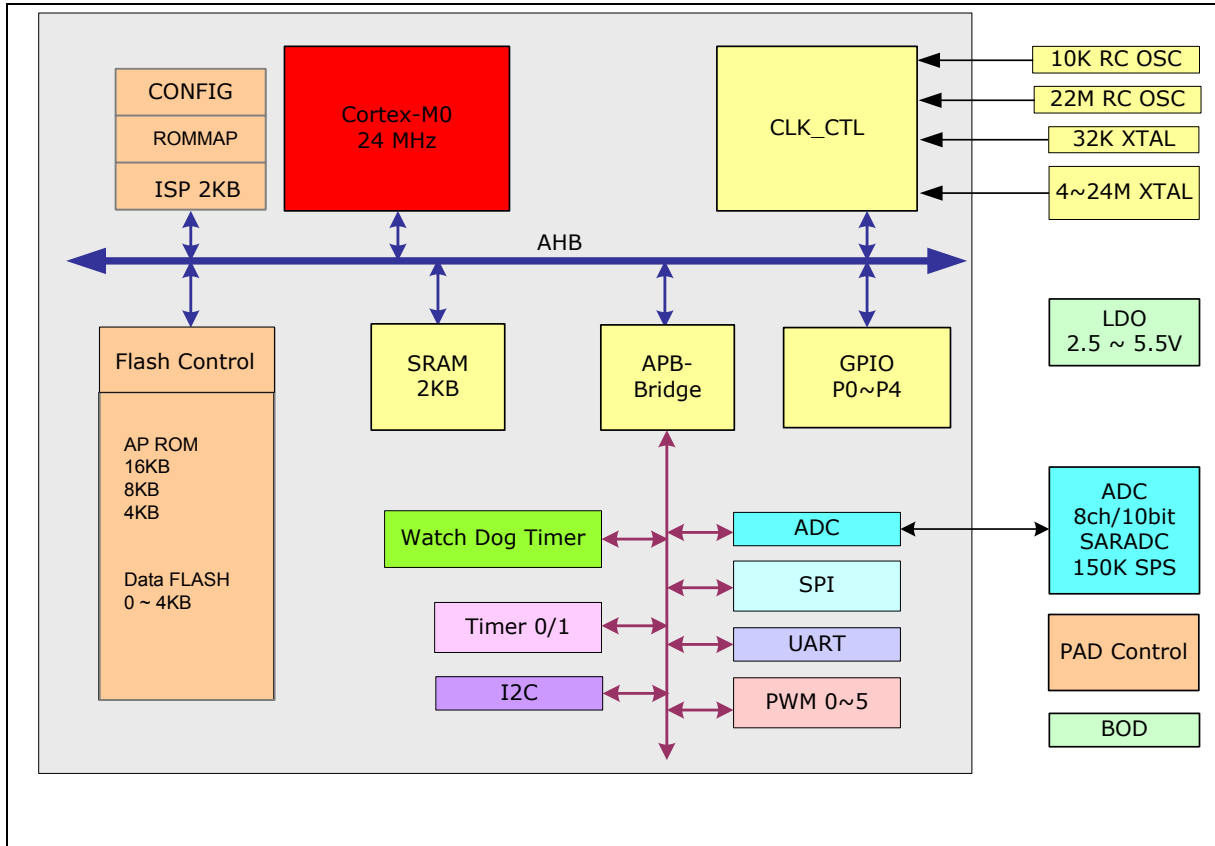


- ◆ Supports timer start & stop external trigger in Pulse width measurement mode.
- Watchdog Timer
 - Programmable clock source and timeout period
 - Support wake-up function in power-down mode and power-sleep mode
 - Interrupt or reset selectable when timeout happens
- PWM
 - Built-in up to three 16-bit PWM generators provide six PWM outputs or three complementarily paired PWM outputs
 - Support edge alignment or center alignment
 - Support fault detection to stop PWM immediately and set PWM output high or low level then generate an interrupt. Trigger by assigned IO or comparator
 - Individual clock source, clock divider, 8-bit pre-scalar and dead-zone generator for each PWM generator
 - PWM interrupt synchronized to PWM period
- UART
 - One UART device.
 - Buffered receiver and transmitter with 16 bytes FIFO
 - Optional flow control function (CTS and RTS)
 - Programmable baud-rate generator up to 1/16 system clock
 - Supports IrDA(SIR) function
 - Supports RS485 function
- SPI
 - One SPI device.
 - Master ($F_{sys} / 1$) up to 24MHz, and Slave ($F_{sys} / 6$) up to 4MHz
 - Support SPI master/slave mode
 - Full duplex synchronous serial data transfer
 - Variable length of transfer data from 1 to 32 bits
 - MSB or LSB first data transfer
 - Rx and Tx on both rising or falling edge of serial clock independently
 - Tx and Rx on both rising or falling edge of serial clock independently
 - Byte suspend mode in 32-bit transmission
- I2C
 - Master/Slave up to 1Mbit/s (Fast-mode Plus)
 - Bidirectional data transfer between masters and slaves
 - Multi-master bus (no central master).
 - Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
 - Serial clock synchronization allows devices with different bit rates to communicate via one serial bus.



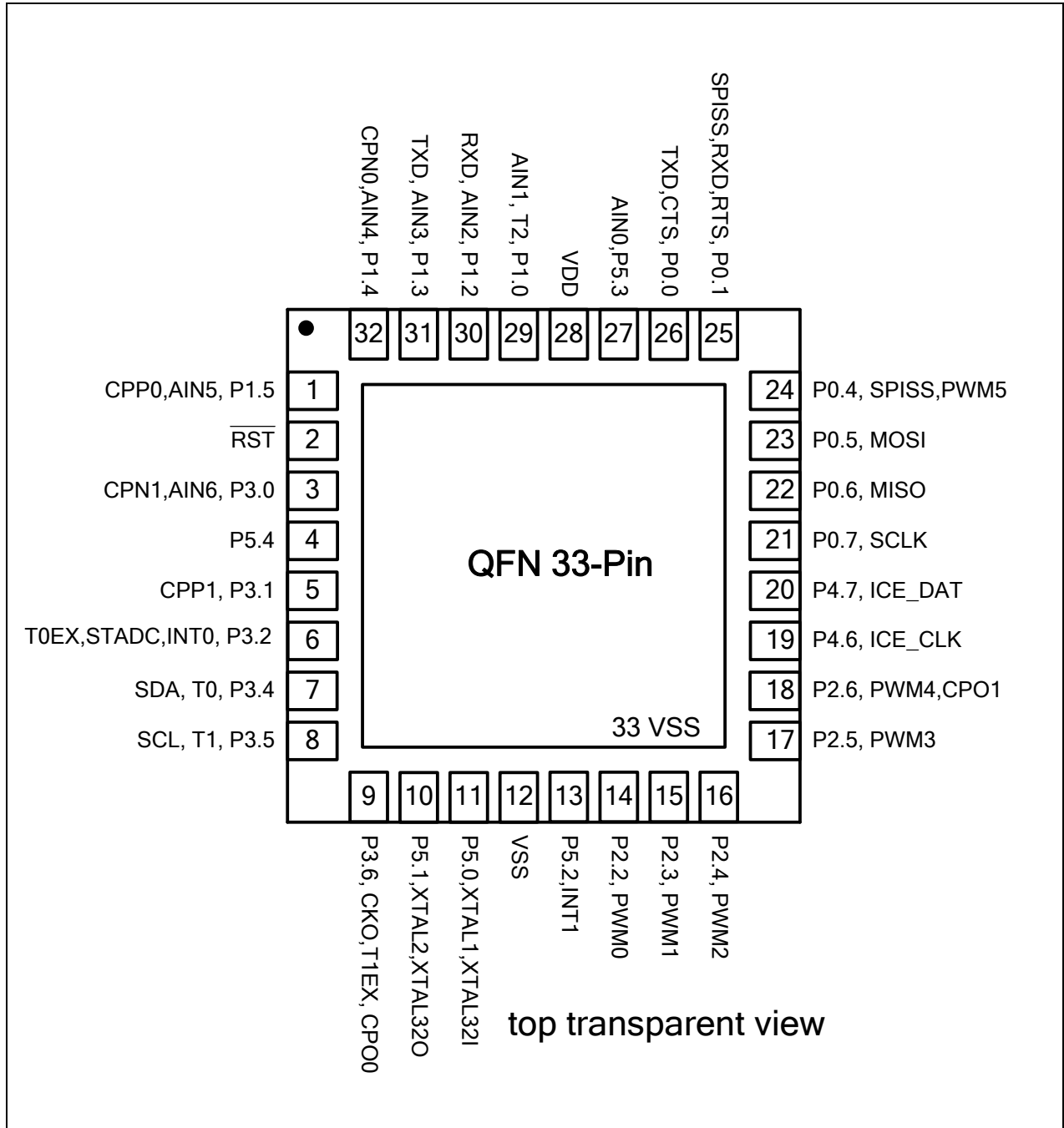
- Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer.
- Programmable clocks allow versatile rate control.
- Support multiple address recognition (two slave address with mask option)
- ADC
 - 10-bit SAR ADC with 150K SPS
 - Up to 8-ch single-end input and one internal input from 1.2V bandgap
 - Conversion started by S/W or external pin
- Two analog comparators with programmable 16-level internal voltage reference (CRV)
- Build-in comparator reference voltage (CRV) generator.
 - $CRV = VDD \times (1/6 + CRVS[3:0] / 24)$.
- BOD Reset
 - Programmable threshold levels: 3.8V/2.7V/2.0V(BOD 2.0V reset always enable)
 - Optional BOD interrupt or reset
- Operating Temperature: -40°C ~85°C
- Packages:
 - Green package (RoHS)
 - 48-pin LQFP (7x7), 33-pin LQFP (5x5) , 33-pin QFN (5x5)

3 BLOCK DIAGRAM

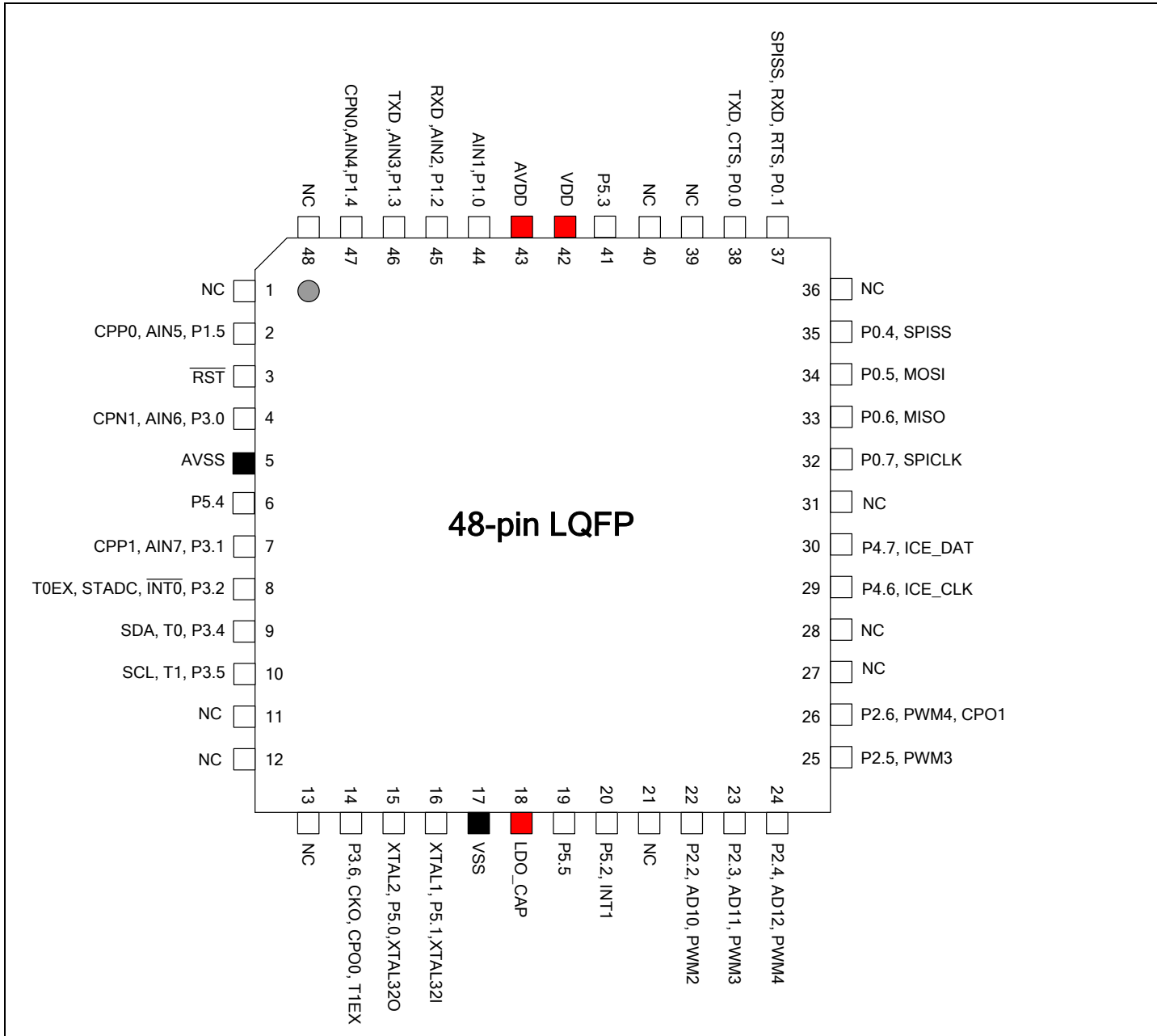


4 PIN CONFIGURATION

4.1 QFN 33 pin / LQFP 33 pin



4.2 LQFP 48 pin





4.3 Pin Description (Preliminary)

Pin number		Symbol	Alternate Function			Type ⁽¹⁾	Description
QFN33 LQFP33	LQFP48		1	2	3		
11	16	P5.0	XTAL1			I/O	<p>XTAL1: This is the input pin to the internal inverting amplifier. The system clock is from external crystal or resonator when FOSC[1:0] (CONFIG3[1:0]) are both logic 1 by default.</p> <p>Note: To set PWRCON[1:0] to select 12MHz or 32KHz crystal clock.</p> <p>GPIO P5.0 function pin.</p>
10	15	P5.1	XTAL2			I/O	<p>XTAL2: This is the output pin from the internal inverting amplifier. It emits the inverted signal of XTAL1.</p> <p>Note: To set PWRCON[1:0] to select 12MHz or 32KHz crystal clock.</p> <p>GPIO P5.1 function pin.</p>
27	41	P5.3	AIN0			I/O	<p>This pin has an alternative function as AIN0 for the 10 bits ADC function used.</p> <p>GPIO P5.3 function pin.</p>
12	17	VSS				P	GROUND: Digital Ground potential.
33							
	19	P5.5				I/O	GPIO P5.5 function pin.
28	42	VDD				P	POWER SUPPLY: Supply voltage for operation.
	5	AVSS				P	GROUND: Analog Ground potential.
4	6	P5.4				I/O	GPIO P5.4 function pin.
	43	AVDD				P	POWER SUPPLY: Supply voltage for analog.
13	20	P5.2	INT1			D,I/O	<p>This pin has an alternative function as INT1 for external interrupt function used.</p> <p>GPIO P5.2 function pin.</p>
13	18	LDO_C AP				P	<p>LDO: LDO output pin</p> <p>Note: It needs to be connected with a 10uF capacitor.</p>

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Pin number		Symbol	Alternate Function			Type ^[1]	Description
QFN33 LQFP33	LQFP48		1	2	3		
2	3	/RST				I (ST)	RESET: /RST pin is a Schmitt trigger input pin for hardware device reset. A "Low" on this pin for 768 clock counter of Internal RC 22M while the system clock is running will reset the device. /RST pin has an internal pull-up resistor allowing power-on reset by simply connecting an external capacitor to GND.
26	38	P0.0	CTS	TXD		D, I/O	PORT0: Port 0 is an 6-bit four mode output pin and two mode input. Its multifunction pins are for PWM, CTS, RTS, CTS, RTS, SPISS, MOSI, MISO, and SPICLK. These pins which are SPISS, MOSI, MISO, and SPICLK for the SPI function used. The RXD/TXD/CTS/RTS pins are for UART function used.
25	37	P0.1	RTS	RXD	SPISS	D, I/O	
24	35	P0.4	SPISS	PWM5		D, I/O	
23	34	P0.5	MOSI			D, I/O	
22	33	P0.6	MISO			D, I/O	
21	32	P0.7	SPICLK			D, I/O	
29	44	P1.0	T2	AIN1		A, I/O	
30	45	P1.2	RXD	AIN2		A, I/O	PORT1: Port 1 is an 5-bit four mode output pin and two mode input. Its multifunction pins are for T2, RXD and TXD. These pins which are AIN1~AIN5 for the 10 bits ADC function used. The RXD/TXD pins are for UART function used. T2: Timer2 external input CPN0/CPN0:Comparator input.
31	46	P1.3	TXD	AIN3		A, I/O	
32	47	P1.4		AIN4	CPN0	A, I/O	
1	2	P1.5		AIN5	CPP0	A, I/O	
14	22	P2.2	PWM0			D, I/O	PORT2: Port 2 is an 5-bit four mode output pin and two mode input. It has an alternative function These pins which are PWM0~PWM4 for the PWM function.
15	23	P2.3	PWM1			D, I/O	
16	24	P2.4	PWM2			D, I/O	
17	25	P2.5	PWM3			D, I/O	
18	26	P2.6	PWM4		CPO1	D, I/O, A	
3	4	P3.0		AIN6	CPN1	A, I/O	PORT3: Port 3 is an 6-bit four mode output pin and two mode input. Its multifunction pins are for CPN1, CPP1, T0EX, T1EX, INT 0, T0 and T1. The SDA/SCK pins are for I2C function used.
5	7	P3.1		AIN7	CPP1	A, I/O	
6	8	P3.2	INT 0	STADC	T0EX	I/O	

Pin number		Symbol	Alternate Function			Type ^[1]	Description
QFN33 LQFP33	LQFP48		1	2	3		
7	9	P3.4	T0	SDA		I/O	CKO: HCLK clock output
8	10	P3.5	T1	SCL		I/O	The STADC pin is for ADC external trigger input.
9	14	P3.6	CPO0	CKO	T1EX	I/O	These pins which are AIN6~AIN7 for the 10 bits ADC function used. T0/T1: Timer0&1 external clock or event counter input T0EX/T1EX : Timer0&1 capture input for pulse width measurement
19	29	P4.6	ICE_CLK			I/O	PORT4: Port 4 is an 2-bit four mode output pin and two mode input. Its multifunction pins are for ICE_CLK and ICE_DAT.
20	30	P4.7	ICE_DAT			I/O	The ICE_CLK/ICE_DAT pins are for JTAG-ICE function used.

[1] I/O type description. I: input, O: output, I/O: quasi bi-direction, D: open-drain, P: power pin, ST: Schmitt trigger. A: Analog input



5 ELECTRICAL CHARACTERISTICS

5.1 Absolute Maximum Ratings

SYMBOL	PARAMETER	Min	MAX	UNIT
DC Power Supply	VDD-VSS	-0.3	+7.0	V
Input Voltage	VIN	VSS-0.3	VDD+0.3	V
Oscillator Frequency	1/t _{CLCL}	0	24	MHz
Operating Temperature	TA	-40	+85	°C
Storage Temperature	TST	-55	+150	°C
Maximum Current into V _{DD}		-	120	mA
Maximum Current out of V _{SS}			120	mA
Maximum Current sunk by a I/O pin			35	mA
Maximum Current sourced by a I/O pin			35	mA
Maximum Current sunk by total I/O pins			100	mA
Maximum Current sourced by total I/O pins			100	mA

Stresses at or above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability.



5.2 DC Electrical Characteristics

(VDD-VSS=3.3V, TA = 25°C, FOSC = 24 MHz unless otherwise specified.)

PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
Operation voltage	V _{DD}	2.5		5.5	V	V _{DD} = 2.5V ~ 5.5V up to 24 MHz
Power Ground	V _{SS} AV _{SS}	-0.3			V	
LDO Output Voltage	V _{LDO}	-10%	1.8	+10%	V	V _{DD} > 2.5V
Analog Operating Voltage	AV _{DD}	0		V _{DD}	V	
Operating Current Normal Run Mode @ 24MHz	I _{DD5}		TBD		mA	V _{DD} = 5.5V@24MHz, enable all IP
	I _{DD6}		TBD		mA	V _{DD} = 5.5V@24MHz, disable all IP
	I _{DD7}		TBD		mA	V _{DD} = 3V@24MHz, enable all IP
	I _{DD8}		TBD		mA	V _{DD} = 3V@24MHz, disable all IP
Operating Current Normal Run Mode @ 12MHz	I _{DD5}		TBD		mA	V _{DD} = 5.5V@12MHz, enable all IP
	I _{DD6}		TBD		mA	V _{DD} = 5.5V@12MHz, disable all IP
	I _{DD7}		TBD		mA	V _{DD} = 3V@12MHz, enable all IP
	I _{DD8}		TBD		mA	V _{DD} = 3V@12MHz, disable all IP
Operating Current Normal Run Mode @ 4MHz	I _{DD9}		TBD		mA	V _{DD} = 5V@4MHz, enable all IP
	I _{DD10}		TBD		mA	V _{DD} = 5V@4MHz, disable all IP
	I _{DD11}		TBD		mA	V _{DD} = 3V@4MHz, enable all IP
	I _{DD12}		TBD		mA	V _{DD} = 3V@4MHz, disable all IP
Operating Current Idle Mode @ 24MHz	I _{IDLE5}		TBD		mA	V _{DD} = 5.5V@24MHz, enable all IP
	I _{IDLE6}		TBD		mA	V _{DD} = 5.5V@24MHz, disable all IP
	I _{IDLE7}		TBD		mA	V _{DD} = 3V@24MHz, enable all IP
	I _{IDLE8}		TBD		mA	V _{DD} = 3V@24MHz, disable all IP
Operating Current Idle Mode @ 12MHz	I _{IDLE5}		TBD		mA	V _{DD} = 5.5V@12MHz, enable all IP
	I _{IDLE6}		TBD		mA	V _{DD} = 5.5V@12MHz, disable all IP
	I _{IDLE7}		TBD		mA	V _{DD} = 3V@12MHz, enable all IP
	I _{IDLE8}		TBD		mA	V _{DD} = 3V@12MHz, disable all IP

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PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
Operating Current Idle Mode @ 4MHz	I _{IDLE9}		TBD		mA	V _{DD} = 5V@4MHz, enable all IP
	I _{IDLE10}		TBD		mA	V _{DD} = 5V@4MHz, disable all IP
	I _{IDLE11}		TBD		mA	V _{DD} = 3V@4MHz, enable all IP
	I _{IDLE12}		TBD		mA	V _{DD} = 3V@4MHz, disable all IP
Standby Current Power-down Mode (Deep Sleep Mode)	I _{PWD1}		TBD		μA	V _{DD} = 5.5V, CPU STOP All IP and Clock OFF
	I _{PWD2}		5		μA	V _{DD} = 3V, CPU STOP All IP and Clock OFF
Input Current P0~P4 (Quasi-bidirectional mode)	I _{IN1}	-60	-	+15	μA	V _{DD} = 5.5V, V _{IN} = 0V or V _{IN} =V _{DD}
Input Current at /RESET ^[1]	I _{IN2}	-55	-45	-30	μA	V _{DD} = 3.3V, V _{IN} = 0.45V
Input Leakage Current P0~P4	I _{LK}	-2	-	+2	μA	V _{DD} = 5.5V, 0<V _{IN} <V _{DD}
Logic 1 to 0 Transition Current P0~P4 (Quasi-bidirectional mode)	I _{TL} ^[3]	-650	-	-200	μA	V _{DD} = 5.5V, V _{IN} <2.0V
Input Low Voltage P0~P4 (TTL input)	V _{IL1}	-0.3	-	0.8	V	V _{DD} = 4.5V
		-0.3	-	0.6		V _{DD} = 2.5V
Input High Voltage P0~P4 (TTL input)	V _{IH1}	2.0	-	V _{DD} +0.2	V	V _{DD} = 5.5V
		1.5	-	V _{DD} +0.2		V _{DD} = 3.0V
Input Low Voltage P0~P4 (Schmitt input)	V _{IL2}				V	
Input High Voltage P0~P4 (Schmitt input)	V _{IH2}		0.2V _{DD}		V	
Hysteresis voltage of P0~P4 (Schmitt input)	V _{HY}		0.2V _{DD}		V	
Input Low Voltage XT1 ^[2]	V _{IL3}	0	-	0.8	V	V _{DD} = 4.5V
		0	-	0.4		V _{DD} = 3.0V
Input High Voltage XT1 ^[2]	V _{IH3}	3.5	-	V _{DD} +0.2	V	V _{DD} = 5.5V
		2.4	-	V _{DD} +0.2		V _{DD} = 3.0V
Negative going threshold (Schmitt input), /RESET	V _{ILS}	-0.5	-	0.3V _{DD}	V	
Positive going threshold (Schmitt input), /RESET	V _{IHS}	0.7V _{DD}	-	V _{DD} +0.5	V	



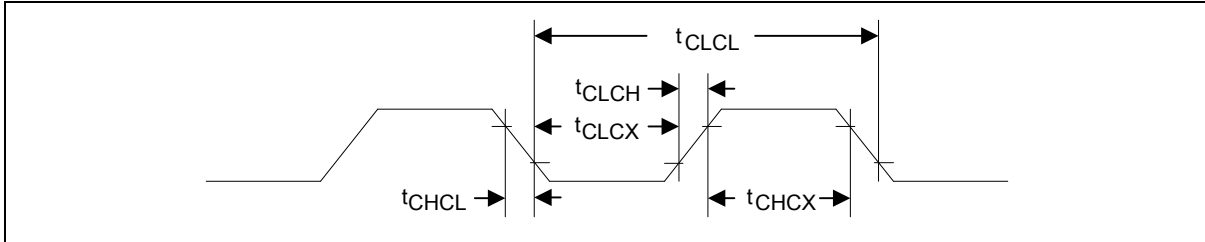
PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
Source Current P0, P1, P2, P3 (Quasi-bidirectional Mode)	I _{SR11}	-300	-370	-450	μA	V _{DD} = 4.5V, V _S = 2.4V
	I _{SR12}	-50	-70	-90	μA	V _{DD} = 2.7V, V _S = 2.2V
	I _{SR12}	-40	-60	-80	μA	V _{DD} = 2.5V, V _S = 2.0V
Source Current P0, P1, P2, P3 (Push-pull Mode)	I _{SR21}	-20	-24	-28	mA	V _{DD} = 4.5V, V _S = 2.4V
	I _{SR22}	-4	-6	-8	mA	V _{DD} = 2.7V, V _S = 2.2V
	I _{SR22}	-3	-5	-7	mA	V _{DD} = 2.5V, V _S = 2.0V
Sink Current P0, P1, P2, P3(Quasi-bidirectional and Push-pull Mode)	I _{SK1}	10	16	20	mA	V _{DD} = 4.5V, V _S = 0.45V
	I _{SK1}	7	10	13	mA	V _{DD} = 2.7V, V _S = 0.45V
	I _{SK1}	6	9	12	mA	V _{DD} = 2.5V, V _S = 0.45V

Notes:

1. /RST pin is a Schmitt trigger input.
2. XTAL1 is a CMOS input.
3. Pins of P0, P1, P2, P3 and P4 can source a transition current when they are being externally driven from 1 to 0. In the condition of V_{DD}=5.5V, the transition current reaches its maximum value when V_{in} approximates to 2V.

5.3 AC ELECTRICAL CHARACTERISTICS

5.3.1 External Crystall



Note: Duty cycle is 50%.

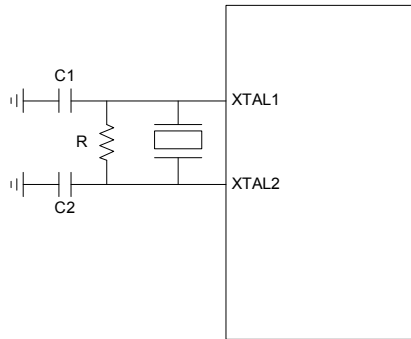
PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNITS	CONDITION
Clock High Time	t_{CHCX}	20.8	-	-	nS	
Clock Low Time	t_{CLCX}	20.8	-	-	nS	
Clock Rise Time	t_{CLCH}	-	-	10	nS	
Clock Fall Time	t_{CHCL}	-	-	10	nS	

5.3.2 External XTAL1 Oscillator

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Input clock frequency	External crystal	4	12	24	MHz
Temperature	-	-40	-	85	°C
V_{DD}	-	2.5	5	5.5	V
Operating current	12MHz@ $V_{DD} = 5V$	-	TBD	-	mA

5.3.3 XTAL1 Typical Crystal Application Circuits

CRYSTAL	C1	C2	R
4MHz ~ 24 MHz	without	without	without



5.3.4 External 32.768 KHz XTAL Oscillator

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Input clock frequency	External crystal	-	32.768	-	KHz
Temperature	-	-40	-	85	°C

5.3.5 Internal 22.1184MHz RC Oscillator

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Supply voltage ^[1]	-	-	1.8	-	V
Center Frequency	-	-	22.1184	-	MHz
Calibrated Internal Oscillator Frequency	+25°C; V _{DD} =5V	-1	-	+1	%
	-40°C~+85°C; V _{DD} =2.5V~5.5V	-5	-	+5	%
Dynamic Calibrated Internal Oscillator Frequency by external 32.768KHz crystal oscillator	-40°C~+85°C; V _{DD} =2.5V~5.5V	-1	-	+1	%
Operating current	V _{DD} =5V	-	TBD	-	uA

5.3.6 Internal 10kHz RC Oscillator

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Supply voltage ^[1]	-	-	1.8	-	V
Center Frequency	-	-	10	-	kHz
Accuracy of Un-calibrated Internal Oscillator Frequency	+25°C; V _{DD} =5V	-30	-	+30	%
	-40°C~+85°C; V _{DD} =2.5V~5.5V	-50	-	+50	%
Operating current	V _{DD} =5V	-	TBD	-	uA

5.4 Analog Characteristics



5.4.1 Specification of Brown Out Reset (BOD)

Parameter	Condition	Min.	Typ.	Max.	Unit
Operation voltage	VDD	2.0		5.5	V
current	BOD20 VDD=5V		1	1.5	μA
	BOD20 + BOD27 + BOD38, VDD=5V		10	15	uA
Temperature		-40	25	85	°C
BOD38	25°C	3.7	3.8	3.9	V
BOD27	25°C	2.6	2.7	2.8	V
BOD20 (Always enable)	-40°C ~ +85°C	1.6	2.0	2.4	V

5.4.2 Specification of Analog Comparator

Parameter	Condition	Min.	Typ.	Max.	Unit
Temperature	-	-40	25	85	°C
VDD	-	2.5	3	5.5	V
Operating current	-	-	20	-	uA
Input offset voltage	-	-	5	15	mV
Output swing	-	0.1	-	VDD-0.1	V
Input common mode range	-	0.1	-	VDD-1.2	V
DC gain	-	-	70	-	dB
Propagation delay	@VCM=1.2V & VDIFF=0.1V	-	200	-	ns
Comparison voltage	20mV@VCM=1V 50mV@VCM=0.1V 50mV@VCM=VDD-1.2 @10mV for non-hysteresis	10	20	-	mV
Hysteresis	One bit control W/O & W. hysteresis @VCM=0.4V ~ VDD-1.2V	-	±10	-	mV
Wake up time	@CINP=1.3V CINN=1.2V	-	-	2	us

5.4.3 Analog Comparator Reference Voltage

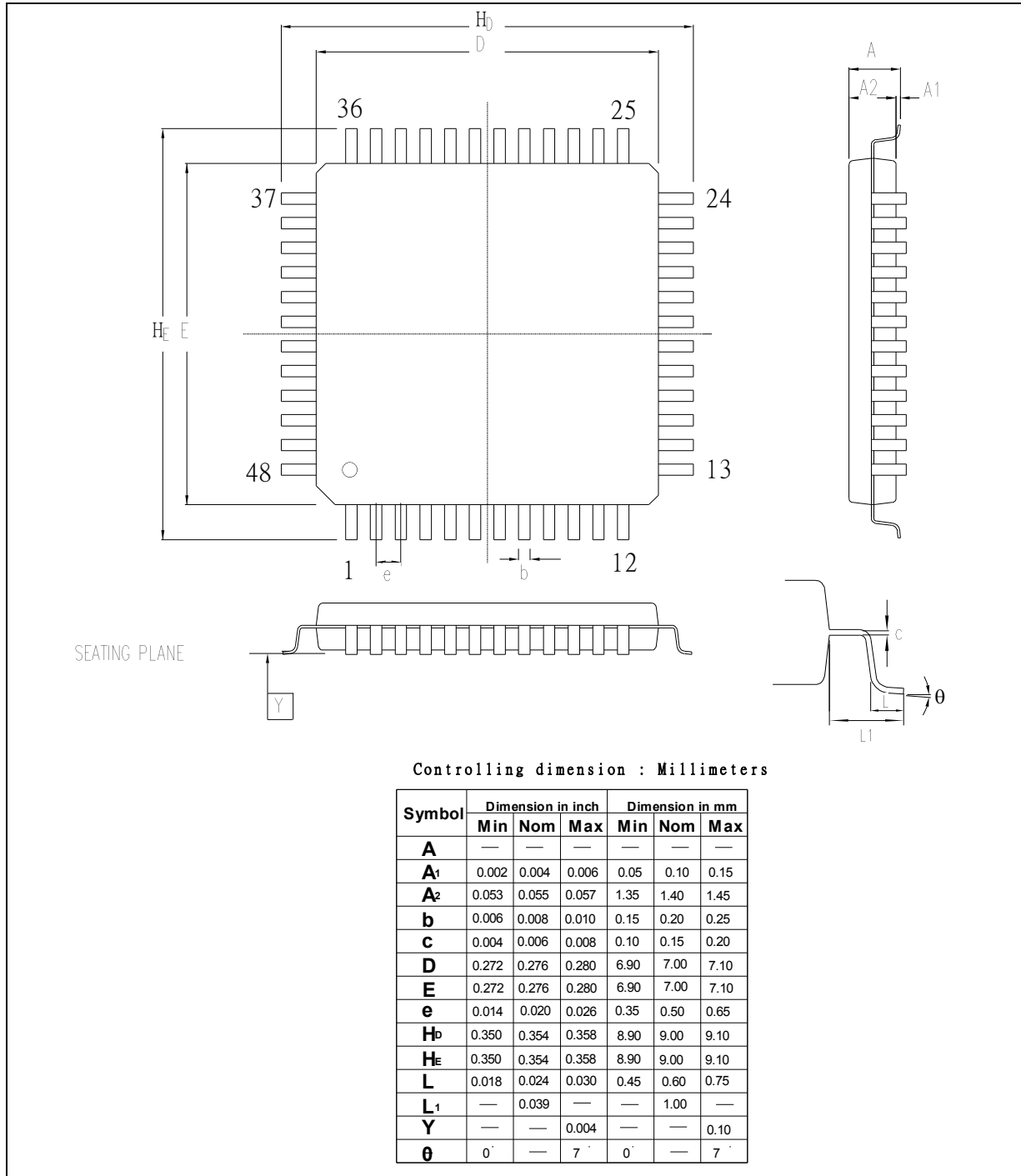
Parameter	Condition	Min.	Typ.	Max.	Unit
VDD	-	2.5		5.5	V
CRV step size	-	-	VDD/24	-	V
CRV output voltage absolute accuracy	-	-5	-	+5	%
Unit resistor value	-	-	2K	-	ohm

5.4.4 Specification of 10-bit SARADC

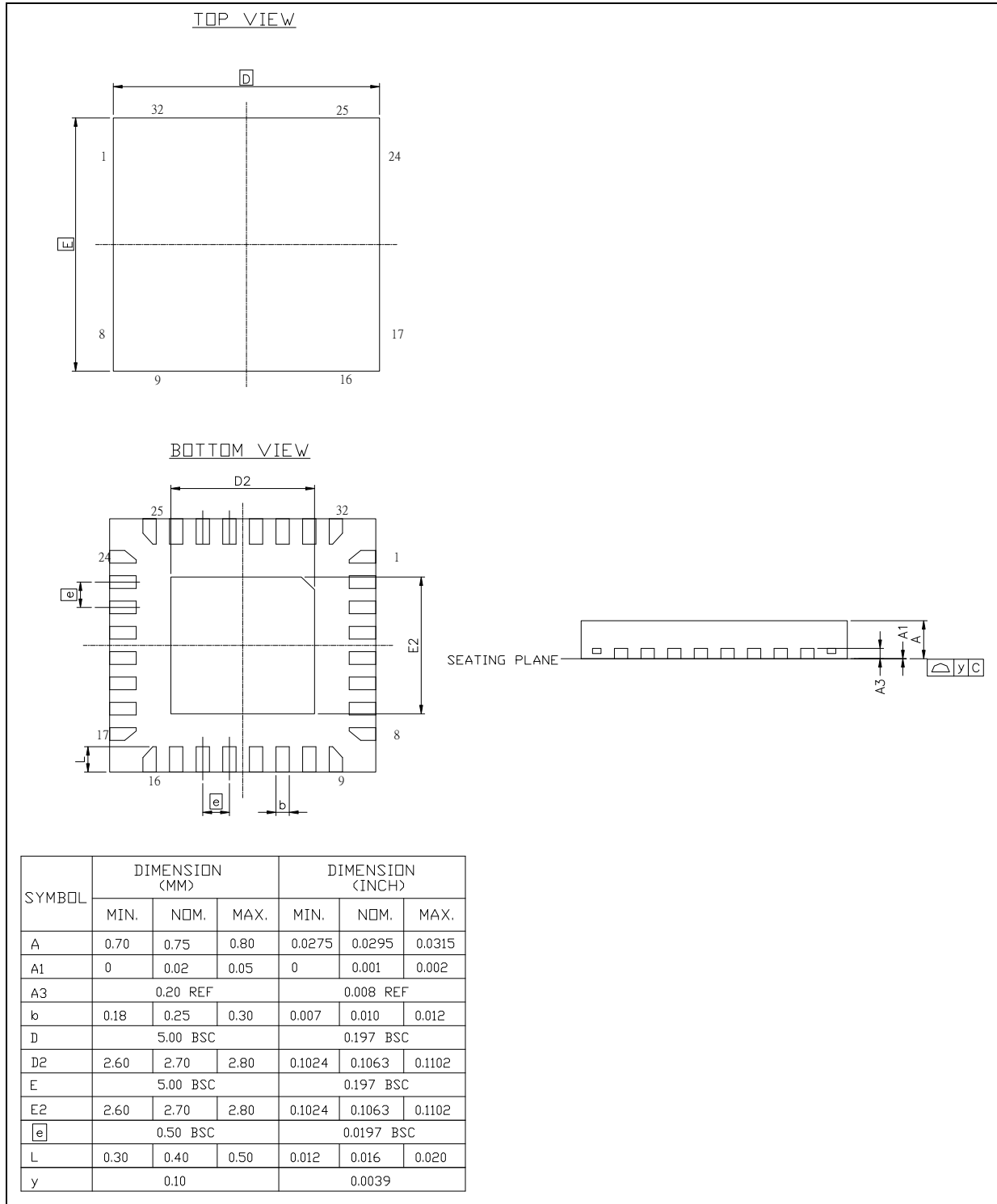
Parameter	Condition	Min.	Typ.	Max.	Unit
VDD/AVDD		2.7		5.5	V
Temperature		-40	25	85	°C
Operation Current	AVDD/VDD = 5V F _{sps} = 150K			1	mA
Resolution				10	bit
Conversion time		6.7			us
Sampling rate (F _{sps})	VDD = 5V	150K			Hz
Integral Non-Linearity Error (INL)		-1		1	LSB
Differential Non-Linearity (DNL)		-1		1	LSB
Gain error		-1		1	LSB
Offset error		TBD		TBD	LSB
Clock frequency				5.25	MHz
Absolute error		-2		2	LSB
Clock cycle		35			cycle
Band-gape		1.152	1.2	1.248	V

6 PACKAGE OUTLINE

6.1 48-Pin LQFP



6.2 33-Pin QFN





7 REVISION HISTORY

VERSION	DATE	PAGE/ CHAP.	DESCRIPTION
V0.1	Feb 10, 2011	-	Initial issued

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