OptiMOS^{TM} Technology

Zhou Ryan

Power Management & Supply Discretes

Infineon Technologies China

Contents

- Requirements for state-of-art MOSFET
- Chip technology
- Package technology

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Requirement of MOSFET at SMPS

- High power density
- High efficiency
- Best cost performance

Die technology

Package

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R_{dson} distribution

Resistance distribution for OptiMOS™ and CoolMOS™ in TO-220 and SSO8

Relative Contribution to total resistance

100%
90%
80%
70%
60%
50%
40%
30%
20%
10%
0%

30V | 30V | 600V

silicon
packaging
2mOhm
silicon
packaging
V_{ds} depending resistance
→ 'silicon limit'
99mOhm
silicon
packaging

Substrate
Epi
Channel
Bond-wires/Clip
Metallisation
Drain-pin
Source-pin

OptiMOS™3
30V in SSO8

OptiMOS™3
30V in TO-220

CoolMOS™
600V in TO-220

- Packaging is crucial for LV MOSFETs
- Epi resistance ~ $V_{ds}^{2.5}$ (silicon limit) → dominating at higher V_{ds}

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Requirement for MOSFET

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Beyond the silicon limit

OptiMOS™

CoolMOS™

normalized on-resistance

Si-limit in TO-220

Si-limit in SuperSO8

Si-limit (die)

Iinfineon-products

0 20 40 60 80 100 120 140 160 600 800 1000

breakdown voltage [V]

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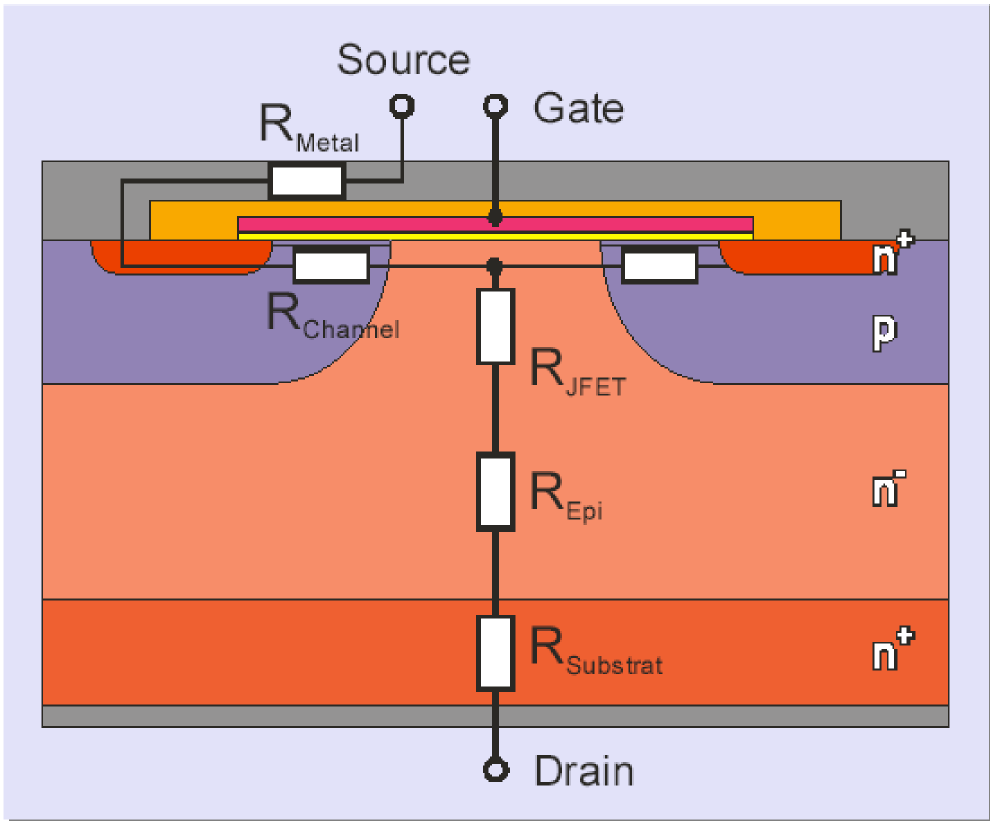
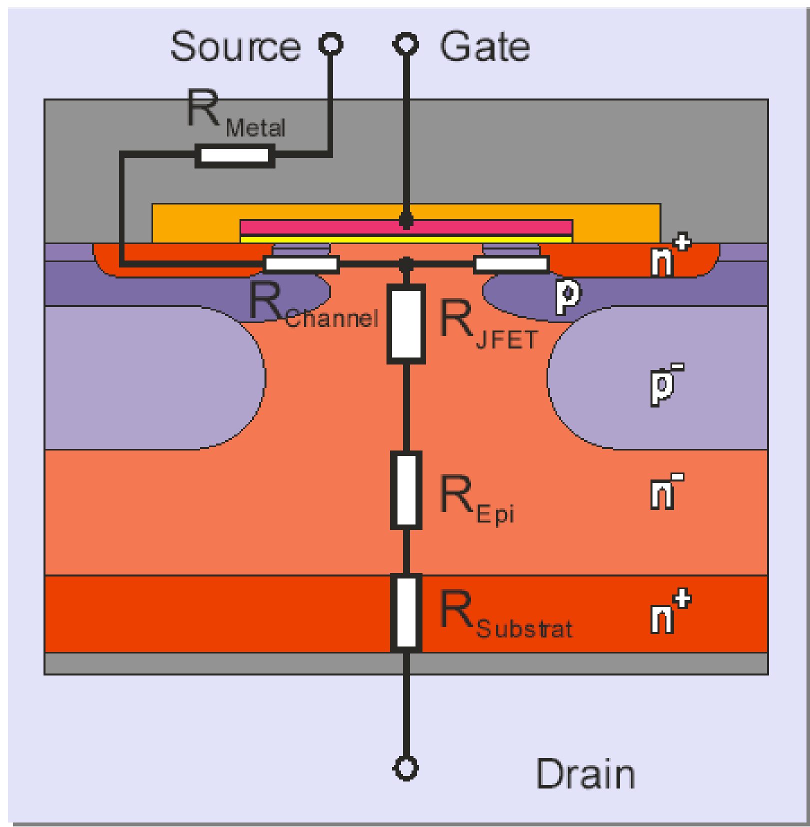
Development of LV MOSFET structure - I

Planar



Advanced planar



Improved

- $R_{Channel}$
- R_{JFET}
- R_{Epi}

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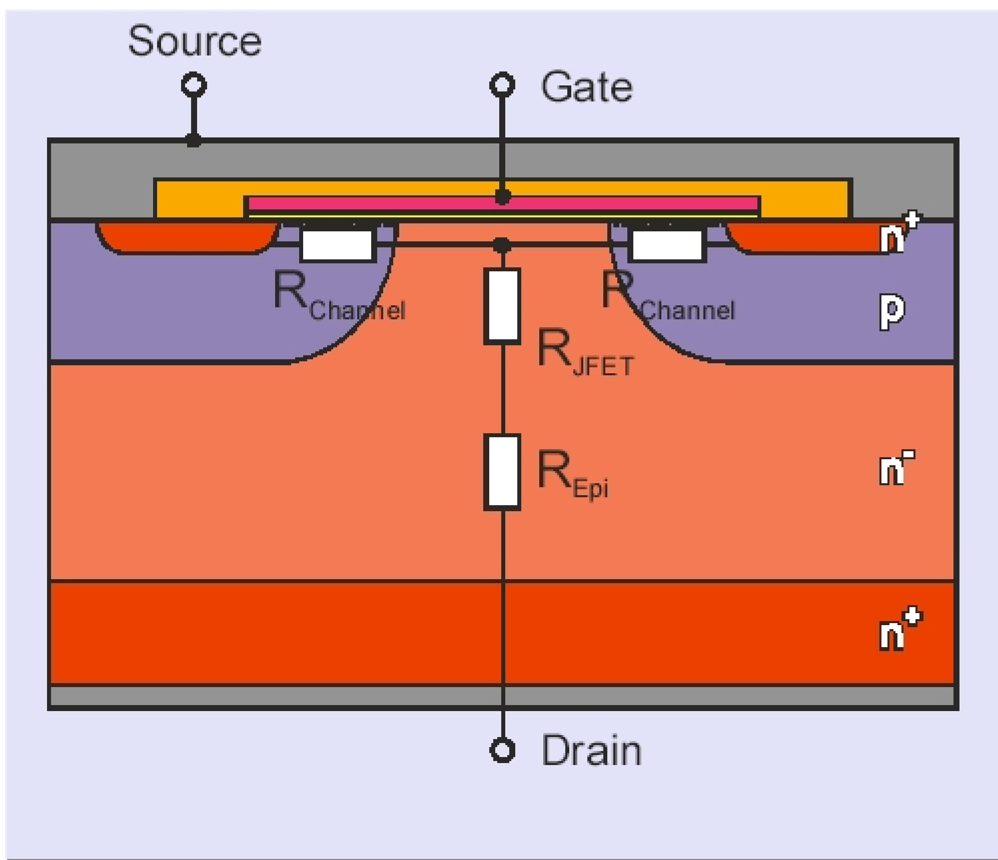
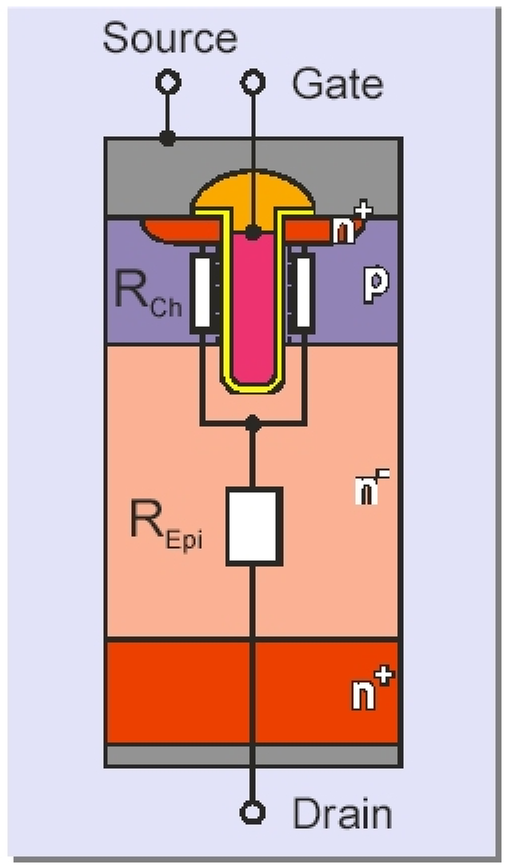
Development of LV MOSFET structure - II

Planar



Trench



- No R_{JFET}
- Lower $R_{Channel}$

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Development trend of LV MOSFET

Infineon Silicon Technology Achievements (30 V)

FOM [mOhm*nC]

1000
100
10

● Ron10 (max) * Qg4.5 (typ)
● Ron10 (max) * Qgd (typ)

SIPMOS
OptiMOS
OptiMOS 2
OptiMOS 3

-53%
-40%
-25%
-63%
-66%
-44%

1994 1996 1998 2000 2002 2004 2006 2008

year of release

With new OptiMOS 3 technology IFX is setting a new benchmark in terms of technology performance!

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Requirement for MOSFET

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Semiconductor's Package Function

1.Electrical

connect the die to the external circuit

2.Thermal

remove heat that the die dissipate

3.Mechanical

protect the die from contaminants and mechanical abuse

Mold compound
Bond wire
Lead mounting
Die
Dimensions:
10.54 mm x 29.33 mm x 4.57 mm

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LV-MOS packaging

- for LV-MOS technologies:

$$R_{package} \sim R_{silicon} \; !$$

- choosing the package is critical

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Package contribution to $R_{ds(on)}$ for Best-in-Class devices

90%
80%
70%
60%
50%
40%
30%
20%
10%
0%

30V
60V
80V
100V
150V

TO-220
D2-Pak
D2-Pak 7pin
SuperSO8
CanPAK M *
S3O8
CanPAK S *

high package contribution, Si technology is **hindered by package**

* without layout contribution

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Package development

SuperSO8	S3O8	D²PAK-7Pin	CanPAK™
	3.3 mm 3.3 mm		Can size M Can size S

*DirectFET(R) is a trademark of international rectifier corporation; DirectFET(R) technology is licensed from international rectifier corporation

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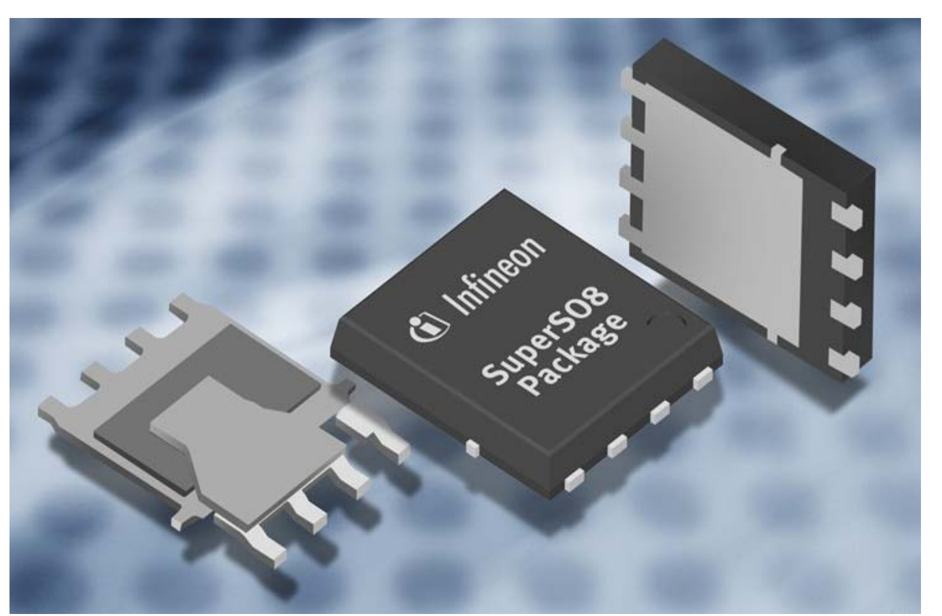
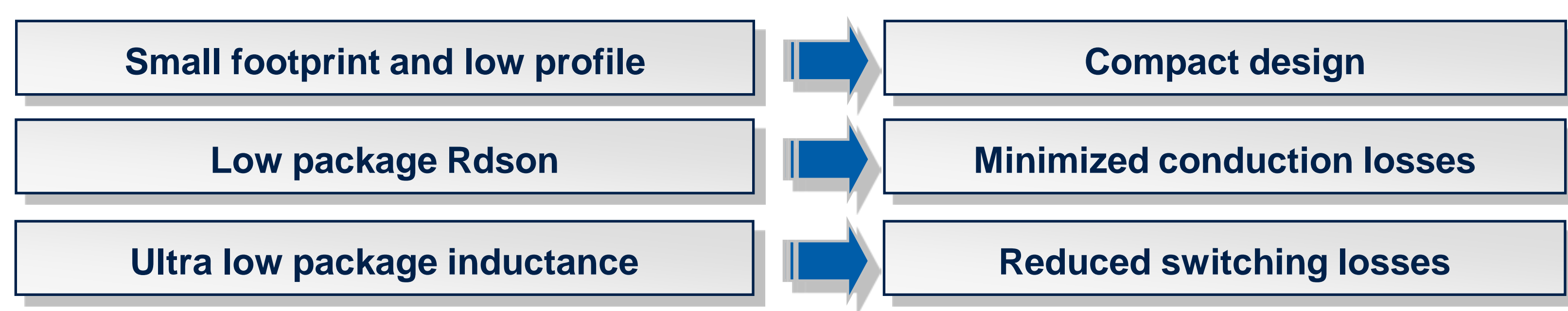
The SuperSO8 Package



Characteristics

U_{DS}	150V
I_D max	50 A
$R_{package}$	0.2 mΩ
R_{thjc}	1 K/W
$T_j$max	150°C

Package optimized for highest power density.



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S3O8 (Shrink Super SO8)
---highest power density on 11mm²

32mm²
5.15×6.15mm

11mm²
3.3×3.3mm

SuperSO8

S3O8

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S3O8 packaging technology

leadless package

•leads do not stand out over mold compound

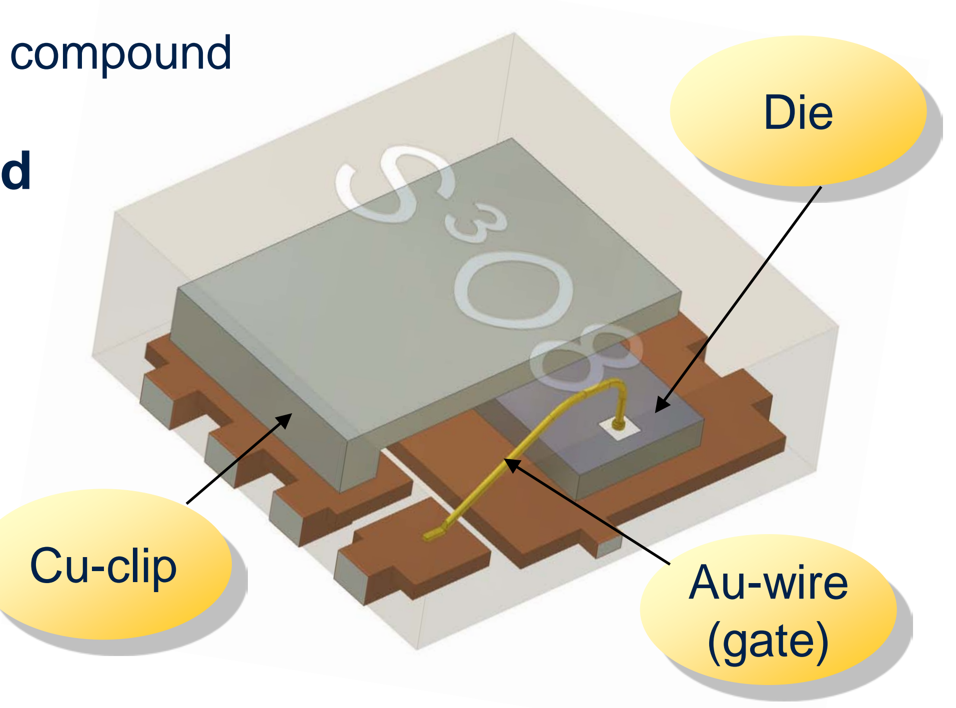
clip technology with soldered interconnect

•lowest $R_{ds(on)}$ possible

•lowest package-inductance

•high current rating

•least influence of package on device performance



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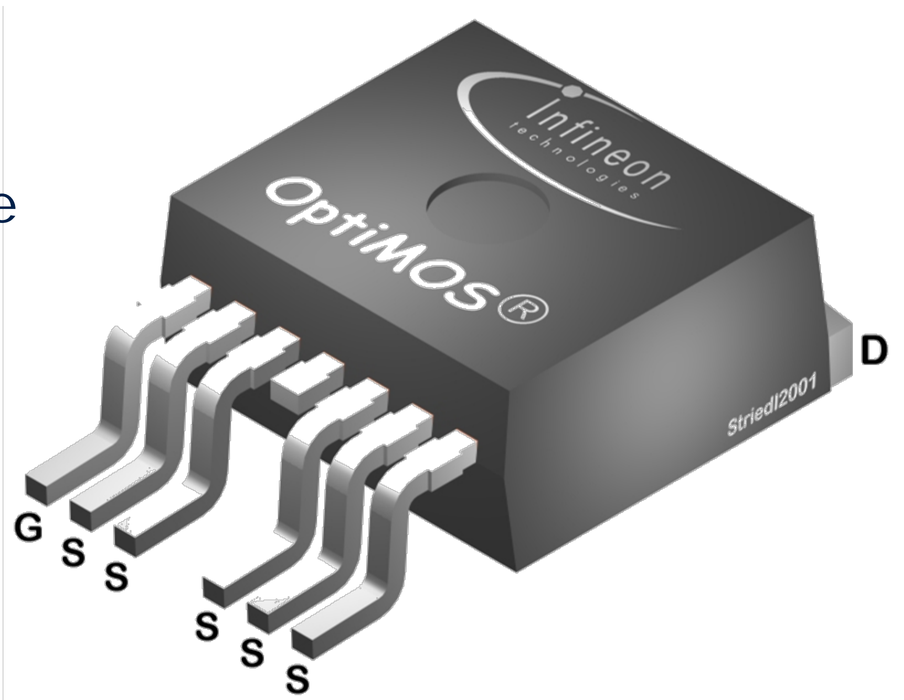
D²-Pak 7Pin packaging technology

Size
- standard D²-Pak(TO263) size

Interconnect
- up to 4*500um Al-bondwire
- <0.5mOhm package resistance

Electrical performance
- up to 180A I_d-dc

Reliability
- very low R_{th}
- large source connection
- no hot spot on source leads



Best for OringFET Application

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Best-in-class $R_{ds(on)}$ in LV-MOS

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Parameter comparison of packages

Package Type	Inductance	Resistance	Top side cooling	Bottom side cooling	Parallel difficulty
DPAK	3.8nH	0.5mΩ	No	Yes	Normal
SO8	1.5nH	2.3mΩ	Limited	No	Normal
SSO8	0.6nH	0.2mΩ	Limited	Yes	Normal
S3O8	0.5nH	0.3mΩ	Limited	Yes	Easy
CanPAK SQ	0.3nH	0.2mΩ	Yes	Yes	Easy
CanPAK MX	0.3nH	0.2mΩ	Yes	Yes	Easy

- **Package resistance not neglectable of total Rdson.**
- **Package inductance have great influence on switching speed and voltage spike.**

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Parameter comparison of packages

	SO8	SSO8	S3O8	CanPak SQ	CanPak MX	Dpak
length×width (mm^2)	4.9×6.0	5.15×6.15	3.3×3.3	4.8×3.8	6.3×4.9	6.1×6.5
height (mm)	1.75	1.00	1.00	0.65	0.65	2.30
P_D[Tc=25˚C] (W)	4	125	70	40	90	90
P_D[Ta=25˚C,6cm^2 copper] (W)	1.56	2.50	2.10	2.2 6.3*	2.8 6.3*	3.00
I_D[Tc=25˚C] (A)	20	100	40	60	100	90
I_D[Ta=25˚C,6cm^2 copper] (A)	15	30	20	15 20*	30 50*	30
Rthja (K/W)	80	50	60	58 20*	45 20*	50
Rthjc[for SO8 Rthjs] (K/W)	30.0	1.0	1.8	1.4	1.4	1.6
Tj max (˚C)	150	150	150	150	150	170
Rdson (mOhm)	5.2 - 20	1.4 - 12	3.5 - 13	4.9 - 7.7	1.9 - 4.9	3.1- 13.5
package inductance (nH)	1.5	0.6	0.5	0.3	0.3	3.8
package resistance (mOhm)	2.3	0.2	0.3	0.2	0.2	0.5
top side cooling	no	limited	limited	yes	yes	no
bottom side cooling	no	yes	yes	yes	yes	yes
paralleling/routing	standard	standard	standard	easy	easy	standard

*top side cooling

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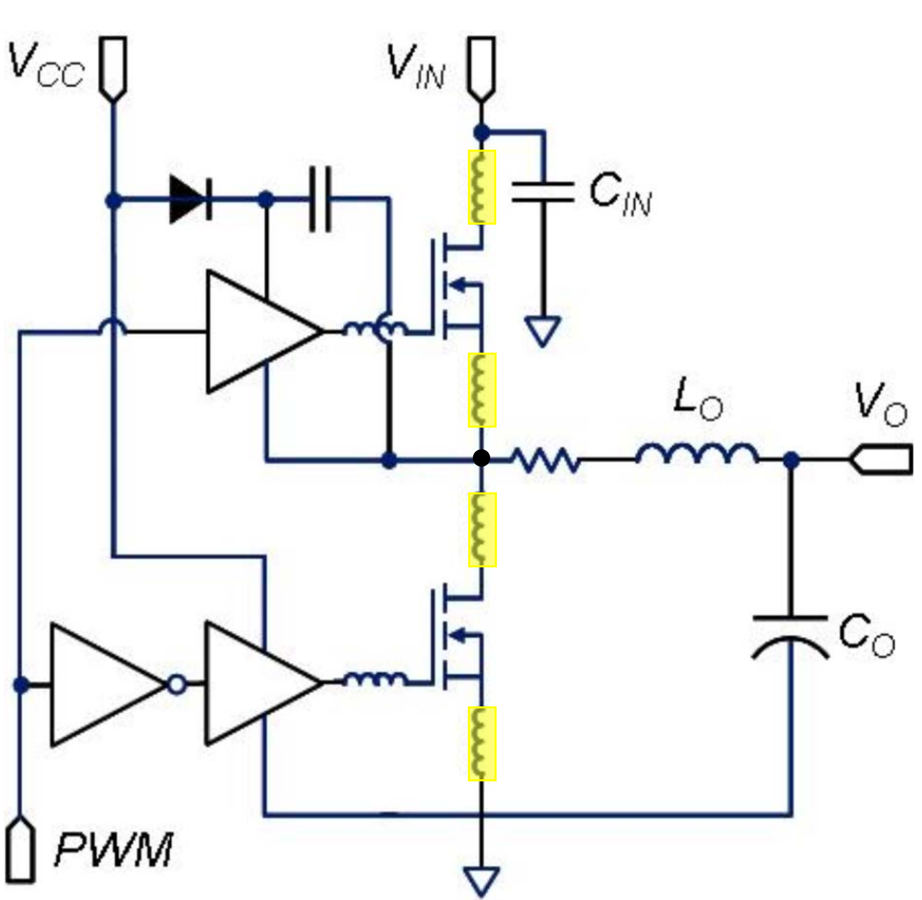
Influence of parasitic inductance



- Increase voltage spike
- Increase power loss

$$P = f_{sw} \times E_{stray} = f_{sw} * 1/2 * L_{stray} * I^2$$

- L_{stray}: total parasitic inductance, package as well as layout route

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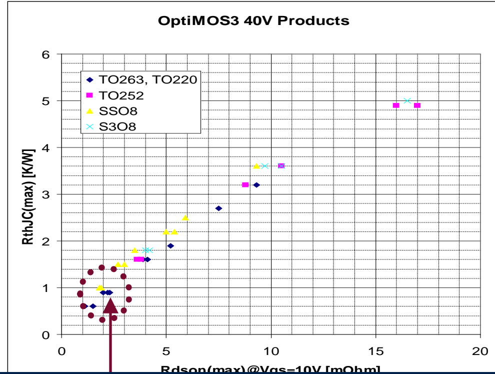
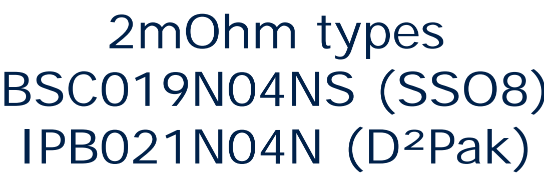
Z_{thjc} comparison ---SSO8 vs. D²Pak





- D²Pak has larger Cu-leadframe than SSO8
  - 10% better Rth
  - 20% better Zth for tpulse between 10ms and 100ms

Zth single pulse

Zth [K/W]: 1, 0.1, 0.01

t pulse [s]: 0.00001, 0.0001, 0.001, 0.01, 0.1, 1, 10

D²-Pak
SSO8

thicker leadframe improves Zth for pulses (10ms – 100ms)

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Comparison Thermal Behavior 35µm PCB

D²Pak-7 | D²Pak | SSO8

85,0°C – 30,0°C

Same Silicon Content on each board!

Simplified schematics

V_{Cu1} R_{Cu1}

V_{MOSFET} R_{Mosfet}

V_{Cu2} R_{Cu2}

	Voltage Drop @ 78A [mV]		
	D²Pak-7	D²Pak	SSO8
V_{Cu1}	7	7	7
V_{MOSFET}	25	32	25
V_{Cu2}	9	11	20

SSO8:
Same Voltage Drop as D²PAK-7

Due to longer trace Mosfet→Screw

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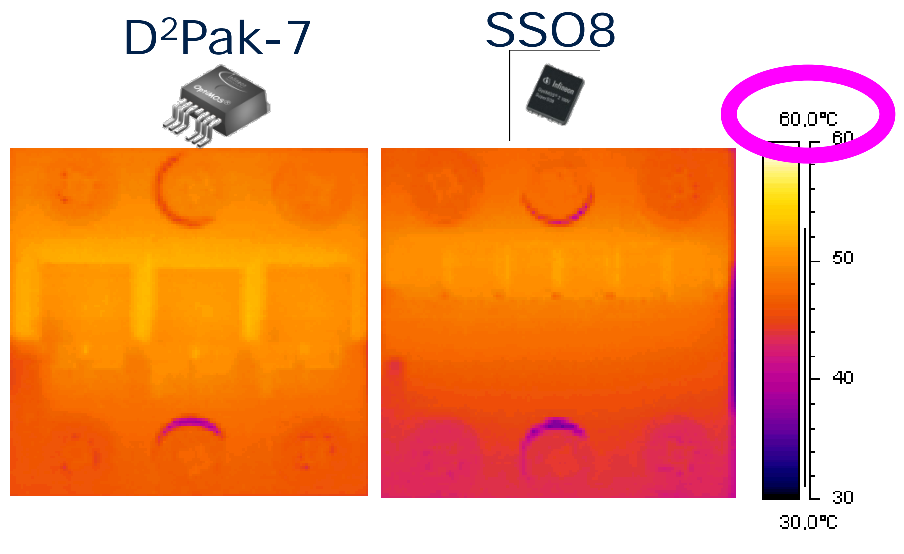
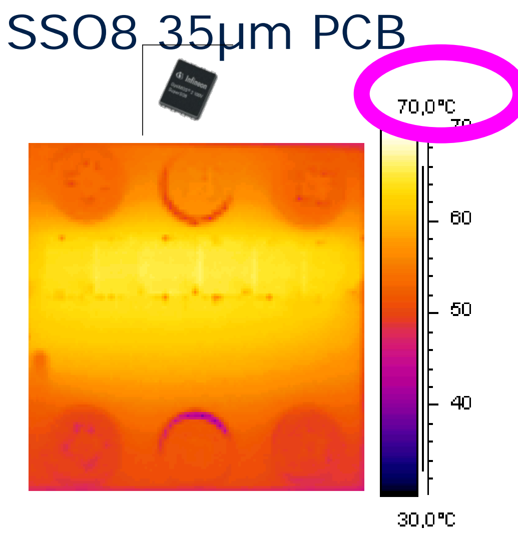
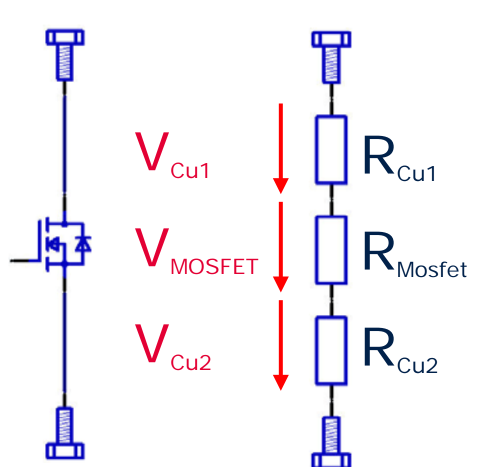
Comparison Thermal Behavior 125µm PCB







	Voltage Drop @ 78A [mV]		
	D²Pak-7 125µm	SSO8 125µm	SSO8 **35µm**
V_{Cu1}	3.6	3.4	5.2
V_{MOSFET}	23.8	22.7	24.0
V_{Cu2}	3.7	7.0	18.4

SSO8 on 125µm: even better than D²Pak-7

Due to longer trace Mosfet→Screw

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We partner.
We create value.