CoolMOS^{TM} Introduction and Datasheet understanding

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Never stop thinking

Introducing CoolMOS™

Datasheet Understanding

- Introducing CoolMOS™

- Datasheet Understanding

CoolMOS^{TM} Series & History

S5 series: the first series of CoolMOS™, market entry in 1998 slow switching, close to conventional MOSFET, Vth 4.5 V, gfs low, Rg high design-in in high power SMPS only

C3 series: the third series of CoolMOS™, market entry in 2001 the „working horse“ of the portfolio, fast switching, symmetrical rise/fall time @10 V Vgs, Vth 3 V, gfs high, Rg very low design-in into all CoolMOS™ segments

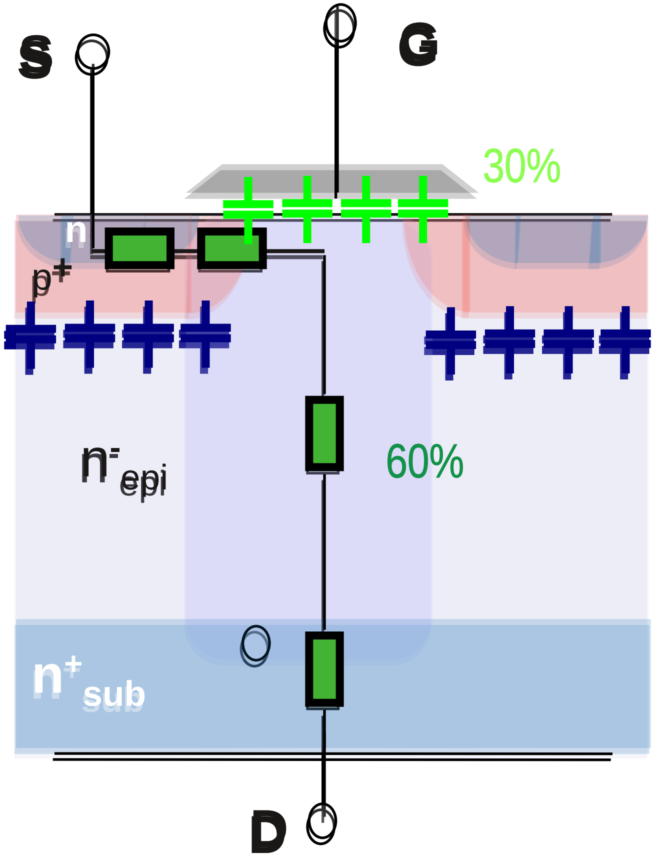
CFD series: the fourth series of CoolMOS™, market entry in 2004, fast body diode, Qrr 1/10th of C3 series, Vth 4 V, gfs high, Rg low pecific for phase-shift ZVS and DC/AC power applications

CP series: the fifth series of CoolMOS™, market entry in 2005, ultra low Rdson, ultra low gate charge, very fast switching Vth 3 V, gfs very high, internal Rg very low

C6/E6 series: the sixth series of CoolMOS^{TM}, launched in 2009 and 2010 respectively as the sixth CoolMOS™ technology is planned to be the successor of C3

CFD2 series: the new technology CoolMOS™ of the successor of CFD, lower Qrr and trr, will come at the begin of 2011

Roadmap of HV MOSFET



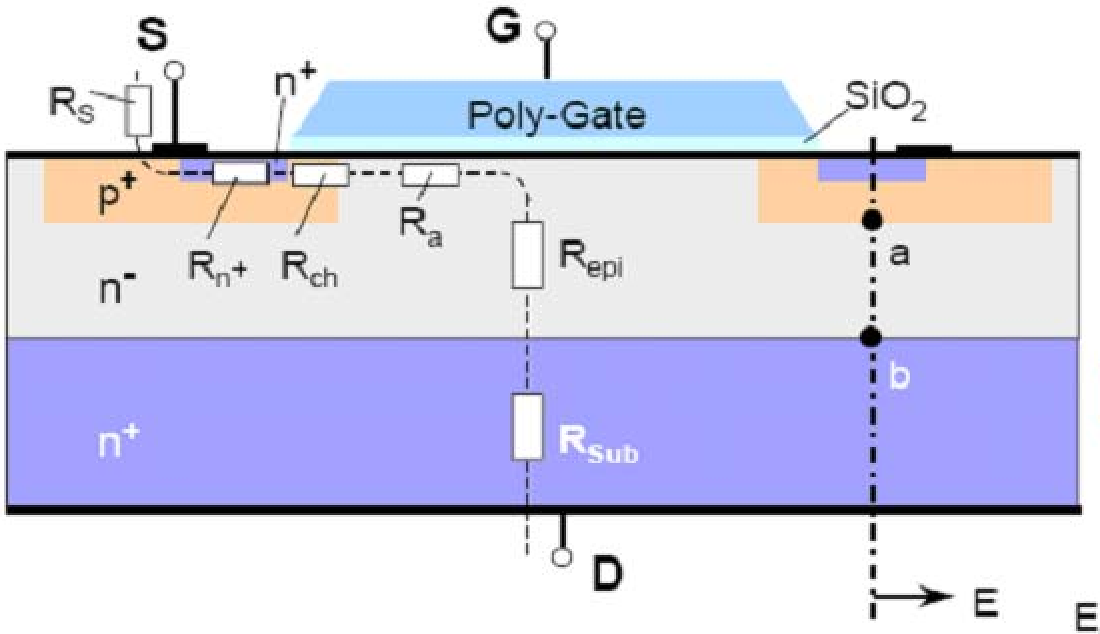
Losses come from

1. *Rdson: 60% conduction loss*
2. *Delay in on/off (Qg..):30% switching loss*
3. *(Dis)Charge Cds Cap.: 10% C_{oss} loss*

To make it better:

1. *Better conductivity ➔Lower Rdson*
2. *Faster switching ➔ lower Qg*
3. *Lower capacitances➔Lower Coss,etc*

Resistance –Rdson, distribution of MOSFET

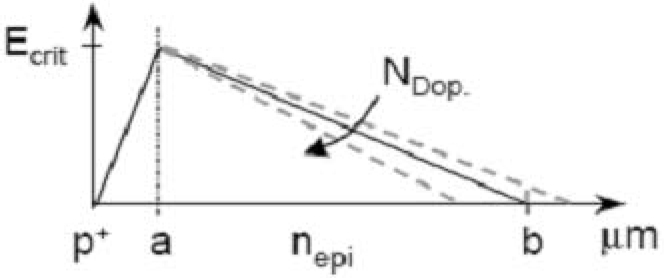


$R_{DS(on)}$

$V_{DS} \approx 30V$		$V_{DS} \approx 600V$	
R_S^*	≈ 7%	R_S	≈ 0.5%
R_{n^+}	≈ 6%	R_{n^+}	≈ 0.5%
R_{ch}	≈ 28%	R_{ch}	≈ 1.5%
R_a	≈ 23%	R_a	≈ 0.5%
R_{epi}	≈ 29%	R_{epi}	≈ 96.5%
R_{Sub}	≈ 7%	R_{Sub}	≈ 0.5%

R_S^* = packaging

$$R_{DS(on)} \sim V_{BR(DSS)}^{\;2.4 \ldots 2.6}$$

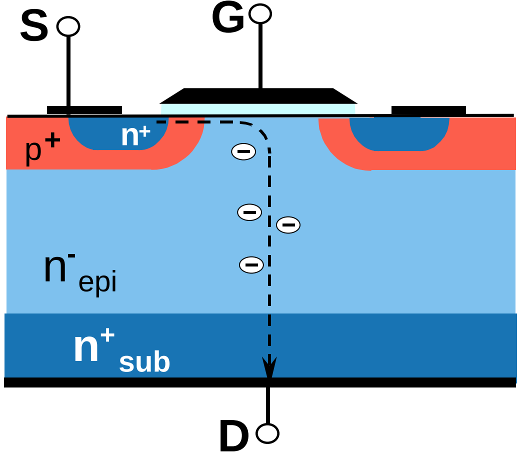


96.5% of $R_{DS(on)}$ for high voltage standard MOSFET determined by the epitaxial resistance

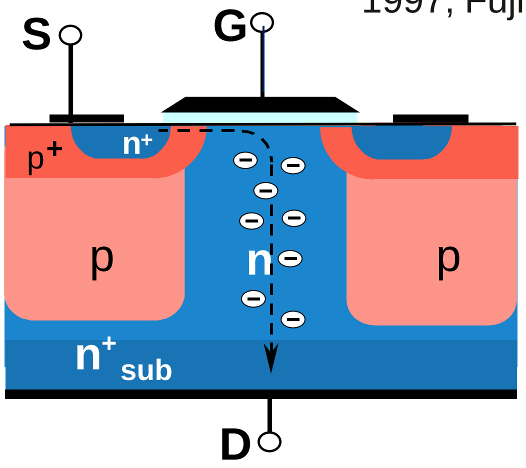
Super Junction Theorem

Power MOSFET | **Cool MOS ™**

1987,Chen Ming-Hu, China

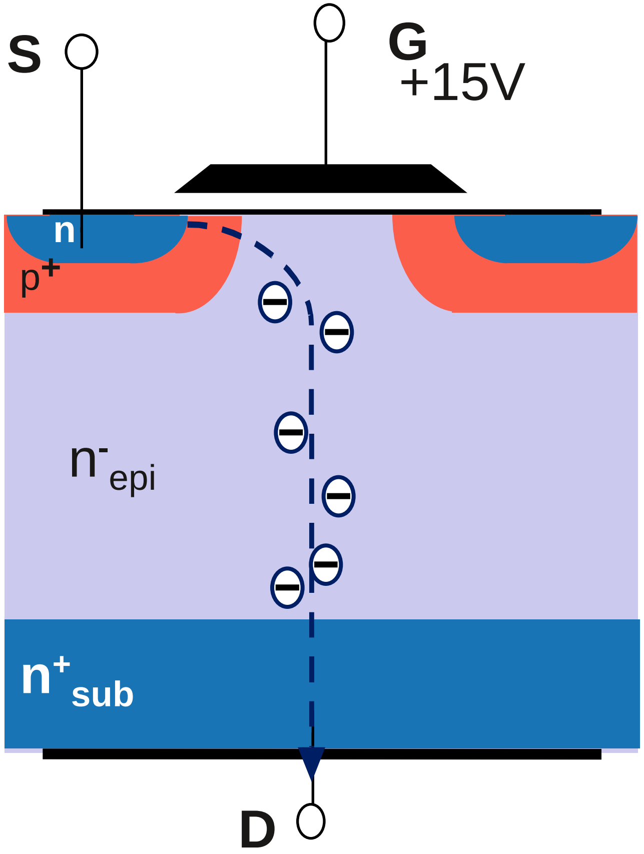


1997, Fujihira, Japan

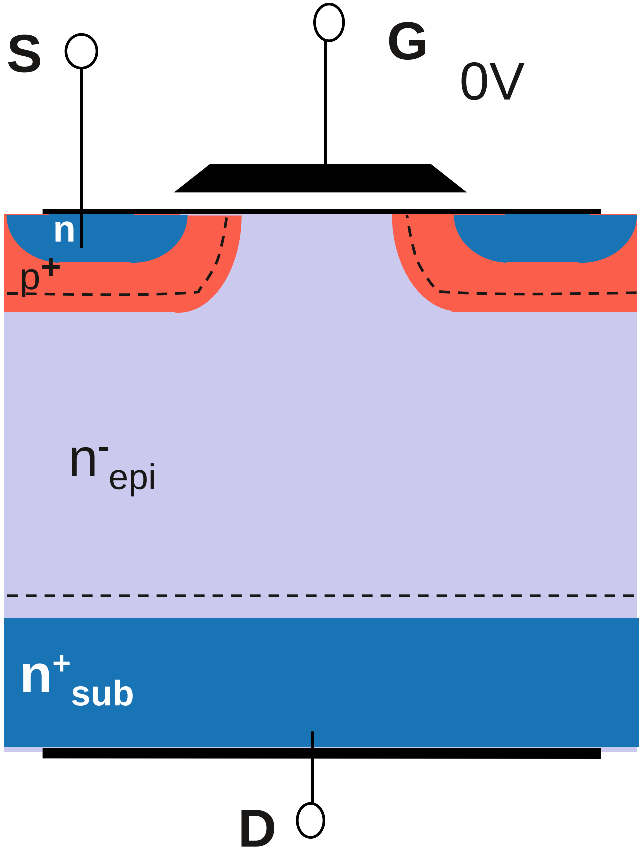


- By controlling the degree of doping and the thickness of these layers, according to the SJ theory, this structure operates as a pn junction with low on-resistance and high breakdown voltage.

Standard MOSFET operating principle

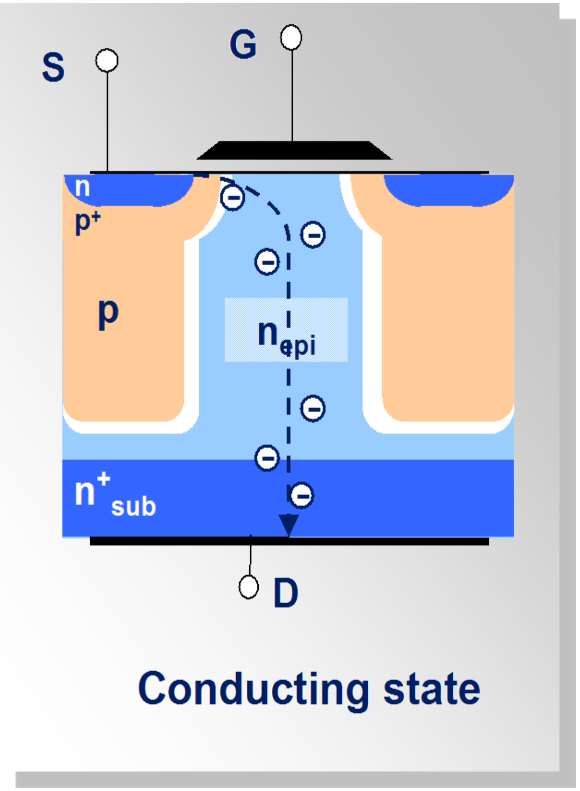


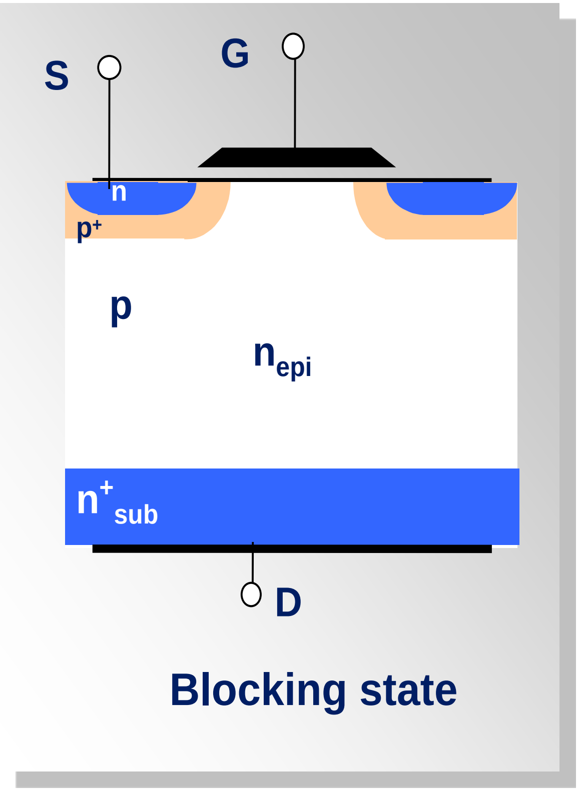
Conducting state



Blocking state

CoolMOS operating principle





Higher doped columns act like a „short“ across the drift region

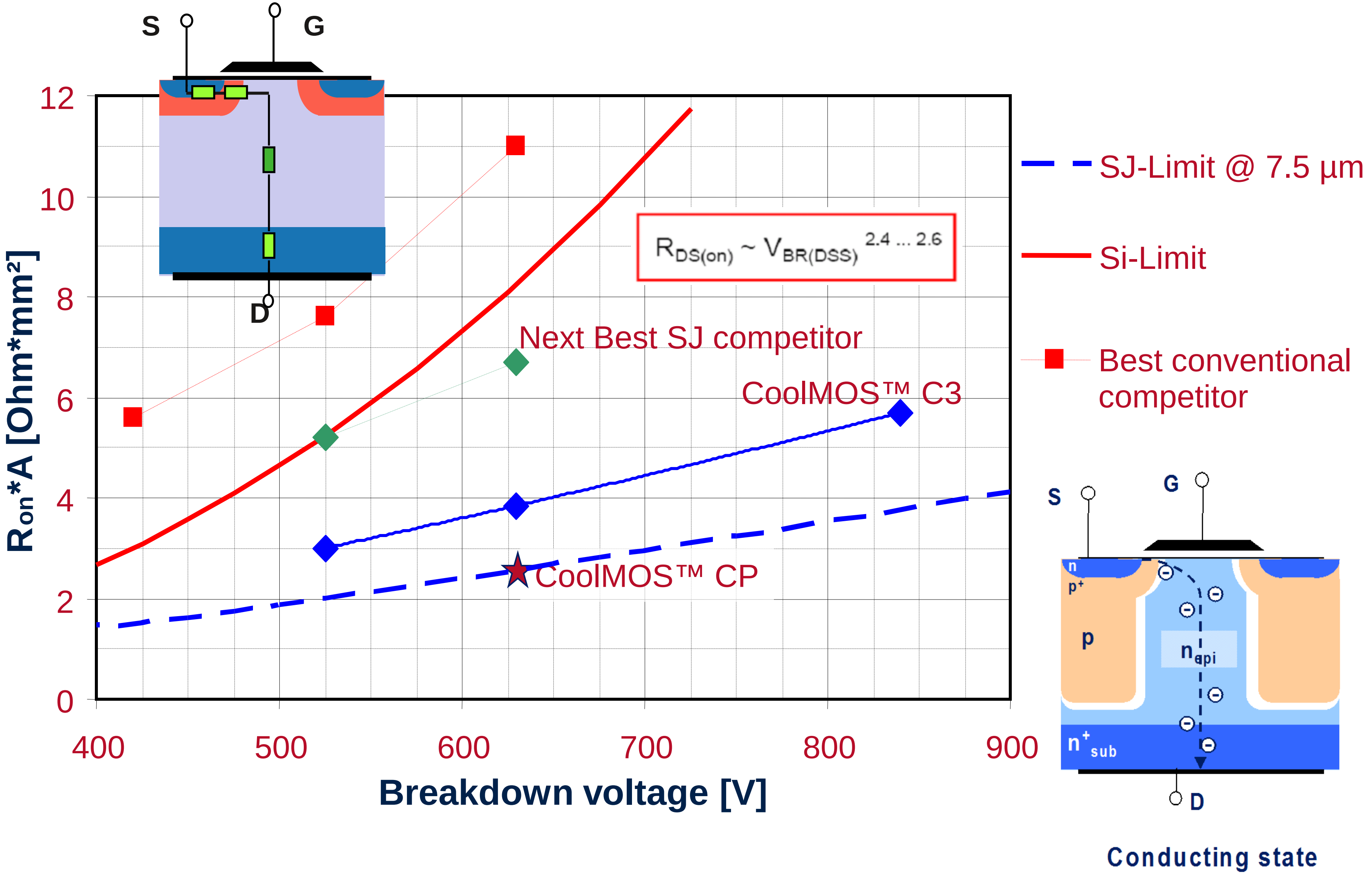
⇨ extremely low RDSon

With applied V_{DS}, the space charge region extends across the entire epi-layer

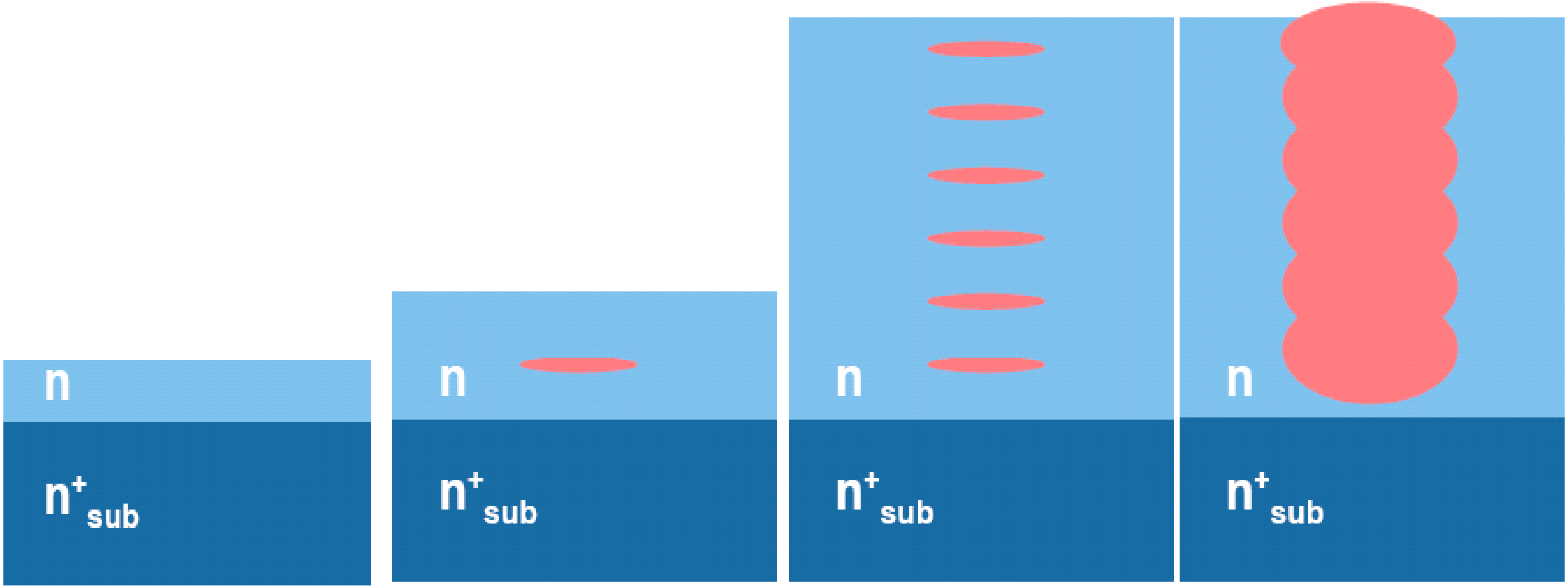
⇨ very low effective doping

⇨ high breakdown voltage

CoolMOS : Lowest area-specific Rds(on)



CoolMOS
basic manufacture process



Substrate wafer,
first epitaxial layer

Boron-I,
deposition
of epi layer

Subsequent
implantation
and epi steps

Diffusion
and cell
technology

Introducing CoolMOS™

Datasheet Understanding

Current & Ptot
---IPW60R041C6 as example

- Current is **calculated** base on Tjmax, Rdson@Tjmax, Rth(jc)!

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current[1)]	I_D	-	-	77.5	A	T_C= 25 °C
				49		T_C= 100°C

$$\left.\begin{aligned} P_{tot} &= R_{on(@Tjmax)} * I^2 \\ P_{tot} * R_{thJC} &= T_{jmax} - T_c \end{aligned}\right\} I = \sqrt{(T_{jmax} - T_c)/R_{on(@Tjmax)}/R_{thJC}}$$

That's why we just put Rds(on) not Id into P/N naming: IPW60R041C6

- Ptot calculated as well:

Power dissipation	P_{tot}	-	-	481	W	T_C=25 °C

$$Ptot = (Tjmax - 25) / Rthjc$$

Junction temperature

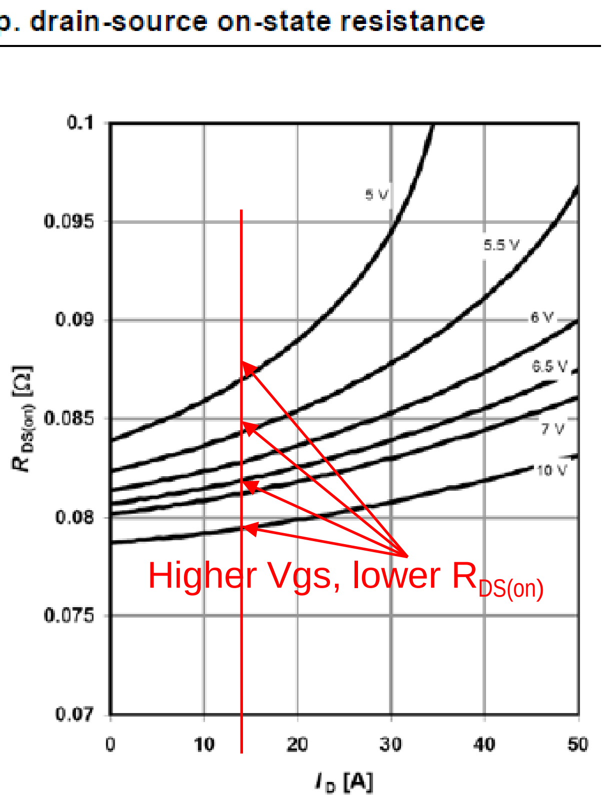
- **Never** exceed Tj max (150 / 175 deg C) at operation, otherwise, will cause MOSFET failure.

Operating and storage temperature	T_j, T_{stg}		-55 ... 150	°C

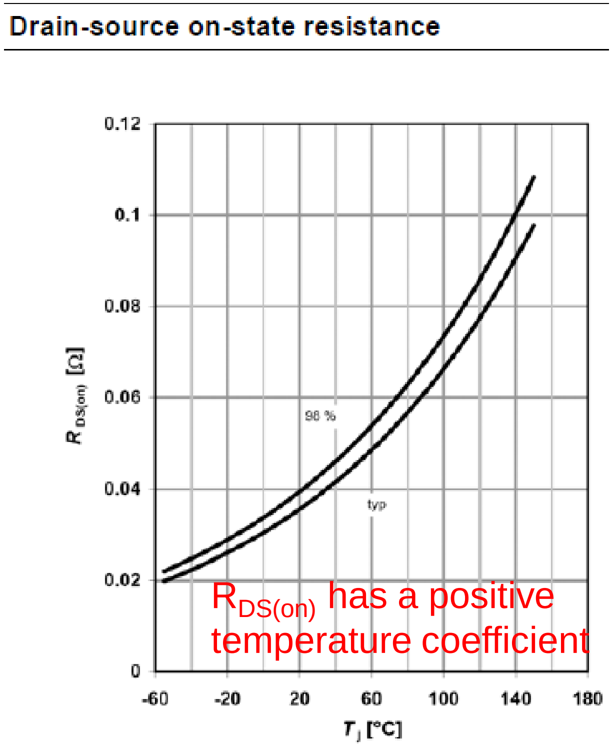
Current & Ptot
---IPW60R041C6 as example

Drain-source on-state resistance	$R_{DS(on)}$	-	0.037	0.041	Ω	V_{GS}=10 V, I_D=44.4 A, T_j=25 °C
		-	0.096	-		V_{GS}=10 V, I_D=44.4 A, T_j=150 °C

- ☐ Vgs level impact Rds(on)
- ☐ Tj also impact Rds(on)


Typ. drain-source on-state resistance

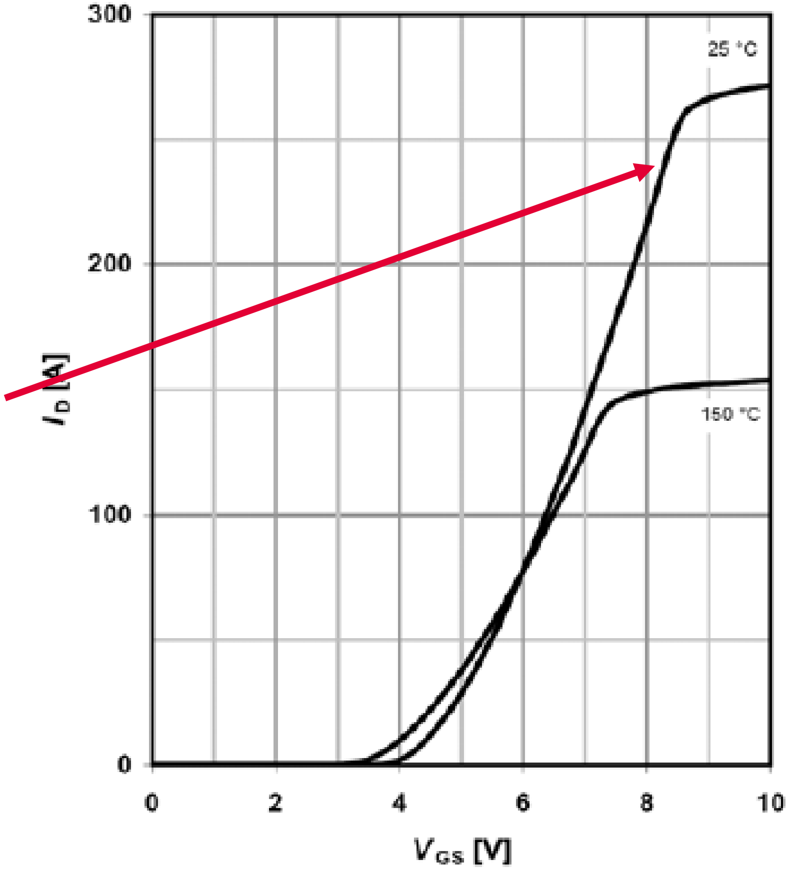
Higher Vgs, lower $R_{DS(on)}$


Drain-source on-state resistance

$R_{DS(on)}$ has a positive temperature coefficient

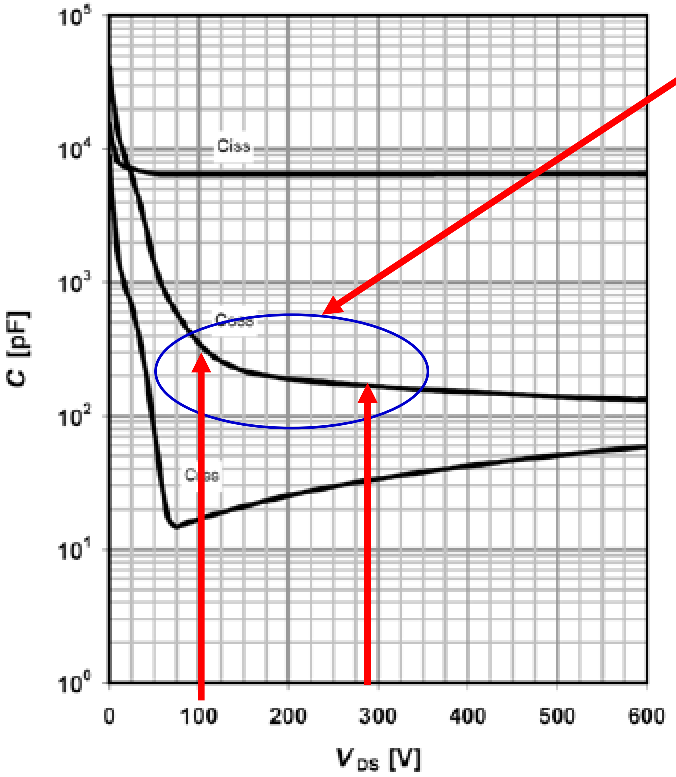
Transfer characteristics

This value is the max current capability of chip inside, which is much larger than nominal current Ids (77.5A for IPW60R041C6)



Capacitive parameters

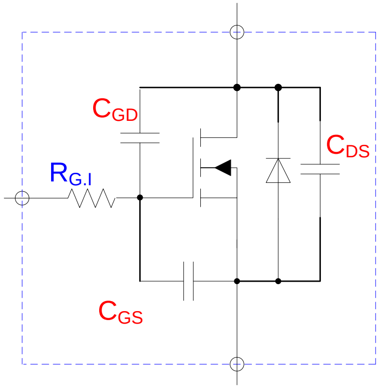
Input capacitance	C_{iss}	-	6530	-	pF	V_{GS}=0 V, V_{DS}=100 V, f=1 MHz
Output capacitance	C_{oss}	-	360	-		



C=f(V_{DS}); V_{GS}=0 V; f=1 MHz

Capacitance is not fixed !
Vary with Vds !
Not recommend for calculation

$C_{iss}=C_{GD}+C_{GS}$
$C_{oss}=C_{GD}+C_{DS}$
$C_{rss}=C_{GD}$

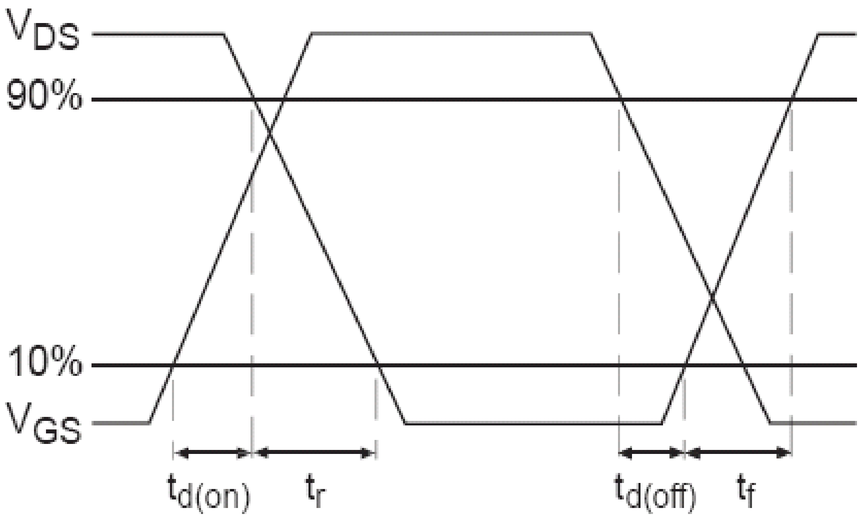


Switching time td(on) / tr / td(off) / tf

Turn-on delay time	$t_{d(on)}$	-	23	-	ns	V_{DD}=400 V, V_{GS}=13 V, I_D=44.4A, R_G= 1.7Ω (see table 16)
Rise time	t_r	-	10	-		
Turn-off delay time	$t_{d(off)}$	-	130	-		
Fall time	t_f	-	7	-		

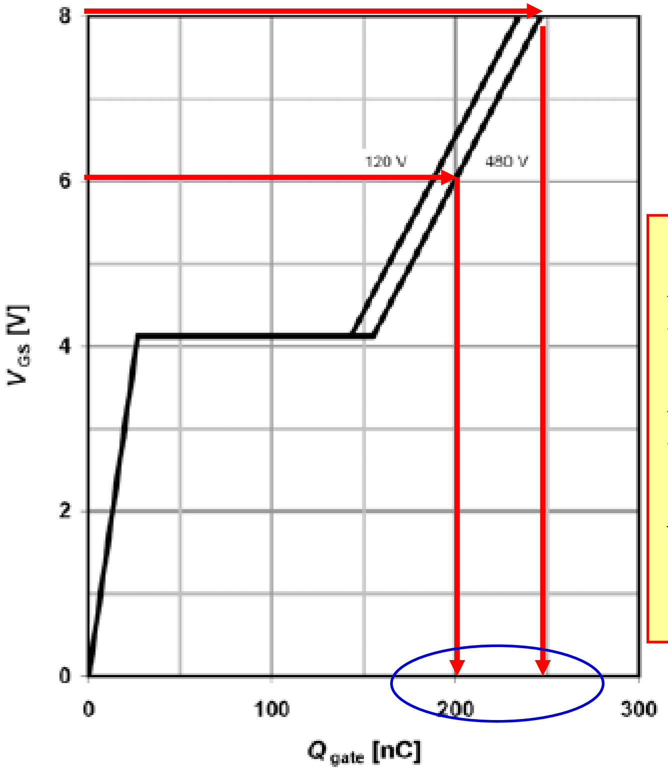
Only recommended value at giving condition

Switching time definition



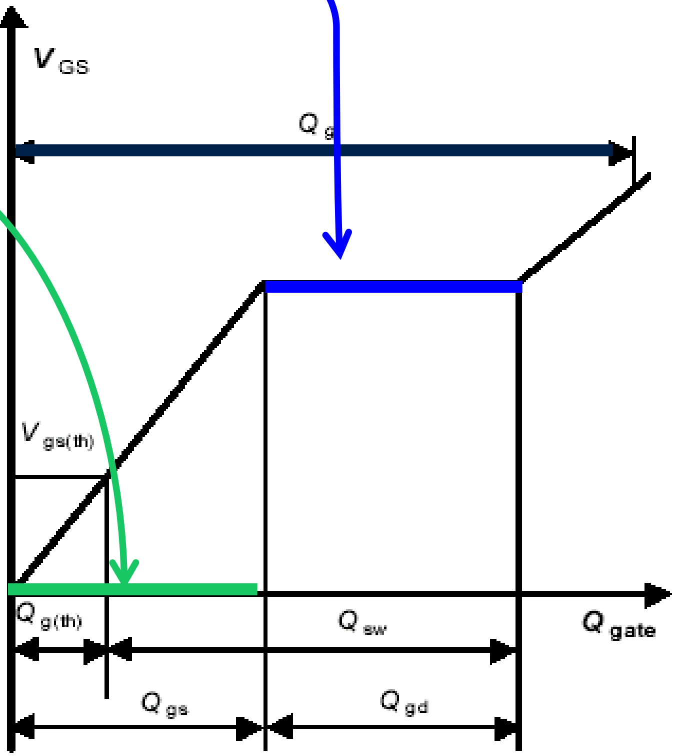
Gate charge & plateau voltage

Gate to source charge	Q_{gs}	-	36	-	nC	V_{DD}=480 V, I_D=44.4 A, V_{GS}=0 to 10 V
Gate to drain charge	Q_{gd}		150	-		
Gate charge total	Q_g	-	290			
Gate plateau voltage	$V_{plateau}$	-	5.4	-	V	



V_{GS}=f(Q_{gate}), I_D=44.4 A pulsed

- ☐ High Vgs means high Qg
- ☐ Higher Vds cause higher switching loss
- ☐ Get trade-off between Rds(on) and Qg

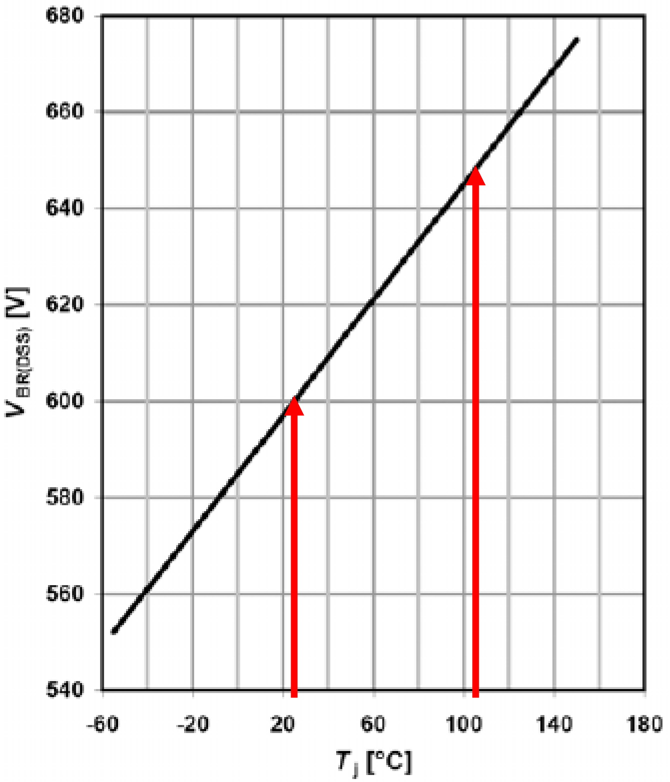


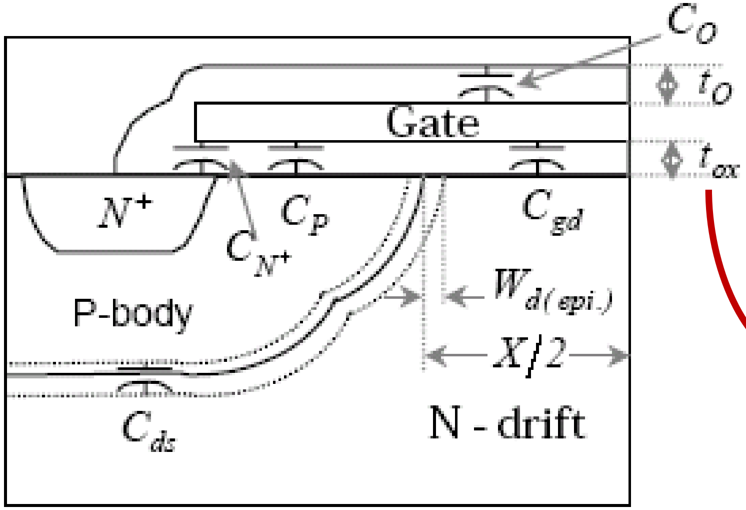
Gate charge waveforms

Breakdown voltage and Gate threshold voltage

Drain-source breakdown voltage	$V_{(BR)DSS}$	600	-	-	V	V_{GS}=0 V, I_D=0.25 mA
Gate threshold voltage	$V_{GS(th)}$	2.5	3	3.5		$V_{DS}=V_{GS}$, I_D=2.96 mA

- ☐ Vary with Junction Temperature
- ☐ Need to be derated for high reliability over years
- ☐ No exceeding !!!



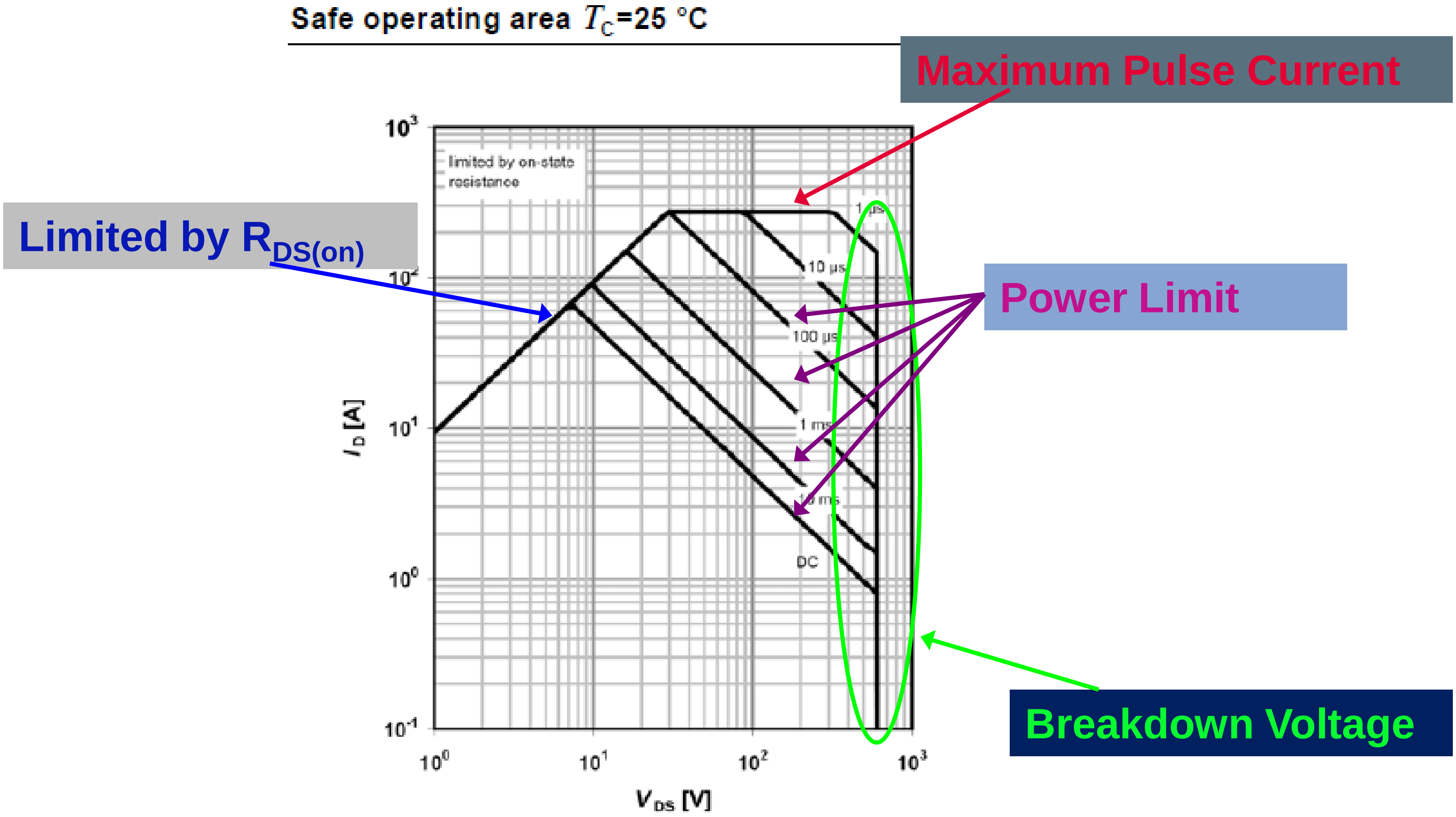


tox is proportional to Vgs(th)

for HV, Vgs(th) is designed 2~4V @25°C

for LV, Vgs(th) is designed 1~2V@25°C

MOSFET SOA



Safe operating area T_C=25 °C

Maximum Pulse Current

Limited by $R_{DS(on)}$

Power Limit

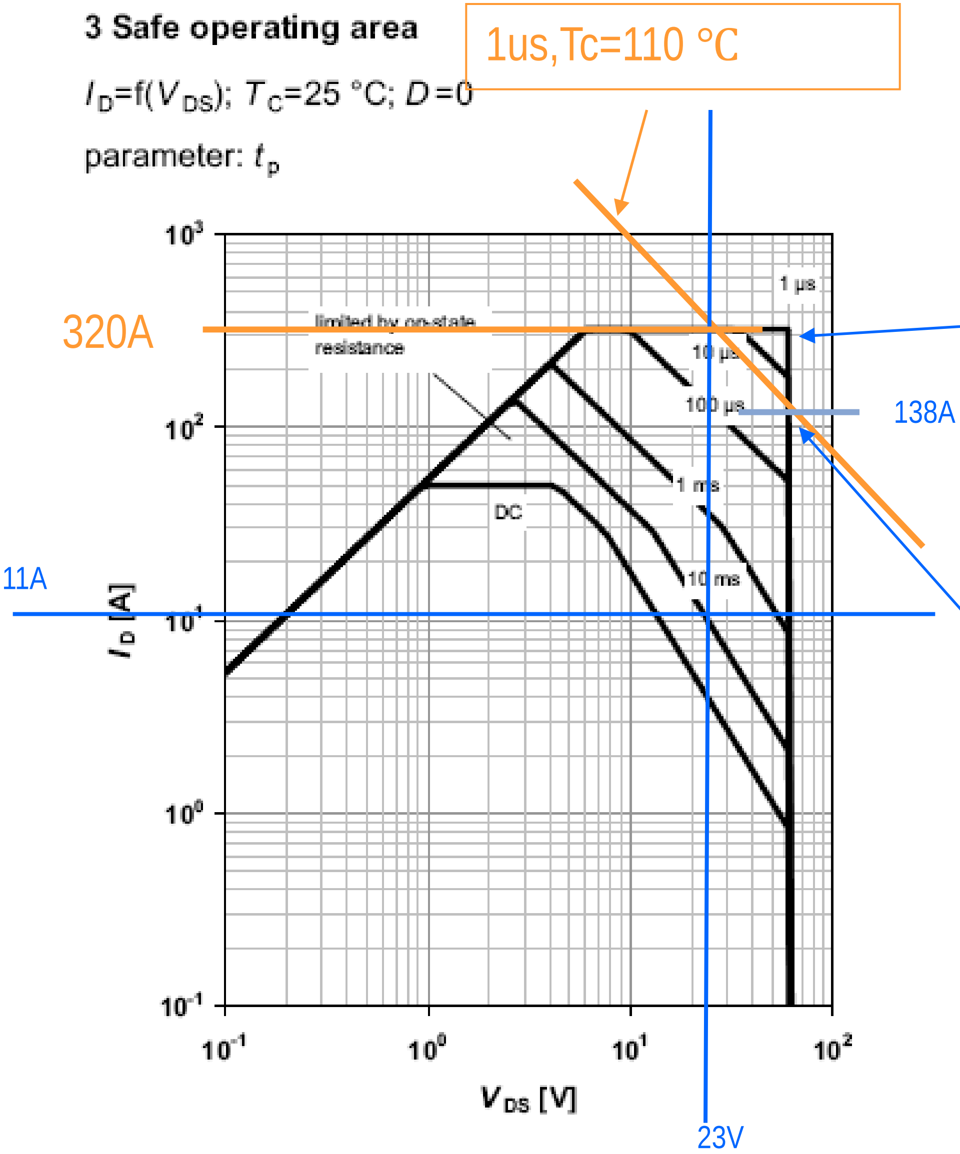
Breakdown Voltage

How to Convert 25 °C to 110 °C SOA

3 Safe operating area

$I_D=f(V_{DS})$; $T_C=25$ °C; $D=0$

parameter: t_p



Pd=V*I=60V*320A=19200

Pd@Tc=25 °C

=(Tj_max-25)/Zthjc

=(175-25)/Z=19200

We can get Z=0.0078

Pd@Tc=110 °C

=(175-110)/0.0078=8333

Id=Pd/V=8333/60=138

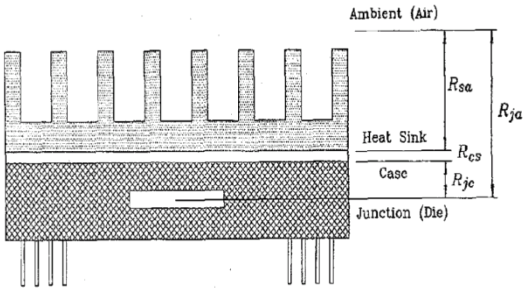
Thermal impedance

Thermal resistance, junction - case	R_{thJC}	-	-	0.26	°C/W	
Thermal resistance, junction - ambient	R_{thJA}	-	-	62		leaded

- Practically, R_{thJC} is not the key concern in the application.
- The system thermal is limited by R_{thJA}:

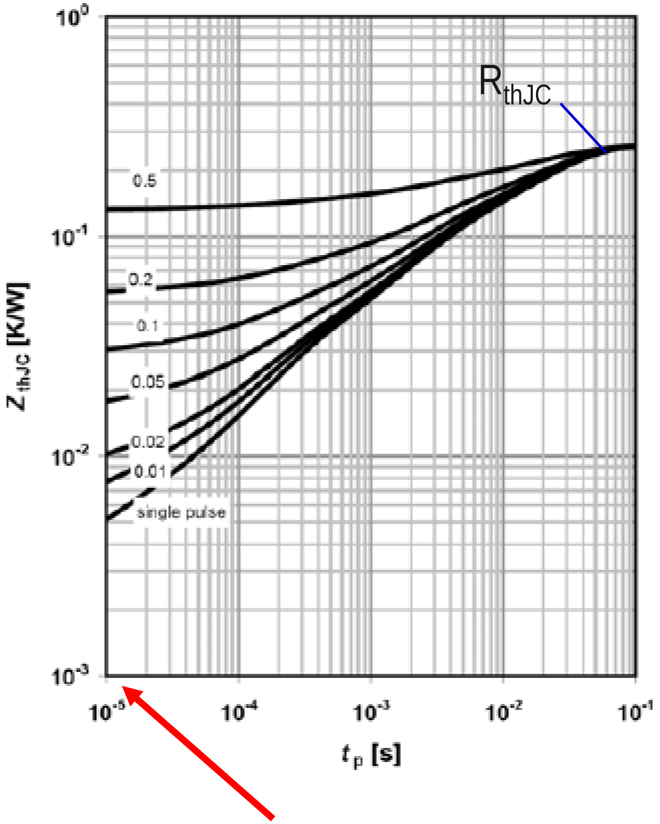
  $R_{thJA}=R_{thJC}+R_{thCS}+R_{thSA}$

  Obviously, $R_{thJA}>>R_{thJC}$
- Thermal rise: $\triangle T= P_{loss} * R_{thJA}$

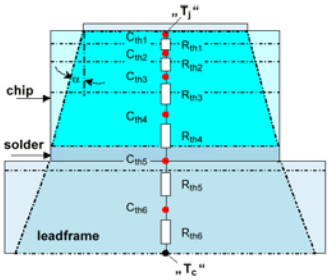


Effort should concentrated on how to reduce R_{thJA} !

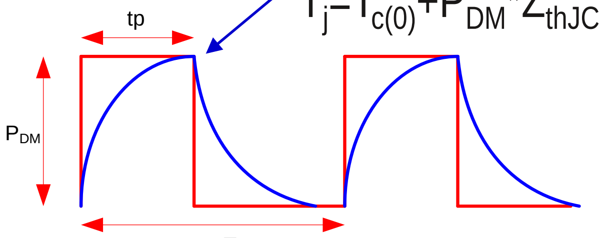
Thermal impedance



For $t_p<10^{-5}$s refer to next slide



☐ Use Z_{thJC} to calculate the instantaneous Tj
☐ With longer tp, Z_{thJC} turn to R_{thJC}
☐ Can be used directly for rectangular power curve



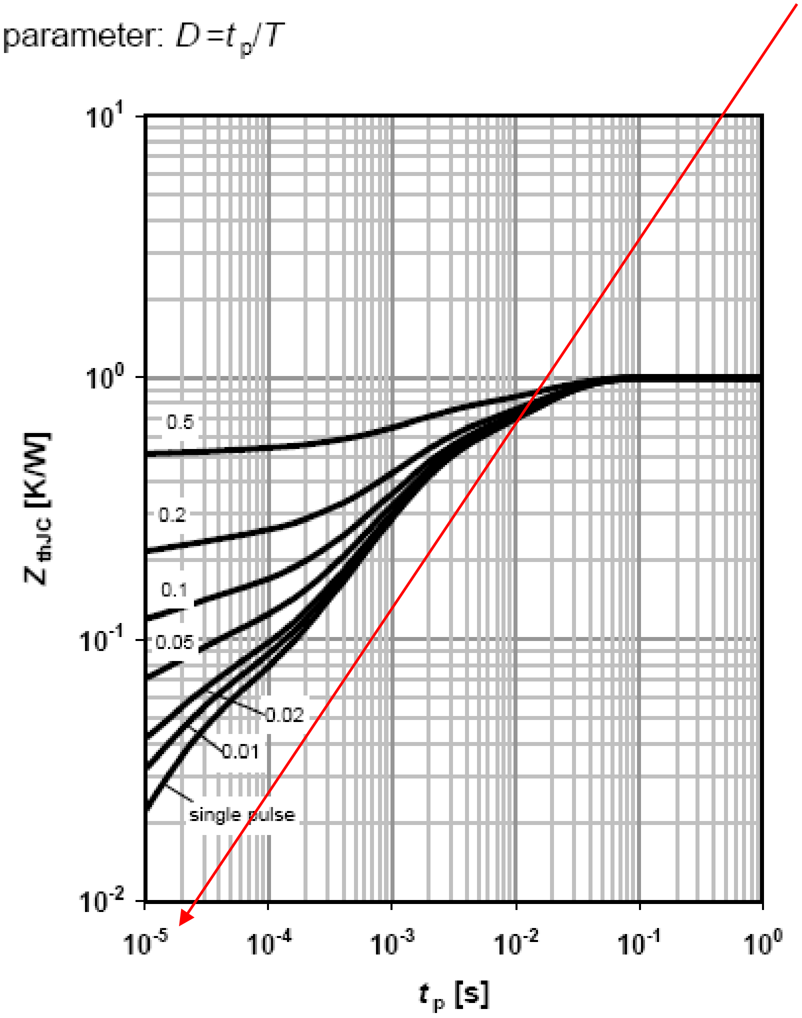
$T_j = T_{c(0)} + P_{DM} * Z_{thJC(tp,D)}$

Transient thermal impedance

4 Max. transient thermal impedance

$Z_{thJC}=f(t_p)$

parameter: $D=t_p/T$



Z_{thJC} is given for pulse widths of as low as tp=10uS.If the Z_{thJC} for a shorter pulse width is required, it can be calculated from equation below:

$$\frac{R_{th(tp1)}}{R_{th(tp2)}} = \sqrt{\frac{tp1}{tp2}}$$

Example

For tp=100ns D=0.1 Z_{thJC}=?

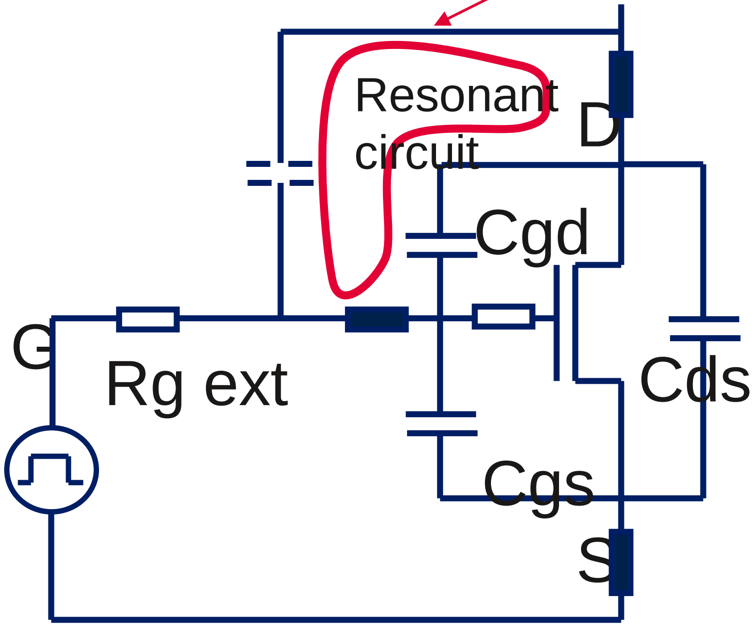
Since tp=10us D=0.1 Z_{thJC}=0.12 (K/W)

Thus $Z_{thJC\ (at\ tp=100ns)} = \sqrt{\frac{100n}{10u}} \cdot 0.12 = 0.012(K/W)$

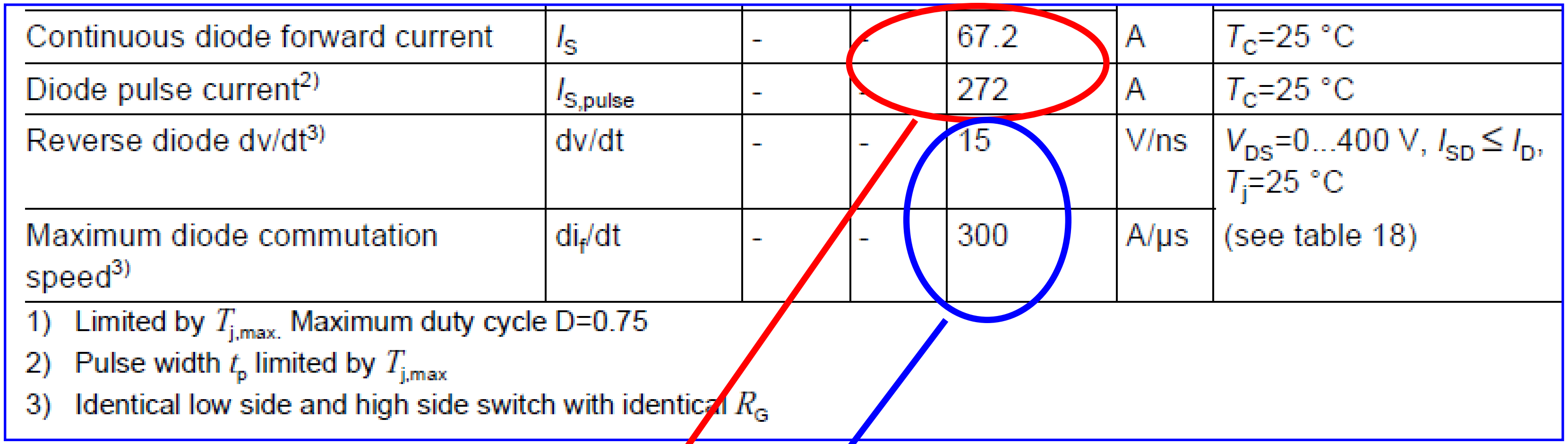
dv/dt

- Recommended value, which consideration of not trigger error turn on at gate side. **Not a maxim rating** as breakdown voltage. It’s decided by actual application.

MOSFET dv/dt ruggedness	dv/dt	-	-	50	V/ns	V_{DS}=0...480 V



Body diode



Continuous diode forward current	I_S	-	-	67.2	A	T_C=25 °C
Diode pulse current[2)]	$I_{S,pulse}$	-	-	272	A	T_C=25 °C
Reverse diode dv/dt[3)]	dv/dt	-	-	15	V/ns	V_{DS}=0...400 V, $I_{SD} \leq I_D$, T_j=25 °C
Maximum diode commutation speed[3)]	di_f/dt	-	-	300	A/µs	(see table 18)

1) Limited by $T_{j,max.}$ Maximum duty cycle D=0.75

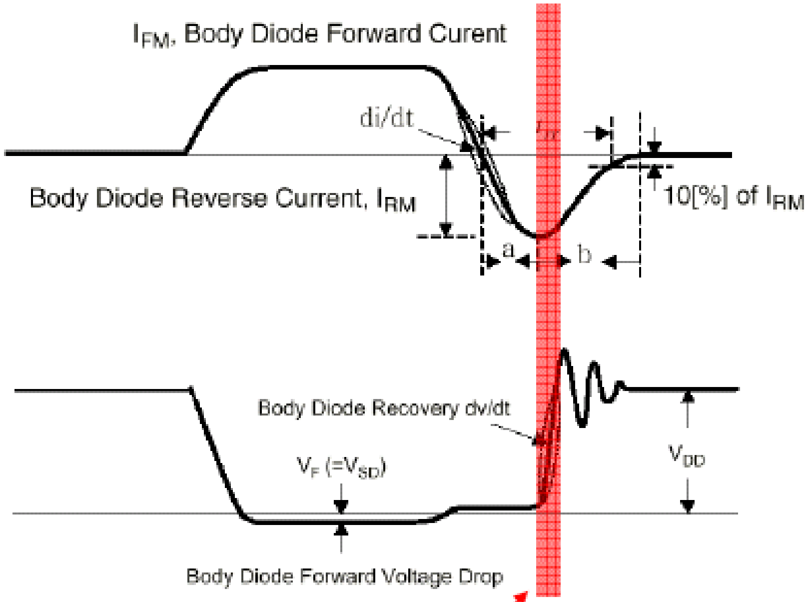
2) Pulse width t_p limited by $T_{j,max}$

3) Identical low side and high side switch with identical R_G

- Same as Id & Idpulse, sometimes derating applied.
- Limited by commutation capability of body diode

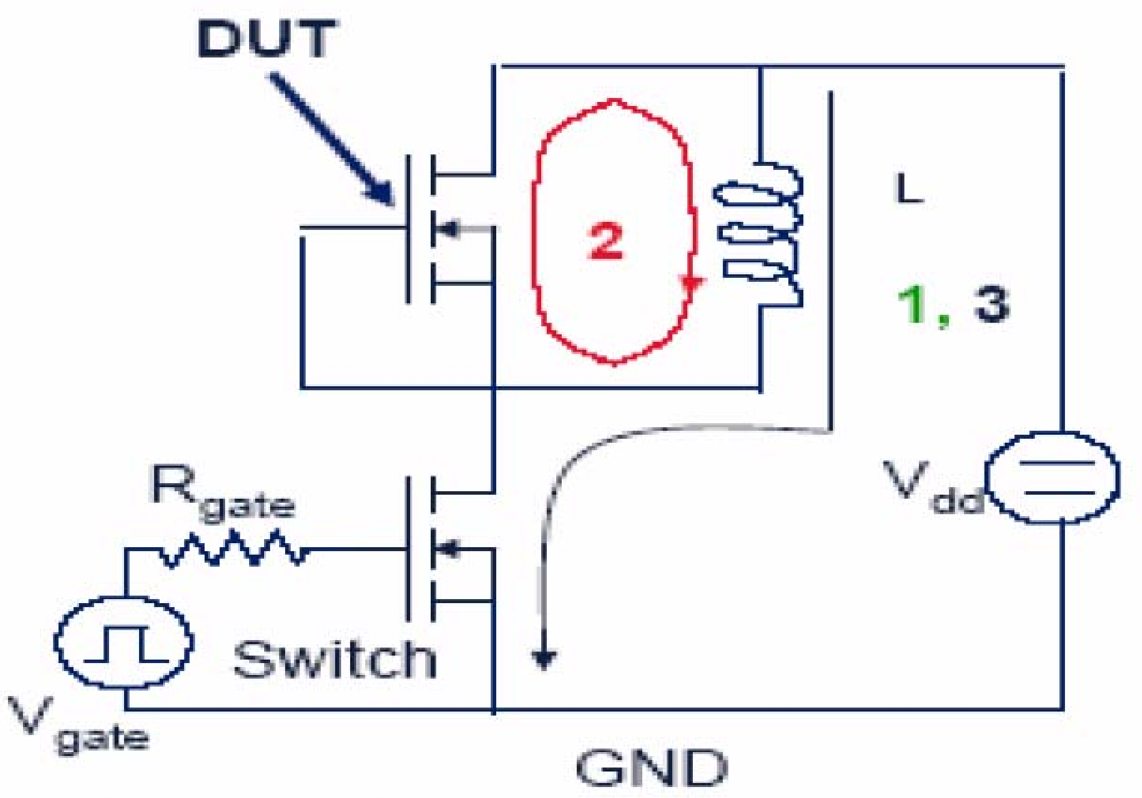
Reverse diode characteristics

Diode forward voltage	V_{SD}	-	0.9	-	V	V_{GS}=0 V, I_F=44.4 A, T_j=25 °C
Reverse recovery time	t_{rr}	-	950	-	ns	V_R=400 V, I_F=44.4 A, di_F/dt=100 A/µs (see table 18)
Reverse recovery charge	Q_{rr}	-	32	-	µC	
Peak reverse recovery current	I_{rrm}	-	62	-	A	



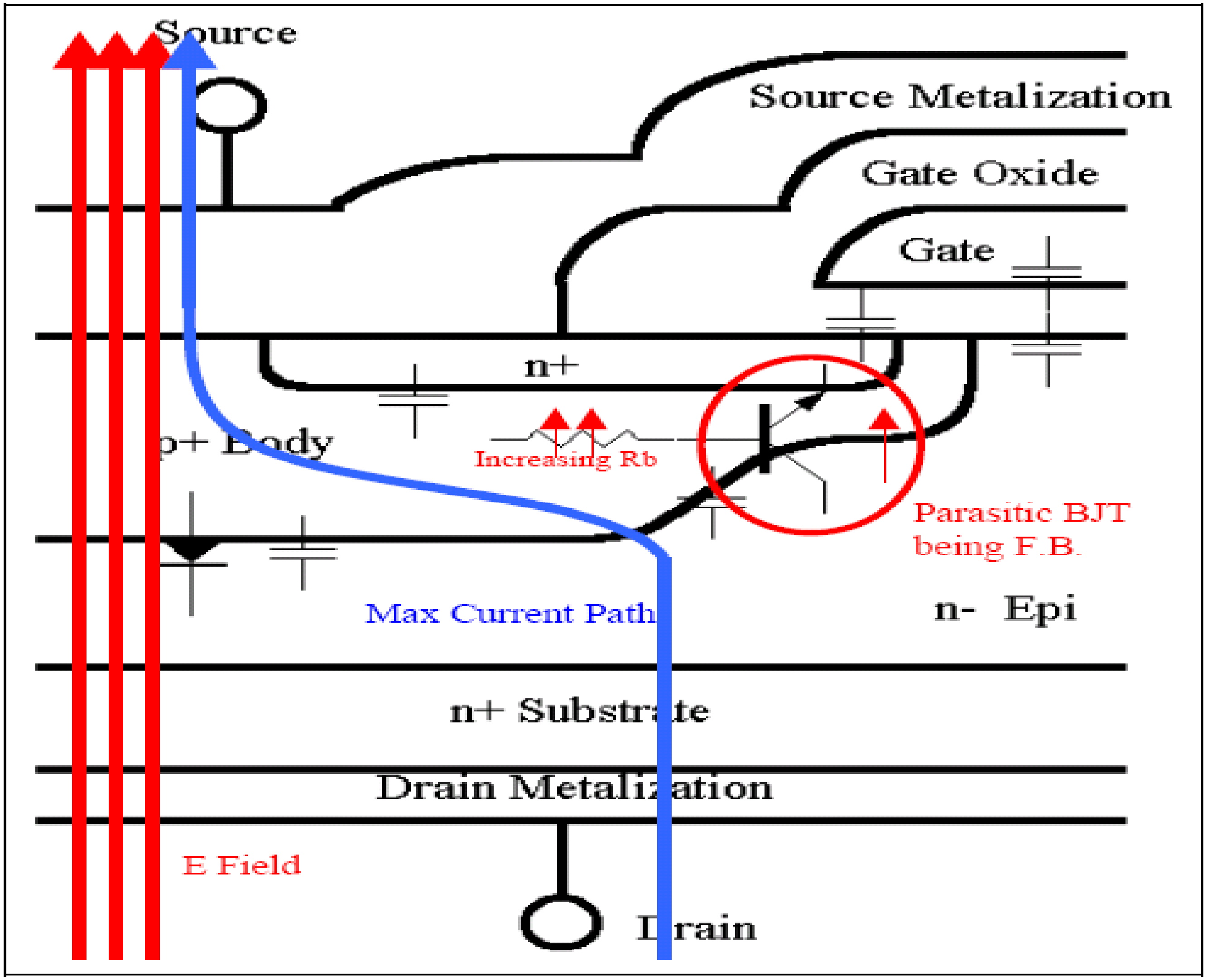
Highest Stress point

Reverse diode characteristics



1. switch turned on → current through L rises linearly
2. nominal current I_d reached → switch turned off
   → current flows through DUT
3. switch turned on → Q_{rr} cleared from DUT
   → current flows through switch

What is the Avalanche Breakdown ?

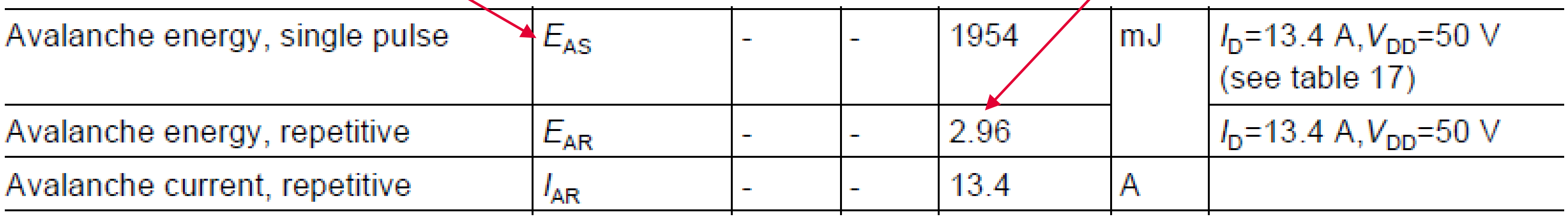


Power MOSFET cross section under Avalanche

How do we specify avalanche?

Repetitive
energy limit

Energy destruction limit,
destruction by excess **thermal** heat

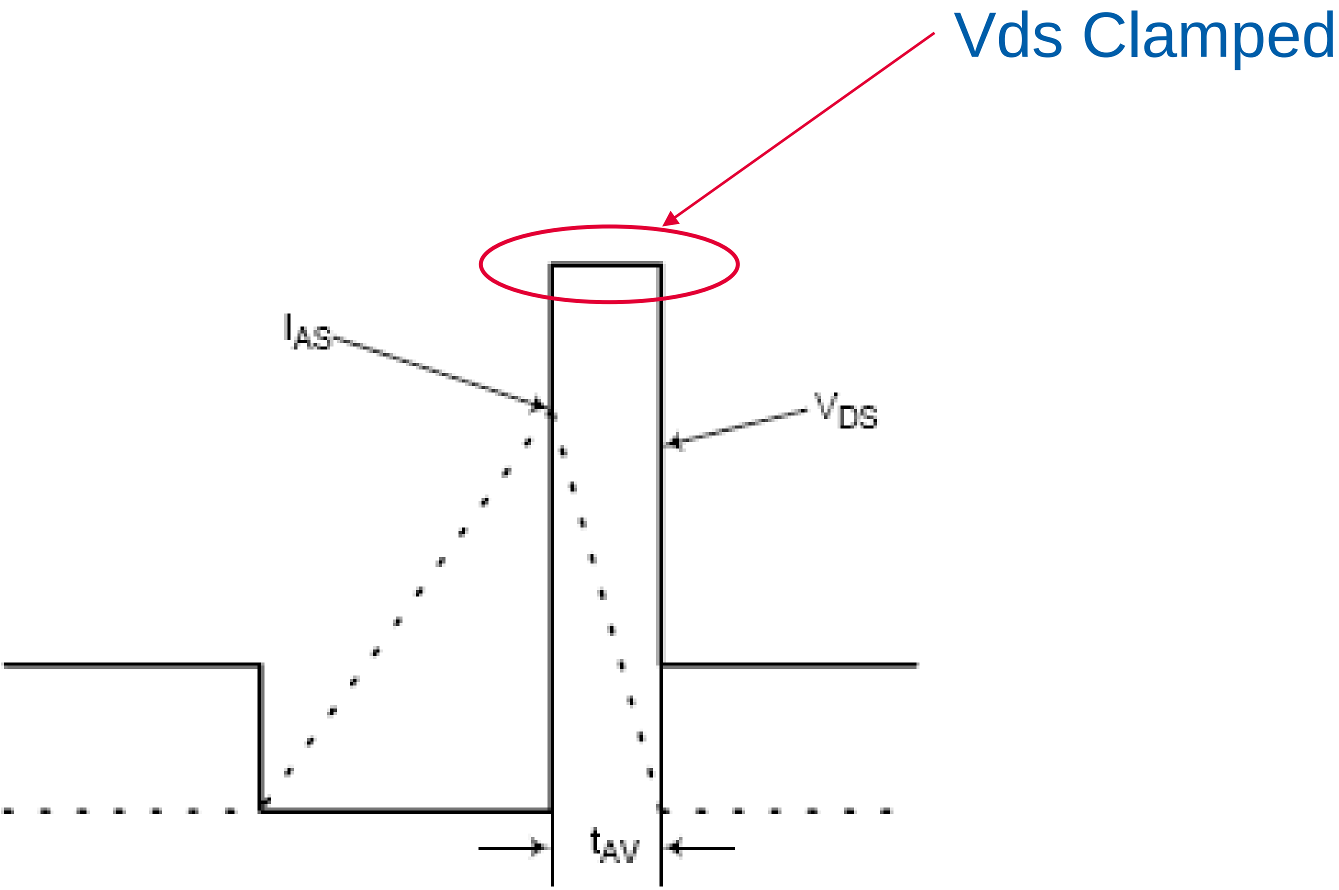


Avalanche energy, single pulse	E_{AS}	-	-	1954	mJ	I_D=13.4 A, V_{DD}=50 V (see table 17)
Avalanche energy, repetitive	E_{AR}	-	-	2.96		I_D=13.4 A, V_{DD}=50 V
Avalanche current, repetitive	I_{AR}	-	-	13.4	A	

Defined as the maximum current which can flow through the device during avalanche operation **without BJT latching**.

All the avalanche operations (single / repetitive) should be below this value!

Avalanche waveform



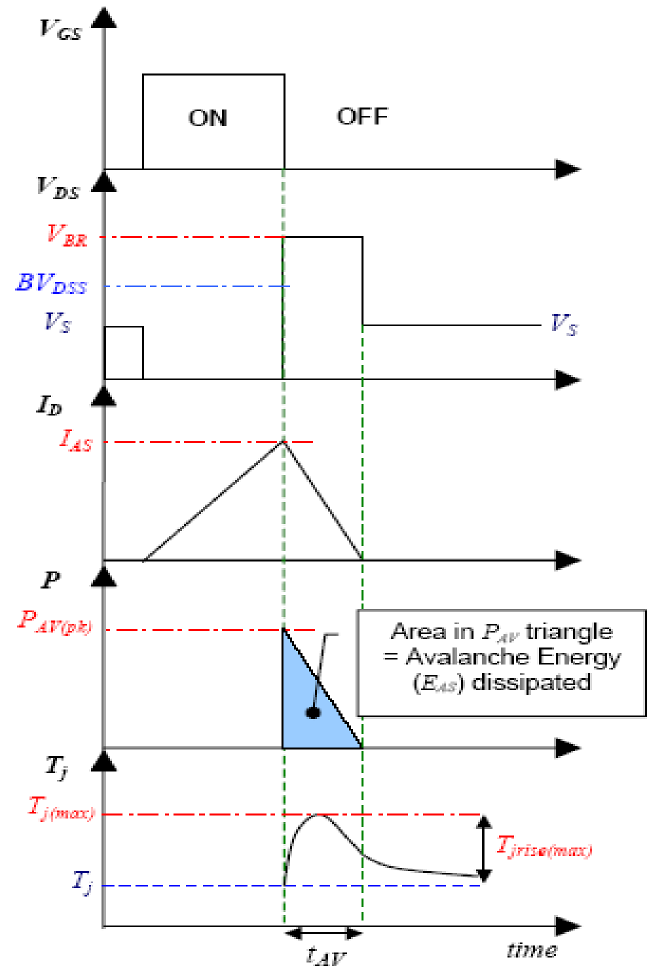
Single avalanche

$$E_{AS} = \frac{1}{2} V_{BR} \bullet I_{AS} \bullet t_{AV}$$

$$= \frac{1}{2} L \bullet I_{AS}^{\ 2} \bullet \frac{V_{BR}}{V_{BR} - V_S}$$

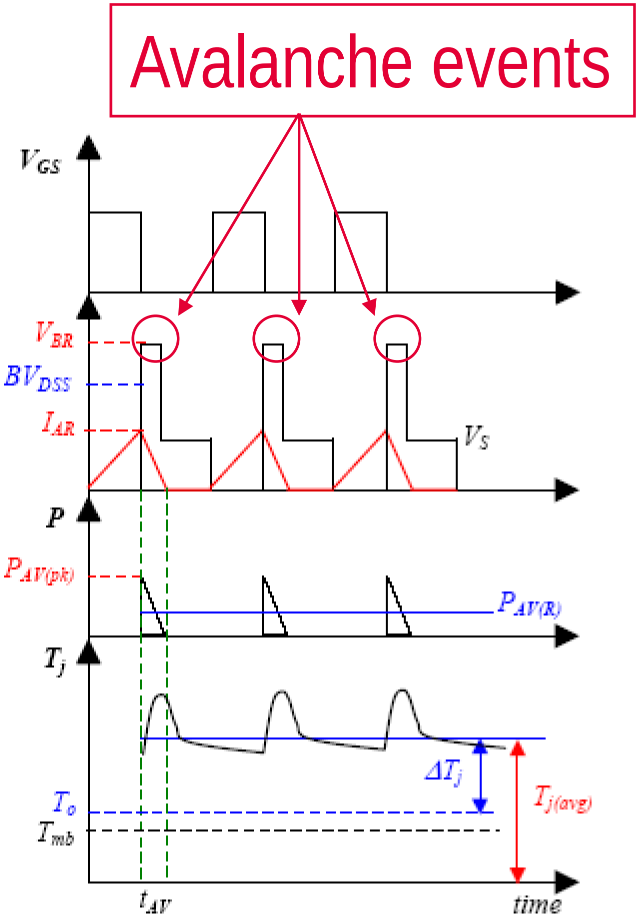
$$V_{BR} \approx 1.3 \times BV_{DSS}$$

L: Magnetic component which provide the avalanche energy



Repetitive avalanche

$$E_{AR} = \frac{1}{2} \bullet V_{BR} \bullet I_{AR} \bullet t_{AV}$$


Avalanche events

We commit.

We innovate.

We partner.

We create value.

infineon

Never stop thinking