Application Note, V1.0, Oct. 2007

AP08066

XC800

Design Guideline for XC800 Microcontroller Board Layout

Microcontrollers

Never stop thinking

Edition 2007-10-12
Published by
Infineon Technologies AG
81726 München, Germany

LEGAL DISCLAIMER

THE INFORMATION GIVEN IN THIS APPLICATION NOTE IS GIVEN AS A HINT FOR THE IMPLEMENTATION OF THE INFINEON TECHNOLOGIES COMPONENT ONLY AND SHALL NOT BE REGARDED AS ANY DESCRIPTION OR WARRANTY OF A CERTAIN FUNCTIONALITY, CONDITION OR QUALITY OF THE INFINEON TECHNOLOGIES COMPONENT. THE RECIPIENT OF THIS APPLICATION NOTE MUST VERIFY ANY FUNCTION DESCRIBED HEREIN IN THE REAL APPLICATION. INFINEON TECHNOLOGIES HEREBY DISCLAIMS ANY AND ALL WARRANTIES AND LIABILITIES OF ANY KIND (INCLUDING WITHOUT LIMITATION WARRANTIES OF NON-INFRINGEMENT OF INTELLECTUAL PROPERTY RIGHTS OF ANY THIRD PARTY) WITH RESPECT TO ANY AND ALL INFORMATION GIVEN IN THIS APPLICATION NOTE.

Information

For further information on technology, delivery terms and conditions and prices please contact your nearest Infineon Technologies Office (**www.infineon.com**).

Warnings

Due to technical requirements components may contain dangerous substances. For information on the types in question please contact your nearest Infineon Technologies Office.

Infineon Technologies Components may only be used in life-support devices or systems with the express written approval of Infineon Technologies, if a failure of such components can reasonably be expected to cause the failure of that life-support device or system, or to affect the safety or effectiveness of that device or system. Life support devices or systems are intended to be implanted in the human body, or to support and/or maintain and sustain and/or protect human life. If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.

AP08066		
Revision History:	2007-10	V1.0
Previous Version:	none	

Page	Subjects (major changes since last revision)

We Listen to Your Comments

Any information within this document that you feel is wrong, unclear or missing at all?
Your feedback will help us to continuously improve the quality of this document.
Please send your proposal (including a reference to this document) to:

mcdocu.comments@infineon.com

Table of Contents **Page**

1 Overview

The XC800 family is an 8-Bit microcontroller family in TSSOP-38, QFP-48 and QFP-64 pin packages. This ApNote gives recommendations concerning electromagnetic compatibility and the power supply system which can lead to a successful PCB design. In addition to the Infineon PCB Design Guidelines for Microcontrollers (AP24026), which gives general design rule information for PCB design, some product-specific recommendations and guidelines for the XC800 family are discussed here.

1.1 General Information:

The XC800 microcontroller family operates at either 3.3V or 5.0 V (VDDP). An on chip EVR (Embedded Voltage Regulator) generates from this voltage 2.5 V (VDDC) for the core logic. The VDDC pin is the output of this regulator and should be connected to an external stabilizing/decoupling capacitor on the application board. The I/O ports are supplied by VDDP. The two supply domains VDDP and VDDC should be decoupled individually.

1.2 Pin-out of XC800

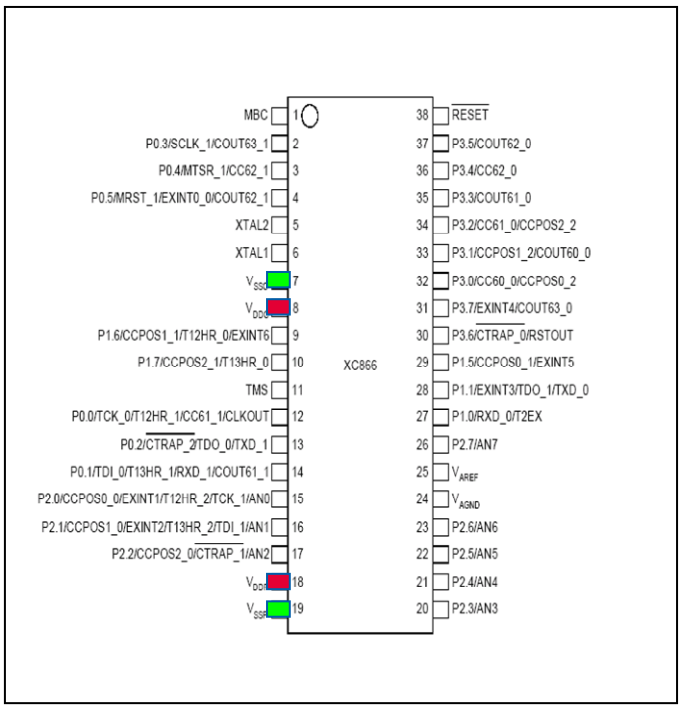

Figure 1 Pin-out of XC866

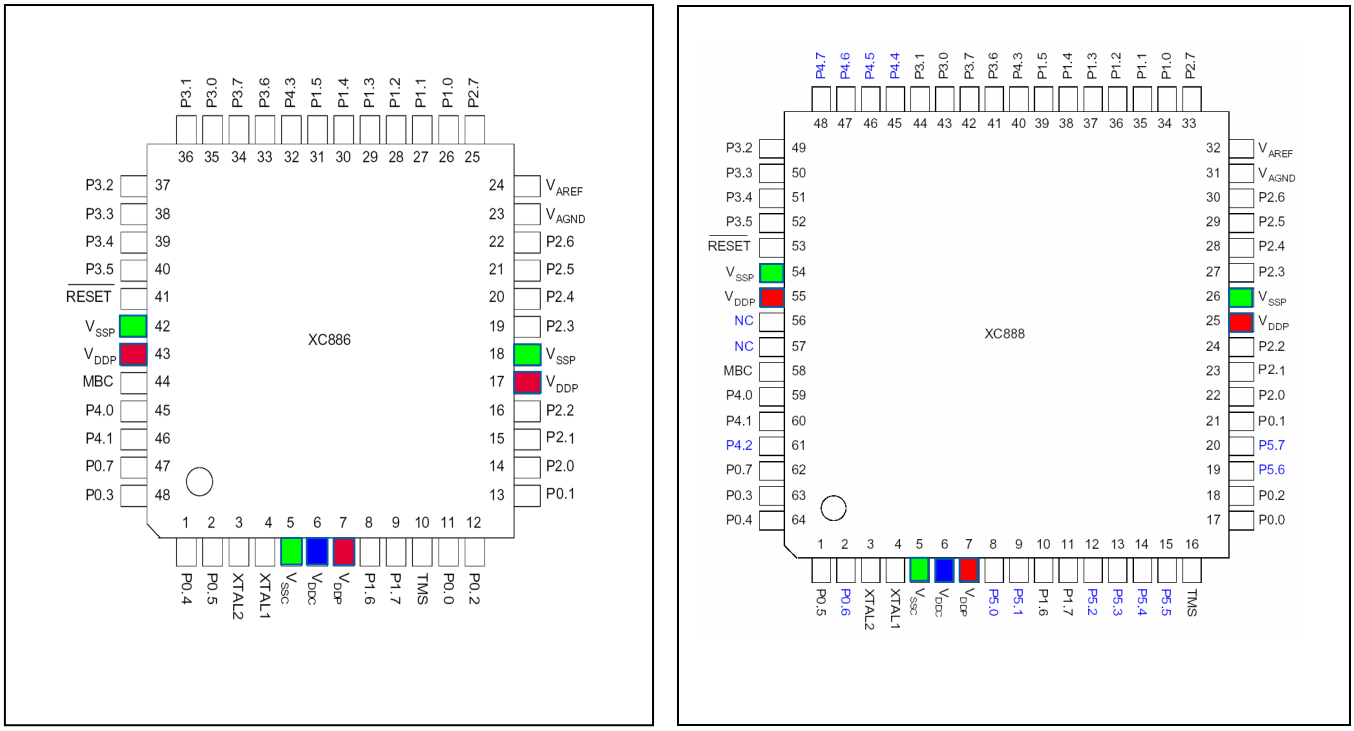

Figure 2 Pin-out of XC886 (48-Pin) and XC888 (64-Pin)

2 PCB Design Recommendations

- To minimize the EMI radiation on the PCB the following signals should to be considered as critical:
  - P0.0 / System clock output
  - Supply pins

  Route these signals with adjacent ground reference and avoid signal and reference layer changes.

  Route them as short as possible. Routing ground on each side can help to reduce coupling to the other signals.

- For unused **"Output, Supply, Input and I/O "** pins following points should be considered:

1. Supply Pins (Modules) :	- (e.g. ADC VAREF/VAGND) See product specification
2. I/O-Pins:	- should be configured as output and driven to static low. - solder-pad should be left open and not be connected to any other net (layout isolated PCB-pad only for soldering)
3.Input Pins without internal pull device:	- For pins with alternate function see product target specification to define the necessary logic level - should be connected with high-ohmic resistor to GND (range 10k – 1Meg) - groups of 8 pins can be used to reduce number of external pull-up/down devices (keep in mind leakage current)
4. Input Pins with internal pull	- For pins with alternate function see product specification to

device:	define the necessary logic level - Should be configured as Pull-down (exception: if the product specification requires high level for alternate functions) - solder-pad should not be connected to any other net (isolated PCB-pad only for soldering)

- The ground system should be designed as follows:

  - Separate analog and digital grounds.

  - The analog ground should be separated into two groups:

    1. Ground for OSC (GND Island),
    2. Ground for ADC (VAGND)

- To reduce the radiation / coupling from the oscillator circuit, a separated ground island on the GND layer should be made. This ground island can be connected at one point to the main GND system with a trace. This helps to keep noise generated by the oscillator circuit isolated on this separated island. The ground connections of the load capacitors and other elements on the island should also be connected to this island. Traces for load capacitors and Crystal should be as short as possible.
- The power distribution from the regulator to each power plane should be made over filters (EMI filter using ferrite beads). Inductance/ferrite beads in the range L ~ 5-10µH should be inserted in the supply paths at the regulator output.
- A low inductance/resistance decoupling capacitors to the supply pins are required (X7R Multilayer Ceramic).
- Use lowest possible frequency for the SYSCLK driver
- Avoid cutting the GND plane by via groups. A solid GND plane should be designed.

2.1 Decoupling

- All supply domains of XC800 should be decoupled separately (see decoupling layout example in Figure 3-5).
- Type of capacitors:
  - Values: 10 nF, 100 nF, 220 nF
  - X7R Ceramic Multilayer (Low ESR and low ESL)
- All power pins (supplied from Voltage Regulator) should be connected first to the dedicated decoupling capacitor and then from the capacitors over vias to the power planes.
- All VSS pins should be connected to the GND layer (see layout example in Figures 3-5).
- Multiple vias can be used at capacitors to get a low impedance connection between capacitors and power/GND planes or pins.
- All capacitors should be placed as close as possible to the related supply pin group.

A power-plane/grounding concept example for a XC800 microcontroller can be seen in Figures 3-5.

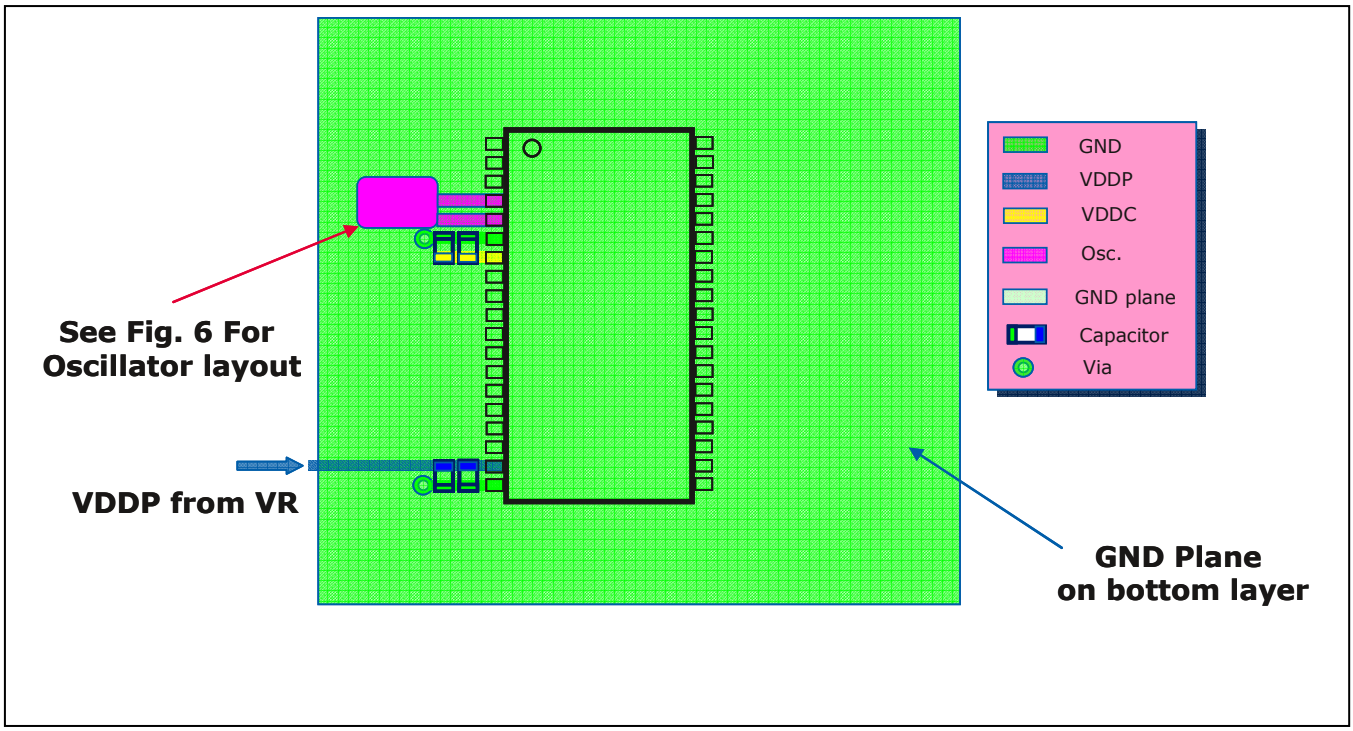

Figure 3 Layout Example for Decoupling of XC866

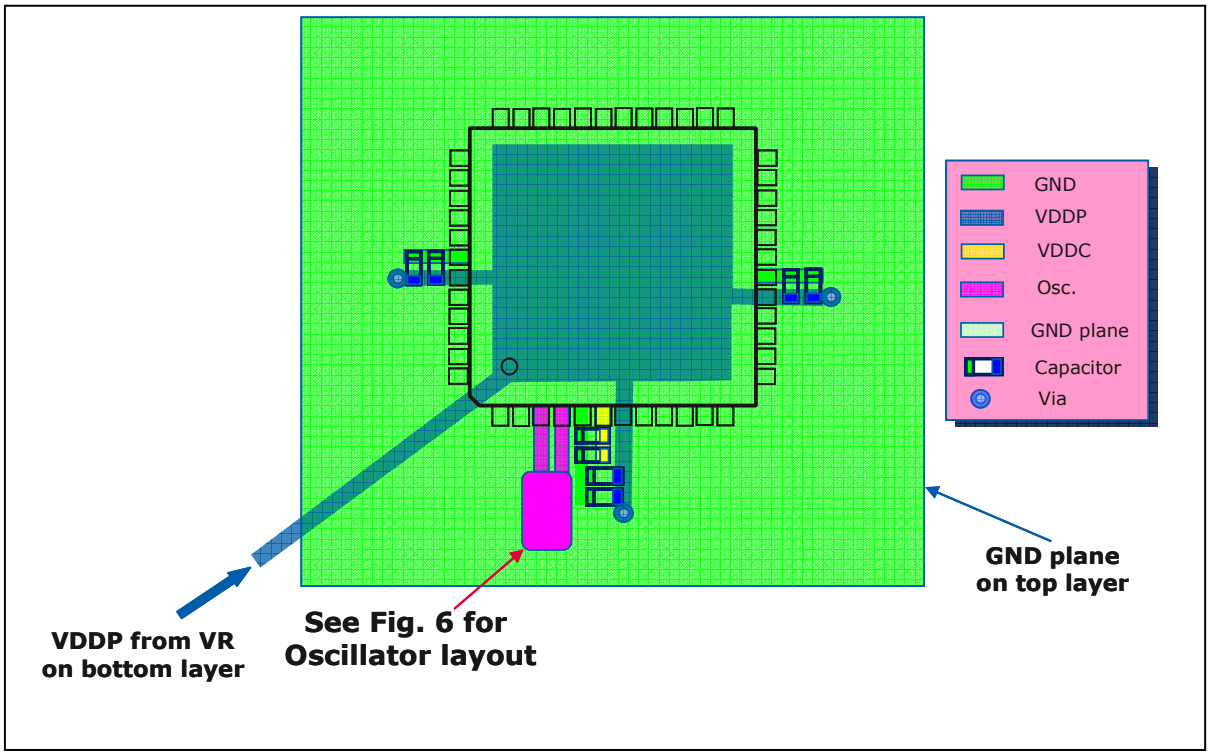

Figure 4 Layout Example for Decoupling of XC886- 48 Pin Package

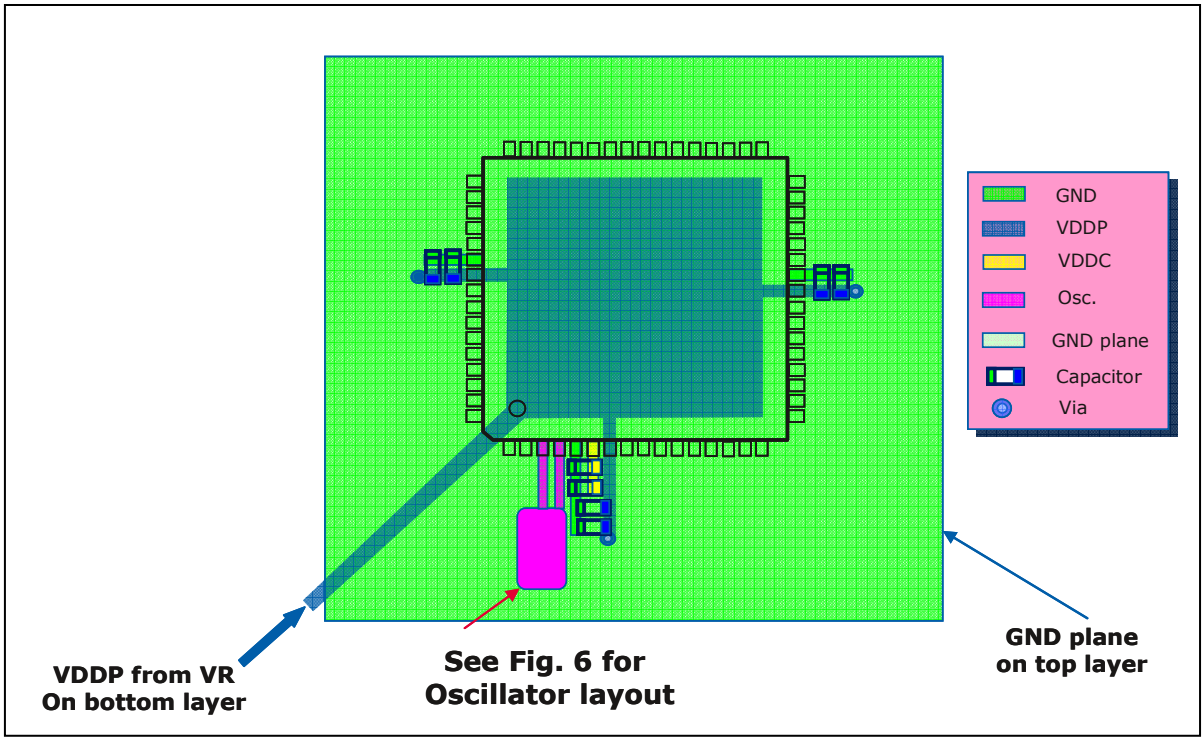

Figure 5 Layout Example for Decoupling of XC888- 64 Pin Package

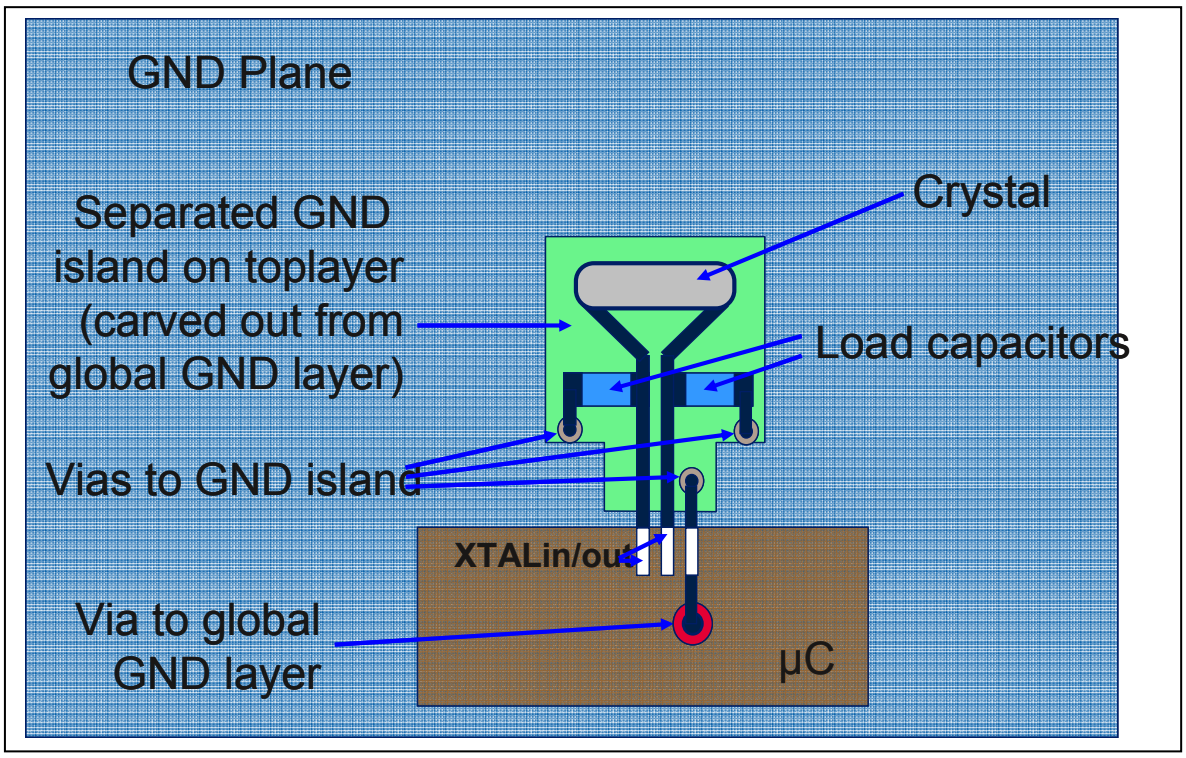

Figure 6 Layout Example for Oscillator Circuit

2.2 Decoupling Capacitor List:

Capacitor	Supply	XC866 Pin (QFP-38)	XC886 Pin (QFP-48)	XC888 Pin (QFP-64)
100 nF // 10 nF	VDDP	19	7	7
100 nF // 10 nF	VDDP	--	17	25
100 nF // 10 nF	VDDP	--	43	55
220 nF // 100 nF	VDDC	7	6	6

http://www.infineon.com

Published by Infineon Technologies AG