PIC18F452 → PIC18F4520 Migration

DEVICE MIGRATIONS

The PIC18F4520 is an extended architecture based on the PIC18F452 family which offers many new features, including extended instruction set, power management modes, higher speed ADC, Enhanced USART and Enhanced CCP modules. This document is intended to describe the functional differences, configuration differences and the electrical specification differences that are present when migrating from one device to the next. Table 1 summarizes the features that may have migration impact on the software code developed for the PIC18F452. Table 2 lists the new and modified features of the PIC18F4520 that should not have any migration impact. Table 3 and Table 4 summarize the differences in the SFRs and configuration memory, respectively. The descriptions in the tables explain the differences in brief. The user should refer to the *"PIC18F2420/2520/4420/4520 Data Sheet"* (DS39631) for detailed explanation.

Note:	This device has been designed to perform to the parameters of its data sheet. It has been tested to an electrical specification designed to determine its conformance with these parameters. Due to process differences in the manufacture of this device, this device may have different performance characteristics than its earlier version. These differences may cause this device to perform differently in your application than the earlier version of this device.

Note:	The user should verify that the device oscillator starts and performs as expected. Adjusting the loading capacitor values and/or the oscillator mode may be required.

Note:	Throughout this document, the PIC18F4520 refers to the family of controllers, PIC18F2420/2520/4420/4520 and the PIC18F452 refers to the family of controllers, PIC18F242/252/442/452.

TABLE 1: PIC18F452 → PIC18F4520 FEATURES AFFECTING SOFTWARE

Module	Comments
Analog-to-Digital Converter (ADC)	The PIC18F4520 has a 100-ksps ADC module, while the PIC18F452 has a 30-ksps ADC module. For more information on ADC acquisition requirements and conversion time per bit, refer to **Section 19.1 "A/D Acquisition Requirements"** and **Section 19.3 "Selecting the A/D Conversion Clock"** of the PIC18F4520 data sheet. The PIC18F4520 ADC module supports auto-acquisition and more analog channels. The PIC18F4520 is defined to maintain 100% pinout compatibility with the PIC18F452. This is achieved by mapping the extra analog inputs with the existing PORTB<4:0> inputs. PORTB<4:0> can be configured either as analog or digital on POR by a configuration bit (CONFIG3H<1>). Bit allocations for the ADCON0 and ADCON1 registers in the PIC18F4520 are different from that of the PIC18F452. ADCON1<3:1> = `0100`, `0101` or `1111` combinations in PIC18F452 may not have an exact equivalence in PIC18F4520 while configuring PORTA pins as digital or analog. For more information, refer to **Section 19.0 "10-Bit Analog-to-Digital Converter (A/D) Module"** of the PIC18F4520 data sheet.
Write to Flash	In the PIC18F4520, a write to program memory is executed on blocks of 32 bytes at a time. In the case of PIC18F452, it is 8 bytes at a time. For more information, refer to **Section 6.5 "Writing to Flash Program Memory"** of the PIC18F4520 data sheet.
Boot Block	The PIC18F4520 has a boot block size of 2 Kbytes (000h to 07FFh) as compared to 512 bytes (000h to 1FFh) in PIC18F452. This may have an impact on software migration, where table read and/or table write instructions are used with any one of the code protection features (write-protect or read-protect). This change in the boot block size may affect the boot loader firmware. For more information, refer to **Section 23.5 "Program Verification and Code Protection"** of the PIC18F4520 data sheet.
MSSP	In I^2C™ Master mode reception, the MSSP module of the PIC18F4520 must be in an Idle state before the RCEN bit is set. For more information, refer to **Section 17.4.11 "I^2C Master Mode Reception"** of the PIC18F4520 data sheet. The I^2C specification mentions the address 0x02 as reserved. The new I^2C module in the PIC18F4520 is compliant to this specification and does not respond to the address 0x02.

TABLE 2: PIC18F452 → PIC18F4520 NEW FEATURES

Module	Comments
Core	In addition to the standard 75 instructions of the PIC18F452 instruction set, the PIC18F4520 also provides an optional extension to the core CPU functionality. The added features include 8 additional instructions. These additional instructions are designed to optimize the applications written in C; they are mainly intended for use by C compilers. A user writing in assembly is not likely to use the additional instructions. The additional features of the extended instruction set are disabled by default. To enable them, the user must set the XINST configuration bit. An additional addressing mode, Indexed Literal Offset, is available when the extended instruction set is enabled. The use of the Indexed Literal Offset Addressing mode effectively changes how the first 96 locations of the Access RAM (00 to 5Fh) are mapped. Also, the execution of some instructions in the PIC18F452 instruction set are changed when the extended instruction set is enabled. For more information, refer to **Section 5.5 "Data Memory and the Extended Instruction Set"** of the PIC18F4520 data sheet. When using Microchip's MPLAB® C18 C compiler, refer to the latest *"MPLAB® C18 C Compiler User's Guide"* (DS51288) for information on the C compiler operation in Extended mode.
Power-Managed Modes	The PIC18F4520 devices offer a total of seven operating modes for more efficient power management. These modes provide a variety of options for selective power conservation in applications where resources may be limited (i.e., battery-powered devices). In addition to the Run and Sleep modes, the PIC18F4520 also offers the Idle mode of operation. The Idle mode allows the controller CPU to shut-down selectively while the peripherals continue to operate. For more information, refer to **Section 3.0 "Power-Managed Modes"** of the PIC18F4520 data sheet.
Multi-Frequency Internal Oscillator Block	The PIC18F4520 includes an internal oscillator block. The main output (INTOSC) is an 8-MHz clock source which can be used to directly drive the device clock. It also drives a postscaler which can provide a range of clock frequencies from 31 kHz to 8 MHz. When used with the PLL, the internal oscillator block can provide clock frequencies of up to 32 MHz. For more information, refer to **Section 2.6 "Internal Oscillator Block"** of the PIC18F4520 data sheet.
Comparator	The analog comparator module is a new peripheral on the PIC18F4520. The PIC18F4520 is defined to maintain 100% pinout compatibility with the PIC18F452. This is achieved by mapping the comparator inputs with the existing ADC channels on PORTA. A programmable reference voltage for the comparator is provided. The comparator module is disabled on power-up. For more information, refer to **Section 20.0 "Comparator Module"** of the PIC18F4520 data sheet.
Interrupts	The PIC18F4520 supports two additional interrupts. These are the oscillator fail interrupt and the comparator interrupt. Bits 7 and 6 are implemented in the PIR2, PIE2 and IPR2 registers for this purpose. By default, these interrupts are disabled. For more information, refer to **Section 9.2 "PIR Registers", Section 9.3 "PIE Registers"** and **Section 9.4 "IPR Registers"** of the PIC18F4520 data sheet.
ECCP	In 40/44 pin devices of the PIC18F4520 family, the CCP1 module is implemented as ECCP (Enhanced CCP). The ECCP module is implemented as a standard CCP module with Enhanced PWM capabilities. These include the selection of 1, 2 or 4 PWM outputs, user selectable polarity, dead-band control and automatic shut-down and restart. By default, the ECCP module is configured in Single Output mode and functions identically to the standard CCP module in PWM mode. For more information, refer to **Section 16.0 "Enhanced Capture/Compare/PWM (ECCP) Module"** of the PIC18F4520 data sheet.

TABLE 2: PIC18F452 → PIC18F4520 NEW FEATURES (CONTINUED)

Module	Comments
EUSART	The USART module in the PIC18F4520 is implemented as EUSART (Enhanced USART). The Enhanced USART module implements additional features, including Automatic Baud Rate Detection and calibration, automatic wake-up on Sync Break reception and 12-bit Break character transmit. These features make it ideal for use in Local Interconnect Network bus (LIN bus) systems. The Baud Rate Generator (BRG) in the PIC18F4520 is a dedicated 8-bit or 16-bit generator that supports both the Asynchronous and Synchronous modes of the EUSART. By default, the BRG operates in the 8-bit mode and all the enhanced features are disabled. For more information, refer to **Section 18.0 "Enhanced Universal Synchronous Receiver Transmitter (EUSART)"** of the PIC18F4520 data sheet.
Timer1	T1CON<6> (T1RUN): This new bit in the PIC18F4520 is a read-only bit which indicates whether the device clock is being provided by the Timer1 oscillator or another source. The Timer1 oscillator in the PIC18F4520 can operate at two distinct levels of power consumption based on the device configuration. When the LPT1OSC configuration bit (CONFIG3H<2>) is set, the Timer1 oscillator operates in a low-power mode. By default, this bit is not set and the Timer1 operates at a high-power level which is compatible with the PIC18F452 device. For more information, refer to **Section 12.3.2 "Low-Power Timer1 Option"** of the PIC18F4520 data sheet.
Two-Speed Start-up	The Two-Speed Start-up feature in the PIC18F4520 helps to minimize the latency period from oscillator start-up to code execution by allowing the microcontroller to use the internal oscillator as a clock source until the primary clock is available. By default, the Two-Speed Start-up is disabled. For more information, refer to **Section 23.3 "Two-Speed Start-up"** of the PIC18F4520 data sheet.
Fail-Safe Clock Monitor	The Fail-Safe Clock Monitor allows the microcontroller to continue operation in the event of an external oscillator failure by automatically switching the device clock to the internal oscillator block. By default, the Fail-Safe Clock Monitor is disabled. For more information, refer to **Section 23.4 "Fail-Safe Clock Monitor"** of the PIC18F4520 data sheet.
WDT	The nominal WDT period in the PIC18F4520 is 4 ms. The 4-ms period of the WDT is multiplied by a 16-bit postscaler. Any output of the WDT postscaler is selected by a multiplexer, controlled by the bits in the CONFIG2H register. Available periods range from 4 ms to 131.072 seconds (2.18 minutes). The typical WDT period in the PIC18F452 is 18 ms. If the WDT option is enabled, the user needs to select the appropriate WDT time-out period for the PIC18F4520. For more information, refer to **Section 23.2 "Watchdog Timer (WDT)"** of the PIC18F4520 data sheet.
HLVD	The LVD module is improved as HLVD (High/Low-Voltage Detect) on the PIC18F4520. For more information, refer to **Section 22.0 "High/Low-Voltage Detect (HLVD)"** of the PIC18F4520 data sheet.
PORTE/$\overline{\text{MCLR}}$	In PIC18F4520, the PORTE<3> pin ($\overline{\text{MCLR}}$/V_{PP}/RE3) is available as an optional digital input only pin. Its operation is controlled by the MCLRE configuration bit (CONFIG3H<7>). By default, this pin acts as the Master Clear input ($\overline{\text{MCLR}}$). For more information, refer to **Section 10.5 "PORTE, TRISE and LATE Registers"** of the PIC18F4520 data sheet.
Enhanced ICD	The PIC18F4520 provides Enhanced ICD features which include three Break points and Break on GPR address and data match.

TABLE 3: PIC18F452 → PIC18F4520 SFR DIFFERENCES

Address	SFRs	Differences From 18F452	Comment
F9Bh	OSCTUNE	Implemented(1)	Control bits for internal oscillator block.
FA0h, FA1h, FA2h	PIE2/PIR2/IPR2	Implemented 2 more bits (bits 7 and 6) in PIE2, PIR2 and IPR2 registers(2)	Bit 7 of each register refers to the oscillator fail interrupt and bit 6 of each register refers to the comparator interrupt.
FACh	TXSTA	Implemented one more bit (TXSTA<3>)(2)	TXSTA<3> for Sync Break character generation.
FB0h	SPBRGH	Implemented(1)	SPBRGH holds the higher byte of the baud rate value when the 16-bit Baud Rate Generator is used.
FB4h	CMCON	Implemented(1)	Comparator register.
FB5h	CVRCON	Implemented(1)	Comparator Voltage Reference register.
FB6h	ECCP1AS	Implemented(1)	ECCP Auto-Shutdown register.
FB7h	PWM1CON	Implemented(1)	ECCP Dead-Band Delay register.
FB8h	BAUDCON	Implemented(1)	Register for the EUSART functionality.
FBDh	CCP1CON	Implemented 2 more bits (CCP1CON<7:6>)(2)	CCP1CON<7:6> for ECCP PWM output selection (1, 2 or 4).
FC0h	ADCON2	Implemented(3)	The ADCON2 register configures the A/D clock source, programmed acquisition time and justification. For more information, refer to **Section 19.0 "10-Bit Analog-to-Digital Converter (A/D) Module**" of the PIC18F4520 data sheet.
FC1h	ADCON1	Changes in bit allocations(3)	The ADCON1 register configures the function of the port pin. For more information, refer to **Section 19.0 "10-Bit Analog-to-Digital Converter (A/D) Module**" of the PIC18F4520 data sheet.
FC2h	ADCON0	Changes in bit allocations(3)	The ADCON0 register controls the operation of the A/D converter module. For more information, refer to **Section 19.0 "10-Bit Analog-to-Digital Converter (A/D) Module**" of the PIC18F4520 data sheet.
FCDh	T1CON	Implemented bit 6 (T1CON<6>)(2)	T1CON<6> (T1RUN) indicates whether the device is running from the Timer1 oscillator or not.
FD2h	HLVDCON	Implemented bit 7 and the register name has changed from LVDCON to HLVDCON(2)	When HLVDCON<7> is cleared, the HLVD module monitors for a drop in V_{DD} below a predetermined set point. When the bit is set, the module monitors for a rise in V_{DD} above the set point.
FD3h	OSCCON	Implemented 6 more bits(2)	Extra bits are for the power management modes.

Note 1: On power-up default, these new registers in the PIC18F4520 do not have any migration impact.

2: On power-up default, these extra bits implemented in the PIC18F4520 do not have any migration impact.

3: The changes in these registers have a migration impact.

TABLE 4: PIC18F452 → PIC18F4520 CONFIGURATION REGISTER DETAILS

Address	Configuration Register	PIC18F452	PIC18F4520
300001h	CONFIG1H	CONFIG1H<2:0>: Oscillator Selection bits. CONFIG1H<5>: Clock Switch Enable bit. By default, the clock switch option is disabled. When, enabled, the SCS bit in the OSCCON register controls the clock switching.	CONFIG1H<3:0> bits can be used for two more oscillator mode selections. CONFIG1H<5> bit is not implemented. OSCCON register controls the clock switching and the power management modes. CONFIG1H<6> bit enables or disables the Fail-Safe Clock Monitor. By default, the Fail-Safe Clock Monitor is disabled. CONFIG1H<7> bit enables or disables the Two-Speed Start-up feature. By default, the Two-Speed Start-up is disabled.
300002h	CONFIG2L	CONFIG2L<1>: BOR Enable or Disable bit.	CONFIG2L<2:1> bits provide 4 modes of BOR selection (software enable of BOR possible with RCON<6> if BOR is disabled in hardware). By default, the BOR is enabled in hardware.
300003h	CONFIG2H	CONFIG2H<3:1>: Watchdog Postscale bits up to 1:128.	CONFIG2H<4:1> bits provide Watchdog Postscale bits up to 1:32768.
300005h	CONFIG3H	PORTB is always digital. There is no low-power oscillator on Timer1.	CONFIG3H<7> bit controls if the RE3 port pin is selected as $\overline{\text{MCLR}}$ or as an input port. By default, $\overline{\text{MCLR}}$ is enabled. CONFIG3H<2> bit allows Timer1 to be operated on a low or high-power oscillator. By default, the high-power oscillator is enabled which is compatible with the PIC18F452. CONFIG3H<1> bit controls the configuration of PORTB<4:0> pins on POR. By default, the PORTB<4:0> pins are configured as analog on POR. For compatibility with the PIC18F452, the user needs to configure PORTB<4:0> as digital.
300006h	CONFIG4L	No Instruction Extension and Indexed Addressing modes.	CONFIG4L<6> bit enables or disables the extended instruction set. By default, the extended instruction set is disabled.
300008h	CONFIG5L	CONFIG5L<0>: Block 0 Code Protection bit (000200-001FFFh).	CONFIG5L<0> bit code-protects Block 0 (000800-001FFFh).
300009h	CONFIG5H	CONFIG5H<6>: Boot Block Code Protection bit (000000-0001FFh).	CONFIG5H<6> bit code-protects Boot Block (000000-0007FFh).
30000Ah	CONFIG6L	CONFIG6L<0>: Block 0 Write Protection bit (000200-001FFFh).	CONFIG6L<0> bit write-protects Block 0 (000800-001FFFh).
30000Bh	CONFIG6H	CONFIG6H<6>: Boot Block Write Protection bit (000000-0001FFh).	CONFIG6H<6> bit write-protects Boot Block (000000-0007FFh).
30000Ch	CONFIG7L	CONFIG7L<0>: Block 0 Read Protection bit (000200-001FFFh).	CONFIG7L<0> bit read-protects Block 0 (000800-001FFFh).
30000Dh	CONFIG7H	CONFIG7H<6>: Boot Block Read Protection bit (000000-0001FFh).	CONFIG7H<6> bit read-protects Boot Block (000000-0007FFh).

Note: If not otherwise mentioned, all bits in the PIC18F452 are implemented in the PIC18F4520. **Some of the configuration bits in the PIC18F4520 erase to '0' state; this may have migration impact.** For more information, refer to **Section 23.1 "Configuration Bits"** of the PIC18F4520 data sheet.

TABLE 5: PIC18F452 → PIC18F4520 ELECTRICAL CHARACTERISTICS DIFFERENCES

Absolute Maximum Ratings	PIC18F452	PIC18F4520
Ambient Temperature under Bias	-40°C to +125°C	-40°C to +125°C

TABLE 6: PIC18F452 → PIC18F4520 DC CHARACTERISTICS DIFFERENCES

Parameter No.	Parameter	PIC18LF452			PIC18LF4520			Units
		Min.	Typical	Max.	Min.	Typical	Max.	
D005	BOR							
	11	1.98	—	2.14	1.96	2.06	2.16	V
	10	2.67	—	2.89	2.64	2.78	2.92	V
	01	4.16	—	4.5	4.11	4.33	4.55	V
	00	4.45	—	4.83	4.41	4.64	4.87	V
		PIC18F452						
	11	NA	—	NA	—	—	—	V
	10	NA	—	NA	—	—	—	V
	01	4.16	—	4.5	—	—	—	V
	00	4.45	—	4.83	—	—	—	V
D420	HLVD-LVD							
	LVV = 0000	-	-	-	2.12	2.17	2.22	V
	LVV = 0001	1.98	2.06	2.14	2.18	2.23	2.28	V
	LVV = 0010	2.18	2.27	2.36	2.31	2.36	2.42	V
	LVV = 0011	2.37	2.47	2.57	2.38	2.44	2.49	V
	LVV = 0100	2.48	2.58	2.68	2.54	2.60	2.66	V
	LVV = 0101	2.67	2.78	2.89	2.72	2.79	2.85	V
	LVV = 0110	2.77	2.89	3.01	2.82	2.89	2.95	V
	LVV = 0111	2.98	3.10	3.22	3.05	3.12	3.19	V
	LVV = 1000	3.27	3.41	3.55	3.31	3.39	3.47	V
	LVV = 1001	3.47	3.61	3.75	3.46	3.55	3.63	V
	LVV = 1010	3.57	3.72	3.87	3.63	3.71	3.80	V
	LVV = 1011	3.76	3.92	4.08	3.81	3.90	3.99	V
	LVV = 1100	3.96	4.13	4.30	4.01	4.11	4.20	V
	LVV = 1101	4.16	4.33	4.50	4.23	4.33	4.43	V
	LVV = 1110	4.45	4.64	4.83	4.48	4.59	4.69	V

Note 1: Refer to **Section 26.2 "DC Characteristics: Power-Down and Supply Current"** of the PIC18F4520 data sheet for more information on current consumption in different low-power modes.

2: For A/D converter characteristics and A/D conversion requirements, refer to the Tables 26-24 and 26-25 in the PIC18F4520 data sheet and the Tables 22-21 and 22-22 in the PIC18F452 data sheet.

3: In the PIC18F4520, RA4 is a Schmitt Trigger input and digital output, whereas in the PIC18F452, it is a Schmitt Trigger input and open-drain output.

NOTES:

Note the following details of the code protection feature on Microchip devices:

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10/20/04