Application Report
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Migrating From MSP430F541x/F543x to MSP430F541xA/F543xA

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ABSTRACT

The purpose of this application report is to facilitate the migration of designs based on the MSP430F541x/F543x device family to the MSP430F541xA/F543xA device family. In the course of this application report, the main differences between the two device families are highlighted, and migration solutions covering both software and hardware aspects are provided.

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1 MSP430F541x/F543x vs MSP430F541xA/F543xA Comparison Overview

The 'A' revisions of the MSP430F541x/F543x silicon offer more performance, lower power, and the full set of advertised features for the F5xx family of devices. This enables a more robust cost-optimized system design. Table 1 shows a general high-level comparison of the two device families, providing an overview of reasons why one should consider migrating.

Table 1. F541x/F543x Versus F541xA/F543xA High-Level Differences

	MSP430F541x/F543x	MSP430F541xA/F543xA
Maximum CPU clock speed	18 MHz	25 MHz
V_{CC} operating range	2.2 V to 3.6 V	1.8 V to 3.6 V
Standby current consumption (LPM3)	2.7 μA	1.9 μA(1)
Minimum voltage for flash ISP	2.2 V	1.8 V
Bootstrap loader	Non-customizable	Customizable peripheral interface
Reliable operating temperature range(2)	-20°C to 85°C	-40°C to 85°C
ADC12 voltage reference	Internal 1.5-V or 2.5-V reference	General-purpose REF module (1.5-V, 2.0-V, or 2.5-V reference)
LPM4.5 exit	LPM4.5 not supported	Exit LPM4.5 using $\overline{\text{RST}}$ and/or port interrupts

(1) The value shown here is the expected current consumption and has not been characterized.
(2) See erratum PMM6 in the *MSP430F541x/F543x Device Erratasheet* (SLAZ046).

2 MSP430F541x/F543x to MSP430F541xA/F543xA Migration - Hardware Considerations

Fortunately, the MSP430F541xA/F543xA versions of silicon have very few differences that affect an application's hardware design. The hardware package and pinout is fully pin-to-pin compatible with the non-A versions.

2.1 PMM Settings and Low Power Consumption

The FLASH28 erratum for the MSP430F541x/F543x family of devices specifies read disturb problems when the Power Management Module (PMM) V_{CORE} levels are < 2 (PMMCOREVx = 10b). This limitation makes it necessary for the device V_{CORE} be initialized to level 2 in the boot code, which is different from the expected default values of level 0 specified in the *MSP430x5xx Family User's Guide*. The higher voltage applied to the core increases the power consumption in active as well as low-power modes. To prevent a condition in which the read-disturb problem negatively impacts the application flow, the user should not lower the V_{CORE} level in attempts to obtain lower power consumption.

The MSP430F541xA/F543xA can operate at all PMM levels, allowing for even lower current consumption than its predecessor. For example, in LFXT1 standby mode (LPM3 using a 32-kHz watch crystal), the standby current consumption of an MSP430F541xA/F543xA device is in the 1.9 μA range, versus 2.7 μA for the non-'A' revisions of silicon. This is a considerable advantage for applications that spend the majority of their time in standby mode.

LPM4.5 support has been added to 'A' revisions of silicon. LPM4.5 is equivalent to LPM4, except that the internal voltage regulator is disabled. All CPU operations, clocks, and peripherals are disabled in LPM4.5. LPM4.5 can be leveraged like LPM4 in previous MSP430 families, because it achieves the lowest power consumption and is intended for shelf-life applications or applications that must sit in the lowest power mode for very long periods of time without any peripheral activity. The contents of RAM are cleared (including all peripheral initializations) when entering LPM4.5, and the device must trigger a BOR to wake into an active mode. This BOR can be triggered by the removal of power, by using the RST line, or through the use of a port interrupt. The ability to use port interrupts adds flexibility to the hardware design in that more than one pin is available for wakeup from LPM4.5 and external hardware resources can wake the device.

2.2 Operating Frequency vs Supply Voltage

Figure 1 and Figure 2 show the frequency vs supply voltage curves for the MSP430F541x/F543x and MSP430F541xA/F543xA device families, respectively. [1]

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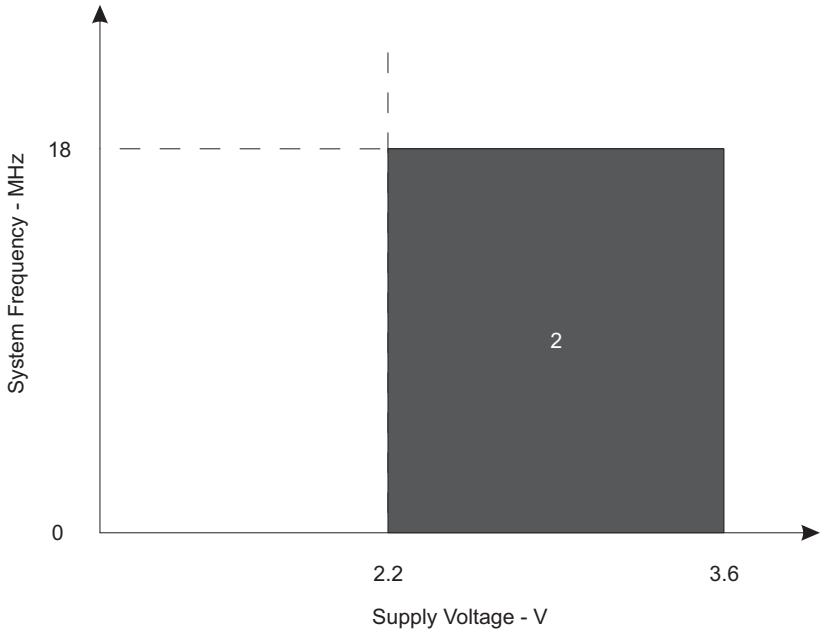
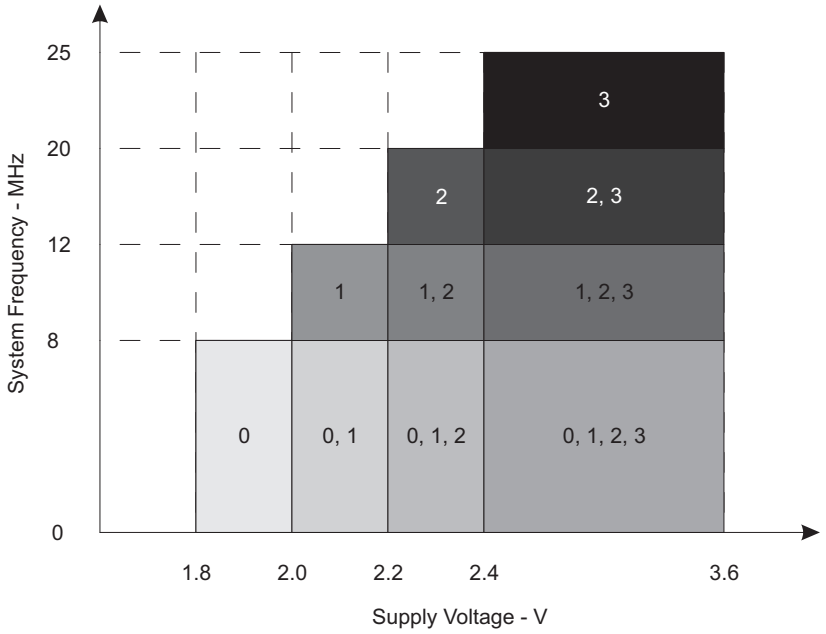


The numbers within the fields denote the supported PMMCOREVx settings.

Figure 1. Frequency vs Supply Voltage MSP430F541x/F543x



The numbers within the fields denote the supported PMMCOREVx settings.

Figure 2. Frequency vs Supply Voltage MSP430F541xA/F543xA

The limitation that a MSP430F541x/F543x device operate at no less than PMMCOREVx level 2 makes the operating range 2.2 V to 3.6 V. Because in-system programming (ISP) for the flash memory is valid over the entire operating range for the device, this also limits the range for flash ISP procedures. Furthermore, non-'A' revisions of F5438 silicon are specified to run up to 18 MHz.

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The MSP430F541xA/F543xA devices can operate from 1.8 V to 3.6 V with valid flash ISP across the entire operating range (see Figure 2). 'A' versions of silicon are also capable of running up to 25 MHz. This flexibility provides both the performance to execute highly CPU-intensive tasks as well as the ability to optimize power consumption according to the speed requirements of the application.

2.3 Internal Voltage Reference

One significant difference in the architecture of the 'A' device family is the replacement of the internal 1.5-V or 2.5-V reference – seen in the ADC12 block diagram in the current *MSP430x5xx Family User's Guide* – with a separate, general-purpose REF module that can provide voltages to the various analog peripherals on a given 5xx device. The implications to the application can be minimal, as the REF module includes a setting that is backward compatible with the non-'A' revisions of silicon (see Section 3 for details on enabling this mode). Note that, for the purpose of future compatibility, it is recommended to use the REF module as a separate module and not in a backward-compatible mode.

At a high level, the improved features that the REF module provides are:

- Centralized trimmed bandgap with excellent PSRR, temperature coefficient, and initial accuracy
- 1.5-V, 2.0-V, and 2.5-V user selectable internal references
- Buffered bandgap voltage available to rest of system
- Power saving features
- Backward compatibility to existing reference system

Details on how to use the REF module are provided in the updated *MSP430x5xx Family User's Guide* (SLAU208), available on the MSP430 web page (www.ti.com/msp430).

2.4 Unified Clock System (UCS) Settings

The logic for the Unified Clock System (UCS) has changed slightly for 'A' revisions of silicon. The changes generally affect the conditions under which the four available reference oscillators, the reference oscillator (REFO), the very low frequency oscillator (VLO), and the two crystal oscillators (XT1 and XT2) are enabled or disabled. These differences are outlined extensively in the UCS chapter of the *MSP430x5xx Family User's Guide* (SLAU208) and should be reviewed for possible optimizations to the UCS configuration and overall power consumption. Existing UCS code should require no modification for proper execution.

2.5 Cyclic Redundancy Check Module

'A' revisions of F541x/F543x silicon add two 'reverse' registers to the Cyclic Redundancy Check (CRC) module: a CRC Data In Reverse Byte (CRCDIRB) register and a CRC Result Reverse register. Data bytes written to CRCDIRB in word mode or the data byte in byte mode are bit-wise reversed before the CRC module adds them to the signature. The bits are reversed in order to enable the MSB bits to be shifted in first to the linear feedback shift register (LFSR) that composes the CRC machine. Similarly, the CRC Result Reverse register provides the byte results of the CRC in bit-wise reversed format.

2.6 Device Errata

In the course of migrating an existing application to the MSP430F541xA/F543xA, it is recommended that the user review and carefully consider the latest device errata sheets to ensure the application is not affected by a known device issue. Furthermore, the errata sheets typically outline workarounds along with the bug descriptions. Large improvements in the errata have been made for the 'A' revisions of silicon that should be taken into account when migrating existing applications. For all MSP430 products, the device errata sheets can be found in the product folders of each product on the MSP430 web page (www.ti.com/msp430). [2]

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3 MSP430F541x/F543x to MSP430F541xA/F543xA Migration - Firmware Considerations

This section outlines important steps to consider when transitioning an existing application to an MSP430F541xA/F543xA device. In general, an application should be rebuilt on a source-code level using the appropriate header and linker command files. This is the first step towards a successful migration to an 'A' device. The following sections provide more details regarding key considerations that should be made for a successful port of the application.

3.1 PMM Default States

3.1.1 PMM Defaults: MSP430F541x/F543x

The default state of the following MSP430F541x/F543x PMM registers are not the default levels shown in the *MSP430x5xx Family User's Guide*.

3.1.1.1 PMMCTL0

15	14	13	12	11	10	9	8
PMMPW, Read as 96h, Must be written as A5h							
rw-1	rw-0	rw-0	rw-1	rw-0	rw-1	rw-1	rw-0
7	6	5	4	3	2	1	0
Reserved	**Reserved**		**PMMREGOFF**	**PMMSWPOR**	**PMMSWBOR**	**PMMCOREV**	
rw-0	r-0	r-0	rw-0	rw-0	rw-0	rw-[0]	rw-[0]

Figure 3. Power Management Module Control Register 0 (PMMCTL0)

Default level: PMMCTL0_L = 0x00 (where '_L' signifies the low byte of the register)

Actual level: PMMCTL0_L = 0x02

The PMMCOREVx bits are set to level 2 in accordance with the FLASH28 erratum.

3.1.1.2 SVSMHCTL

15	14	13	12	11	10	9	8
SVMHFP	**SVMHE**	**Reserved**	**SVMHOVPE**	**SVSHFP**	**SVSHE**	**SVSHRVL**	
rw-[0]	rw-1	r-0	rw-[0]	rw-[0]	rw-1	rw-[0]	rw-[0]
7	6	5	4	3	2	1	0
SVSMHACE	**SVSMHEVM**	**Reserved**	**SVSHMD**	**SVSMHDLYST**	**SVSMHRRL**		
rw-[0]	rw-0	r-0	rw-0	r-0	rw-[0]	rw-[0]	rw-[0]

Figure 4. Supply Voltage Supervisor and Monitor High-Side Control Register (SVSMHCTL)

Default level: SVSMHCTL = 0x4400

Actual level: SVSMHCTL = 0x4602

To monitor operation at the proper V_{CC} voltage in accordance to the PMMCOREVx level 2, the SVS and SVM high-side levels are both set to level 2. Note that the default state of the SVS and SVM high-side modules is ON (SVMHE = SVSHE = 1).

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3.1.1.3 SVSMLCTL

15	14	13	12	11	10	9	8
SVMLFP	**SVMLE**	**Reserved**	**SVMLOVPE**	**SVSLFP**	**SVSLE**	**SVSLRVL**	
rw-[0]	rw-1	r-0	rw-[0]	rw-[0]	rw-1	rw-[0]	rw-[0]
7	6	5	4	3	2	1	0
SVSMLACE	**SVSMLEVM**	**Reserved**	**SVSLMD**	**SVSMLDLYST**	**SVSMLRRL**		
rw-[0]	rw-0	r-0	rw-0	r-0	rw-[0]	rw-[0]	rw-[0]

Figure 5. Supply Voltage Supervisor and Monitor Low-Side Control Register (SVSMLCTL)

Default level: SVSMLCTL = 0x4400

Actual level: SVSMLCTL = 0x4602

To monitor V_{CORE} at the proper voltage in accordance to the PMMCOREVx level 2, the SVS and SVM low-side levels are both set to level 2. Note that the default state of the SVS and SVM low-side modules is ON (SVMLE = SVSLE = 1).

3.1.1.4 PMMRIE

15	14	13	12	11	10	9	8
Reserved		**SVMHVLRPE**	**SVSHPE**	**Reserved**		**SVMLVLRPE**	**SVSLPE**
r-0	r-0	rw-[0]	rw-[0]	r-0	r-0	rw-[0]	rw-[0]
7	6	5	4	3	2	1	0
Reserved	**SVMHVLRIE**	**SVMHIE**	**SVSMHDLYIE**	**Reserved**	**SVMLVLRIE**	**SVMLIE**	**SVSMLDLYIE**
r-0	rw-0	rw-0	rw-0	r-0	rw-0	rw-0	rw-0

Figure 6. Power Management Module Reset and Interrupt Enable Register (PMMRIE)

Default level: PMMRIE = 0x0000

Actual level: PMMRIE = 0x1100

In accordance with erratum PMM7, the SVS Low and SVS High Side POR Enable bits (SVSLPE/SVSHPE) in PMMRIE are set by default such that the SVS will be configured to trigger a POR signal in the condition that the monitored voltages fall below the SVS level(s).

3.1.2 PMM Defaults: MSP430F541xA/F543xA

The PMM levels on the MSP430F541xA/F543xA are all set to the default levels specified in the user's guide. This has an important implication on the application. The default PMMCOREVx level of zero, for example, limits the maximum DCO speed to 8 MHz. To operate at higher frequencies, the application must first increase the V_{CORE} voltage – and the respective SVS/SVM settings – during initialization procedures.

NOTE: The procedure to increment the PMMCOREVx and SVS/SVM levels requires specific steps, documented in the PMM chapter of the *MSP430x5xx Family User's Guide*. The files, msp430x54xA_PMM.h/.c, in the MSP430F543xA Code Examples implement this procedure in the SetVCore(level) function. This function should be used to increment or decrement the PMMCOREVx levels.

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3.2 Internal Voltage Reference

Figure 8 shows the REF module control register. The REF module is used to source the internal voltage references of the ADC12_A and other analog peripherals in a modular fashion with improved flexibility and stability. The simplest way to port an application that uses the ADC12 module is to reset the REFMSTR bit when initializing the ADC12 registers and to account for the increase in settling time for the internal reference, from 35 µs to 75 µs. The REF module is recommended to be used as the internal reference:

```
REFCTL0 &= ~REFMSTR;
```

REFMSTR	Bit 7	REF master control
	0	Reference system controlled by legacy control bits inside the ADC12_A module when available.
	1	Reference system controlled by REFCTL register. Common settings inside the ADC12_A module (if they exist) are do not care.

Figure 7. REFMSTR Bit Description

15	14	13	12	11	10	9	8
Reserved	**Reserved**	**Reserved**	**Reserved**	**BGMODE**	**REFGENBUSY**	**REFBGACT**	**REFGENACT**
r0	r0	r0	r0	r-(0)	r-(0)	r-(0)	r-(0)
7	6	5	4	3	2	1	0
REFMSTR	**Reserved**	**REFVSEL**		**REFTCOFF**	**Reserved**	**REFOUT**	**REFON**
rw-(1)	r0	rw-(0)	rw-(0)	rw-(0)	r0	rw-(0)	rw-(0)

Modifiable only when REFGENBUSY = 0

Figure 8. REFCTL0, REF Control Register 0

For information on using the REF module, see the *MSP430x5xx Family User's Guide* (SLAU208).

3.2.1 ADC12 Temperature Sensor Equation

There is an on-chip temperature sensor available on the analog input channel 10. The result of sampling the temperature sensor is translated to a temperature value by applying a transfer function, shown in Figure 9.

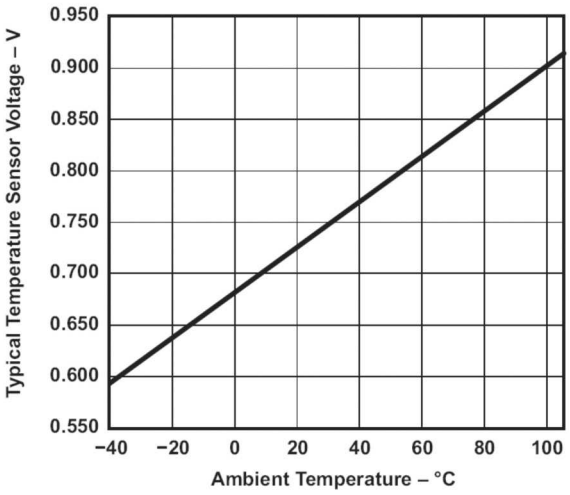

Figure 9. Typical Temperature Sensor Transfer Function

This transfer function has two key parameters that are used to calculate the Temperature in degrees Celsius, TC_{SENSOR} and V_{SENSOR} (see Equation 1).

$$V_{SENSE} = TC_{SENSOR} \times (\text{Temperature, C}) + V_{SENSOR} \quad (1)$$

The typical values for TC_{SENSOR} and V_{SENSOR} are specified in the section *12-bit ADC, Temperature Sensor and Built-In VMID* of the data sheet. It is important to note that these values differ between the MSP430F5438 and the MSP430F5438A, and this difference should be accounted for in the application.

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3.3 Bootstrap Loader (BSL)

The SYS4 erratum, fixed in the 'A' revisions, states that the Bootstrap Loader (BSL) is non-programmable. Read disturb issues when executing code from non-Main memory segments of Flash were worked around in the current BSL using carefully aligned instructions, forcing it to be locked from user edit. These read disturb issues do not affect 'A' revisions of silicon; therefore, the peripheral interface to the BSL is now user-programmable. See the MSP430 Memory Programming User's Guide (SLAU265) for further information concerning how to program the peripheral interface of the BSL.

4 References

1. MSP430F541x, MSP430F543x data sheet (SLAS612)
   MSP430F541xA, MSP430F543xA data sheet (SLAS655)
2. *Migrating From MSP430F16x to MSP430F261x* (SLAA380)
3. *MSP430x5xx Family User's Guide* (SLAU208)

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