Mitigation Methods for Parasitic Turn-on effect due to Miller Capacitor

White Paper

Introduction

One of the common problems faced when switching an IGBT is parasitic turn-on due to Miller capacitor. This effect is noticeable in single supply gate driver (0 to +15V). Due to this gate-collector coupling, a high dV/dt transient created during IGBT turn-off can induce parasitic turn-on (Gate voltage, VGE) which is potentially dangerous (Figure 1).

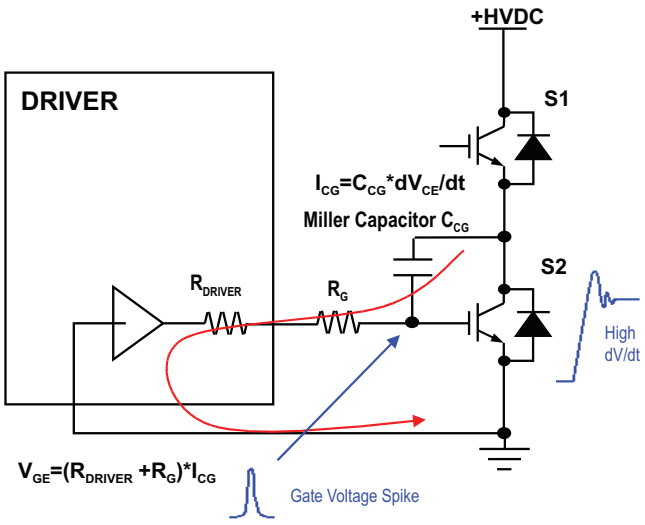

Figure 1. Bottom IGBT Parasitic Turn-On due to Miller Capacitor

Parasitic Turn-on due to Miller Capacitor

When turning on the upper IGBT, S1 in a half-bridge, a voltage change dV_{CE}/dt occurs across the lower IGBT, S2. A current flows through the parasitic Miller capacitor C_{CG} of S2, the gate resistor R_G and internal driver gate resistor, R_{DRIVER}. Figure 1 shows the current flow through the capacitor. This current value can be approximated by the following formula:

$$I_{CG} = C_{CG} \frac{dV_{CE}}{dt} \quad (1)$$

This current creates a voltage drop across the gate resistor. If this voltage exceeds the IGBT gate threshold voltage, a parasitic turn-on occurs. Designers should be aware that rising IGBT chip temperature would lead to a slight reduction of gate threshold voltage, usually in the range of mV/°C.

This parasitic turn-on can also be seen on S1 when S2 is turned on.

Parasitic Turn-on Mitigation Solutions

There are three classical solutions to the above problem; the first being to vary the gate resistor (Figure 2), second to add a capacitor between gate and emitter (Figure 3) and third to use negative gate drive (Figure 4). A fourth simple and effective solution is the Active Clamp technique (Figure 5).

Separate gate resistor for turn-on and turn-off

The on-gate resistor, R_{GON} influences the voltage and current change during IGBT turn-on. Increasing this resistor reduces the voltage and current changes but increases switching losses.

Parasitic turn-on can be prevented by reducing the off-gate resistor, R_{GOFF}. The smaller R_{GOFF} will also reduce switching loss during IGBT turn-off. However, the trade off is higher over-shoot Vce and oscillation during turn-off due to stray inductances.

Due to the above, some design optimization of both gate resistors would be required (Figure 2).

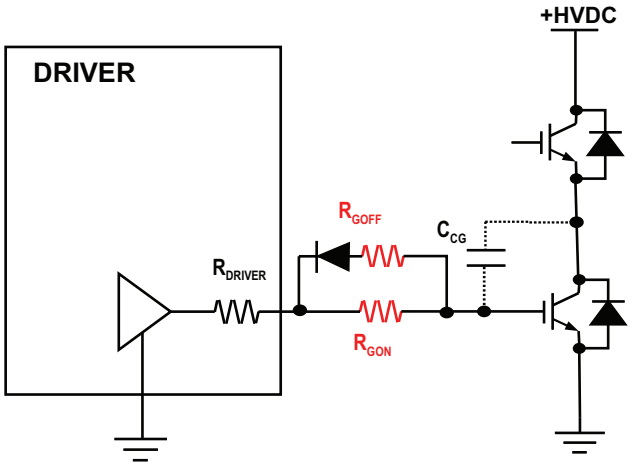

Figure 2. Separate On and Off Gate resistor

Additional gate emitter capacitor to shunt the Miller current

The additional capacitor C_G between gate and emitter will influence the switching behavior of the IGBT. C_G is to take up additional charge originating from the Miller capacitance. Due to the fact that the total input capacitance of the IGBT is $C_G||C_{CG}$, the gate charge necessary to reach the threshold voltage is increased (Figure 3).

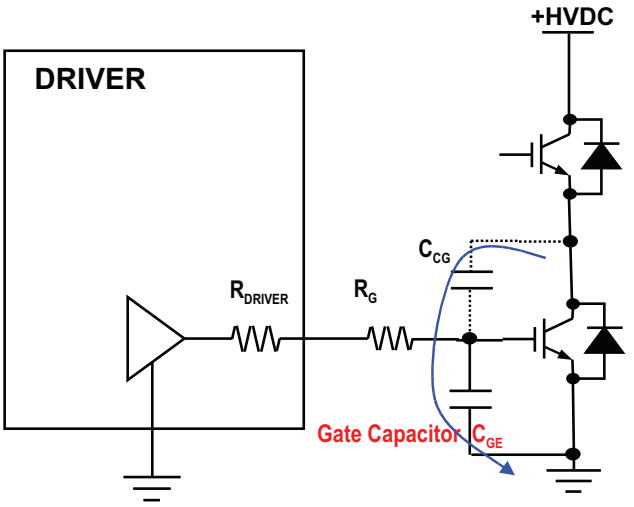

Figure 3. Additional capacitor between gate and emitter

Due to this additional capacitor, the required driver power is increased and the IGBT shows higher switching losses for the same R_G.

Negative Power Supply to Increase Threshold Voltage

The usage of negative gate voltage to safely turn-off and block IGBT is typically used in application with nominal current above 100A. Due to cost, negative gate voltage is often not utilized in IGBT application below 100A. Figure 3 shows a typical circuit using negative supply voltage.

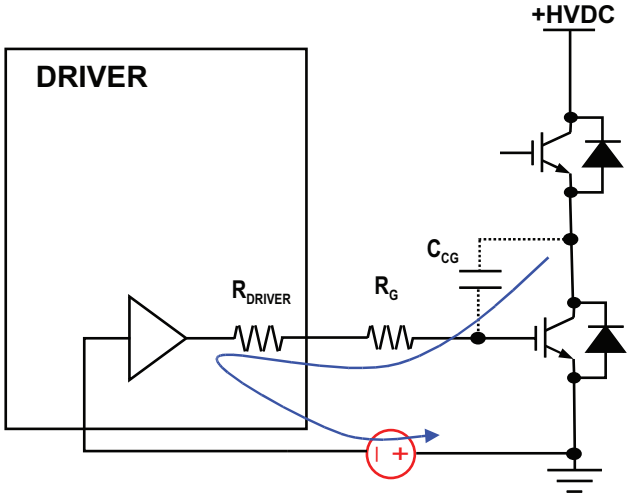

Figure 4. Negative Supply Voltage

The addition of negative supply voltage increases design complexity and size of the design.

Active Miller Clamp Solution

In order to avoid R_G optimization problem, efficiency loss due to C_G and additional cost for negative supply voltage, another measure to prevent the unwanted IGBT turn-on is proposed by shorting the gate to emitter path. This can be achieved by an additional transistor between gate and emitter. This 'switch' shorts the gate-emitter region after a certain V_{GE} is reached. The occurring currents across the Miller capacitance are shunted by the transistor instead of flowing through the output driver pin, V_{out}. This technique is called Active Miller Clamp (Figure 5).

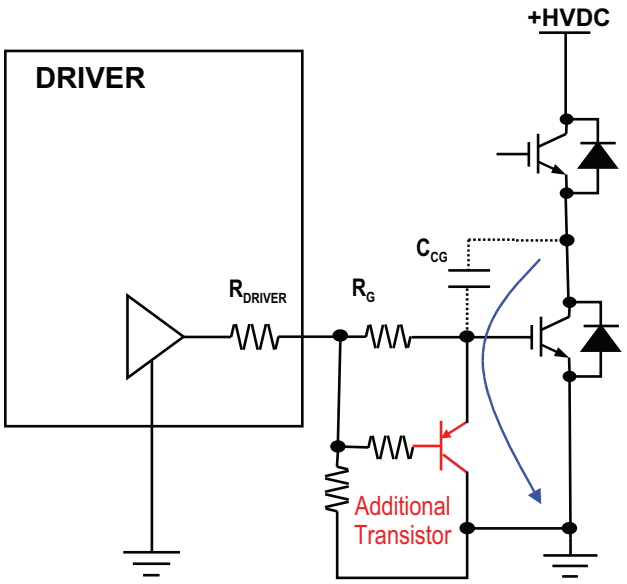

Figure 5. Active Miller Clamping using additional transistor

The addition of the transistor would increase design complexity of the driver circuit.

CONCLUSION

Table 1 shows the comparison between the four techniques presented earlier.

Table 1. Comparison of Parasitic Turn-on Due to Miller Capacitor Solutions

	Effect on reducing Miller capacitor parasitic turn-on	Cost of Solution	Switching Losses	Other Consideration
Reducing R_{GOFF}	+	Low	▼	High over-voltage, Optimization required
Additional C_{GE}	+	Low	▲	Efficiency reduce, Optimization required
Negative Supply Voltage	++	High	▼	Increase design complexity
Active Miller Clamp	++	Medium	▼	Increase design complexity

In recent years, integrated IGBT gate drivers have included the active miller clamp solution along with desaturation protection and under-voltage lock-out, namely Avago Technologies ACPL-331J and ACPL-332J. This has helped to reduce design complexity and product size for many power designers and industrial/consumer manufacturers.

References

1. Avago Gate Optocoupler Datasheet ACPL-332J
2. Avago Application Note, Active Miller Clamp
3. Semikron Application Manual, Chapter 3.5 Driver
4. International Rectifier Application Note AN983. IGBT Characteristic

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