# Miller capacitance and Gain-Bandwidth Product

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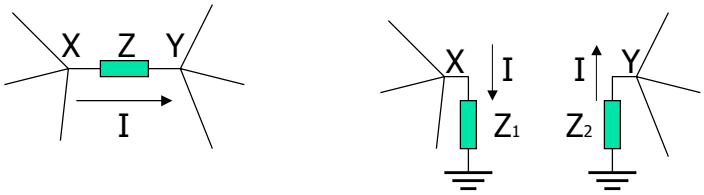
## Miller Effect

- Miller Theorem
- Miller Capacitance
  - Miller Effect in digital circuits
  - Miller multiplier
  - Impact of Miller Capacitance on propagation delay
  - Impact on Power consumption
  - Applications of Miller Effect
- Gain Bandwidth Product
- Conclusion

# Miller Theorem

An important phenomenon that occurs in many analog and digital circuits is related to "Miller Effect", as described by Miller in a theorem.

Miller theorem describes the way to convert a floating load into two grounded loads, in such way that the voltages and currents are remained unchanged.

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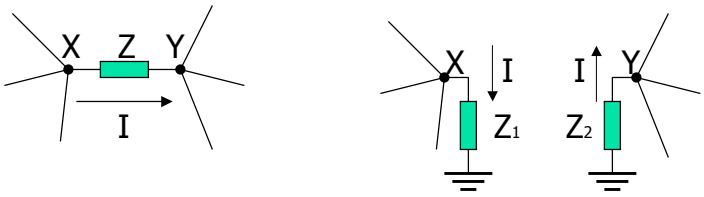
# Miller Theorem (Cont'd)




$$I = \frac{V_X - V_Y}{Z}, A = \frac{V_Y}{V_X}$$

$$V_X = Z_1 I = Z_1 \frac{V_X - V_Y}{Z} \Rightarrow Z_1 = \frac{Z}{1 - \frac{V_Y}{V_X}} \Rightarrow \boxed{Z_1 = \frac{Z}{1 - A}}$$

$$V_Y = Z_2 I = Z_2 \frac{V_X - V_Y}{Z} \Rightarrow Z_2 = \frac{Z}{1 - \frac{V_X}{V_Y}} \Rightarrow \boxed{Z_2 = \frac{Z}{1 - \frac{1}{A}}}$$

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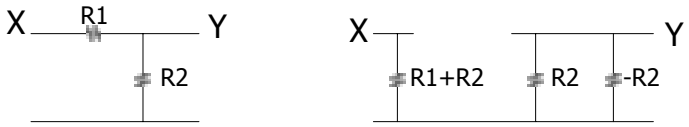
# Miller Theorem (Cont'd)

It is important to know when this theorem is valid. Miller's theorem does not stipulate the conditions under which this coversion is valid. If the impedance Z forms the only signal path between X and Y, then the conversion is often invalid.

An example of improper use of Miller effect::

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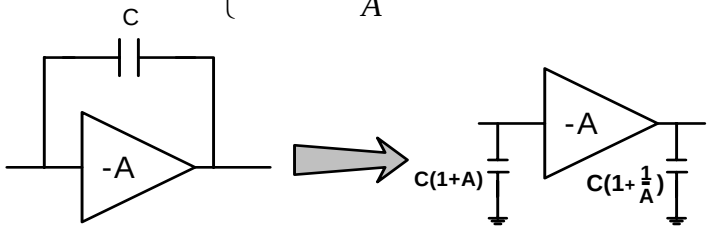
# Miller Capacitance

Assume $Z = \frac{1}{Cs} \Rightarrow \begin{cases} Z_1 = \frac{1}{(1+A)Cs} = \frac{1}{C_1 s} \Rightarrow C_1 = C(1+A) \\ Z_2 = \frac{1}{(1+\frac{1}{A})Cs} = \frac{1}{C_2 s} \Rightarrow C_2 = C(1+\frac{1}{A}) \end{cases}$

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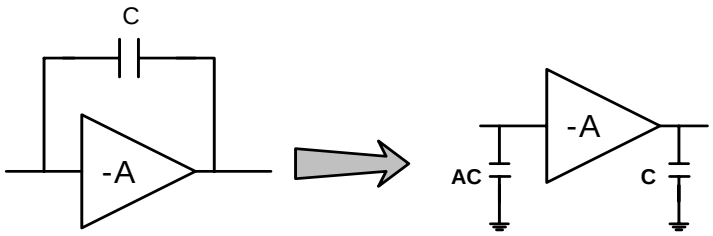
# Miller Capacitance (Cont'd)

Miller capacitance for large gain:




$$A >> 1 \Rightarrow \begin{cases} 1 + A \approx A \\ 1 + \dfrac{1}{A} \approx 1 \end{cases}$$

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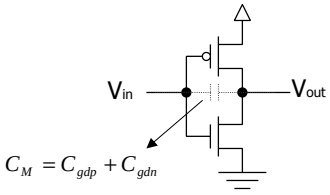
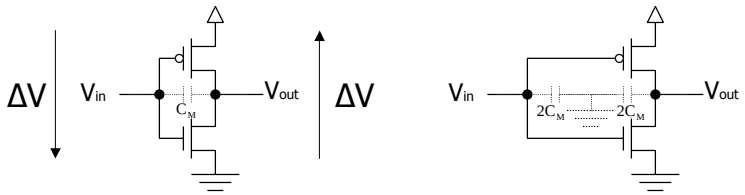
# Miller Effect in digital circuits

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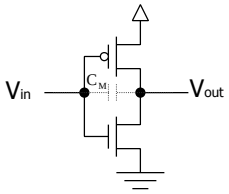
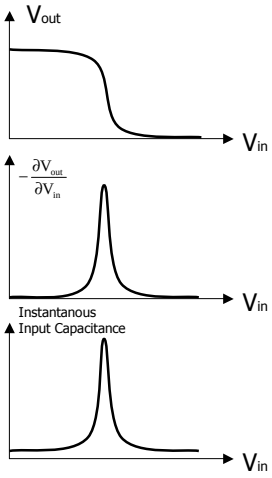
# Miller Effect in digital circuits




Instantanous Input Capacitance:

$$C_{iM}(V_{in}) = \frac{\partial Q_M}{\partial V_{in}} = C_M[1 - A(V_{in})]$$

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# Miller Multiplier

$$C_{iM}(V_{in}) = \frac{\partial Q_M}{\partial V_{in}} = C_M[1 - A(V_{in})]$$

**Miller Multiplier =** $\frac{C_{iM}}{C_M}$

As the input voltage varies,the Miller Capacitance follows the gain curve.The Multiplier is 1 across nearly the whole input range and rises to about 30 in a narrow range about $V_{inv}$ .

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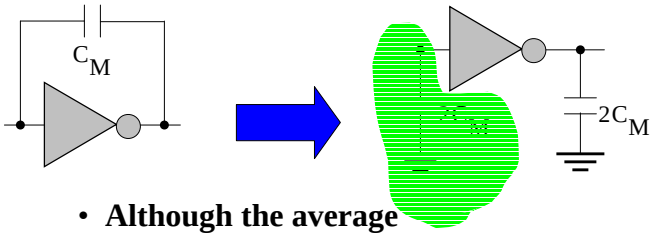
# Impact on propagation delay




- **Although the average Miller Multiplier for a full swing signal is 2, for slowly varying signal in the high gain region of the inverter can be 20 or more.**

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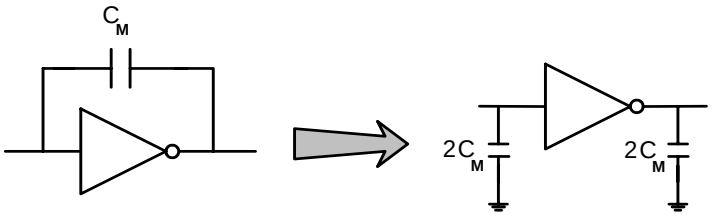
# Impact on power consumption




☑ **4 Times Greater Capacitance Increases Power Consumption**

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# Frequency Response

**A Three pole Transfer Function:**

$$H(s)=\frac{K}{(1+\frac{s}{\omega_1})(1+\frac{s}{\omega_2})(1+\frac{s}{\omega_3})}$$

$$\angle H(j\omega)=\begin{cases}0^\circ & \omega << \omega_1 \\ 270^\circ & \omega >> \omega_3\end{cases}$$

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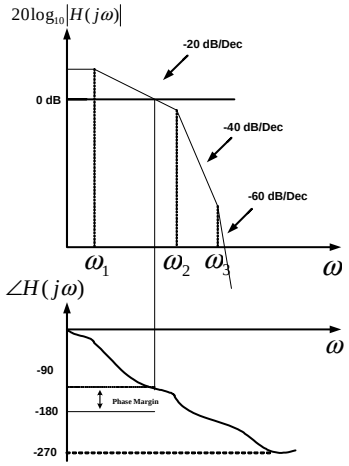
# Stability Issue (Phase Margin)




$$\phi_M = 180 + \angle H(j\omega_c)$$

***When:*** $|H(j\omega_c)| = 1$

**For Stability Phase Margin Must be Greater Than 0.**

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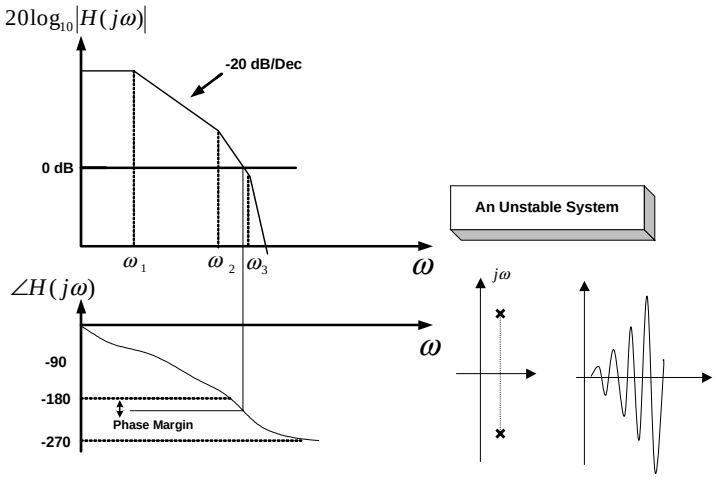
# Negative Phase Margin

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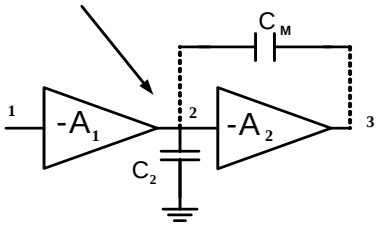
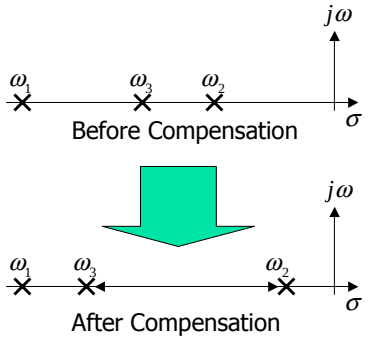
# Compensation

Assume this node gives dominant pole ( $\omega_2$ )

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# Compensation (cont'd)

**Effects of Miller Capacitance in Frequency Compensation:**

1. **Closes Dominant pole toward Origin**
2. **Causes to Split First and Second poles**
3. **Increases Phase Margin and Make System Stable**

**But:**

**REDUCES BANDWIDTH !!**

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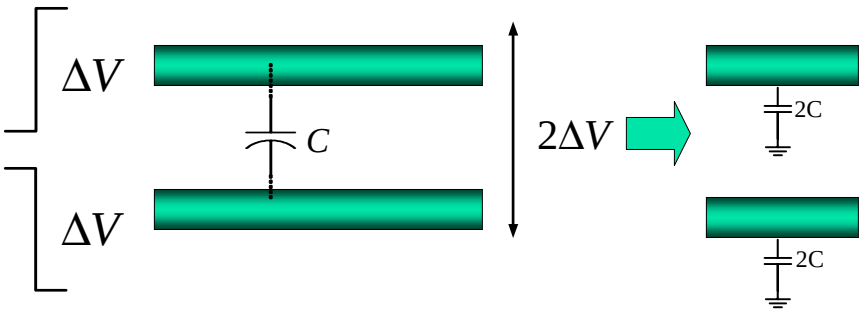
# Miller Effect Between Wires




**It seems that there is a 2 times larger capacitance between the wires.**

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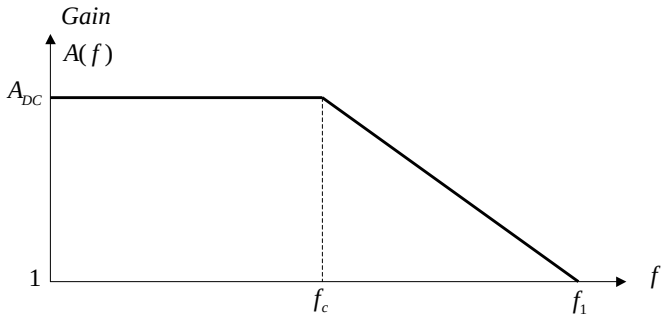
# Gain Bandwidth Product

At high frequencies the gain of the static CMOS gate is much smaller than DC gain.

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# GBP (Cont'd)

Above cutoff frequency,gain rolls off linearly with frequency crossing unity at unity-gain frequency.

In this high frequency region, the gain-bandwith product is constant:

$$fA(f) = f_1 \qquad (f > f_c)$$

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## GBP (Cont'd)

Calculating $f_1$:

For small-signal sine wave: $\frac{dv_{out}}{dt} = \frac{i}{C} = \frac{g_m v_{in}}{C}$

At the point of unity gain:

$$\omega_1 = \frac{g_m}{C} \approx \frac{I_{DSS}}{V_{DD}C} = \frac{1}{\tau} \Rightarrow f_1 = \frac{1}{2\pi\tau}$$

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## GBP (Cont'd)

Example: $\tau_{inv} = 30ps \Rightarrow f_1 = 5.3GHz$

As we know: $A_{DC} \approx \frac{4}{(V_{GS} - V_T)(\lambda_n + \lambda_p)}$

Assuming: $\lambda_n + \lambda_p = 0.2, V_{GS} - V_T = 1$

$\Rightarrow A_{DC} = 20 \Rightarrow f_c = 265\text{MHz}$

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# Conclusion

- Miller capacitance in digital applications usually slows down the speed of the circuits and increases the power consumption.
- In analog circuits Miller effect can be used to stabilize the system.
- Miller capacitance between two wires reduces noise margin and speed.
- Gain-Bandwith product is a constant value above the cutoff frequency.

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