Get Rid of the Miller Effect with Zero-Voltage Switching

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When designing power supplies, engineers often focus on the efficiency drop linked to conduction losses of their MOSFET. In the presence of large RMS currents, such as those experienced by converters operating in the discontinuous conduction mode (DCM), designers may select a low-$R_{DS(on)}$ MOSFET, which implies a bigger die size and a larger input capacitance. Thus, a reduction in conduction losses comes at the expense of greater input capacitance and the associated increase in power dissipation by the controller. The problem becomes nastier as the switching frequency increases.

Consider the typical gate current when switching a MOSFET on and off. During the on time, the peak current flowing in the controller V_{CC} pin charges the MOSFET gate to V_{CC}. During the off time, the stored current circulates back into the chip ground. If we integrate the corresponding area, actually performing

$$\int igate(t).dt\ ,$$

we obtain the gate-charge Q_g of the transistor we drive. Multiplying this value by the switching frequency F_{sw}, we obtain the average current delivered by the controller V_{CC} (the average current in the gate being null, of course). As a result, the total switching power dissipated by the controller (neglecting shoot-through losses) is:

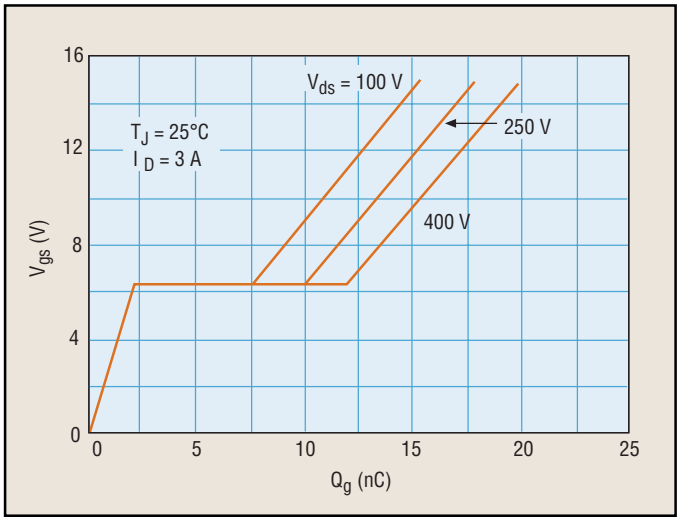

Fig. 1. *A typical MOSFET gate-charge graph.*

$$P_{drv} = F_{sw} \times Q_g \times V_{CC} \quad (1).$$

If we drive a 100-nC gate-charge MOSFET from a 12-V controller at a 100-kHz switching speed, the power dissipated in the driver will be:

100 nC × 100 kHz × 12 V = 10 mA × 12 V = 120 mW.

Zero-voltage switching may be achieved inexpensively by operating a flyback converter in quasi-resonant mode.

Given its physical construction, a MOSFET features numerous parasitic elements among which capacitors play a significant role. A basic configuration of these elements in the MOSFET would show C_{gd} as a capacitor connected from gate to drain, C_{gs} as a capacitor connected from gate to source and C_{ds} as a capacitor connected from drain to source. These terms define the following datasheet notations:

$C_{iss} = C_{gs} + C_{gd}$, where d-s is shorted
$C_{rss} = C_{gd}$
$C_{oss} = C_{ds} + C_{gd}$, where g-s is shorted.

What the driver sees is actually the gate-to-source connection. When a voltage V featuring a slope dt is applied to a capacitor C (e.g., the output voltage of our driver), it pushes a current inside the capacitor of:

$$I = C \times dV/dt \quad (2).$$

As a result, when we apply a voltage to our MOSFET, we create an input current I_{gate} equal to $I_{gate} = i1 + i2$. Using equation 2 with the right voltage nodes leads to:

$$I1 = C_{gd} \times d(V_{gs} - V_{ds})/dt = C_{gd} \times (dV_{gs}/dt - dV_{ds}/dt) \quad (3)$$

$$I2 = C_{gs} \times d(V_{gs}/dt) \quad (4).$$

When we force a voltage V_{gs} on the gate-source of the MOSFET, we know that its drain-source voltage V_{ds} will

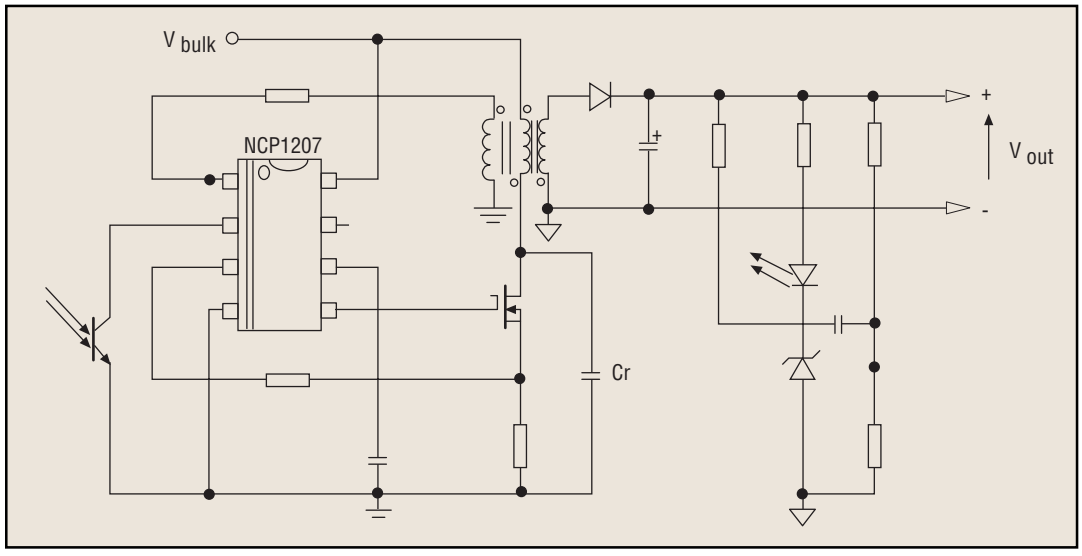

Fig. 2. *A simple QR converter based on a dedicated controller.*

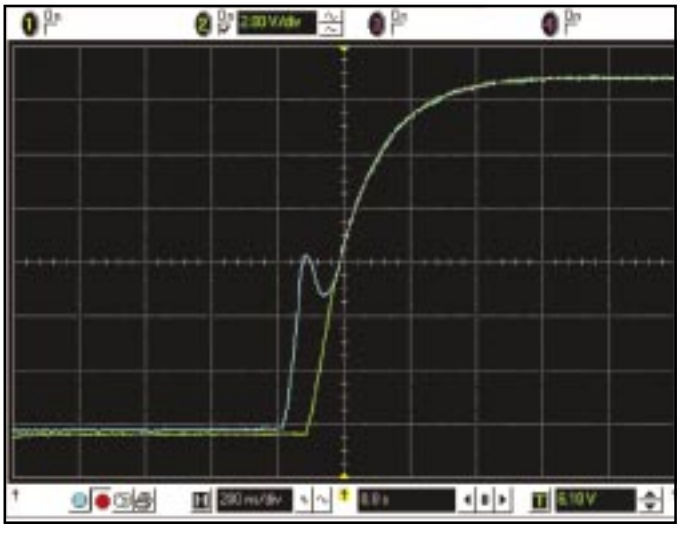

Fig. 3. *When a MOSFET switch is activated at zero V_{ds}, the Miller plateau goes away.*

move down, even if it is nonlinear. Therefore, we can define a negative gain linking these two voltages by:

$$A_v = - \delta V_{ds}/\delta V_{gs} \quad (4),$$

plugging this definition in equations 3 and 4 and factoring dV_{gs}/dt, gives:

$$I1 = C_{gd} \times dV_{gs}/dt \times (1 - \delta V_{ds}/\delta V_{gs}) = C_{gd} \times dV_{gs}/dt \times (1 - A_v) \quad (5).$$

The total equivalent capacitor C_{eq} "seen" from the gate-source electrodes during the transition (on or off) is:

$$I_{gate} = (C_{gd} \times (1 - A_v) + C_{gs}) \times dV_{gs}/dt = C_{eq} \times dV_{gs}/dt \quad (6).$$

The term $(1 - A_v)$ is called the "Miller Effect" and describes a capacitive feedback between the output and the input of an electronic device. John M. Miller first studied this phenomenon in vacuum tubes many years ago. The Miller effect actually occurs when the gate-drain voltage comes close to zero because this is where the sharpest transition takes place.

Fig. 1 represents a typical gate-charge graph of a power MOSFET. This graph is obtained by constant current charging the gate and observing the gate-source voltage. When C_{iss} suddenly increases according to equation 5, the current keeps flowing. However, because the capacitor has dramatically increased, the corresponding voltage increase dV_{gs} is severely limited; hence, the almost zero slope: This is the plateau depicted in Fig. 1.

As the Q_g graph also shows, decreasing the point from which $V_{ds}(t)$ starts to decrease during the transition helps lower the plateau effect. We can see that at V_{ds} = 100 V, the plateau width (which corresponds to injected coulombs) is reduced compared to V_{ds} = 400 V. The area below the curve goes down as well. Thus, if we manage to turn on a MOSFET when its V_{ds} equals zero, the Miller Effect disappears. The technique used to operate a power switch at zero voltage is called zero-voltage switching (ZVS).

An inexpensive way of doing this uses a flyback converter in quasi-resonant (QR) mode. Instead of turning the switch on the next clock cycle, we wait until the natural ringing on the drain pushes the voltage close to zero. At this time, detected via a dedicated pin, the controller reactivates the transistor. The ZVS operation is obtained by reflecting enough "flyback" voltage at the switch opening ($N \times [V_{out} + V_f]$), thus requiring a high-voltage MOSFET of typically 800 V (universal range). Fig. 2 shows a QR sketch based on the NCP1207 from ON Semiconductor, directly operated from the high-voltage rail. Fig. 3 shows the gate-source voltage and the drain waveform of this converter when operated in ZVS. There is no traditional Miller plateau.

In conclusion, if large Q_g MOSFETs are needed, operating a flyback converter in ZVS is a good idea to reduce the penalty linked to the average drive current. This technique also is widely employed in resonance converters. **PETech**

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