DSP-Based Multiple-Loop Control Strategy for UPS Inverters With Effective Control Delay Elimination

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Abstract This paper presents the design of a digital multiple-loop control strategy for high performance UPS inverters based on a discrete-time dynamic model. In digital control implement for UPS inverters, one of the most important factors, which limit the dynamic performance, is the control delay. The effects of different control delays in multiple-loop control system are investigated and resolved through adopting improved pulse-width modulation (PWM) methods which contributes to improve stability and robustness of the inverter system. The control method is implemented on a 16-bit single chip DSP-controller and tested on a single-phase 3.3kVA IGBT-based inverter prototype. Both the simulation and experimental results verify that the system with proposed control strategy achieves low THD (<1.9%) with nonlinear load, possesses very fast dynamic response and lends itself to linear and nonlinear load applications.

Keywords: Power electronics, UPS, inverter, control delay, multiple-loop control

1 Introduction

Uninterruptible power supplies (UPS) systems provide uninterrupted, reliable, and high quality power for vital loads, such as computer system, medical facilities, life supporting system, telecommunications, etc. They also suppress power line transients and harmonic disturbances. In UPS systems, the overall performance is mostly dependent upon the inverter performance which is measured in terms of static-state error, total harmonic distortion (THD), and the dynamic response, etc. To achieve the desired dynamic response and attain good robustness with respect to disturbance or parameter variations, multiple feedback loop control techniques with the inductor or the capacitor current feedback of the output LC filter have been applied to control the inverter[1-4]. Compared with other control schemes, multiple-loop control strategy is easy to implement and insensitivity to parameter variations[5-7]. This kind of control schemes employs an inner current loop together with an outer voltage loop to split the pair of underdamped poles caused by the LC filter so that the closed loop system can have stable and fast dynamic response, although frequency-domain-based analog control has excellent dynamic response, there are several drawbacks that hinder the performance of analog controllers, such as temperature drift, aging effect, complexity in component adjustment, and susceptibility to electromagnetic interference (EMI). With the rapid progress in microelectronics technology, digital control of power converters using advanced microcontroller and digital signal processor (DSP) becomes an active research area in this field. In digital control implement for UPS, one of the most important factors, which limit the dynamic performance, is the control delay between the sampling instant and the duty-cycle update instant.

This paper presents a digital multiple-loop control strategy for UPS inverters based on the deadbeat theory so that it can achieve fast response. Further more, to improve both the stability and the robustness of the inverter system, the effects of different control delays are investigated based on a discrete-time dynamic model and resolved through adopting improved pulse-width modulation (PWM)

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methods. Both simulation and experimental results on a single-phase 3.3kVA UPS inverter prototype are given in this paper, which verify that the system, with proposed control strategy, possesses very fast dynamic response, achieves low THD even with nonlinear load.

2 Dynamic model of the PWM inverter

Fig.1 shows a PWM inverter together with its output LC-filter. We assume only the single-phase case, since three-phase systems with neutral wire can be considered three independent single-phase systems, and a three-phase systems without neutral wire can be easily converted into two decoupled sing-phase systems in the stationary-frame(α-β) coordinates[7].

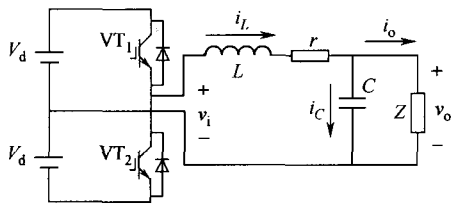


Fig.1 Main circuit of the PWM inverter with an output filter and a load

According to the circuit shown in Fig.1, the continuous time state space equations of the PWM inverter with the LC filter can be written as:

$$\begin{pmatrix} \frac{di_L}{dt} \\ \frac{dv_C}{dt} \end{pmatrix} = \begin{pmatrix} -\frac{r}{L} & -\frac{1}{L} \\ \frac{1}{C} & 0 \end{pmatrix} \begin{pmatrix} i_L \\ v_C \end{pmatrix} + \begin{pmatrix} \frac{1}{L} \\ 0 \end{pmatrix} v_i + \begin{pmatrix} 0 \\ -\frac{1}{C} \end{pmatrix} i_o \quad (1)$$

$$v_o = \begin{pmatrix} 0 & 1 \end{pmatrix} \begin{pmatrix} i_L \\ v_C \end{pmatrix} \quad (2)$$

where i_L, v_C are chosen as the state variables, the load current i_o is treated as the disturbance input and the inverter bridge output voltage v_i is the control input. Based on Eqs. (1), (2), and Fig.1 the analog model of the PWM inverter with the LC filter and a load is shown in the dashed area of Fig.2, where it can be seen that the output voltage v_o acts as a disturbance on the inductor current i_L while the output current i_o acts as a disturbance on the output voltage. In order to achieve a fast transient response and good disturbance rejec- tion, the disturbances acting on both the inductor current i_L and the output voltage v_o must be compensated or decoupled. Further more, both the dc-link voltage variation and the control delay here should be taken into consideration.

3 Analysis and design of a multiple-loop digital controller

Fig.2 shows a basic multiple-loop control scheme for the regulation of PWM inverters. Three signals are sensed as feedback signals: the capacitor current i_C, output voltage v_o, and DC-link voltage V_d. The current in the filter capacitor is sensed for the regulation of the current loop, which can achieve excellent disturbance rejection and thus provide a fast dynamic response because the disturbance i_o is involved in the current loop. The output voltage is sensed for both voltage regulation and voltage decoupling from current loop. DC-link voltage V_d variation is also feed-forward compensated through sensing V_d. In the following section, we will analyze and design the gains of the current loop and the voltage loop respectively based on the deadbeat control theory. The effects of the different control delays in multi-loop control inverters will also be analyzed in detail based on a discrete-time dynamic model.

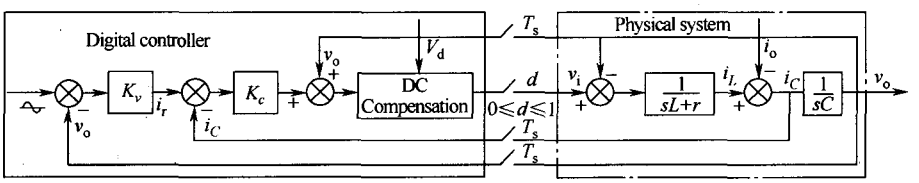


Fig.2 Basic multiple feedback loop control systems of PWM inverters

3.1 Effects of the control delay on current-loop controller

Considering a perfect output voltage decoupling from current loop and a completely compensation of dc-link voltage variation. A digital model for the current loop is depicted in Fig.3, where a zero order

holder (ZOH) is used to determine the digital equivalent model of the current loop. The discrete-time transfer function of the augmented system $P_c(z)$ shown in Fig.3 is

$$P_c(z)=Z\left[\left(\frac{1-e^{-T_s s}}{s}\right)\cdot\left(\frac{1}{sL+r}\right)\right]=\frac{1}{r}\frac{1-e^{-\frac{r}{L}T_s}}{z-e^{-\frac{r}{L}T_s}} \quad (3)$$

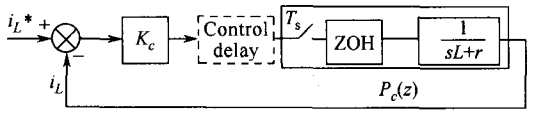


Fig.3 Digital model of the inner current loop

It is easy to get the transfer function of the current loop with no control delay is assumption as

$$\frac{i_L}{i_L^*}=\frac{K_cP_c(z)}{1+K_cP_c(z)}=\frac{K_c\frac{1-e^{-\frac{r}{L}T_s}}{r}}{z-e^{-\frac{r}{L}T_s}+K_c\frac{1-e^{-\frac{r}{L}T_s}}{r}} \quad (4)$$

The characteristic equation of the closed current loop is

$$z-e^{-\frac{r}{L}T_s}+K_c\frac{1-e^{-\frac{r}{L}T_s}}{r}=0 \quad (5)$$

The maximum gain $K_{c\_\lim}$ is designed as follows so that the root of Eq.(5) can be placed at zero to achieve deadbeat effect:

$$K_{c\_\lim}=\frac{re^{-\frac{r}{L}T_s}}{1-e^{-\frac{r}{L}T_s}} \quad (6)$$

With the design parameters given in Tab.1, one has $K_{c\_\lim}$=16.905. If we ignore the equivalent inductor resistance r, we can get

$$K_{c\_\lim}=\lim_{r\to 0}\frac{re^{-\frac{r}{L}T_s}}{1-e^{-\frac{r}{L}T_s}}=\frac{L}{T_s}$$

which is a little bigger than that of Eq.(6).

Tab.1 Parameters of the inverter system

Sampling frequency/kHz	16
Switching frequency/kHz	16
Reference sine frequency/Hz	50
Dead time/μs	2.6
Filter inductor/mH	2
Filter capacitor/μF	24.7
DC-link voltage/V	720
Output voltage (RMS)/V	220
Output capacity/kVA	3.3

It is a unique feature for a digital control system to achieve its fast dynamic response if all the closed-loop poles are placed at the origin of a z-plane.

Unfortunately, a time delay, due to both the analog-to-digital (A/D) conversion time in sampling system variables and the computation time needed to determine the switching pulse-width, is introduced in these digital feedback control systems. This can significantly affect the performance of the inverter. The control delay T_d is denoted as $(1-m)T_s$, where m is control delay factor, $0\leqslant m\leqslant 1$. The discrete-time transfer function of the current loop with control delay T_d becomes

$$\frac{i_L'}{i_L^*}=\frac{K_c\frac{1-e^{-aT_s}}{r}(mz-m+1)}{z^2+z(mK_c\frac{1-e^{-aT_s}}{r}-e^{-aT_s})+(1-m)K_c\frac{1-e^{-aT_s}}{r}} \quad (7)$$

where, $a=r/L$. Substitution of Eq.(6) to Eq. (7), the two roots of the characteristic equation given by the transfer function (7) can be written as

$$z_{1,2}=\frac{(1-m)e^{-aT_s}\pm\sqrt{(1-m)^2e^{-2aT_s}-4(1-m)e^{-aT_s}}}{2} \quad (8)$$

The roots locus of Eq.(8) with the control delay factor m variation was described in Fig.4. One must emphasize that the effect of the control delay in the current loop is very important. Traditionally, the current gain as given by $K_{c\_\lim}$ shown in Eq. (6) is used for a deadbeat control implementation if no control delay is assumed. Eq.(8) and Fig.4 illuminate that the control delay will transform a first order system with a pole in the origin into a second order system with two com- plex conjugate poles located on the vicinity of unity circle. One-sample period delay will especially lead to the two complex conjugate poles located on the unity circle and the stability cannot be guaranteed. The unit-step response of the closed current loop, shown in Fig.5, demonstrates that the closed-loop output will completely follow the step command after one sampling period without any control delay (Fig.5a). While with half-sampling period control delay, unit-step response exhibits over-shooting and ringing, the closed-loop output will follow the step command after several sampling periods (Fig.5b).

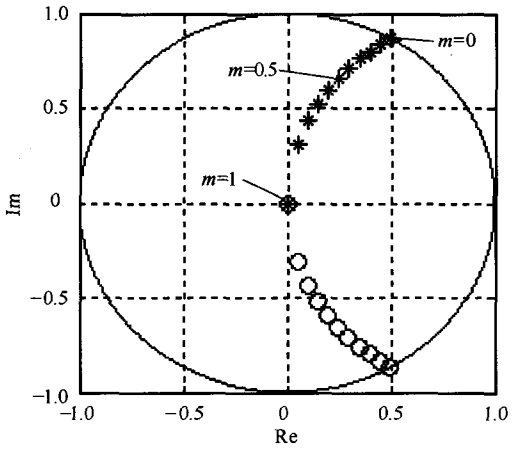
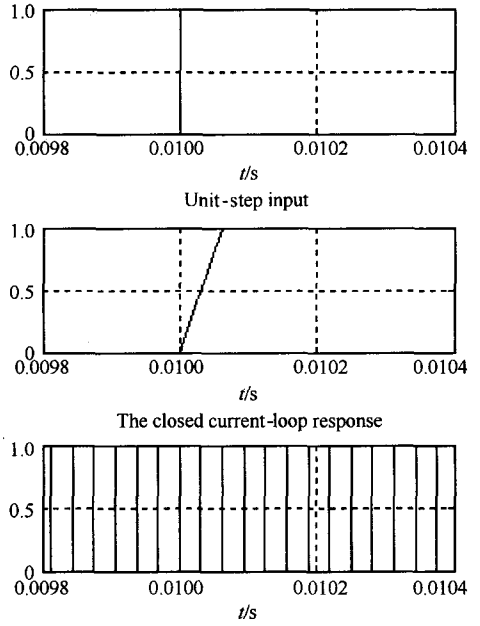


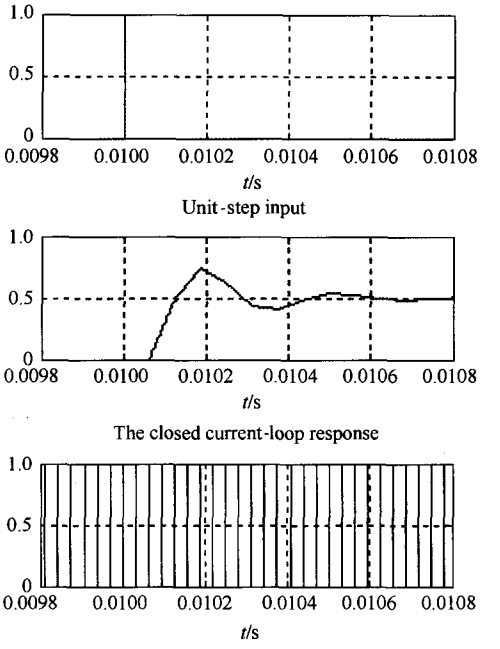
Fig.4　Roots locus of closed current loop with control delay increasing from 0 to T_s

As aforementioned, a traditional digital control implementation for a UPS inverter introduces a time delay equal to one switching period, strongly limiting the system bandwidth, the control delay can be reduced to half of the switching period in the "double-update" mode. Following methods were proposed to deal with the control delay in the previous references:

（1）Decreasing the current gain[8]. To guarantee the stability, $K_c \leqslant K_{c\text{-lim}}$has to be satisfied. A smaller current gain will make the system more robust but the current bandwidth will be reduced and as a result, the output impedance of the inverter will be increased; thus, the distortion will increase in the presence of nonlinear loads[2].



(a) No control delay is assumed



(b) With half period control delay

Fig.5　Unit-step response of the closed current loop

（2）State observer[7-10]. The control delay can be compensated by a state observer, however, this algorithm requires inverter models, and it increases the complexity of the calculations required to determine the pulse-width. Further more, it introduces additional errors in the system due to the estimation or prediction errors.

（3）Modified PWM methods, which contain two-polarity method, asymmetric PWM method, and so on[11]. This method can totally avoid the dependency on accurate inverter models and easy to implement by using a digital micro-controller.

（4）Kalman filter[12], predictor based on autoregressive, external input model of inverters [13-14].

3.2　A modified PWM method to eliminate the control delay[11]

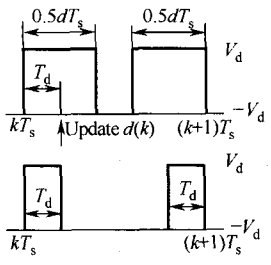
For an inverter system with a digital controller, as shown in Fig.6, execution of pulse-width calculation for a k^{th} sampling interval is started at $t=kT_s$. After the execution time T_d, the pulse-width is determined at $t=kT_s+T_d$. Usually, the calculation results for the k^{th} sampling interval will be updated during $(k+1)^{th}$ sampling interval which introduced one sampling period control delay.

If we update the calculation results for the k^{th} sampling interval at the instant $t=kT_s+T_d$, we can minimize the control delay. For a PWM pattern with active-low polarity, shown in Fig.6a, the pulse is located at the two ends of the switching interval. The pulse-width should be large enough since the pulse cannot fall during the execution time T_d, which means the minimum pulse-width ratio d_{min} is limited to $d_{min}=\frac{2T_d}{T_s}$, shown in the bottom diagram of Fig.6a. Thus, when the PWM pattern with active-low polarity as shown in Fig.6a, the available pulse-width ratio d is limited to

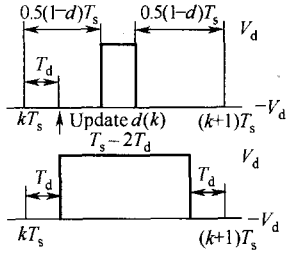
$$\frac{2T_d}{T_s}<d(k)<1 \tag{9}$$

Another kind of PWM pattern with active-high polarity is shown in Fig.6b. Unlike in Fig.6a, when the PWM pattern with active-high polarity, the pulse is centered in the sampling interval and the pulse-width should be small enough since the pulse cannot be produced during the execution time T_d. The available pulse-width ratio d is limited to

$$0<d(k)<\frac{1-2T_d}{T_s} \tag{10}$$



(a) Active-low polarity and limitation of minimum pulse-width



(b) Active-high polarity and limitation of maximum pulse-width

Fig.6 Two PWM patterns

From Eqs.(9) and (10), we found that a smaller T_d, which means less program processing time, but leads to a larger range of pulse-width ratio d with each PWM pattern. When $T_d\leqslant 0.25T_s$, the modified PWM method with both polarities can be used for the full range of the duty ratio, $0<d(k)<1$. If setting the duty-ratio threshold at which the changeover from active-high to active-low (active-low to active-high) occurs at 0.5, the PWM pattern with active-low polarity is applied for a large duty ratio ($0.5<d(k)\leqslant 1$ =, while the PWM pattern with active-high polarity is applied for a small duty ratio ($0<d(k)\leqslant 0.5=$. Thus, the full range of duty ratio between 0 and 1 is achieved on condition that the maximum value of execution time T_d is $0.25T_s$.

With DSP implementation, adding hysteresis ($+D_{hys}$) to duty-ratio changeover threshold, the PWM pattern works as follows:

(1) $0<d(k)\leqslant 0.5-D_{hys}$: PWM pattern with active-high polarity $0.5-D_{hys}<d(k)\leqslant 0.5+D_{hys}$: Keeping the PWM pattern same as last sampling period.

(2) $0.5+D_{hys}<d(k)\leqslant 1$: PWM pattern with active-low polarity.

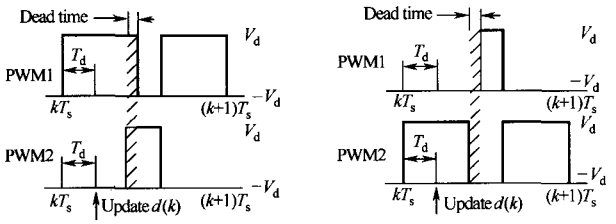
Although adding the hysteresis will reduce the maximum value of execution time T_d from $0.25T_s$ to $(0.25-0.5D_{hys})T_s$, it has following advantages:

(1) Avoiding several times alternation form active-high to active-low (active-low to active-high) at the preset duty-ratio threshold, which may distort the output voltage.

(2) The point where the PWM pattern is changed, move from 0.5 to $0.5+D_{hys}$, which indicates that the output voltage is more smooth because of smaller disturbance on inverter bridge output voltage v_i introduced by PWM pattern alternation.

To avoid shoot-though of two switching devices in each leg of the inverter, a dead time should be inserted to the PWM gate signals. Nowadays, most DSP's PWM circuits associated with compare units make it possible to generate PWM signals with programmable dead time and output polarity. Fig.7 demonstrates typical PWM signals of one leg with inserted dead time (TMS320LF240X DSP of TI Company). It shows that PWM1&PWM2 are both high level with active-low polarity while PWM1& PWM2 are both low level with

active-high polarity in the dead time interval, shown in Fig.7a and Fig.7b respectively. The level of each PWM pattern is different with each other in the dead time interval, therefore the internal dead-time generation unit of DSP is not available. An external dead time gener- ation unit using CPLD or analog implement is alternative.



(a) Active-low polarity　　(b) Active-high polarity

Fig.7　Two PWM pattern with dead time

3.3 Voltage-loop controller design

Since control delay can be eliminated by the modified PWM pattern, the inner current loop can reject most of the disturbance and follow the current command faithfully, it is reasonable to neglect the dynamic of inner current loop and take it as a constant gain in design of the outer loop controller. According to the simplified model, shown in Fig.8, the discrete-time transfer function of the outer loop is

$$\frac{v_o}{v_r}=\frac{K_v\dfrac{T_s}{C}}{z+K_v\dfrac{T_s}{C}-1} \tag{11}$$

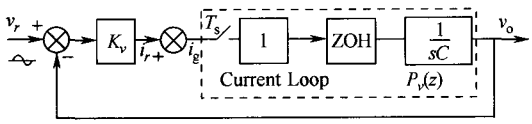


Fig.8　Digital model of the outer voltage loop

Similarly, we place the root of the closed-loop system at zero to achieve deadbeat effect, the gain K_v can be designed as

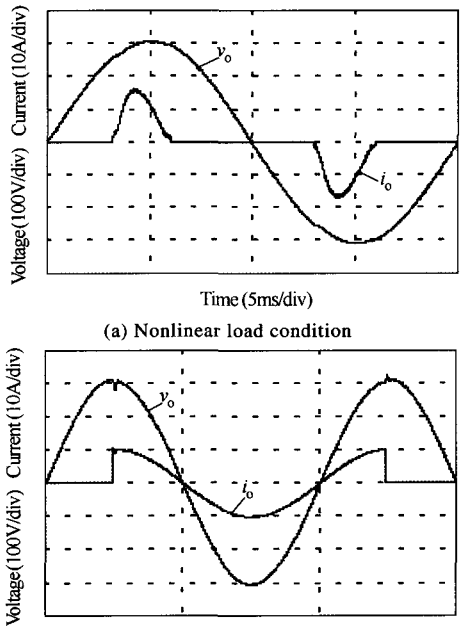
$$K_v=\frac{C}{T_s} \tag{12}$$

Substitution of parameters given in Tab.1 to Eq.(12) leads to K_v=0.3952.

4 Simulations and experimental results

The simulation and experimental verification of the developed digital multiple-loop control scheme is carried out on a single-phase 3.3kVA UPS inverter with specification shown in Tab.1.

The digital controller depicted in Fig.2 was simulated in the discrete time domain. The current loop gain and the voltage loop gain are given by Eqs.(6) and (12) respectively. Fig.9a shows output voltage wave with a nonlinear load, while Fig.9b shows the dynamic response to abrupt load change condition.



(a) Nonlinear load condition

(b) Abrupt load change

Fig.9　Simulation results of output voltage and current

The control algorithm has also been implemented by a 16-bit DSP chip TMS320LF2407A, which offers an increased processing performance (40MIPS). For comparison purpose, experiments with traditional multiple-loop controller proposed in Ref.[4] were also carried out, the results of which are shown in Fig.10, where the control time delay equals to one switching period. The traditional multiple-loop control inverter with the large current gain (half of K_{c_lim} in Eq.(6)) will lead to instability shown in Fig.10a, while with a smaller gain will increase the distortion of output voltage shown in Fig.10b, which validated the analysis in section 3.

Fig.11a～Fig.11c show the experimental results of output voltage and current under nonlinear load, abrupt load change, and resistance load condition with proposed modified PWM method. In our experimental system, only 7.2μs was needed for sampling and

calculation which is short enough to satisfy $T_d < (0.25-0.5D_{hys})T_s$, where $D_{hys}=0.05$. The experimental results show that the output voltage has very low distortion under both resistance load and nonlinear load condition. At the same time, the system has fast dynamic response, we can find the output voltage with small over-regulating magnitude and short regulating time against load change.

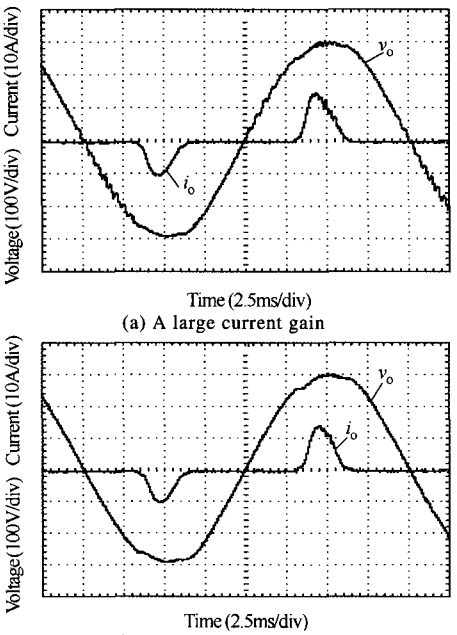
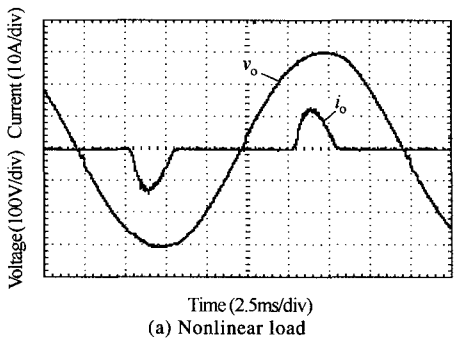


Fig.10 Experimental results of traditional multiple-loop control inverter with one-sample period delay

Both simulation and experimental results given above confirm that the proposed digital multiple-loop with modified PWM pattern is capable of maintaining good steady-state and dynamic response. The THD of the output voltage under various load condition are given in Tab.2, which demonstrate the system with proposed control strategy has significant improvement in reducing the THD of the output voltage values under nonlinear condition.



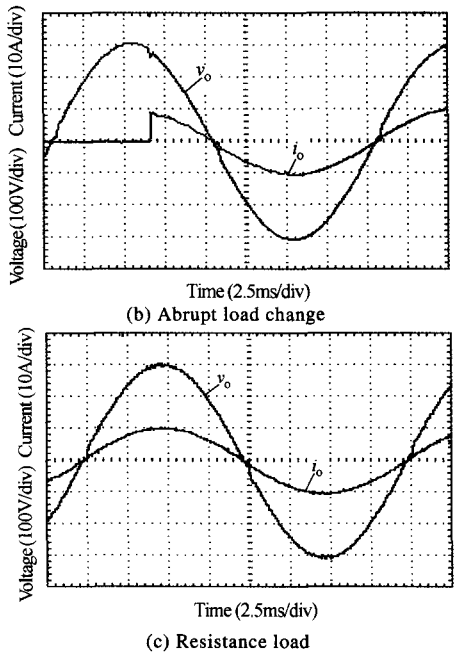


Fig.11 Experimental results of output voltage and current

Tab.2 THD of output voltage

	No load	Nominal resistance load	Nonlinear load
Simulation results (%)	0.571	0.8065	1.289
Experimental results (%)	1.103	1.333	1.899

5 Conclusion

This paper presented a DSP-based high performance multiple-loop control strategy for the UPS inverter, which incorporates an inner capacitor current loop and an outer voltage loop to regulate the output voltage, the corresponding gains are designed based on deadbeat theory so that the PWM inverter can achieve fast dynamic response. In addition, the dc-link voltage variation is compensated with feed-forward loop. Further more, one of the most important factors, which limit the dynamic performance, is the control delay. The effect of control delay is investigated in detail and resolved through adopting improved pulse-width modulation (PWM) methods. Both the simulation and experimental results verify that the system with proposed control strategy possesses outstanding stead-state & dynamic performance and lends itself to linear and nonlinear load applications.

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Brief notes

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基于 DSP 的有效消除数字控制延时的 UPS 逆变器多环控制策略

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摘要　基于逆变器离散动态模型提出了一种高性能 UPS 逆变器多环控制方案，在数字控制 UPS 逆变器中，控制延时是限制其动态性能的一个重要因素，本文详细分析了不同控制延时对多环控制逆变器性能的影响，比较了各种消除逆变器控制延时的方法，采用了更改 PWM 有效模式的方法以有效消除控制延时，该方法简单可靠，不会涉及预测误差，并且很容易用 DSP 控制器实现。控制延时的有效消除极大改进了逆变器系统的稳定性和鲁棒性。此外，内外环增益通过无差拍控制理论确定以实现快速动态响应。将本文提出的控制策略应用于 16 位定点 DSP 控制的 3.3kVA 的逆变器样机中，并对比了传统的多环控制逆变器系统，仿真和实验结果表明，本文提出的控制方法能实现非线性负载下低 THD (<1.9%)，快速动态响应，适用于线性和非线性负载。

关键词：电力电子　UPS　逆变器　控制延时　多环控制

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