Entertainment Services and Technology Association

United States Institute for Theatre Technology, Inc.

DRAFT

BSR E1.11, Entertainment Technology - USITT DMX512-A Asynchronous Serial Digital Data Transmission Standard for Controlling Lighting Equipment and Accessories

Revision 3

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Foreword

The **Entertainment Services and Technology Association** (ESTA) is a non-profit trade association representing the North American entertainment technology industry. Its members include dealers, manufacturers, manufacturer representatives, service and production companies, scenic houses, designers and consultants. The Association addresses areas of common concern such as technical standards, customer service, equipment quality, business practices, insurance, and credit reporting, and provides a wide variety of services to Members.

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The **United States Institute for Theatre Technology, Inc**. (USITT) is the Association of Design, Production, and Technology Professionals in the Performing Arts and Entertainment Industry. Founded in 1960, the mission of the Institute is to advance the professions of design and technology in the performing arts by disseminating information, actively promoting the advancement of knowledge and skills and facilitating national and international communication among its members. USITT is the United States Center of OISTAT, the International Organization of Scenographers, Theatre Architects and Technicians.

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Introduction

The original version of the DMX512 Standard was developed in 1986 by the Engineering Commission of the United States Institute for Theatre Technology, Inc. (USITT). Minor revisions were made in 1990. DMX512 has gained international acceptance throughout the entertainment industry, even though USITT is not formally accredited as a standards making body. The earlier versions of this Standard covered only data used by dimmers. In practice this Standard has been used by a wide variety of devices; this version recognizes this fact.

In 1998, it became evident that additional updates to the Standard were necessary and formal recognition through an internationally recognized standards organization was required. The USITT DMX512 Subcommittee issued a Call for Comments in order to solicit recommendations for changes to the Standard. At the same time, USITT transferred maintenance of DMX512 to the Entertainment Services and Technology Association (ESTA), which is the secretariat for the ANSI Accredited Standards Committee *E1, Safety and Compatibility of Entertainment Technical Equipment and Practices* (more commonly known as the ESTA Technical Standards Program - TSP).

A Task Group established under the ESTA TSP's Control Protocols Working Group acted on the proposals received in response to the Call for Comments. The primary goal was to make editorial updates to DMX512 appropriate for current times, including the addition of technical features while maintaining a balance with backward compatibility. Many proposals, while technically innovative, could not be accepted because their implementation would not have been backward compatible and would have immediately rendered obsolete most of the installed base of equipment.

This document is a result of the actions taken on those proposals and subsequent development under the *Policies and Procedures* of the ESTA Technical Standards Program.

1 General

1.1 Scope

This Standard describes a method of digital data transmission between controllers and lighting equipment and accessories, including dimmers. It covers electrical characteristics, data format, data protocol, connector type, and recommended cable types.

This Standard is intended as a guide for:

1. Equipment manufacturers and system specifiers who wish to integrate systems of lighting equipment and accessories, including dimmers, with controllers made by different manufacturers.
2. Equipment manufacturers seeking to implement a standard digital transmission protocol in their lighting control and accessory products.
3. System specifiers and consultants to gain detailed information about recommended cable types and allowed connectors.

This standard is not intended to replace existing protocols other than USITT DMX512 and DMX512/1990.

Equipment compliant with this standard will be marked DMX512-A in order to distinguish it from the previous (informally recognized) versions. Unless otherwise noted, references to DMX512 in this document refer to DMX512-A.

1.2 Overview and Architecture

This standard uses a simple asynchronous eight-bit serial protocol consisting of an untyped byte stream produced by standard UARTs, The physical media is normally, but not exclusively, a two-pair cable, with each pair serving as a data link. The media is driven using ANSI/TIA/EIA-485-A-1998 (hereafter referred to as EIA-485-A in this document) balanced data transmission techniques. Physical connection at devices is via 5-pin XLR connectors or by “hard-wiring” to terminals.

The first pair of wires in any DMX512 data cable is used as the primary data link. The second pair, when implemented, is used for a variety of purposes, all of which fall within the scope of EIA-485-A, but not defined in this standard. Identification of the required circuit topology for any particular implementation is defined.

Certain exceptions to the above cabling and connection schemes are permitted where detailed in this standard.

Data on the primary data link is sent in packets of up to 513 slots. The first slot is a START CODE, which defines the information in the subsequent slots in the packet. The interoperability of equipment complying with the standard is largely due to the use of the NULL START Code by transmitting devices. A NULL START Code is one that contains eight data bits all of zero value (a NULL byte) and indicates that all subsequent data within the packet is sequentially numbered bytes of uncategorized data. Proper function is dependent upon the receiving device(s) isolating the pertinent data for processing from each transmitted packet.

1.3 Appropriate uses of this Standard

Equipment designers and general users of this Standard must recognize that this Standard is intended to fill only a limited range of uses. Other standards will be more appropriate for different uses. This is not intended to support a venue wide network that can carry data for lighting, sound, and scenery mechanization, for example, all on the same wire.

This Standard performs no error checking of NULL START Code packets. There is no assurance that all DMX512 packets will be delivered. It is common practice for merge units and protocol convertors to drop packets that they cannot process in a timely manner. The 1986 and 1990 versions of the USITT Standard specifically allow dimmers to ignore packets that they cannot process in a timely manner, and this concept survives in this version of the Standard with respect to NULL START Code packets.

1.4 Classes of data appropriate for transmission over links designed to this Standard

DMX512 is designed to carry repetitive control data from a single controller to one or more receivers. This protocol is intended to be used to control dimmers, other lighting control devices and related non-hazardous effects equipment.

1.5 Classes of data not allowed on this Standard

DMX512 is not an appropriate control protocol for hazardous applications, including but not limited to Pyrotechnic Control and Scenery Mechanization.

Data that controls any device that has a reasonable potential to cause serious physical injury shall not be transmitted over data links built to this Standard. No one shall make, market, or sell such a system while claiming to be DMX512 or DMX512 compatible or any similar such wording.

1.6 Compliance

Compliance with this Standard is strictly voluntary and the responsibility of the manufacturer. Markings and identification or other claims of compliance do not constitute certification or approval by the E1 Accredited Standards Committee. See clause 11 for Marking and Disclosure requirements.

2 Normative references

ANSI/TIA/EIA-485-A-1998 *Electrical Characteristics of Generators & Receivers for Use in Balanced Digital Multipoint Systems*

This standard will be referred to as EIA-485-A in this document.

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Note: EIA-485-A is compatible with: *ISO/IEC 8482:1993 Information Technology - Telecommunications and information exchange between systems - Twisted pair multipoint interconnections*.

ISO/IEC 11801 *Information Technology – Generic cabling for customer premises*

ISO/IEC 646 *Information Technology - ISO 7-bit Coded Character Set for Information Interchange*

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3 Definitions

3.1 Asynchronous: signals that start at any time and are not locked or synchronized to the receiving device by a separate clock line.

3.2 Balanced Line: a data communications line where two wires are present, the signal and its opposite (complement), the actual signal being the difference between the voltages on the two wires. Balanced lines have excellent noise and interference rejection properties.

3.3 Break: a high to low transition (space) followed by a low of at least 88 microseconds followed by a low to high transition.

3.4 Common: see Data Link and Signal Common.

3.5 Common-Mode Voltage: a voltage appearing equally on the data + (plus) and data - (minus) lines relative to signal common. $Vcm = (Va + Vb)/2$ where:

Vcm is the Common Mode Voltage
Va is the voltage on DMX512 data + with respect to signal common
Vb is the voltage on DMX512 data - with respect to signal common

3.6 Controller: a transmitting device that originates DMX512 data.

3.7 Data +: true signal.

3.8 Data -: complementary data signal.

3.9 Data Link: physical connection between transmitting and receiving devices.

3.10 Data Link Common: the connection to signal common at the point of interconnection (DMX512 Port) of the product.

3.11 DMX512 Port: see Port.

3.12 DMX512 Processing Device: a piece of equipment that regenerates the timing of any DMX512 packet or has provision for other signal inputs from which the outgoing DMX512 packet is generated. In the absence of any DMX512 transmitting capability, the device has provision for other signal outputs which are controlled in some manner by the incoming DMX512 packet. Basic buffer products are not normally considered processing devices.

3.13 Driver: the circuit which drives the transmit signal and is directly connected to the DMX512 line. See Line Driver.

3.14 Enhanced Functionality: Active use of the optional secondary data link of a DMX512 port.

3.15 Idle: the time that the DMX512 line is high and not sending any information (also known as the 'Mark' condition).

3.16 In-Line Device: any component that receives and re-transmits DMX512.

3.17 Isolation: circuit topology in which the output is completely electrically disconnected from the input.

3.18 Isolation voltage: voltage specification between input and output stages of an isolated system at or below which damage or breakdown of circuit components will not occur.

3.19 Legacy Equipment: transmitting and receiving devices complying with the original USITT DMX512 or DMX512/1990 in all aspects of those standards. (Exception: receiving devices that are not dimmers but comply with all other aspects of DMX512/1990 shall be considered to be Legacy Equipment.)

3.20 LEN: (Load Equivalent Number) the number or fractions of Unit Loads as defined by EIA-485-A.

3.21 Line Driver: an electrical circuit providing differential voltage excursions on a data link, operating within a defined Common Mode voltage range and with a specified response to overload and overvoltage conditions.

3.22 Line Receiver: an electrical circuit allowing detection of differential voltage excursions on a data link, operating within a defined Common Mode voltage range and with a specified response to overload and overvoltage conditions.

3.23 Loop-Through Connection: a connector or terminal port which connects the signals present on at least Pins 1, 2 and 3 of one port to another port. Frequently abbreviated to Loop or Thru.

3.24 Manufacturer ID: a two-byte value assigned to a Manufacturer/Organization by the E1 Accredited Standards Committee for use with Alternate START Codes 91h and CFh. This ID serves as an identifier that the data following in that packet is proprietary to that entity and should be ignored by all others.

3.25 Mark: a line condition where Signal True is high with respect to Signal Complement.

3.26 MAB (MaB): Mark After Break – the period of time between the low to high transition which signifies the end of Break and the high to low transition which is the start bit of the START Code (slot 0).

3.27 MBB (MbB): Mark Before Break – the period of time between the end of the last stop bit of the last slot and the high to low transition which signifies the start of Break.

3.28 Merge Unit: a product comprising one or more receiving devices and one or more transmitting devices that generate a DMX512 packet derived from the manufacturers declared logical combination of the DMX512 input packets.

3.29 NULL START Code: a START Code with a value of 00h.

3.30 Packet (in DMX512-A): a Reset Sequence followed by all slots up to a Mark Before Break and the start of the next Reset Sequence.

3.31 Port: a DMX512 signal connection point (connector or terminal strip).

3.32 Receiver: see Line Receiver.

3.33 Receiving Device: a piece of equipment which accepts a DMX512 signal.

3.34 Reset: see Break.

3.35 Reset Sequence: a sequence of a Break, Mark After Break, and START Code.

3.36 Signal Common: the common reference (zero volt supply) of the EIA-485-A driver or receiver circuitry.

3.37 Slot: a sequentially numbered framed byte in a DMX512 packet. A single Universe contains a maximum of 513 Slots, starting at slot 0. Slot 0 is the START Code.

3.38 Slot Footprint: the number of slots of data used by a product in its operation.

Note: A 24 way dimmer rack may have a footprint of 24, it may be more if some slots are used to provide additional control functions using NULL START Code packets. Automated fixtures usually require a Slot Footprint of greater than one.

3.39 Space: a line condition where Signal True is low with respect to Signal Complement.

3.40 Start Bit: the extra bit attached to the beginning of a byte to indicate to the receiver that a new byte is being sent. The start bit is always low, i.e., Space.

3.41 START Code: the first slot sent after Break, indicating the type of information to follow.

3.42 Stop Bit: the extra bit(s) attached to a byte to indicate the end of the byte – DMX512 has 2 stop bits. The stop bit is always high, i.e., Mark.

3.43 Terminator: a device or circuit topology that is designed to minimize unwanted signal reflections on a data link.

3.44 Transmitting Device: a piece of equipment that produces a DMX512 signal.

3.45 UART: Universal Asynchronous Receiver/Transmitter

3.46 Universe: a DMX512 data link originating from a single DMX512 source. Control of up to 512 DMX512 data slots comprises a single universe.

3.47 Update (Refresh) Rate: the number of DMX512 packets with a NULL START Code sent per second.

4 Electrical Specifications and Physical Layer

4.1 General

Except where specifically called out in this document the electrical specifications of this Standard are those of EIA-485-A. Where a conflict between EIA-485-A and this document exists, this document is controlling as far as this Standard is concerned.

The physical layer of a DMX512 data link is constrained by earth grounding practices, termination methods, signal levels, EMC, and accidental damage by connection to other devices.

Equipment designers shall pay particular attention to EIA-485-A requirements for line drivers, line receiver design, line voltage levels, line loading, and the Common Mode requirements of EIA-485-A. Further, equipment designers must comply with the non EIA-485-A requirements of clauses 5 and 6.

4.2 Electrical isolation

EIA-485-A makes no general provisions for electrical isolation. However, this Standard does, and suitable optical isolation, transformer isolation, or other means may be employed to prevent the undesirable propagation of voltages which exceed the Common Mode limits of EIA-485-A (see clauses 5 and 6). The inclusion of such isolation does not, however, alter the requirement that a transmitter or receiver shall conform to EIA-485-A.

4.3 Topology

A data link shall consist of a single active differential line driver, a terminated transmission line and one or more differential line receivers. The transmission line shall be a data cable with a nominal characteristic impedance of 100 to 120 ohms as specified in clause 8. The differential drivers and receivers shall meet the requirements of EIA-485-A and all additional requirements of this Standard.

4.4 Ports

A DMX512 Port is the DMX512 signal connection point between the internal electronics of a device and the physical media of the transmission line. It may be made either by the prescribed connector as defined in clause 7 or by a terminal strip. Terminals and connector contacts are referred to as Pins in this Standard. A DMX512 port has five pins, designated 1 through 5.

Pin 1 of a DMX512 Port is the signal common. All DMX512 ports shall connect Pin 1 to the signal common on the physical media.

4.5 Data link common and grounding topologies

Various paragraphs of clause 5 and Annex A deal with shield-to-earth grounding topologies. In all cases there shall be a low impedance connection between Pin 1 of the DMX512 port and signal common of the EIA-485-A driver or receiver circuitry.

4.6 Preferred method of earth grounding data link common

DMX512 systems should make use of earth ground referenced transmitting devices and isolated receiving devices. This approach provides for a single point solid ground/chassis connection at the source, and allows for variations in building ground potentials between transmitting and receiving devices. This is to ensure that interoperability of equipment is achieved in situations that do not in their own right constitute a safety hazard, but might otherwise exceed the Common Mode limitations of EIA-485-A. See EIA-485-A clause 4.3.1. Other approaches are covered in Annex A.

4.7 Primary data link

Pins 2 and 3 of a DMX512 Port form the primary data link. Pin 2 is the data - signal. Pin 3 is the data + signal. Format of the data is covered in clause 9. Limited use of multiple data link drivers for half-duplex, bi-directional data transmission on the primary data link is permitted in accordance with Enhanced Functionality as described in Annex B.

4.8 Optional secondary data link (Enhanced Functionality)

4.8.1 Secondary data link - active use

Pins 4 and 5 of a DMX512 Port provide a secondary EIA-485-A data link. Implementation of this data link is optional. Active use of Pins 4 and 5 is known as Enhanced Functionality. Pin 4 is the data - signal. Pin 5 is the data + signal. Several different network topologies are associated with the implementation of Enhanced Functionality. Approved uses of the secondary data link and their associated topologies are described in Annex B.

4.8.2 Secondary data link - passive use

In order to extend Enhanced Functionality across a network, devices containing two ports for receive and transmit that do not actively process data on Pins 4 and 5 must provide a direct passive link of these pins between the two ports. Devices containing three or more ports may wire the passive secondary data link between only two of the ports. These two ports shall be declared as required in Clause 11 and should be marked on the product.

4.9 Data Link signal designations summary

Table 1 - Signal designations summary

Function	Pin Reference within Standard	DMX512 Function
Data Link Common	**1**	Common (Screen)
Primary Data Link	**2**	Data 1 -
	3	Data 1 +
Secondary Data Link (Optional - see clause 4.8)	**4**	Data 2 -
	5	Data 2 +

While the generic reference to Pins 1 through 5 correlates to the physical pinout used on the XLR style connectors as defined in clause 7 of this Standard, there are other situations where different physical pinouts may be encountered, such as a terminal strip in a fixed installation with internal connections.

4.10 Data termination procedures

DMX512 data links shall be terminated to eliminate ringing and signal reflection which can cause mis-operation of an otherwise properly designed system. To comply with this Standard, all equipment connected to a DMX512 data link shall operate in accordance with the stated manufacturer's specification when the data link is terminated. The impedance of this terminator shall be equal to the characteristic impedance of the transmission line – 120 ohms, optionally in series with a 0.047µf capacitor between Data + and Data -.

Receiving devices without a loop-through connection shall be permanently terminated. Receiving devices with loop-through shall not be permanently terminated.

In the preferred topology where the transmitter is connected to one end of the data link, the far end of the data link shall be terminated. In the case where the transmitter cannot be connected at one end of the data link, then both ends of the data link shall be terminated.

Manufacturers of receiving devices may provide internal termination of the data link. Where such termination is provided, it shall comply with the electrical and marking requirements of this Standard. It is recommended that termination components be chosen to withstand continuous voltages of at least 30 VAC/42 VDC.

Unpowered connected DMX512 devices shall not degrade the performance of the DMX512 transmission system.

5 Nominal Operating Characteristics

5.1 General

Operation limits generally follow the detailed requirements of EIA-485-A for generator characteristics. Where appropriate, separate limits are given for isolated products.

5.2 Earth grounding of data link common for transmitters

In recognition of the need for DMX512 compliant product to be capable of interconnection as part of large and potentially complex systems, this Standard defines two allowable topologies for the earth grounding of data link common and signal common for transmitters, to be known as "Ground Referenced" and "Isolated". The preferred method is "Ground Referenced." "Isolated" is covered in Annex A.

5.3 Transmitter characteristics

All electrical characteristics shall be measured at the output terminals of the product. Transmitting devices shall deliver open circuit output voltage not less than 1.5V and not more than 6V as defined in EIA-485-A clause 4.2.1. Transmitting devices shall comply with the requirements of EIA-485-A clause 4.2.2 for differential and offset output voltages, which requires that the magnitude of the differential output voltage be not less than 1.5V and not more than 5V when connected to a test load of 54 ohms.

The requirements of EIA-485-A clause 4.2.2 for generator offset voltage and EIA-485-A clause 4.2.3 for Differential Output voltage (Common Mode loading) shall be met. The requirements of EIA-485-A clause 4.2.4 for Off-state output current shall be met, provided that the Unit load for the generator in the off state does not exceed 1.

Transmitting devices shall comply with the requirements of EIA-485-A clause 4.2.7, for which the unit interval (t_{ui}) shall be regarded as 4 microseconds.

In battery operated equipment or equipment which has no inherent provision for connection to protective ground, chassis shall be deemed to be any exposed metal connector parts which do not carry signals. All such parts shall be at equal potential.

5.4 Ground referenced transmitters

Ground referenced transmitting device outputs shall meet the following conditions in table 2 during normal operation under open circuit condition.

Table 2 - Ground Referenced Transmitter Characteristics

Connection	Limit	Comment
Pin 2 to Pin 1 or Pin 3 to Pin 1	0 ≤ v ≤ +6 VDC	
Pin 4 to Pin 1 or Pin 5 to Pin 1	0 ≤ v ≤ +6 VDC	Enhanced Function devices only
Pin 1 to Chassis	0V	Ground Referenced transmitting devices shall have a direct connection between Pin 1 and chassis.
Pin 2 to Chassis or Pin 3 to Chassis	0 ≤ v ≤ +6 VDC	
Pin 4 to Chassis or Pin 5 to Chassis	0 ≤ v ≤ +6 VDC	Enhanced Function devices only
Pin 2 to Pin 3	+/- 6V (open circuit)	
Pin 4 to Pin 5	+/- 6V (open circuit)	

Figure 1 illustrates a ground referenced transmitter port. It is characterized by the direct connection of the shield (Pin 1) to chassis and protective earth. Therefore, devices employing ground referenced transmitters shall be provided with provision for connection to protective earth. Any impedance (A) between Pin 1 and zero volt supply of the transmitter circuit shall be less than 100 ohms. Any impedance (B) between Pin 1 and chassis shall be less than 20 ohms and is preferably zero ohms.

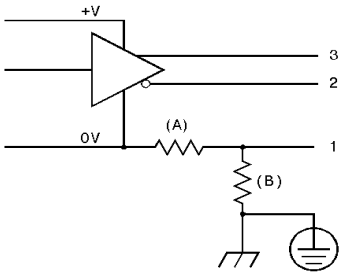

Figure Key

1 - DMX512 Pin 1
2 - DMX512 Pin 2 (or Pin 4)
3 - DMX512 Pin 3 (or Pin 5)
A - Optional Impedance (see text)
B - Optional Impedance (see text)

Figure 1 - Ground Referenced Transmitter

A DMX512 device may have any number of Grounded transmitter ports. Grounded transmitter ports may be used by all DMX512 devices including ones that provide any number of non-DMX512 input or output ports. Adherence to this topology allows a DMX512 transmitter connector to be marked as GROUNDED.

Because the transmitter in this topology is grounded, the existence of an isolation barrier between the transmitter and any other part of the device shall NOT qualify output for marking as ISOLATED.

5.5 Earth grounding of data link common for receivers

This Standard defines several allowable topologies for earth grounding of data link common and signal common for receiving devices. These are to be known as “non-isolated” and “isolated”. The preferred method is “isolated.” A specific concession is available to manufacturers of non-isolated receivers who, for reasons beyond the scope of this Standard, require a direct link between data link common and chassis. Both of these alternatives are addressed in Annex A.

5.6 Isolated Receiver characteristics

For isolated devices, a capacitor shall be fitted between Pin 1 and chassis for the purpose of Radio Frequency bypass. Devices shall continue to operate correctly when exposed to any of the conditions in table 3.

Table 3 - Isolated Receiver characteristics

Connection	Limit	Comment
Pin 2 to Pin 1 or Pin 3 to Pin 1	+12 / -7 VDC	Common Mode range
Pin 4 to Pin 1 or Pin 5 to Pin 1	+12 / -7 VDC	Enhanced Function devices only
Pin 1 to Chassis	$\geq$ 22M ohm @ 42 VDC	
Pin 2 to Chassis or Pin 3 to Chassis	$\geq$ 22M ohm @ 42 VDC	
Pin 4 to Chassis or Pin 5 to Chassis	$\geq$ 22M ohm @ 42 VDC	Enhanced Function devices only
Pin 2 to Pin 3	+/- 6 V	
Pin 4 to Pin 5	+/- 6 V	Enhanced Function devices only
Any Pin to Chassis	30 VAC / 42 VDC	

Figure 2 illustrates an isolated receiver. Any pin of the DMX512 isolated receiver shall present a resistance (B) greater than 22 Mohm at 42 VDC with respect to Chassis, with respect to Protective Ground (where fitted), with respect to any other signal inputs or outputs, and with respect to other ground referenced electronics. There shall be a capacitance (not shown) between Pin 1 and chassis for Radio Frequency bypass. Any resistance (A) between pin 1 and zero volt supply of the receiver circuit shall be less than 100 ohms.

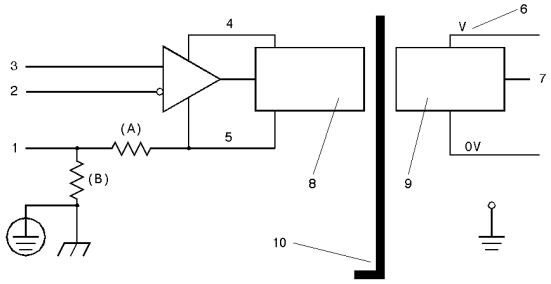

Figure Key

1 - DMX512 Pin 1
2 - DMX512 Pin 2 (or Pin 4)
3 - DMX512 Pin 3 (or Pin 5)
4 - Isolated Supply
5 - Isolated 0V
6 - V (+ or -)
7 - I / O
8 - Isolated Electronics
9 - Non-Isolated Electronics (optional)
10 - Isolation Barrier
A - Optional Impedance (see text)
B - Optional Impedance (see text)

Figure 2 - Isolated Receiver

Adherence to this topology allows a DMX512 receiver port to be marked as ISOLATED. Isolated receiver ports may be used by all DMX512 devices including ones that provide any number of non-DMX512 input or output ports. A DMX512 device may have any number of Isolated receiver ports.

5.7 Disallowed receiver topologies

This configuration is not permitted, although it may exist on some legacy products. While this topology is described as one possible topology in EIA-485-A, it is not appropriate when considering operation of DMX512 receiving devices in systems encountering differential ground potentials.

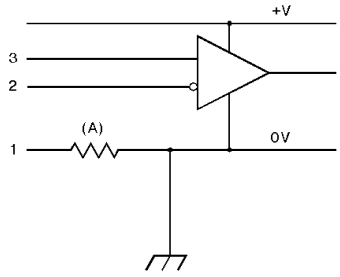

Figure Key

1 - DMX512 Pin 1

2 - DMX512 Pin 2 (or Pin 4)

3 - DMX512 Pin 3 (or Pin 5)

A - R $\geq$ 0.2 ohm

Figure 3 - Receiver Topology NOT Allowed

5.8 Processing devices

It is also permissible to design processing devices based on the Isolated Receiver / Ground Referenced Transmitter or Isolated Receiver / Isolated Transmitter models (see Annex A) already described.

5.9 Loading designation

As per EIA-485-A, the total load permitted on a DMX512 data link is 32 unit loads. Transmitters designed for this Standard shall be capable of driving 32 unit loads on a DMX512 data link. All DMX512 devices shall have a unit load (LEN) of 1or less.

A receiver biased to any voltage from -7 to +12 volts shall not present a capacitive load to the line of more than 200pf per unit load. If this value is frequency dependent, the value given shall be the capacitive load when driven by a 650kHz sine wave.

Declaring or marking of the unit load is not required by this standard. If a manufacturer chooses to declare or mark their products with a unit load value, the declared or marked value shall be the greater of either the DC unit load determined by EIA-485-A clause 4.1 or the unit load as determined by the capacitive loading. In either case, if the unit load is declared the capacitive load values must also be declared.

6 Protection

6.1 Minimum protection against interconnection damage

Clause 4.2 of EIA-485-A recognizes that certain other extraneous conditions may overstress the system and that these conditions should be specified in the referencing standard. Extensive use of temporary and portable equipment in Entertainment Lighting Industry results in frequent connection and disconnection of equipment and gives rise to the possibility of equipment misconnection.

Equipment may be protected against damage resulting from accidental connection to voltages in excess of the minimum defined in EIA-485-A clauses 4.2.5 and 4.2.6, and is recommended. See Annex C. This does not negate the need to comply with EIA-485-A clause 4.2.6 - Transient overvoltage tolerance.

6.2 Minimum Electro Static Discharge (ESD) protection

Manufacturers shall ensure that any pins can withstand a minimum of 4kV ESD for contact discharge and 8kV ESD for air discharge in accordance with IEC 61000-4-2 or other local regulations which may require higher levels of protection. The acceptance criteria for this requirement shall allow temporary loss of function, provided the function is self recoverable or can be restored by the operation of controls. Meeting this requirement does not alter the fact that a manufacturer may have to meet other more stringent ESD requirements to conform to local EMC regulations.

7 Connection Methods

7.1 Equipment fitted with external user accessible pluggable data link connections

This category includes all portable products.

Female connectors shall be used on controllers and other transmitting devices and male connectors shall be used on dimmers and other receiving devices. Female connectors shall also be used where loop-through connections are provided.

Marking and identification of all ports shall be as required in clause 11. Each DMX512 port with Enhanced Functionality shall be marked in accordance with clause 11 and Annex B.

7.1.1 Required Connector

Equipment in this category shall use 5-pin XLR connectors. The physical pinout of the 5-pin XLR shall be in accordance with the Pin reference in this Standard as defined in table 1.

7.1.2 Concession for use of an alternate connector (NCC DMX512-A)

A concession to use an alternate connector is available only when it is physically impossible to mount a 5-pin XLR connector on the product. In such cases the following additional requirements shall be met :

1) The alternate connector shall not be any type of XLR connector.
2) The alternate connector shall not be any type of RJ45 type connector except as allowed in clause 7.4.
3) Provided that all other requirements of this Standard are met, when marking is applied to any such alternate connector, it may be marked as NCC DMX512-A (Not Connector Compatible).
4) The manufacturer shall make available an adapter cable with the appropriate connections to a standard 5-pin XLR connector for all DMX512 ports included in the alternate connector.
5) The Enhanced Functionality, if applicable, and ground/isolation declarations shall continue to be declared for each port.

7.2 Equipment intended for fixed installation with internal connections to the data link

Products in this category may optionally use the 5-pin XLR connector, but shall not use any other XLR connector. Where a non 5-pin XLR connector is used, this Standard makes no other restriction or stipulation on connector choice.

When use is made of the 5-pin XLR connector, female connectors shall be used on controllers and other transmitting devices and male connectors shall be used on dimmers and other receiving devices. Female connectors shall also be used where loop-through connections are provided. In all other cases, the connector sex is not specified.

Products in this category with Enhanced Functionality shall be marked in accordance with the provisions of clause 11 and Annex B.

7.3 Passive Data Outlets or Wall plate panels

Products in this category designed for temporary and generally accessible access to DMX512 data links shall use 5-pin XLR connectors. Marking of such panels shall be in accordance with clause 11.5.4.

Panels which provide a data source on the primary data link shall use female connectors. Panels which are intended to provide primary data link input signals back to another location shall use male connectors.

7.4 RJ45 type connectors

Limited use of ISO IEC 11801 compliant cable schemes is permitted in accordance with clause 8.5 of this Standard. The use of RJ45 type connectors (plugs/jacks) and punchdown terminal blocks with this cable shall be limited to connections which are part of a fixed installation and not normally accessible or intended for regular connection and disconnection.

External (user accessible) RJ45 type connectors are permitted only on patch and data distribution products and only when installed in controlled access areas.

Products in this category with Enhanced Functionality shall be marked in accordance with the provisions of clause 11 and Annex B.

Installations using Category 5 cable implementing the one pair functionality of Cable Scheme C1 are referred to as Cable Scheme C5.1. This configuration limits systems to the basic functionality offered by TYPE 0 ports, but does permit two universes to be carried on one cable.

Installations using Category 5 cable implementing the two pair functionality of Cable Scheme C2 are referred to as Cable Scheme C5.2. The use of Cable Scheme C2 is required for the interconnection of products with EF1, EF2, or EF3 topologies, and is the preferred implementation.

Table 4 - Connection Schedule for DMX512 systems using ISO IEC 11801 Cable

Pair	Wire #	Color	Function	DMX512 Pin
Pair 2	1	white / orange	data 1 +	DMX512 Pin 3
	2	orange	data 1 -	DMX512 Pin 2
Pair 3	3	white / green	data 2+	DMX512 Pin 5
	6	green	data 2 -	DMX512 Pin 4
Pair 1	4	blue	Not assigned	
	5	white / blue	Not assigned	
Pair 4	7	white / brown	Signal Common (0 v)	DMX512 Pin 1
	8	brown	Signal Common (0 v)	DMX512 Pin 1
Shield		drain		

Note: ISO IEC 11801 cable wire pair numbering and color in accordance with TIA T568B.

***Warning**: Accidental connection to non-DMX512 equipment likely to be encountered (e.g., an Ethernet Hub at a patch bay) may result in damage to equipment.*

***Warning**: Wires 4 and 7 are used for various purposes in other wiring standards, including telephone ringing voltage. Some manufacturers whose distributed DMX512 buffering products require low voltage DC power may use these wires for this purpose. Because of these various uses, misplugging unlike systems could cause serious damage. However, since these wires are never connected to an end user XLR connector, mitigation of potential problems involving such systems are currently beyond the scope of this Standard.*

8 Cable

8.1 Background

The data transmission rate (250 kbits/s) used by DMX512 requires the selection of a cable which does not significantly distort the signal or give rise to spurious signal reflections. Cables intended for use with audio systems (microphone cables), while having the convenience of flexibility, availability and relative low cost, are **NOT** suitable for use with DMX512 because of their high capacitance and incorrect characteristic impedance; at DMX512 data rates this will give rise to bit time distortion and signal reflections/overshoot, particularly over long (greater than 10 meter) distances.

8.2 General

Cabling systems shall provide a balanced, nominal 120 ohm terminated transmission system, and be made of cables with a characteristic impedance in the range 100-120 ohm.

Note: Note that mixing cables of different impedances and other characteristics not isolated by buffers or other processing devices may affect system reliability.

Cables with one pair are referred to as Cable Scheme C1 in this Standard. The use of Cable Scheme C1 does not allow for Enhanced Functionality and is restricted to portable cables only. Enhanced Functionality product may be interconnected but operation will be limited to transfer of data on the primary data link.

Cables with two pairs are referred to as Cable Scheme C2 in this Standard. The use of Cable Scheme C2 is required for permanent wiring and for portable cables used for the interconnection of products with Enhanced Functionality.

8.3 General Applications and between all Portable Equipment

Cable for general application shall be shielded twisted pair approved by its manufacturer for EIA-422/EIA-485-A use at high data transmission rates and distances of at least 500 meters. Conductors in cable for portable equipment shall be of stranded construction.

8.4 Cable between permanently installed fixed equipment

Any two-pair cable satisfying the requirements of clauses 8.2 and 8.3 may be used for connections between items of fixed equipment, subject to local regulatory requirements regarding voltage and insulation styles.

The use of shielded or unshielded 100 ohm or 120 ohm ISO IEC 11801 compliant cable shall be permitted.

Conductors in cable installed permanently between fixed equipment shall be permitted to be solid.

8.5 Cable application rules

Table 4 summarizes the various constructions of cable suitable for use with DMX512 and how they can be implemented.

Table 5 - Cable application rules

	Solid Conductors			Stranded Conductors		
Use	**EIA-485-A**	**UTP 100 or 120 ohm ISO IEC 11801**	**STP/FTP 100 or 120 ohm ISO IEC 11801**	**EIA-485-A**	**UTP 100 or 120 ohm ISO IEC 11801**	**STP/FTP 100 or 120 ohm ISO IEC 11801**
Portable	No	No	No	OK - Note 1 -	No	OK - Note 1 -
Permanent	OK	In Earthed Metal Conduit Only	OK - Note 2 -	OK - Note 2 -	In Earthed Metal Conduit Only	OK - Note 2 -

Note 1: It is recommended that braided shield be used for better durability

Note 2: Use of Plenum Rated cable without conduit allowed

9 Data Protocol

9.1 Format

Data transmitted shall be in asynchronous serial format. DMX512 slots shall be transmitted sequentially, beginning with slot 0 and ending with the last implemented slot, up to a maximum of 513. Prior to the first data slot being transmitted, a Reset Sequence shall be transmitted – a BREAK, followed by a MARK AFTER BREAK, and a START Code. Valid DMX512 slot values under a NULL START Code shall be 0 to 255 decimal.

9.2 Slot format

The data transmission format for each data value transmitted shall be as follows:

Table 6 - Data slot format

Bit Position	Description
1	Start Bit, Low or SPACE
2 through 9	Slot Value Data Bits, Least Significant Bit to Most Significant Bit Positive logic
10, 11	Stop Bits, High or MARK
Parity	Not transmitted

9.3 Break

The BREAK (Timing Diagram, Designation #1) shall be defined as a high-to-low transition followed by a low of 88 microseconds (two slot times) duration or longer followed by a low to high transition. The BREAK indicates the start of a new packet.

9.4 Mark After Break

The duration of the MARK separating the BREAK and the START Code (Timing Diagram, Designation #2) shall be not less than 8 microseconds and not greater than 1 second. All DMX512 transmitters shall produce a MARK AFTER BREAK of not less than 8 microseconds. All receivers shall recognize an 8 microsecond MARK AFTER BREAK.

Note: The 1986 version of this standard specified a 4 microsecond MARK AFTER BREAK. The 1990 version of the standard changed that value to 8 microseconds, but added an option for receivers capable of recognizing the 4 microsecond MARK AFTER BREAK to be identified as having that capability. Some transmitters may still be in use that generate the shorter 4 microsecond MARK AFTER BREAK, and they may not work with equipment built to this standard.

9.5 START Code

The START Code is the first byte following a MARK AFTER BREAK. The START Code identifies the function of subsequent data in that packet.

9.5.1 NULL START Code

The NULL START Code (a NULL byte – all zeros) identifies subsequent data as sequential 8-bit information.

9.5.2 Other START Codes

In order to provide for future expansion and flexibility, DMX512 makes provision for 255 additional non NULL START Codes (1 through 255 decimal, 01 through FF hexadecimal), henceforth referred to as Alternate START Codes. Where it is required to send proprietary information over a DMX512 data link, a packet starting with a registered Alternate START Code shall be used.

Annex D states the requirements for transmitting, processing, and receiving Alternate START Codes.

Several Alternate START Codes are reserved. See Annex E.

See Annex F for Alternate START Code Registration Policies.

9.5.3 START Code processing

All receiving devices other than in-line processing devices shall process the START Code and differentiate between those packets with NULL START Codes and those with Alternate START Codes. Devices shall not ignore START Codes by assuming that all packets received are NULL START Code packets.

9.6 Maximum number of data slots

Each data link shall support up to 512 data slots. Multiple links shall be used where larger numbers of slots are required.

9.7 Minimum number of data slots

There shall be no minimum number of data slots on the data link. DMX512 data packets with fewer than 512 slots may be transmitted, subject to the minimum timing requirements of this standard – see clause 9.10 and figure 4.

9.8 Defined line state between slots

The time between any two slots of a data packet (Timing Diagram, Designation #9) may vary between 0 microseconds and 1 second. The line must remain in a "marking" state during any such idle period. A receiver must be capable of accepting a data packet having no idle time (0 microseconds) between any of its slots.

9.9 Defined line state between data packets (Mark Before Break)

Every data packet transmitted on the data link, regardless of START Code or length, must begin with a BREAK, MARK AFTER BREAK, and START Code sequence as defined above. The time between the second stop bit of the last data slot of one data packet and the falling edge of the beginning of the BREAK for the next data packet (Timing Diagram, Designation #10) may vary between 0 microseconds and 1 second. The line shall remain in an idle ("marking") state throughout any such period greater than 0 microseconds. Transmitters, therefore, shall not produce multiple BREAKs between data packets. Receivers, however, shall be capable of recovering from multiple BREAKs produced by data link line errors.

9.10 Break-to-Break spacing

The period between the falling edge at the start of any one BREAK shall be not less than 1196 microseconds from the falling edge at the start of the next BREAK, nor more than 1.025 seconds.

9.11 Dimmer class data

Valid dimmer levels shall be 0 to 255 decimal (00 to FF hexadecimal) representing dimmer control input. 0 shall represent a dimmer output of OFF or minimum and 255 shall represent an output of FULL. A dimmer shall respond to increasing the DMX512 slot value for 0 to 255 by fading from its minimum level (off) to its maximum level (full). The exact relationship between DMX512 slot values and dimmer output is beyond the scope of this Standard.

9.12 Timing Diagram - output of transmitting UART

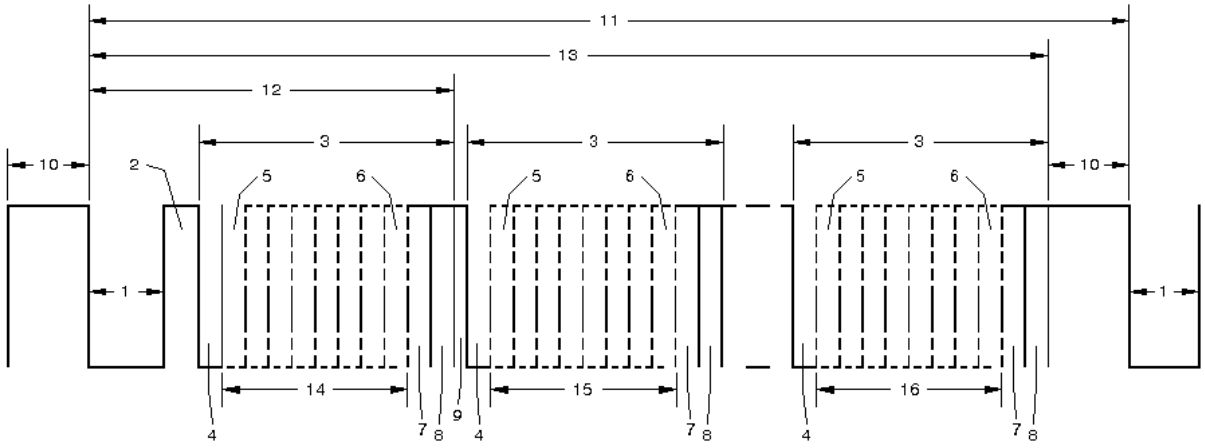

Figure Key

1 - "SPACE" for BREAK
2 - "MARK" After BREAK (MAB)
3 - Slot Time
4 - START Bit
5 - LEAST SIGNIFICANT Data BIT
6 - MOST SIGNIFICANT Data BIT
7 - STOP Bit
8 - STOP Bit
9 - "MARK" Time Between slots
10 - "MARK" Before BREAK (MBB)
11 - BREAK to BREAK Time
12 - RESET Sequence (BREAK, MAB, START Code)
13 - DMX512 Packet
14 - START CODE (Slot 0 Data)
15 - SLOT 1 DATA
16 - SLOT nnn DATA (Maximum 512)

Figure 4 - Timing Diagram

Table 7 - Timing Diagram Values

Designation	Description	Min	Typical	Max	Unit
-	Bit Rate	245	250	255	kbit / s
-	Bit Time	3.92	4	4.08	µs
-	Minimum Update Time for 513 slots	–	22.7	–	ms
-	Maximum Update Rate for 513 slots	–	44	–	/ s
1	"SPACE" for BREAK	88	–	–	µs
2	"MARK" After BREAK (MAB)	8	–	< 1.00	µs s
9	"MARK" Time between slots	0	–	< 1.00	s
10	"MARK" Before BREAK (MBB)	0	–	< 1.00	s
11	BREAK to BREAK Time	1196	–	– 1.00	µs s
13	DMX512 Packet	1196	–	– 1.00	µs s

10 Receiver Performance

10.1 Loss of data tolerance / Resumption of acceptance of data

A receiver not receiving a Reset Sequence (a sequence of a Break, Mark After Break, and START Code) within one second of the previous Reset Sequence shall be considered to have lost data input.

Although this Standard does not specify loss of data handling procedures, manufacturers shall state what their Loss of Data handling procedures are.

Note: In the absence of overriding safety issues or an alternative source of control data, when encountering a loss of data condition a receiving device should remain in an operating condition for at least 60 seconds, awaiting resumption of the DMX512 signal.

10.2 Receiver performance at maximum update rate

Any device incorporating a DMX512 receiver shall operate correctly when receiving continuous transmission of valid data packets containing any number of slot values.

10.3 Inactive receiver input circuitry

Unpowered connected DMX512 devices shall not degrade the performance of the DMX512 transmission system.

10.4 Packet processing latency

Some products may provide their specified functionality without processing or being able to process every consecutive DMX512 packet. Such products will have an inherent latency to data changes between packets, which shall be declared by the manufacturer in accordance with the disclosure requirements of clause 11.

11 Marking and Disclosures

11.1 Identification

Only equipment conforming to this Standard may be marked and identified with "USITT DMX512-A" or "DMX512-A".

11.2 Port marking

Where required by clauses 11.3 through 11.4, all ports shall be marked as to the applicable Enhanced Functionality as defined in table B1 (Annex B). All information provided by marking shall also be provided in the equipment manual.

Where declaration of pinout detail is required by clauses 11.3 through 11.4, manufacturers shall use the signal designations from table 1 in any marking of pin, contact or terminal functions appearing on or within a product and associated with installation or connection. Such details are dependent on the declared Enhanced Functionality of the port. Where it is necessary to use abbreviations, only those detailed in table 8 shall be permitted.

Table 8 - Signal designations abbreviations allowed for marking

Function	Abbreviation
Common (Screen)	COM
Primary Data Link – Data 1-	D1-
Primary Data Link – Data 1+	D1+
Secondary Data Link – Data 2-	D2-
Secondary Data Link – Data 2+	D2+

11.3 Data line termination marking

On portable products and products fitted with external pluggable data link connectors, clear and appropriate identification of the termination state shall be provided when the port termination is switchable.

11.4 Ground / Isolation marking

All DMX512 ports shall also be marked as to the relationship between Pin 1 and earth ground. The allowed grounding topologies are shown in table 9.

Table 9 - Ground / Isolation marking

Function of Port	Defining Figure	Comment	Approved Marking
Transmitter	fig 1	Ground Referenced	*no mark required*
Transmitter	fig A1	Isolated (See Annex A)	ISO or ISOLATED
Transmitter	fig A4	Floating (See Annex A)	FLT or FLOAT or FLOATING
Receiver	fig A2	Non-Isolated, 100 ohm 2 Watt resistor	NON-ISO or NON-ISOLATED
Receiver	fig A3	Grounded – concession per note 3 of the figures (See Annex A)	⚠ PIN 1 ⏚
Receiver	fig 2	Isolated	*no mark required*; ISO or ISOLATED
Receiver	fig A4	Floating	FLT or FLOAT or FLOATING

11.5 Required disclosures

11.5.1 Portable products and products fitted with external pluggable data link connectors

Ports on these products shall be marked in accordance with clause 11.2. Ports on these products shall provide Ground/Isolation marking in accordance with clause 11.4.

If use has been made on any non-XLR connector in conjunction with the supply of an adapter cable, the non-XLR connector may be also be marked as NCC DMX512-A.

11.5.2 Equipment intended for fixed installation with internal connections to the data link

Ports on these products shall be marked in accordance with clause 11.2. Ports on these products shall provide Ground/Isolation marking in accordance with clause 11.4.

Clearly identified connector pinout detail shall be marked on or within any product in accordance with clause 11.2.

11.5.3 Internal connections and specialized products for use with ISO IEC 11801 cable schemes

Ports on these products shall be marked in accordance with clause 11.2. Ports on these products shall provide Ground/Isolation marking in accordance with clause 11.4.

11.5.4 Data outlet or wall plates fitted with 5-pin XLR connectors

Where a 5-pin XLR female or male connector is fitted to a wall plate or facility panel in a manner that links it directly back to a patch panel or data distribution buffer, its Enhanced Functionality, if it exists, cannot be determined without reference to the product to which it is ultimately patched and the cable scheme implemented. Therefore, manufacturers and installers of such data outlets shall be permitted to mark the XLR connectors in accordance with table 10. If the site cable scheme or pinout does not follow this table, no reference to DMX512, including use of the term “DMX”, shall be permitted.

No reference to DMX512-A shall be permitted, since the “A" indicates electrical characteristics of active electronics compliant with this edition of the Standard, which cannot always be known at the passive wall plate.

Table 10 - 5-pin XLR data outlet / wall plate marking

5-pin XLR - Pins Wired	Cable Scheme	Permitted Marking at XLR (the word “Scheme” is optional)	Comments
1, 2, 3	C1	DMX512 Scheme C1	Not allowed for new installations
1, 2, 3, 4, 5	C2	DMX512 Scheme C2	Required for new Installations

11.5.5 Loss of data handling procedure

This Standard does not define loss of data handling procedures (clause 8.1) beyond requiring that manufacturers declare their own products’ procedure(s). Such declarations shall be made in the equipment manual.

11.5.6 Packet Processing latency

Manufacturers shall declare any inherent latency to data changes between packets in the equipment manual. This may be in terms of response time or other wording as chosen by the manufacturer, but shall clearly indicate if the product design might legitimately ignore some packets in normal operation.

11.5.7 NULL START Code functionality

Manufacturers of transmitting devices shall declare in the device manual the full range of slot values transmitted in conjunction with packets sent using the NULL START Code.

Manufacturers of receiving devices shall declare the response to packets received containing the NULL START Code, with particular reference to any functionality requiring limited or restricted slot data values, in the equipment manual.

11.5.8 Slot footprint

Manufacturers of receiving devices shall declare the slot footprint in the equipment manual.

= END =

Annex A - Alternate (not preferred) topologies (Normative)

A1 Isolated transmitters

This standard permits the use of isolated transmitter ports. They are used in systems where legacy receivers or grounded receivers are used and large common mode voltages are expected.

Figure A1 illustrates an isolated transmitter port. To be considered an isolated transmitter, any pin of the DMX512 output shall present a resistance (B) greater than 22 Mohm at 42 VDC with respect to Chassis, and with respect to Protective Ground (where fitted). If there are any other signal inputs or outputs any pin of the DMX512 output shall present a resistance greater than 22 Mohm at 42 VDC with respect to these inputs or outputs. The power supply for the transmitter and any directly connected electronics shall be isolated from earth ground and any other grounded referenced electronics to levels at least as high as those required of the output pins. Any impedance (A) between pin 1 and zero volt supply of the transmitter circuit shall be less than 100 ohms. There shall be a capacitance (not shown) between Pin 1 and chassis for the purpose of Radio Frequency bypass.

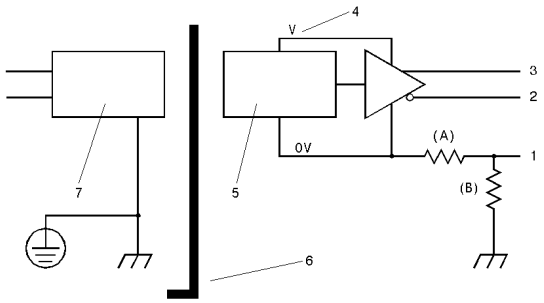

Figure Key

1 - DMX512 Pin 1
2 - DMX512 Pin 2 (or Pin 4)
3 - DMX512 Pin 3 (or Pin 5)
4 - V (+ or -)
5 - Other Isolated Electronics
6 - Isolation Barrier
7 - Non-Isolated Electronics (optional)
A - Optional Impedance (see text)
B - Impedance (see text)

Figure A1 - Isolated Transmitter

Table A1 - Isolated Transmitter characteristics

Connection	Limit	Comment
Pin 2 to Pin 1 or Pin 3 to Pin 1	+/- 6 V	Common Mode range
Pin 4 to Pin 1 or Pin 5 to Pin 1	+/- 6 V	Enhanced Function devices only
Pin 1 to Chassis	$\geq$ 22M ohm @ 42 VDC	
Pin 2 to Chassis or Pin 3 to Chassis	$\geq$ 22M ohm @ 42 VDC	
Pin 4 to Chassis or Pin 5 to Chassis	$\geq$ 22M ohm @ 42 VDC	Enhanced Function devices only
Pin 2 to Pin 3	+/- 6 V	
Pin 4 to Pin 5	+/- 6 V	Enhanced Function devices only
Any Pin to Chassis	30 VAC / 42 VDC	

A DMX512 device may have any number of isolated transmitter ports.

Adherence to this topology allows a DMX512 transmitter connector to be marked ISO or ISOLATED.

A2 Non-isolated receivers

While not the preferred topology, this non-isolated topology exhibits considerable improvement in common tolerance compared to other grounded or non-isolated topologies. In this topology there shall be a resistance (B) of 100 ohms between pin 1 and chassis. This resistance shall be able to safely dissipate two watts. No other connection between circuit common and chassis is permitted. Common mode voltage present between the chassis of this device and the chassis of any other device connected to the DMX shield will cause a current flow. This current will cause a voltage drop in the resistance (B). This voltage drop effectively decreases the common mode voltage at this receiver. Any resistance (A) between pin 1 and zero volt supply of the receiver circuit shall be less than 100 ohms.

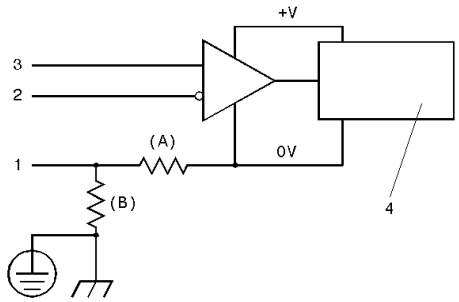

Figure Key

1 - DMX512 Pin 1
2 - DMX512 Pin 2 (or Pin 4)
3 - DMX512 Pin 3 (or Pin 5)
4 - Other Electronics
A - Optional Impedance (see text)
B - Optional Impedance (see text)

Figure A2 - Non-Isolated Receiver

Since 0 V is not directly referenced to Chassis, local product safety standards may restrict choice of power supply (e.g., use of a Class 2 supply).

A DMX512 receiver may have any number of non-isolated receiver ports. Where multiple ports are implemented, the total parallel resistance (B) shall be 100 ohms.

Table A2 - Non-Isolated Receiver characteristics

Connection	Limit	Comment
Pin 2 to Pin 1 or Pin 3 to Pin 1	+12 / -7 VDC	Common Mode range
Pin 4 to Pin 1 or Pin 5 to Pin 1	+12 / -7 VDC	Enhanced Function devices only
Pin 1 to Chassis	100 ohms	-Note 1-
Pin 2 to Chassis or Pin 3 to Chassis	+12 / -7 VDC	
Pin 4 to Chassis or Pin 5 to Chassis	+12 / -7 VDC	Enhanced Function devices only
Pin 2 to Pin 3	+/- 6V	
Pin 4 to Pin 5	+/- 6V	Enhanced Function devices only
Any Pin to Chassis	N/A	

Note 1 : This cannot be characterized in terms of voltage. Manufacturers shall be permitted to fit a resistance of 100 ohms +/-20% between Chassis and Pin 1 for the purpose of limiting current in the screen due to small differential ground potentials. This method provides for reduction of Common Mode voltage at the line receiver.

The only output permitted to be directly connected to this topology is a single passive DMX512 loop through port. No other inputs or outputs are allowed with this topology unless they meet the requirements of clause A4.

A3 Grounded Receivers

he topology of figure A3 is allowed for the construction of entry level receivers where the cost of isolation might prove an untenable burden. It may be used by manufacturers of receivers who, for reasons beyond the scope of this Standard require a direct link between data link common and protective earth. It is not a recommended practice and requires special marking and special explanatory text in all manuals.

This topology is characterized by the direct connection of the shield (Pin 1) to chassis and protective earth. Therefore, devices employing ground referenced receivers shall be provided with provision for connection to protective earth. Any resistance (A) between pin 1 and zero volt supply of the transmitter circuit shall be less than 100 ohms.

The only DMX512 output permitted to be directly connected to this topology is a single passive DMX512 loop through port.

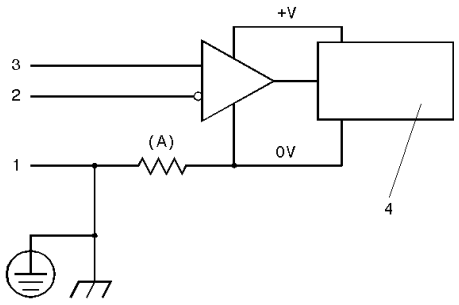

Figure Key

1 - DMX512 Pin 1
2 - DMX512 Pin 2 (or Pin 4)
3 - DMX512 Pin 3 (or Pin 5)
4 - Other Electronics
A - Optional Impedance (see text)
B - Optional Impedance (see text)

Figure A3 - Grounded Receiver

Ports using this topology shall be marked using the standard symbol representation as defined in clause 11.4 and be declared.

A4 Earth grounding of data link common for floating devices

Figure A4 illustrates a floating topology. Floating is both an input and an output topology and is an additional allowable topology. It is often confused with the isolated DMX topology. As with the isolated topology any input or output pin shall present a resistance (B) greater than 22 Mohm at 42 VDC with respect to Chassis, and with respect to Protective Ground (where fitted). It differs from an isolated topology in that there is no requirement of isolation between DMX512 inputs and outputs. The resistance between pin 1 of the DMX512 input and pin 1 of the DMX512 output shall be less than 0.2 ohms. There shall be a capacitance (not shown) between Pin 1 and chassis for the purpose of Radio Frequency bypass. Any resistance(B) between any pin 1 and the zero volt supply of the transmitter and receiver circuits shall be less than 100 ohms.

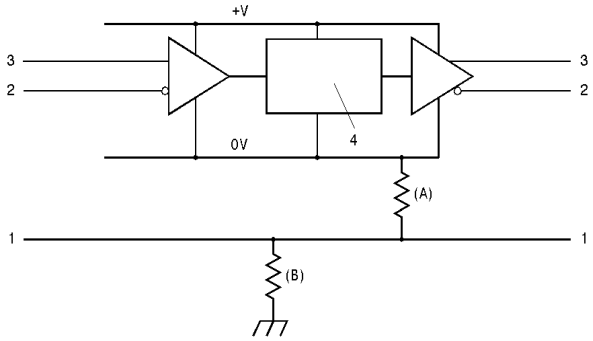

Figure Key

1 - DMX512 Pin 1 (Data Link Common)

2 - DMX512 Pin 2 (or Pin 4)

3 - DMX512 Pin 3 (or Pin 5)

4 - Other Electronics

A - Optional Impedance (see text)

B - Optional Impedance (see text)

Figure A4 - DMX512 Device, Floating

The grounding of a device using this topology is determined by the connected devices. For that reason this topology shall not be used for devices that provide ground referenced non-DMX512 input or output ports unless those ports are isolated from DMX512 lines by an impedance of at least 22 Mohms.

Both input and output ports of a floating device shall be marked FLT, FLOAT, or FLOATING. A device may have only one floating DMX512 receiver port.

-end of Annex A-

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Annex B (Normative) - Enhanced DMX512, the second data link

B1 General

The original and 1990 versions of USITT DMX512 called out an “Optional Second Data Link.” There was no detailed guidance for it use. The majority of legacy systems did not use the second data pair at all. Many uses of the second data pair have been implemented over the years. While many of these were reasonable, a few uses clearly were not compliant with EIA-485-A. These uses vary in both their electrical requirements and in the data protocol used. One of the purposes of this standard is to regularize the use of the second data pair. It is no longer possible to select a single implementation and forbid all others. However, not all historical uses will be allowed to continue. Others are allowed so that manufactures may support installed legacy equipment, will not be recommended for new designs. New uses of the second data link will be permitted when it is determined that they offer general benefit to the end user while not adversely affecting interoperability of existing compliant equipment.

The network topologies needed to support Enhanced Functions are identified by an EF number. This edition of the standard supports three different EF topologies.

The introduction of standard EF topologies in no way changes backward compatibility of primary data link functions. In all cases, regardless of the EF topology, all DMX512 transmitters and receivers shall be able to interchange DMX512 data on the primary data link. All DMX512 devices shall be able to be connected without damage. All DMX512 devices shall not be damaged by connection to compliant legacy devices.

B2 Summary of Enhanced Function Topologies

The Enhanced Function topologies are summarized in table B1. The difference between basic DMX512-A and EF1 or EF2 is the signal topology of the secondary data link only. EF3 allows for the limited use of the primary data link in a bi-directional mode.

Table B1 - Enhanced Function topologies

EF #	Symbol	Description	Comment
1	➜ ➜	unidirectional DMX512 data Pins 2, 3 (EIA-485-A signals) and return EIA-485-A signals on Pins 4, 5	
2	➜ ⟷	unidirectional DMX512 data Pins 2, 3 (EIA-485-A signals) and half duplex EIA-485-A signals on Pins 4, 5	refer to manufacturers instructions
3	⟷ ⟷	half duplex EIA-485-A signals on both pairs; return signal on Pins 2, 3 controlled by a registered Alternate START Code	the data format on 2 & 3 must be compatible with standard DMX512

Note: References to unidirectional data are with respect to a transmitting device.

Different physical ports on a product may be of different EF topologies and must be declared and marked as required in clause 11.

B3 Identification of data protocols on the secondary data link

The EF topology specifies the electrical and operating mode for the data links. It does not detail the data structure or protocol. The method of identifying data structures or protocols using the defined EF numbers is by way of an additional registered number placed after the EF number, separated from the EF number by a period. The registry for these designations will be maintained by Secretariat for the ANSI E1 Accredited Standards Committee – ESTA (see Annexes E and F). Numbers ending in zero are reserved for future development of the standard (e.g., EF1.0, EF1.10, EF2.20).

B3.1 EF1- Full duplex DMX512

The EF1 topology uses the second data link to provide a data path to return status information from controlled devices. The data on second data link shall be unidirectional flowing from the controlled devices to the controller. This data link will operate in multi transmitter multipoint mode. In this mode the primary and secondary links comprise a full duplex data link. A DMX512 controlled device capable of returning status information is referred to as a responder in this standard.

Each responder shall have an EIA-485-A transmitter for the second data link with a driver enable control. The driver enable control shall be driven so that each responder can control the state of the return data link while transmitting its response bytes. Once configured only one responder shall be enabled at once and there shall be at least one bit time between one responder going inactive and the next going active. In general, the line driver can be enabled one bit time prior to transmission, and disabled one bit time after the last bit has been sent.

Once configured, any functions using EF1 shall use collision free data protocols. EF1 protocols shall also be structured to allow the use of data distribution amplifiers that meet the requirements of clause B3.1.3.

B3.1.1 Wiring of EF1 ports

EF1 responders having two ports for receive and transmit must provide a direct passive link on Pins 4 and 5 between those ports (clause 4.8.2). The responder transmitter shall be connected to this passive link. Devices having three or more ports shall wire the additional ports in a manner appropriate for the device's functionality. The manner in which these ports are wired shall be clearly detailed in the product's manual. Devices having three or more ports shall have two ports wired as a loop through with an attached responder transmitter.

B3.1.2 Bi-directional distribution amplifiers

Systems using EF1 topologies require bi-directional distribution/return data combiners. The DMX512 primary data pair data may be split and separately buffered as in standard DMX512 buffers. Return data receivers shall be "wire-OR" connected within a unit. This combined received data signal is used to drive back to the return data monitor.

The bi-directional distribution amplifier shall not perform any processing on the data, since some talkback protocols depend upon the relationship with outbound DMX512 to synchronize the return data.

B3.2 EF2 Half duplex on the second data pair

Systems that send data in both directions on the secondary data link are classified as EF2. These systems shall use the primary data link to send a standard unidirectional DMX512 signal.

B3.3 EF3 Protocols that use the primary and the secondary data links in ways not covered above

Systems that send data in both directions on the primary data link are classified as EF3. These systems shall use the primary data link for both the Null START code DMX512 signal packets as well as return data controlled by the use of Alternate START Code packets. EF3 is not recommended for new implementations.

In an EF3 system, use of the secondary data link is optional. However, all devices that are primarily receivers or that act as processing devices shall support the use of half-duplex bi-directional communication on the secondary pair.

An EF3 system shall used polled feedback on the primary data link, such that a receiving device can not transmit a packet unless instructed to by an appropriate Alternate START Code packet from the controller. All response packets shall begin with an Alternate START Code.

All packets in an EF3 system shall follow the normal timing and rules for a DMX512 packet.

A response message to an ASC packet sent from the controller shall not be sent less than 90uS after receiving the command from the controller. This is to allow for turnaround time in the transceiver. The controller shall allow up to 2.5mS for the response message to be received. After that time, the controller can assume the response to be lost, and resume NSC packets or send another ASC request packet.

A receiver in transmit mode sending a response message shall release the line back to the controller within 44uS of completing its packet.

-end of Annex B-

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Annex C (Informative) - Higher Protection Levels

Some manufactures feel it is prudent to employ higher levels of protection on their DMX512 ports than is specified in EIA-485-A. Many semiconductor manufacturers have recognized the need for higher protection and have produced "fault protected transceivers." The tables below indicate the minimum requirements for a protected DMX512 port. If manufacturer's DMX512 port meets these requirements, the port can be declared as protected.

Table C1 - Transmitter protection

Connection	Minimum Protection Limit			Comment
Pin 2 to Pin 1 or Pin 3 to Pin 1	30 VAC / ± 42 VDC			
Pin 4 to Pin 1 or Pin 5 to Pin 1	30 VAC / ± 42 VDC			
Pin 2 to Pin 3	30 VAC / ± 42 VDC			
Pin 4 to Pin 5	30 VAC / ± 42 VDC			
	Ground Referenced	Isolated	Floating (Note 1)	
Pin 1 to Chassis	shall not exceed 0.2 ohms	N/A	N/A	See clause 6.3
Any other Pin to Chassis	30 VAC / ± 42 VDC	N/A	N/A	
Any Pin to Chassis	N/A	30 VAC / ± 42 VDC	30 VAC / ± 42 VDC	

Note 1 : Floating heading to indicate that this is only encountered on DMX512 Processing equipment.

Table C2 - Receiver protection

Connection	Minimum Protection Limit			Comment
Pin 2 to Pin 1 or Pin 3 to Pin 1	30 VAC / ± 42 VDC			
Pin 4 to Pin 1 or Pin 5 to Pin 1	30 VAC / ± 42 VDC			
Pin 2 to Pin 3	30 VAC / ± 42 VDC			
Pin 4 to Pin 5	30 VAC / ± 42 VDC			
	Non-Isolated	Isolated	Floating (Note 2)	
Pin 1 to Chassis	-note 1-	N/A	N/A	
Any other Pin to Chassis	30 VAC / ± 42 VDC	N/A	N/A	
Any Pin to Chassis	N/A	30 VAC / ± 42 VDC 100Mohm at 50 VDC	30 VAC / ± 42 VDC ≥ 22Mohm at 50 VDC	

Note 1: This cannot be characterized in terms of voltage. Clause A2 (Receiver Characteristics) allows manufacturers to fit a resistance between chassis and Pin 1 for the purpose of limiting the current in the screen (shield) due to small ground differentials. Any such resistance shall survive continuous connection to voltages within the EIA-485 Common Mode range of -7/+12 VDC. Manufacturers shall ensure that any failure of this component due to exposure to voltages not exceeding 30 VAC / 42 VDC will not cause a safety hazard.

Note 2: Floating heading to indicate that this is only encountered on DMX512 Processing equipment.

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Annex D (Normative) - Alternate START Codes Implementation

D1 ASC refresh interval

A DMX512 transmitter interleaving NULL START Code packets with Alternate START Code packets shall send a NULL START Code packet at least once per second.

D2 Timing differences for Alternate START Code packets

To ensure that in-line processing devices do not lose essential Alternate START Code data, a reduction in the Alternate START Code update rate may be necessary. Recommended methods of achieving this are:

1) Alternate START Code packets may be transmitted slower than the minimum timings specified in clause 9.12 by increasing the break to break time to 10% more than the minimum required for the Alternate START Code packets number of slots.

2) Transmitters may interlace non essential Null START Code packets with Alternate START Code packets.

D3 Handling of Alternate START Code packets by in-line devices

DMX512 processing devices or any device that receives and re-transmits DMX512 shall state in the manual for the product how they process Alternate START Code packets. The acceptable processing methods are:

1) Block all packets containing particular Alternate START Codes. The START Codes blocked must be declared (and may be all Alternate START Codes).

2) Pass unmodified all packets containing particular Alternate START Codes. The START Codes passed must be declared.

3) Process the information contained in packets containing particular Alternate START Codes. The algorithm must be stated in enough detail to allow the user to decide if the device will satisfy their needs.

DMX512 in-line repeating transmitters should not pass some packets with a particular Alternate START Code while blocking other packets containing the same Alternate START Code unless doing so as part of a stated processing algorithm.

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Annex E (Normative) - Reserved Alternate START Codes

E1 Reserved Alternate START Codes

Several Alternate START Codes are reserved for special purposes or for future development of the Standard.

Table E1 - Reserved Alternate START Codes

Alternate START Code		Purpose	Note
Hexadecimal	**Decimal**		
17	23	Text Packet	see Annex Clause E2 for implementation
55	85	Test Packet	see Annex Clause E3 for implementation
90	144	90h is reserved for future expansion	
91	145	91h followed by a 2 byte Manufacturer ID field is reserved for Manufacturer/Organization specific use – the first byte after the Manufacturers ID would normally be a manufacturer's sub-code	The Manufacturer ID serves as an identifier that the data following in that packet is proprietary to that entity and should be ignored by all others
92 - A9	146 - 169	possible future revisions of this Standard	No equipment shall be manufactured that generates any of these codes until their use is defined by the Standard
AB - CD	171 - 205	possible future revisions of this Standard	No equipment shall be manufactured that generates any of these codes until their use is defined by the Standard
CF	207	System Information Packet	see Annex E4 for implementation
F0 - F7	240 - 247	prototyping/experimental use while the manufacturer/organization is waiting for their registered Alternate START Code to be assigned	Manufacturers shall not advertise or sell products or devices that use Alternate START Codes F0 - F7.

E2 ASC text packet

Alternate START Code 17h (23 decimal) shall designate a special packet of between 3 and 512 data slots. The purpose of the ASC text packet is to allow equipment to send diagnostic information formatted for display.

Slot allocation is as follows:

Slot 1: Page number of one of the possible 256 text pages.

Slot 2: Characters per Line. Indicates the number of characters per line that the transmitting device has used for the purposes of formatting the text. A slot value of zero indicates ignore this field.

Slots 3-512: Consecutive display characters in ASCII format. All characters are allowed and where a DMX512 text viewer is capable, it shall display the data using the ISO/IEC 646 standard character set. A slot value of zero shall terminate the ASCII string.

E3 ASC test packet

Alternate START Code 55h (85 decimal) shall designate a special test packet of 512 data slots, where all data slots carry the value 55h (85 decimal). Test packets shall be sent so that the time from the start of the Break until the stop bit of the 513th slot shall be no more than 25 milliseconds. When test packets are sent back to back, the Mark Before Break time shall be no more than 88 microseconds. The Break timing for test packets shall be greater than or equal to 88 microseconds, and less than or equal to 120 microseconds. The Mark After Break time shall be greater than or equal to 8 microseconds and less than or equal to 16 microseconds.

E4 System Information Packet (SIP) Alternate START Code

Alternate START Code CFh (207 decimal) is reserved for a System Information Packet (SIP). The SIP includes a method of sending checksum data relating to the previous packet on the data link and other control information.

E4.1 Application

Manufacturers of control consoles are encouraged to transmit SIPs, either as a background to normal processing or, in conjunction with the special test packet, as part of their suite of system test functions. One of the current problems with testing of DMX512 installations is that it must be done with static test packets – certain modes of testers cannot be used while a console is actually running the show, as by definition the DMX512 packets are varying as each cue runs. The interleaving of SIP's would allow some degree of live testing, particularly if one of more test packets were also sent applicable to the functionality of the receiving device.

Note: For systems requiring a more reliable link, manufacturers would have the option of following every normal packet with a SIP packet, although it is recognized that this would degrade data throughput. It could be used with systems that send packets of fewer than 512 DMX512 data slots or refresh data at less than the maximum rate.

E4.2 SIP format

The SIP Packet Length is from 24 to 255 data slots, in the format specified in Table E1. Equipment that implements SIPs shall be required to transmit them at least once every 15 seconds.

Table E2 - SIP Format

Slot	Definition	Refer to Clause
1	SIP Byte Count/SIP Checksum pointer (valid values in the range of 24 - 255)	
2	Control Bit Field	E4.3
3	MSB of Optional 16 bit additive Checksum of previous packet	E4.4
4	8 bit additive or the LSB of the Optional 16 bit Checksum of previous packet	
5	SIP sequence number	E4.5
6	DMX512 universe number	E4.6
7	DMX512 processing level	E4.7
8	Version of Software sending this SIP	E4.8
9	Standard Packet Len MSB	
10	Standard Packet Len LSB	E4.9
11	Number of Packets transmitted by originating device since last SIP MSB	
12	Number of Packets transmitted by originating device since last SIP LSB	
13	Originating Device's Manufacturer ID MSB	E4.10
14	Originating Device's Manufacturer ID LSB	E4.11
15	Second Device's Manufacturer ID MSB	
16	Second Device's Manufacturer ID LSB	E4.12
17	3rd Predecessor to Last Device's Manufacturer ID MSB	
18	3rd Predecessor to Last Device's Manufacturer ID LSB	
19	4th Predecessor's Device Manufacturer ID MSB	
20	4th Predecessor's Device Manufacturer ID LSB	
21	5th Predecessor's Device Manufacturer ID MSB	
22	5th Predecessor's Device Manufacturer ID LSB	
23	*reserved for future use*	
nn	Checksum of the SIP (max 255)	E4.13

E4.3 Control bit field

d7	d6	d5	d4	d3	d2	d1	d0
1 = MSB checksum exists	1=LSB checksum exists	reserved transmit as 0	reserved transmit as 0	reserved transmit as 0	reserved transmit as 0	reserved transmit as 0	control bit set=1

Processing of the Control Bit is optional. If implemented, when the Control Bit is set (=1), the subsequent NULL START Code packet shall be held pending the reception of the next SIP for validation of the checksum. If a second NULL START Code packet is received without a preceding SIP, the receiver shall return to an immediate use mode and flag this as an error condition.

E4.4 Checksums

8 bit additive checksum (or optional 16 bit additive checksum) of all slots in the previous packet. The checksum includes the START Code. Bits must be set in the control bit field to indicate which type of checksum is being sent.

E4.5 SIP Sequence number

A free running 8 bit counter identifying the SIP and incremented by a SIP generator by 01h on every subsequent SIP. This field may be checked to ensure that SIPS are not being dropped randomly.

E4.6 Originating universe

This slot indicates the (originating) DMX512 universe currently transmitted on this link. 00h is not used. Valid values 01h - FFh (1 decimal - 255 decimal).

E4.7 DMX512 processing level

This slot indicates the level of post console processing. Originating devices shall always transmit a value of 00h in this field. Processing devices such as merge units or any that regenerate or provide a media conversion (e.g., Ethernet to DMX512) facility shall increment the value of this field by 01h. The content of this field indicates a level of process “hops” that data on the link has been subjected to relative to the originating transmitting device.

E4.8 Software version

00h	not implemented
01h - FFh	firmware version of last device

NOTE: This slot for use by the manufacturer and may not correlate with any formally published release identifier.

E4.9 Packet lengths

This declares the standard length of packets for START Code 00, normally transmitted on this link.

Valid values are	0000h	packet length not declared
	0001h - 0200h	designates value of fixed packet length
	0201h - 7FFFh	are not used
	8000h	Dynamic Packet, length not declared
	8001h - 8200h	length of last dynamic packet
	8201h - FFFFh	are not used

E4.10 Number of packets

A 16 bit count of the number of packets transmitted by the originating device since last SIP was transmitted. This count should not increment past FFFFh.

E4.11 Manufacturer ID

Manufacturer ID will be the same 16 bit assignment as used for the Manufacturer's ID field used with Alternate START Code 91h (see Annex E - clause E1).

an ID == 0000h indicates that Manufacturer is not declared.
an ID == FFFFh indicates that Manufacturer has applied for, but not been granted, and ID and that this transmission originates from a product under development.

E4.12 Packet history

Specialist DMX512 Processing devices and media converters shall be required to insert their own Manufacturer's ID into the next available SIP slot. An originating device shall always send its Manufacturer's ID in SIP slots 13 and 14, with 0000h in slots 15, 16; 17, 18; 19, 20 and 21, 22. The next downstream processing device shall insert its own Manufacturers ID into slots 15, 16. The next+1 downstream processing device shall insert its own Manufacturer's ID into slots 17, 18 and so on.

NOTE: This scheme allows for a packet processing history to be traced back though a complex installation of products.

E4.13 SIP Checksum

8 bit additive checksum of the SIP START Code (CFh) and first 23 slots of SIP data.

-end of Annex E-

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Annex F (Normative) - Alternate START Code, Manufacturer ID, and Enhanced Functionality Registration

F1 Alternate START Code Registration Policy: 1 - 255 decimal (01 - FF hexadecimal).

Slot 0 of a DMX512 packet is the START Code. The value of this slot identifies intended use of data in the rest of the packet. The Standard provides for a non NULL or “Alternate” START Code. Where it is required to send proprietary information over a DMX512 data link, a packet starting with a registered Alternate START Code shall be used.

F2 Authorized use

The E1 Accredited Standards Committee or any organization that it authorizes may use an Alternate START Code to provide further extensions to the DMX512 Standard.

F3 Reserved Alternate START Codes

Several Alternate START Codes are reserved for special purposes or for future development of the Standard. See Annex E.

F4 Requests for Registration of New START Codes

Any manufacturer or organizations involved in the use of DMX512 may request that a START Code or Manufacturer ID be registered for their use. Although not encouraged, an Alternate START Code and Manufacturer ID may be registered for proprietary use. Requests shall be forwarded to the Secretariat for the ANSI E1 Accredited Standards Committee – ESTA. ESTA will attempt to honor such reasonable requests as described below.

F4.1 Number of Alternate START Codes per entity

No more than one Alternate START Code may be registered to any one manufacturer/organization. Manufacturers and Organizations with Alternate START Codes registered prior to the publication of this Standard may request one additional Alternate START Code.

F4.2 Selection of the Alternate START Code value and Manufacturer ID

The assignment of any particular numeric START Code or Manufacturer ID value to any particular entity is solely at the discretion of Accredited Standards Committee E1. Assignment depends on the availability of unused and unreserved START Codes and Manufacturer IDs.

F5 Requirements for registration of an EF protocol

No EF protocol intended for use between multiple Manufacturer's will be registered as an EF protocol unless its basic structure is available to anyone by request and can be used freely by any manufacturer. The entire message structure for the protocol does not have to be made public, only the portions that are for public use. It is expected that some protocols may still have portions of the message structure that are reserved for proprietary use (i.e., vendor specific messages). Registration is at the discretion of Accredited Standards Committee E1.

F6 Documentation Register

F.6.1 Documentation for use of Alternate START Codes

The manufacturer/organization requesting registration of an Alternate START Code shall provide a 2-line description of the purpose of the Alternate START Code. They shall list the minimum and maximum number of slots, including the START Code, in any proposed packet. Any provided description (subject to editing) shall be included in the Register. This is not required for functions associated with a manufacturer specific ID under Alternate START Code 91. It is recommended, but not required, for Alternate START Codes assigned prior to the adoption of this version of the Standard.

F6.2 Maintenance and Publication

The ANSI E1 Accredited Standards Committee through its secretariat (ESTA) shall maintain a Register of Alternate START Codes and Manufacturer IDs. ESTA will publish the Registry as needed.

F6.3 Supplemental documentation

If the manufacturer/organization wishes detailed documentation to be in the Public Domain, a note will be added to the Registry, but they will be responsible for such publication.

F7 Ownership

The DMX512 Standards are copyrighted. By registering a START Code or Manufacturer ID, no ownership rights are conferred to any third party. Alternate START Codes are registered to particular entities solely to allow for orderly management of the Standard. The registrant does not own the Alternate START Code or Manufacturer ID.

-end of Annex F-

Inside Back Cover

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