AAT11671

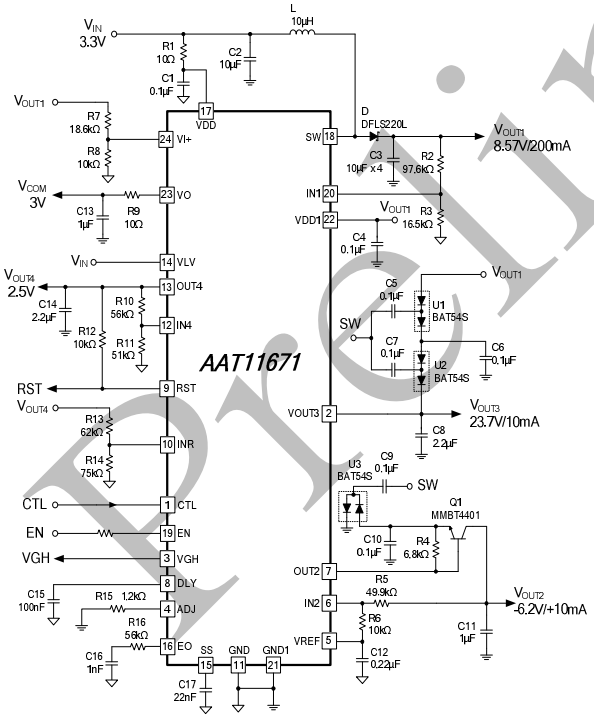
Product information presented is current as of publication date. Details are subject to change without notice.

INTEGRATED TFT LCD POWER SOLUTION

FEATURES

- **Built In 2A (Max.), 0.2Ω Switching NMOS**
- **Negative LDO Driver Down to –14V/+20mA**
- **V_{COM} Operational Amplifier**
- **Up to 350mA LDO**
- **Reset Signal Output for T_{COM}**
- **28V High Voltage Switch for VGH**
- **Adjustable Soft-Start Function**
- **1.2MHz Fixed Switching Frequency**
- **Fault and Thermal Protection**
- **Low Dissipation Current :**
  Typical 2.3mA In Operation
- **VQFN24-4*4 Package Available**

TYPICAL APPLICATION

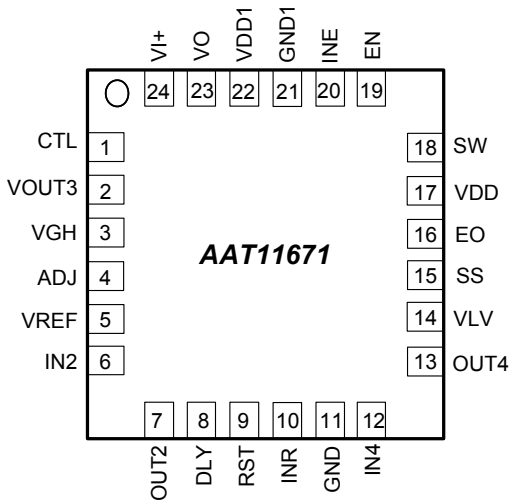


GENERAL DESCRIPTION

The AAT11671 provides a step-up PWM controller, negative high voltage LDO drivers, low dropout linear regulator, V_{COM} operational amplifier and one high voltage switch (up to 28V) for TFT LCD display. RST pin will issue a reset signal to T_{COM} when V_{DD} voltage is too low. The PWM controller consists of an on-chip voltage reference, oscillator, error amplifier, current sense circuit, comparator, under-voltage lockout protection and soft-start control circuit. The thermal and power fault protection prevents excessive power damaging internal circuit. The negative high voltage LDO drivers generate V_{OUT2} voltage (VGL) setting by external resistor divider. For the flicker compensation, VGH will be connected to V_{OUT3} when CTL is high and connected to ADJ when CTL goes low. The AAT11671 contains one operational amplifier capable of supplying 200mA to V_{COM}.

With the minimal external components, the AAT11671 offers a simple and economical solution for TFT LCD power.

PIN CONFIGURATION



ORDERING INFORMATION

DEVICE TYPE	PART NUMBER	PACKAGE	PACKING	TEMP. RANGE	MARKING	MARKING DESCRIPTION
AAT11671	AAT11671 - Q7-T	Q7: VQFN24-4*4	T: Tape and Reel	–40 °C to +85 °C	AAT11671 XXXXX XXXX	1. Part Name 2. Lot No. (6~9 Digits) 3. Date Code (4 Digits)

Note: All AAT products are lead free and halogen free.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
VDD, CTL, VLV to GND	V_{DD}	7	V
VDD1, SW to GND	V_{H1}	14	V
VOUT3 to GND	V_{H2}	28	V
OUT2 to GND	V_{H3}	–14	V
Input Voltage 1 (IN1, IN2, IN4 , INR, DLY, EN, SS)	V_{I1}	V_{DD} +0.3	V
Input Voltage 2 (VI+)	V_{I2}	V_{H1} +0.3	V
Output Voltage1 (EO, RST, OUT4, VREF)	V_{O1}	V_{DD} +0.3	V
Output Voltage 2 (VO)	V_{O2}	V_{H1} +0.3	V
Output Voltage 3 (ADJ, VGH)	V_{O3}	V_{H2} +0.3	V
Operating Free-Air Temperature Range	T_C	–40 to +85	°C
Storage Temperature Range	$T_{STORAGE}$	–65 to +150	°C
Power Dissipation	P_d	1,300	mW

ELECTRICAL CHARACTERISTICS

(V_{IN} = 3.3V, V_{DD1} = 10V, unless otherwise specified.)

Operating Power

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
VDD Input Voltage Range	V_{DD}		2.3	-	5.5	V
VDD1 Input Voltage Range	V_{DD1}		6	-	14	V
VDD Under Voltage Lockout	V_{UVLO}	Rising	2.11	2.21	2.31	V
		Falling	2.01	2.11	2.21	
VDD Operating Current	I_{VDD}	V_{IN1} = 1.5V, Not Switching	-	0.4	0.8	mA
		V_{IN1} = 1.2V, Switching	-	2.3	5.0	mA
VDD1 Operating Current	I_{VDD1}	V_{VI+} = 4V	-	1.2	3.0	mA
VLV Operating Current	I_{VLV}	V_{VLV} = 5V, I_{OUT4} = 0mA	-	0.2	0.4	mA
Thermal Shutdown	T_{SHDN}		-	160	-	°C

Reference Voltage

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
Reference Voltage	V_{REF}	$I_{V_{REF}}$ = 100µA	1.224	1.240	1.256	V
Line Regulation		$I_{V_{REF}}$ = 100µA, V_{DD} = 2.6V~5.5V	-	2	5	%/V
Load Regulation		$I_{V_{REF}}$ = 0~100µA	-	1	5	%/mA

Oscillator

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
Oscillation Frequency	f_{OSC}		1.0	1.2	1.4	MHz
Maximum Duty Cycle	D_{MAX}		86	90	94	%

ELECTRICAL CHARACTERISTICS

(V_{IN} = 3.3V, V_{DD1} = 10V, unless otherwise specified.)

Soft Start & Fault Detect

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
Channel 1 Soft Start Current	I_{SS}	V_{SS} = 1V	–2	–4	–6	µA
During Fault Protect Trigger Time	t_{FP}		150	164	180	ms
Channel 1 to Channel 2 Delay	t_{D12}		30	34	38	ms
Channel 2 to Channel 3 Delay	t_{D23}		23	27	31	ms
IN1 Fault Protection Voltage	V_{F1}		1.00	1.05	1.10	V
IN2 Fault Protection Voltage	V_{F2}		0.20	0.25	0.30	V

EN Control Inputs Characteristics

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
Input Low Voltage	V_{IL}		-	-	0.4	V
Input High Voltage	V_{IH}		1.4	-	-	V

Error Amplifier (Channel 1)

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
Feedback Voltage	V_{IN1}		1.224	1.240	1.256	V
Input Bias Current	I_{B1}	V_{IN1} = 1V to 1.5V	–40	0	+40	nA
Feedback-Voltage Line Regulation		Level to Produce V_{EO} =1.24V 2.3V < V_{DD} < 5.5V	-	0.05	0.15	%/V
Transconductance	Gm	ΔI = 5µA	-	85	-	µS
Voltage Gain	Av		-	1,500	-	V/V

ELECTRICAL CHARACTERISTICS

(V_{IN} = 3.3V, V_{DD1} = 10V, unless otherwise specified.)

N-MOS Switch

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
Current Limit	I_{LIM}		-	2	-	A
On-Resistance	R_{ON}	I_{SW} = 1.0A	-	0.2	-	Ω
Leakage Current	I_{SWOFF}	V_{SW} = 12V	-	0.01	20.00	µA

Negative LDO Driver (Channel 2)

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
IN2 Threshold Voltage	V_{IN2}	I_{OUT2} = –100µA	–15	0	+15	mV
IN2 Input Bias Current	I_{B2}	V_{IN2} = –0.25V to +0.25V	–40	0	+40	nA
OUT2 Source Current	I_{OUT2}	V_{IN2} = 0.5V, OUT2 = –10V	4	20	40	mA

Low Voltage LDO

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
Input Voltage Range	V_{VLV}		2.5	-	5.5	V
IN4 Threshold Voltage	V_{IN4}	I_{OUT4} = 100mA	1.224	1.240	1.256	V
IN4 Input Bias Current	I_{B4}	V_{IN4} = 0V to 1.5V	–40	0	+40	nA
Dropout Voltage	V_{DROP}	I_{OUT4} = 250mA	-	350	500	mV
LDO Output Current	I_{OUT4}		350	-	-	mA
LDO Output Current Limit	I_{LIM4}		-	500	-	mA
Line Regulation		Measure V_{IN4}, V_{VLV} = 2.5 ~ 5V	-	-	5	%/V
Load Regulation		Measure V_{IN4}, I_{OUT4} = 20mA ~ 300mA	-	-	0.1	%/mA

ELECTRICAL CHARACTERISTICS

(V_{IN} = 3.3V, V_{DD1} = 10V, unless otherwise specified.)

High Voltage Switch Controller

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
CTL Input Low Voltage	V_{IL}		-	-	0.5	V
CTL Input High Voltage	V_{IH}		2	-	-	V
CTL Input Bias Current	I_{B4}	CTL = 0 to V_{DD}	–40	0	+40	nA
Propagation Delay CTL to VGH (Form Low to High)	T_{PPLH}	V_{OUT3} = 25V	-	170	-	ns
Propagation Delay CTL to VGH (Form High to Low)	T_{PPHL}	V_{OUT3} = 25V	-	110	-	ns
VOUT3 to VGH Switch R-On	R_{ONSC}	DLY = 1.5V, CTL = VDD	-	30	60	Ω
ADJ to VGH Switch R-On	R_{ONDC}	DLY = 1.5V, CTL = GND	-	50	100	Ω

Reset Output

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
Operating Voltage	V_{OP}		1.6	-	-	V
RST Output Voltage	V_{RST}	I_{RST} = 1.2mA	-	-	0.2	V
INR Threshold Voltage	V_{INR}		-	1.1	-	V
DLY Source Current	I_{DLY}	V_{DLY} = 1V	–5	–10	–15	µA
DLY Threshold Voltage	V_{DLY}		1.20	1.24	1.28	V

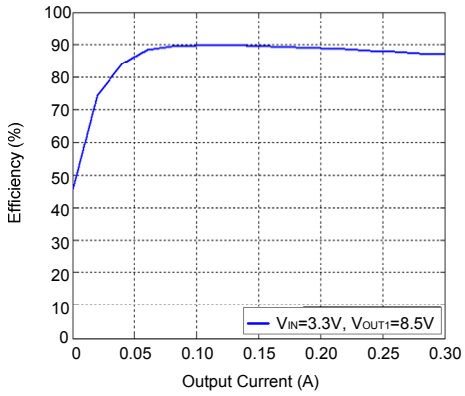
V_{COM} Buffer

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
Input Offset Voltage	V_{OS}	V_{VI+} = 4V	-	2	12	mV
Input Bias Current	I_{B5}	V_{VI+} = 4V	–40	0	+40	nA
Output Swing	V_{OH}	I_{VO} = –50mA, V_{VI+} = 4V	-	4.53	4.76	V
	V_{OL}	I_{VO} = 50mA, V_{VI+} = 4V	3.24	3.47	-	
Short Circuit Current	I_{SHORT}	Measure I_{VO}	-	±200	-	mA
Slew Rate	SR	V_{VI+} = 2V to 8V, V_{VI+} = 8V to 2V, 20% to 80%	-	12	-	µs
Settling Time	t_S	V_{VI+} = 3.5V to 4.5V, 90%	-	5	-	µs

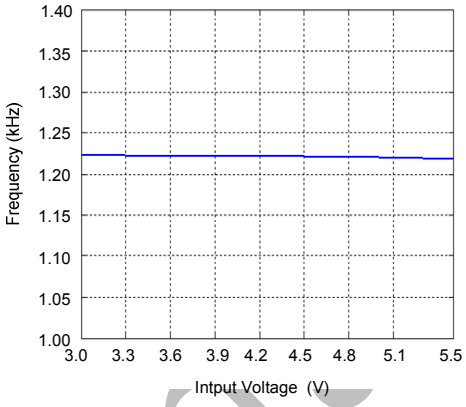
TYPICAL OPERATING CHARACTERISTICS

(V_{IN} = 3.3V, V_{OUT1} = 8.5 V, V_{OUT2} = -6 V, V_{OUT3} = 22 V, T_C= +25°C, unless otherwise noted.)

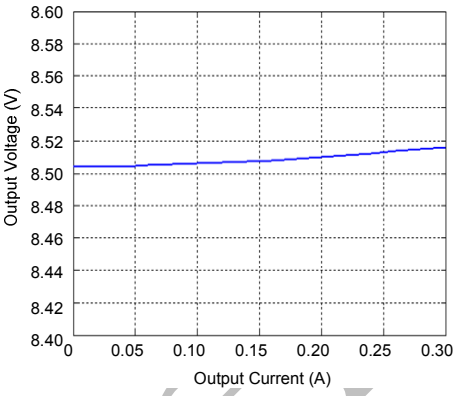
Boost Converter
Efficiency vs. Output Current



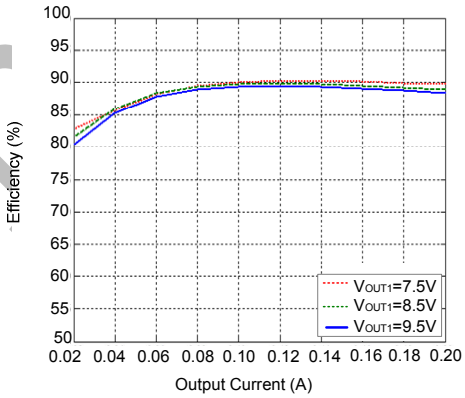
Boost Converter
Frequency vs. Input Voltage



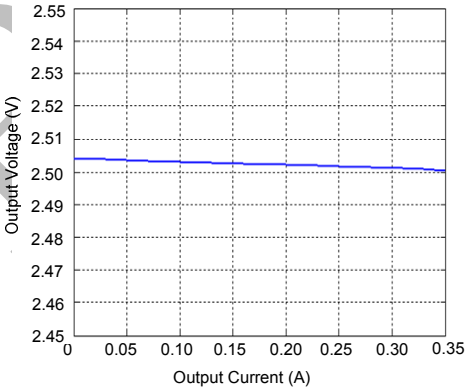
Boost Converter
Output Voltage vs. Output Current



Boost Converter
Efficiency vs. Output Current



VOUT4
Output Voltage vs. Output Current

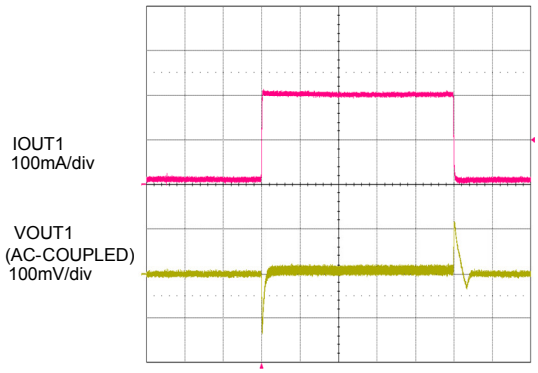


TYPICAL OPERATING CHARACTERISTICS

(V_{IN} = 3.3V, V_{OUT1} = 8.5 V, V_{OUT2} = -6 V, V_{OUT3} = 22 V, T_C= +25°C, unless otherwise noted.)

Boost Converter Transient Response

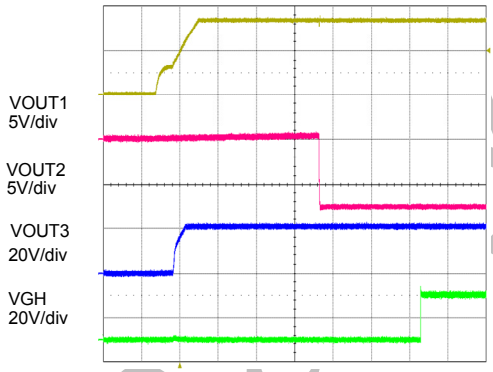
IOUT1=10mA to 200mA



Power On Sequence

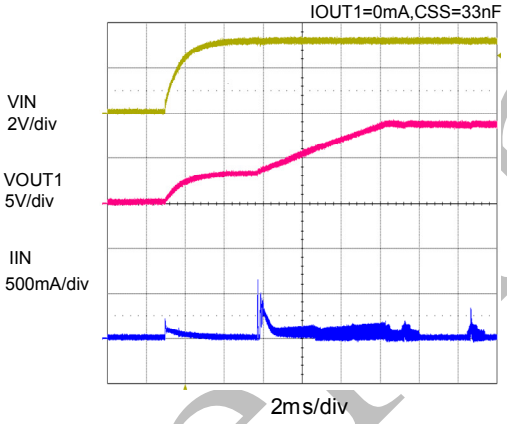
CDLY=0.1µF, CSS=33nF

IOUT1=200mA, IOUT2=10mA,IOUT3 =5mA



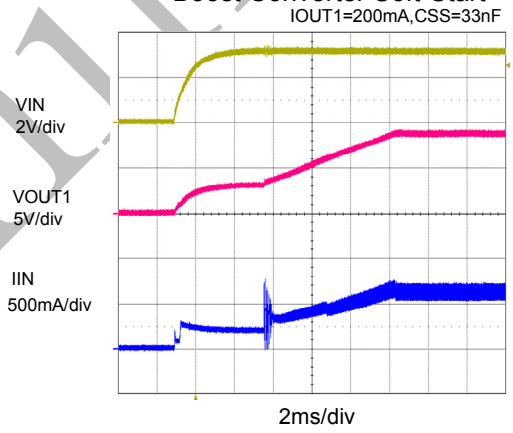
Boost Converter Soft-Start

IOUT1=0mA,CSS=33nF



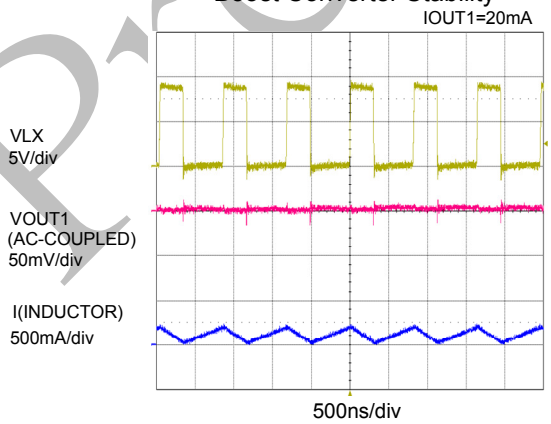
Boost Converter Soft-Start

IOUT1=200mA,CSS=33nF



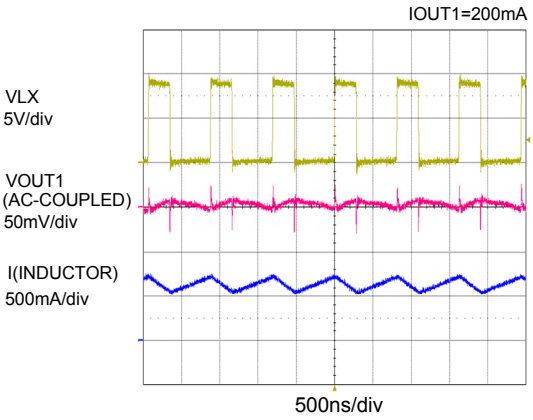
Boost Converter Stability

IOUT1=20mA



Boost Converter Stability

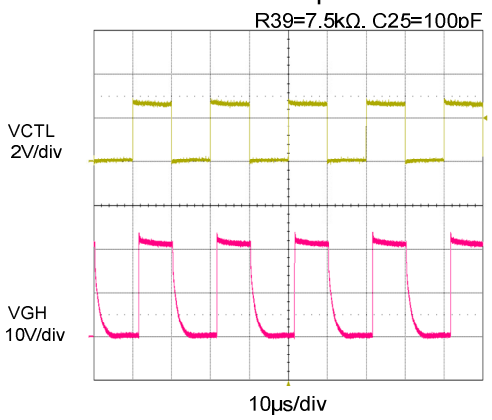
IOUT1=200mA



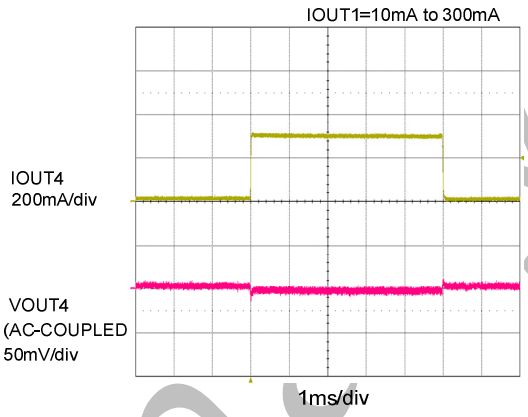
TYPICAL OPERATING CHARACTERISTICS

(V_{IN} = 3.3V, V_{OUT1} = 8.5 V, V_{OUT2} = -6 V, V_{OUT3} = 22 V, T_C= +25°C, unless otherwise noted.)

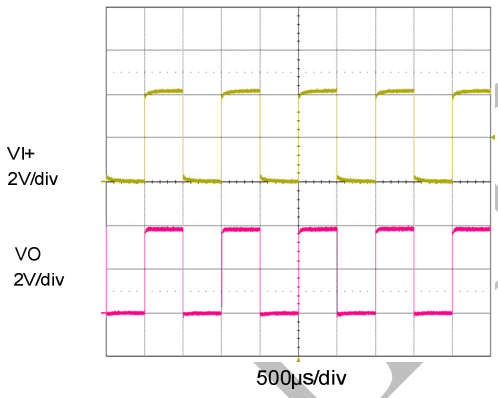
Flicker Compensator



V_{OUT4} Transient Response



Operational Amplifier Large Signal Response

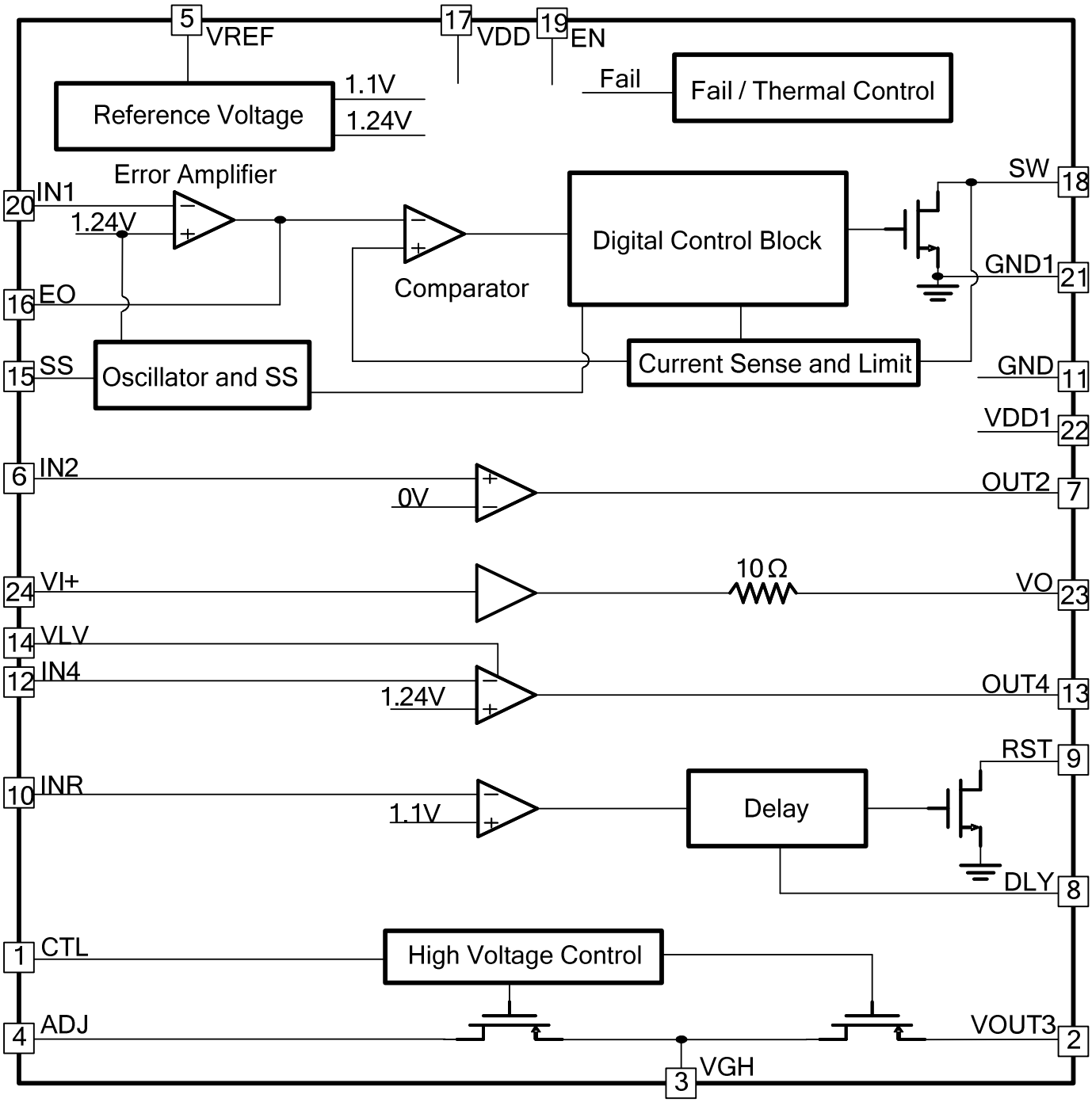


PIN DESCRIPTION

PIN NO. QFN-24	NAME	I/O	DESCRIPTION
1	CTL	I	High Voltage Switch Control Pin
2	VOUT3	-	Gate High Voltage Input (Channel 3 Output Voltage)
3	VGH	O	Switching Gate High Voltage for TFT
4	ADJ	O	Gate High Voltage Fall Time Setting Pin
5	VREF	O	Internal Reference Voltage Output
6	IN2	I	Negative Voltage LDO Feedback Pin
7	OUT2	O	Negative Voltage LDO Output
8	DLY	I	Reset Signal Delay Control
9	RST	O	Reset Signal Output
10	INR	I	Reset Signal Detection Input
11	GND	-	Ground
12	IN4	I	Low Voltage LDO Feedback Pin
13	OUT4	O	Low Voltage LDO Output Pin
14	VLV	-	Low Voltage Power Pin
15	SS	I	Main PWM Soft Start Control Pin
16	EO	O	Main PWM Error Amplifier Output
17	VDD	-	Power Supply Input
18	SW	-	Main PWM Switching Pin
19	EN	I	Main PWM Enable and OCP Control Pin
20	IN1	I	Main PWM Feedback Pin
21	GND1	-	SW MOS Ground
22	VDD1	-	High Voltage Power Supply Input
23	VO	O	Operational Amplifier Output
24	VI+	I	Operational Amplifier Positive Input

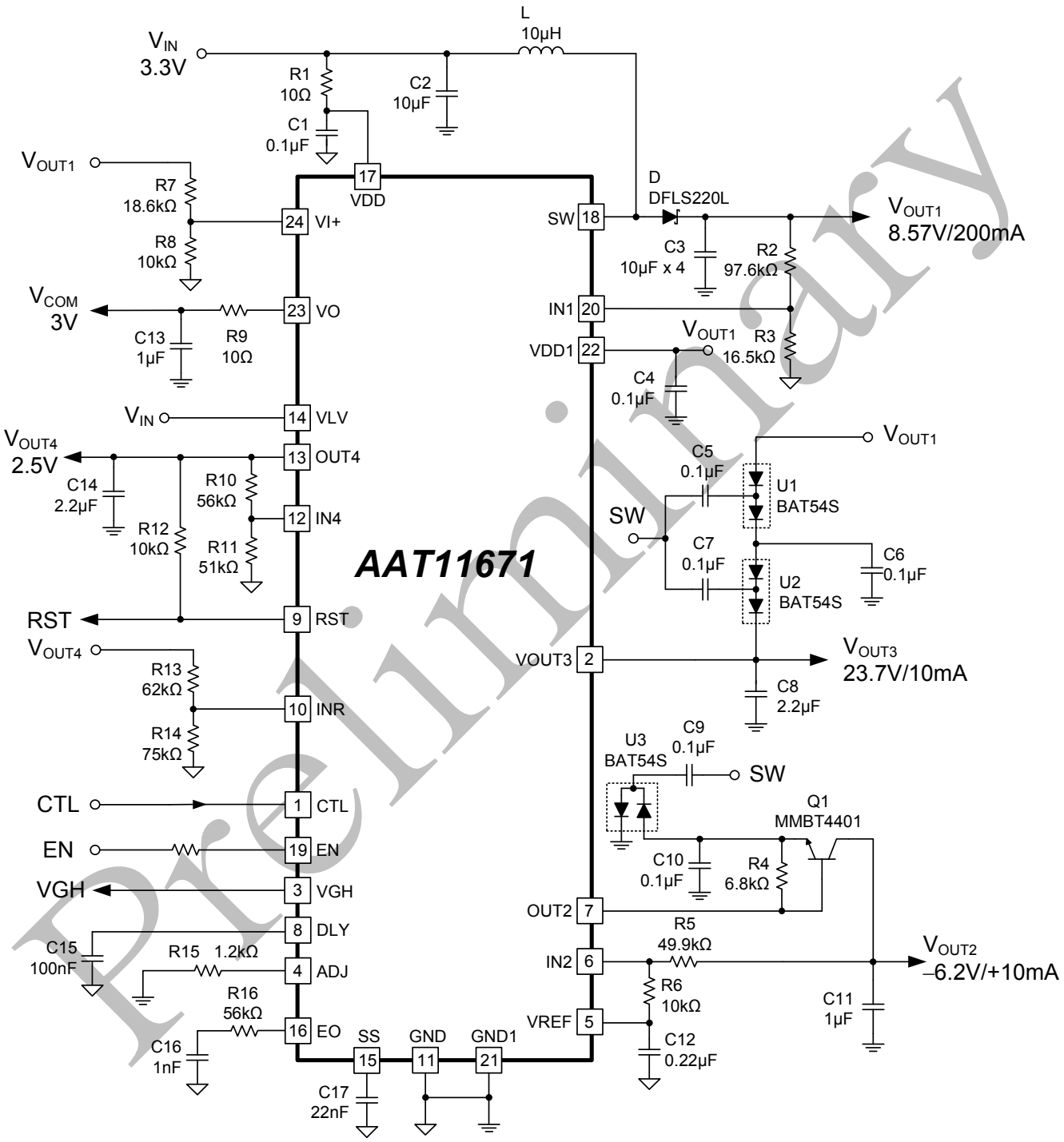
FUNCTION BLOCK DIAGRAM

AAT11671



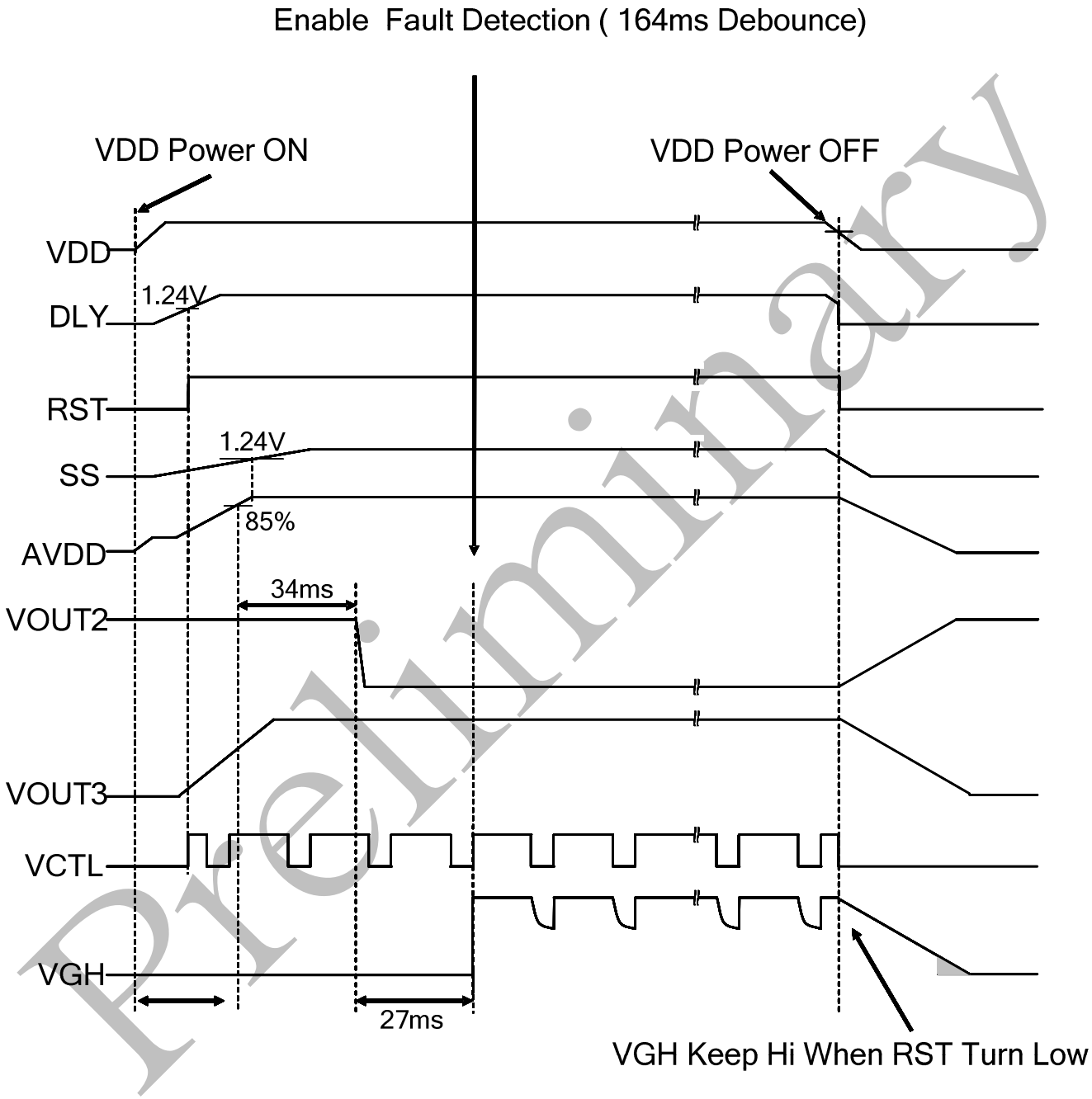
TYPICAL APPLICATION CIRCUIT

AAT11671



POWER ON AND POWER OFF TIMING CHART

AAT11671



DESIGN PROCEDURE

Boost Converter Design

Inductor Selection

The minimum inductor value is selected to make sure that the system operates in continuous conduction mode (CCM) for high efficiency and to prevent EMI. The equation of inductor used a parameter κ, which is the ratio of the inductor peak to peak ripple current to the input DC current. The best trade-off between voltage ripple of transient output current and permanent output current has a κ between 0.2 and 0.4.

$$L \geq \frac{\eta V_O}{\kappa I_O f_S} D(1-D)^2, \quad D = 1 - \frac{V_{IN}}{V_O}, \quad \kappa = \frac{\Delta I_{Lpeak\text{-}peak}}{I_{IN}}$$

η: Boost converter efficiency
κ: The ratio of the inductor peak to peak ripple current to the input DC current
V_{IN}: Input voltage
V_O: Output voltage
I_O: Output load current
f_S: Switching frequency
D: Duty cycle
$\Delta I_{Lpeak\text{-}peak}$: Inductor peak to peak ripple current
I_{IN}: Input DC current

The AAT11671 SW current limit (I_{LIM}) and inductor's saturation current rating (I_{LSAT}) should exceed $I_{L(peak)}$, and the inductor's DC current rating should exceed I_{IN}. For the best efficiency, choose an inductor with less DC resistance (r_L).

I_{LIM} and $I_{LSAT} > I_{L(peak)}$
$I_{LDC} > I_{IN}$

$$I_{L(peak)} = I_{IN} + \frac{V_{IN} D}{2Lf_S},$$

$$I_{IN} = \frac{I_O}{\eta(1-D)}, \quad P_{DCR} \approx \left(\frac{I_O}{\eta(1-D)}\right)^2 r_L$$

I_{LDC}: DC current rating of inductor
P_{DCR}: Power loss of inductor series resistance

Table 1. Inductor Data List

C6-K1.8L	r_L	DC CURRENT RATING
3.9µH	41mΩ	2.5A
6.8µH	68mΩ	2.2A
10µH	81mΩ	1.8A
MITSUMI Product-Max Height: 1.9mm		

Example: In the typical application circuit (Figure 1) the output load current is 200mA with 8.6V output voltage and input voltage of 3.3V. Choose a κ of 0.3 and efficiency of 90%.

$$L \geq \frac{0.9 * 8.6}{0.3 * 0.2 * 1.2^6} 0.6163(0.3837)^2 \approx 10\mu H$$

$$I_{IN} = \frac{I_O}{\eta(1-D)} = 0.579A$$

$$I_{L(peak)} = I_{IN} + \frac{V_{IN} D}{2Lf_s} = 0.664A$$

P_{DCR} = 0.0272W or 1.58% power loss

Rectifier Diode Selection

The Schottky diode is recommended to apply in switching converter. To achieve the best efficiency, choose a Schottky diode with less recovery capacitor (C_T) for fast recovery time and low forward voltage (V_F). For boost converter, the reverse voltage rating (V_R) should be higher than the maximum output voltage, and the current rating should exceed the maximum inductor current.

$P_{DIODE} = P_{DSW} + P_{DCOM}$
$P_{DSW} = (1-D)\ V_F Q_R f_S$
$Q_R = V_R C_T$
$P_{DCOM} = V_F I_O\ (1-D)$
P_{DIODE}: Total power loss of diode for boost converter
P_{DSW}: Switching loss of diode for boost converter
P_{DCOM}: Conduction loss of diode for boost converter

Table 2. Schottky Data List

SMA	V_F	V_R	C_T
B220A	0.24V	14V	150pF
B240A	0.24V	28V	150pF
DIODES Product-MAX Height: 2.3mm			

Input Capacitor Selection

The input capacitors have two important functions in PWM controller. First, an input capacitor provides the power for soft start procedure and supply the current for the gate-driving circuit. A 10µA ceramic capacitor is sufficient for most of the applications. Second, an input bypass capacitor reduces the current peaks, the input voltage drop, and noise injection into the IC. A low ESR ceramics capacitor 0.1µF is used in typical circuit. The bypass capacitor is required as close as possible from VDD (Pin17) and GND (Pin11). To ensure the low noise supply at VDD, VDD is decoupled from input capacitor using an RC low pass filter.

Output Capacitor Selection

The output capacitor maintains the DC output voltage. A Low ESR (r_C) ceramic capacitor is recommended for the smaller output ripple and power loss. There are two parameters which can affect the output voltage ripple: 1. the voltage drops when the inductor current flows through the ESR of output capacitor; 2. charging and discharging of the output capacitor also affect the output voltage ripple.

$$V_{RIPPLE} = V_{RIPPLE}(C_{OUT}) + V_{RIPPLE}(ESR)$$

$$V_{RIPPLE}(C_{OUT}) \approx \frac{I_O D}{f_S C_{OUT}}$$

$$V_{RIPPLE}(ESR) \approx I_{L(peak)} r_C$$

Setting the Output Voltage

The output voltage of boost converter is set by the resistor divider from the output (V_{OUT1}) to GND with the center tap connected to the IN1. Where V_{IN1}, the boost converter feedback regulation voltage is 1.24V. Choose R_2 (Figure 1) between 5.1kΩ and 51kΩ and calculate R_1 to satisfy the following equation.

$$R_1 = R_2\left(\frac{V_{OUT1}}{V_{IN1}} - 1\right)$$

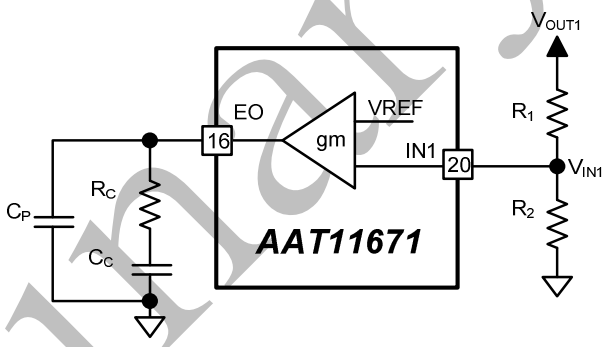


Figure 1. Feedback Circuit

Loop Compensation Design

The loop compensation is consisted by the external resistor R_C, capacitor C_C and capacitor C_P. Choose R_C to set the high frequency integrator gain for fast transient response. Choose C_C to set the integrator zero to maintain loop stability. To improve the transient response, either the R_C value can be increased or the C_C value can be reduced. However, resistor value that is too high or capacitor value that is too low will reduce loop stability. The better compensation value for V_{IN} = 3.3V is recommended by R_C = 56k, C_C = 1nF, C_P = NC.

Soft-Start Selection

The AAT11671 has an adjustable soft-start to prevent high inrush current during start up. The soft-start function is implemented by the external capacitor with a 4µA constant current. The typical soft-start capacitance range is from 22nF to 220nF. A 100nF capacitor is usually sufficient for most of the applications.

Negative LDO Driver Output Voltage Selection

The output voltage of negative LDO driver is set by a resistive divider from the output (V_{OUT2}) to VREF with the center tap connected to the IN2, where IN2, the negative LDO driver feedback regulation voltage is 0V. Choose R6 (Figure 2) between 5.1kΩ and 51kΩ and calculate R5 with the following equation:

$$R5 = R6\left(\frac{-V_{OUT2}}{VREF}\right)$$

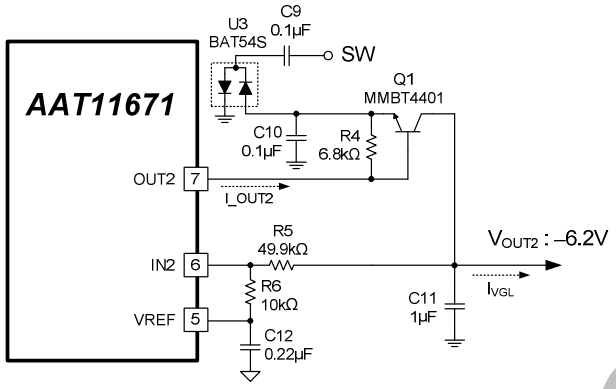


Figure 2. The Negative LDO Driver

Calculation of Negative LDO Driver Base-Emitter Resistor

For the AAT11671, the minimum drive current for negative LDO driver is 4mA, thus the minimum base-emitter resistance can be calculated by the following equation:

$$R4_{(min)} \geq V_{BE(max)} / (I\_OUT2_{(min)} - (I_{VGL} / h_{fe(min)}))$$

Choose resistor R4 to be 6.8kΩ is usually sufficient for most of the applications.

Table 3. Pass Transistor Specifications

	MMBT4401 (NPN)
$V_{BE(max)}$	0.65V
$h_{fe(min)}$	130
DIODES Product, Case: SOT23	

Flying Capacitors

Increasing the flying capacitor (Figure 2, C9) values can lower output voltage ripples. A 0.1µF ceramic capacitor works well in negative LDO driver.

LDO Driver Diode

To achieve high efficiency, a Schottky diode should be used. BAT54S (Figure 2, U3) has fast recovery time and low forward voltage for the best efficiency.

Setting the LDO Voltage

The LDO voltage is set by the resistor divider from the V_{OUT4} to GND with the center tap connected to the IN4. Where IN4, the LDO feedback regulation voltage is 1.24V. Choose R_2 (Figure 3) between 5.1kΩ and 51kΩ and calculate R_1 to satisfy the following equation.

$$R13 = R14\left(\frac{V_{OUT4}}{IN4} - 1\right)$$

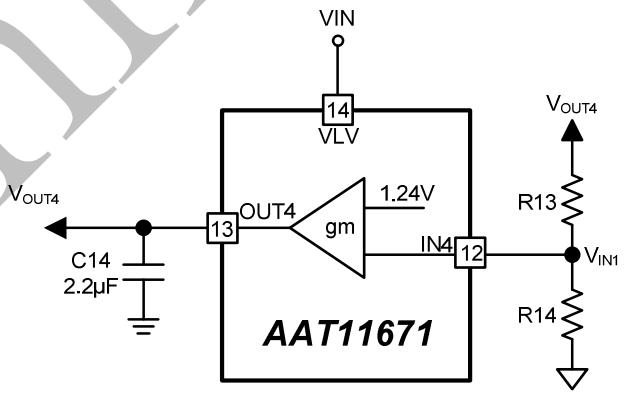


Figure 3. LDO Circuit

Reset Voltage design

The AAT11671 has an integrated reset voltage detector with an open drain output. When V_{INR} value is under the INR threshold voltage 1.1V, the pin RST would be pulled low by inside MOS. The $V_{Detector}$ can be calculated as below :

$$V_{Detector} = 1.1V \times (1 + \frac{R13}{R14})$$

$$R13 = (\frac{V_{Detector}}{1.1V} - 1) \times R14$$

R14 is recommended to be between 5.1kΩ and 30kΩ.

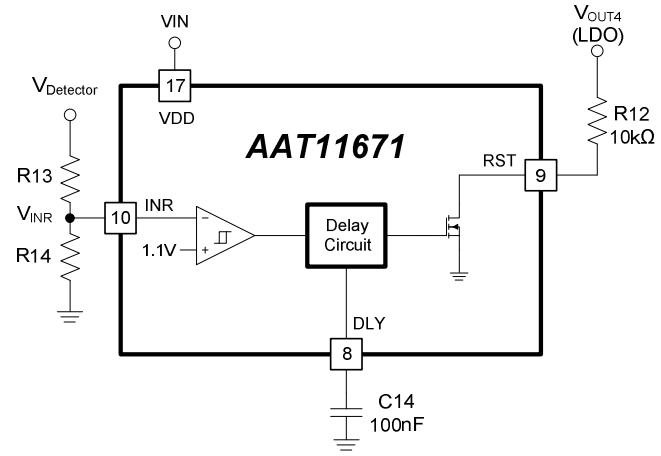


Figure 4. The Application Circuit of Reset Function

The delay time (TD) is set by capacitor C14. The delay time (TD) can be calculated as below:

$$T_D = \frac{C14 * 1.24V}{10\mu A}$$

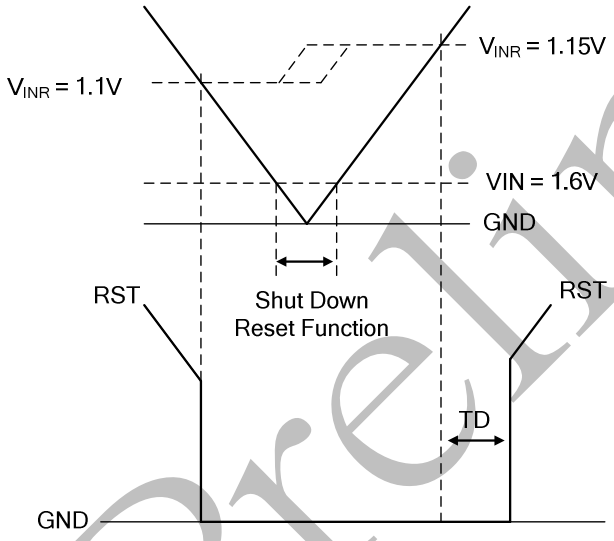


Figure 5. The Timing Chart of Reset Function

V_{COM} Buffer

The VCOM buffer is usually used to drive V_{COM} for TFT-LCD. The buffer is not designed to drive high capacitive loads, so it is recommended to connect a low pass filter with 10Ω resistor and 1µF capacitor. This would provide stable operation when driving high capacitive load.

LAYOUT CONSIDERATION

The system's performances including switching noise, transient response, and PWM feedback loop stability are greatly affected by the PC board layout and grounding. There are some general guidelines for layout:

Inductor

Always try to use a low EMI inductor with a ferrite core.

Filter Capacitors

Place low ESR ceramics filter capacitors (between 0.1µF and 0.22µF) close to VDD and VREF pins. This will eliminate as much trace inductance effects as possible and give the internal IC rail a cleaner voltage supply. The ground connection of the VDD and VREF by pass capacitor should be connected to the analog ground pin (GND) with a wide trace.

Output Capacitors

Minimize the length and maximize the width of traces to get the best transient response and reduce the ripple noise. We choose 10µF ceramics capacitor to reduce the ripple voltage, and use 0.1µF ceramics capacitor to reduce the ripple noise.

Feedback

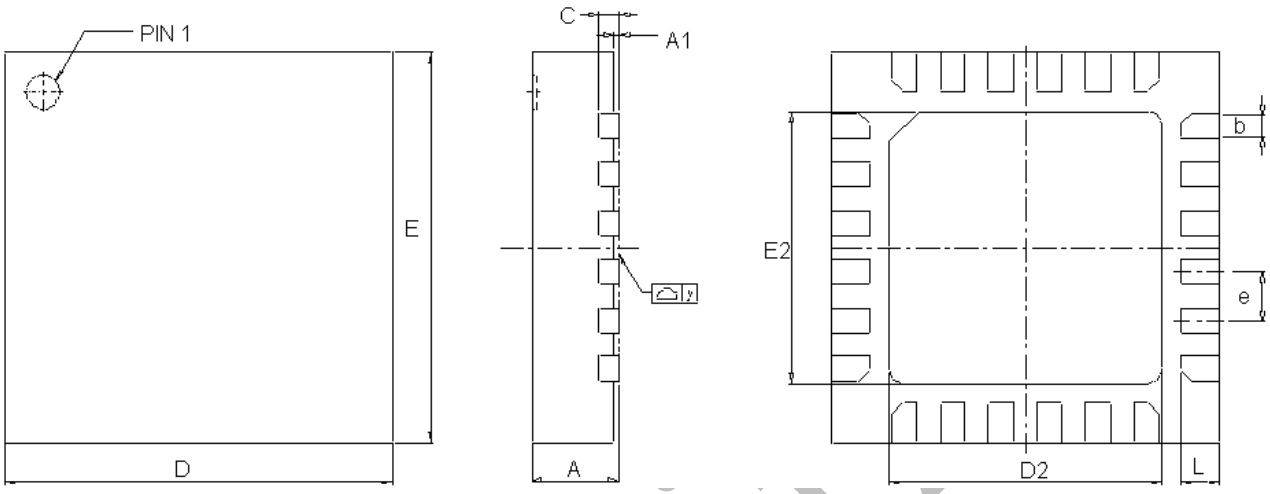
If external compensation components are needed for stability, they should also be placed close to the IC. Take care to avoid the feedback voltage-divider resistors' trace near the SW. Minimize feedback track lengths to avoid the digital signal noise of TFT control board.

Ground Plane

The grounds of the IC, input capacitors, and output capacitors should be connected close to a ground plane. It would be a good design rule to have a ground plane on the PCB. This will reduce noise and ground loop errors as well as absorb more of the EMI radiated by the inductor. For boards with more than two layers, a ground plane can be used to separate the power plane and the signal plane for improved performance.

PACKAGE DIMENSION

VQFN-24 4*4



Symbol	Dimensions In Millimeters		
	MIN	TYP	MAX
A	0.75	0.90	1.00
A1	0	0.02	0.05
b	0.18	0.23	0.30
C	0.19	0.20	0.25
D	3.90	4.00	4.10
D2	2.70	2.80	2.90
E	3.90	4.00	4.10
E2	2.70	2.80	2.90
e	-----	0.50	-----
L	0.30	0.40	0.50
y	0	-----	0.076