**APPLICATION NOTE**

# Read/Write Devices based on the HITAG Read/Write IC HTRC110

**AN 98080**

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**Abstract**

*Designing read/write device (RWD) units for industrial RF-Identification applications is strongly facilitated by the Philips HITAG Reader Chip HTRC110. All needed function blocks, like the antenna driver, modulator demodulator and antenna diagnosis unit, are integrated in the HTRC110. Therefore only a minimum number of additional passive components are required for a complete RWD.*

*This Application Note describes how to design an industrial RF-Identification system with the HTRC110. The major focus is dimensioning of the antenna, all other external components including clock and power supply, as well as the demodulation principle and its implementation.*

*All presented numeric parameters base on the HTRC110 HITAG Reader Chip data sheet [1].*

## APPLICATION NOTE

# Read/Write Devices based on the HITAG Read/Write IC HTRC110

## AN 98080

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# 1. Introduction

With the HITAG Reader Chip, HTRC110 a highly integrated RWD with a powerful circuit implementation is available.

The HTRC110 is ideally suited to design an advanced RWD for industrial applications. The device incorporates all necessary functions to facilitate reading and writing to an external transponder.

It makes use of a unique demodulation technique that extends the system operation range compared with first generation envelope detection based systems.

The HTRC110 is optimized to operate with the Philips transponder family HITAG1 and HITAG2.

Device characteristics, like receiver gain and bandwidth, or transmit timing, are widely programmable, in order to match the RWD to the applied transponder.

For the purpose of system diagnostics, the HTRC110 provides antenna failure detection.

Designed for low power consumption employing CMOS technology, the device supports IDLE and POWER-DOWN modes.

Requiring only few external components and coming in the compact SO14 plastic package the HTRC110 guarantees a minimized overall size.

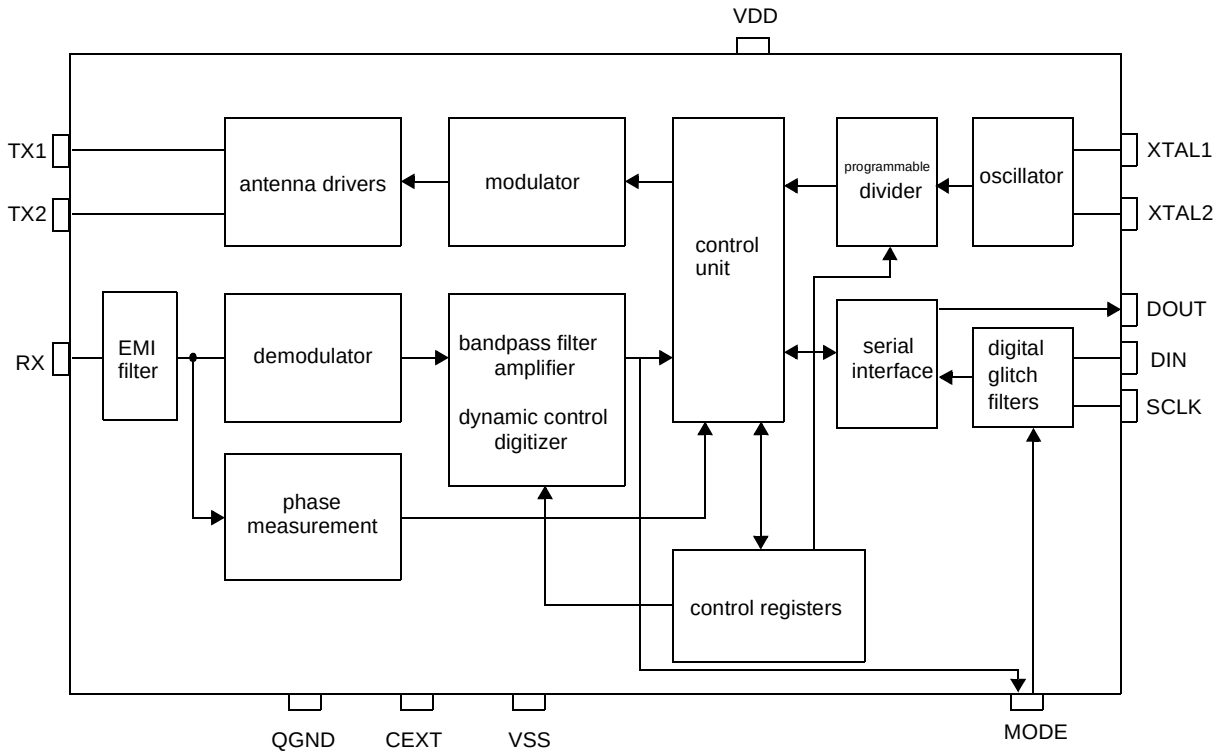



Fig.1 HTRC110 block diagram

# 2. Power supply

The supply current of the HTRC110 consists of two components:

- 10 $mA_{DC}$ maximum for the supply of the IC with its internal function blocks
- the current driven into the antenna resonance circuit

As the antenna current is nearly sine shaped, the average DC-current component can be calculated by:

$$I_{ant_{DC}} = \frac{2}{\pi} \hat{I}_{ant}$$

where $\hat{I}_{ant}$ describes the antenna current amplitude. With $\hat{I}_{ant}$ = 200 mA the maximum overall supply current results in 10 mA + 2/π * 200 mA = 137 mA. Using the burst mode, where $\hat{I}_{ant}$ = 400 mA is allowed for $t_{on}$ < 400 ms at a pulse/pause ratio of 1:4, $I_{ant_{DC}}$ = 265 mA respectively.

When switching on the power supply, the HTRC110 performs an internal power-on reset, where all internal registers (e.g. the configuration pages) are reset to their initial settings (see [1]).

## 2.1 Supply regulation and ripple criteria

Any supply voltage fluctuations or ripple are transferred into antenna current fluctuations by the antenna driver transistors. This is equal to a current modulation that results in a voltage modulation at the antenna tap point. There is no possibility for the demodulator to distinguish this modulation from the transponder modulation. Especially in the passband of the demodulator filters, the system is very sensitive against supply hum and ripple.

Therefore, supply fluctuations cause strong signal disturbances at the demodulator output. Because of this, selecting a proper stable supply regulator is essential for good system performance.

## 2.2 Bypass capacitors

The power supply **shall** be bypassed/decoupled via a 10µF or larger capacitor in parallel to a 100nF capacitor. It is recommended to choose SMD-components being placed close to the VDD- and VSS-pins (Pin-Nr. 1 and 3) in the immediate vicinity of the HTRC110.

The bypass capacitors are extraordinary important because of the following reason: When the field is switched off during the WRITE-pulses, the energy stored in the resonant circuitry results in a current driven into the HTRC110 after switching off the drivers. By this, the current direction at the HTRC110 VDD pin is inverted from sink to source. Normal voltage regulators are only capable to act as source, not as sink. By this, the whole system supply voltage level would be increased even by some volts, if not buffer capacitor of sufficient size is applied. The regulator tries to compensate this effect and stops sourcing current. After the increased voltage is dissipated, normally the recovery time of the regulator leads to an undervoltage for a period of time. This undervoltage can also be in the range of some volts if the buffer capacitors are omitted.

These effects caused by insufficient bypassing can lead to spikes on the supply, that may disturb e.g. µP's connected to the same supply or even cause hardware damage to sensible components of the system.

## 2.3 Power-down modes

Three different power-down modes have been implemented in the HTRC110 for energy saving. After switching back into normal operation mode from all of these three PD modes, it is essential to invoke the settling procedure described in section 11. to allow a fast filter and threshold settling. Without this procedure, settling (being not ready for transponder data) may require several ten milliseconds.

### 2.3.1 Driver-off mode

By setting the TXDIS bit, the antenna drivers can be switched off. All remaining circuitries of the HTRC110 stay active. Driver-off mode is activated by setting the following bit combination via SET_CONFIG_PAGE_1:

PD_MODE = don't care
PD = 0
TXDIS = 1

The other bits in the configuration page 1 don't affect this mode. The drivers are reactivated by resetting the TXDIS bit.

### 2.3.2 Idle mode

In some applications, the HTRC110 oscillator is used to clock the microprocessor. In this case, the oscillator has still to run while the rest of the HTRC110 functionality is powered down. For this purpose, the so called idle mode has been implemented. The idle mode is entered by setting the following bit combination:

PD_MODE = 0
PD = 1
TXDIS = don't care

Resetting the PD-bit exits the idle mode.

### 2.3.3 Power-down mode

It is possible to switch off the whole IC (except the serial interface) by putting it into the power-down mode. The power-down mode can be activated by the following settings:

PD_MODE = 1
PD = 1
TXDIS = don't care

Resetting the PD-bit leaves the power-down mode.

## 3. External filtering capacitors

For bypassing the internal analog virtual ground (~2V), a 100nF capacitor has to be connected from the QGND-pin to the VSS-pin. This capacitor connection should be low impedance and close to the IC.

Another 100nF capacitor is connected from CEXT to VSS which is needed for the 2nd high pass filter. Both capacitors can be ordinary ceramic capacitors.

Leakage currents into CEXT, e.g. caused by dirt or humidity on the PCB, can cause offsets in the demodulator reducing the sensitivity. Therefore it is recommended to place a guard ring at the QGND potential around the CEXT-pin - capacitor lead. The implementation of this guard ring is facilitated because the QGND- and CEXT-pins are next to each other and pin 11 is not connected.

## 4. Clock

The HTRC110 contains an internal clock oscillator being capable to operate with an external quartz or ceramic resonator for frequency stabilization. It is also possible to use this oscillator for clocking a connected microcontroller. Further, the HTRC110 can be clocked by e.g. a microcontroller (Fig.2).

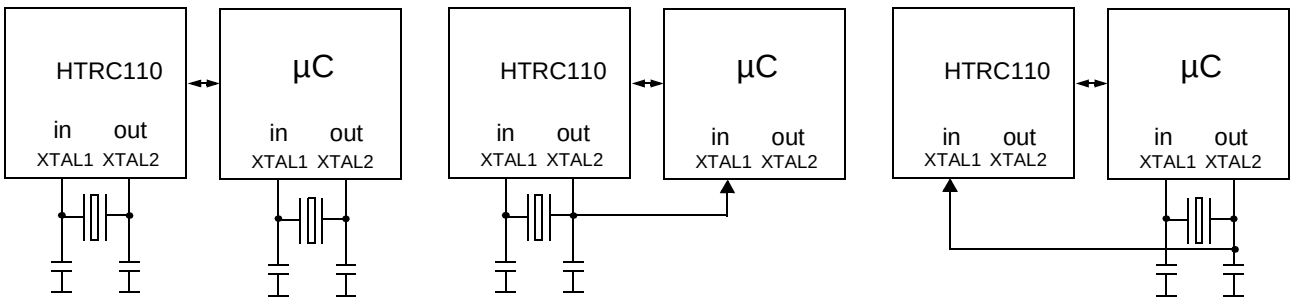



Fig.2 HTRC110 Clock

The internal oscillator is well suited for standard parallel resonance quartz crystals. The capacitors to VSS should be chosen according to the quartz manufacturer specification.

With ceramic resonators, the capacitors are often included internally in the resonator package. Ceramic resonators have a higher tolerance than quartz crystals (e.g. 0.5%-1%). This tolerance adds to the resonance frequency tolerances of the basestation antenna as well as on the transponder tolerance. That means a system frequency shift caused by oscillator tolerances causes a relative shift versus transponder and basestation centre frequency. Systems with relatively high coupling factor and high field strength at the transponder location naturally have a large safe operation tolerance area. In this cases the additional transponder oscillator tolerance does not cause problems. In more critical systems, where the safe operating area regarding frequency tolerance is small because of a low coupling factor or a low field strength at the transponder, we recommend to use a quartz crystal.

In applications, where the HTRC110 is mounted together with the µC on the same PCB, only one clock oscillator is needed, resulting in saving e.g. one quartz crystal which is a relatively expensive component. The HTRC110 oscillator output XTAL2 can be directly connected to most microcontroller clock inputs. It is also possible to use the microcontroller oscillator to clock the HTRC110 via XTAL1.

Jitter on the HTRC110 clock is transferred directly into demodulator noise depending on the sampling phase. Therefore, supplying the HTRC110 with an external high jitter oscillator may strongly reduce the system performance. Special care has been taken at the internal HTRC110 oscillator design to avoid jitter and also to guarantee a fast power on oscillator settling. Therefore, if there are doubts about the quality of the µC-oscillator, it's a good idea to supply the µC with the HTRC110 clock. Some µPs apply clock frequency doublers or PLL clock multipliers. Those devices are especially critical according to jitter considerations.

When supplying the µC with the HTRC110 clock, it is important not to use the power-down mode, because in this case the oscillator is switched off, also stopping the µC. The idle mode is recommended for that case.

Special care has to be taken in systems, that are permanently connected to the battery power supply *and* where the µP is clocked by the HTRC110 oscillator. If the HTRC110 is put into PD-mode, by a transmission error or a software bug, the clock is switched off for both, the HTRC110 and the µP. The only possibility to recover the system from this deadlock is disconnecting the power supply or issuing the oscillator start condition.

Hum picked up by EMI or capacitive feed through on the PCB into the clock connection between HTRC110 and µC can also cause clock jitter. Therefore a short lead length of this interconnection is recommended.

The HTRC110 oscillator works at 4, 8, 12 and 16 MHz quartz crystals. Also external clock signals at the same frequencies can be supplied into XTAL1. The system frequency of 125kHz is generated internally from this clock via a software programmable frequency divider.

The division factor should be set during the HTRC110 initialization phase after power-up by configuring the bits FSEL0 and FSEL1 if the clock frequency is different to the initial value of 4 MHz.

This is done via the command SET_CONFIG_PAGE 3. E.g. adjusting to a clock frequency of 12 MHz is done by the command:

SET_CONFIG_PAGE 3, xx10b

## 5. MODE-pin

MODE is a multi-function pin. In normal operation, it is used for switching on and off the internal digital glitch filters on DIN and SCLK.

If MODE is permanently connected to VSS, the glitch filters are in off-state and the serial interface can be used at high data rates only limited by the specified setup and hold times [1].

### 5.1 Glitch filters

Connecting MODE permanently to VDD activates the internal glitch filters. They offer improved immunity against glitches on the interface signals but reduce the maximum transmission speed. The glitch filter on-mode is intended to be used in the so called 'Active Antenna Applications' where the microcontroller and the basestation communicate via long lines.

The digital glitch filtering is implemented by sampling SCLK and DIN with an 8 µs clock. An input state change is only accepted, when two successive samples have the same result. That means, that each input state at DIN and SCLK has to be longer than 16 µs to pass the filter independently on the time relation between signal and clock. Signals of <8µs duration are suppressed in all cases. Signals with a duration between 8µs and 16µs can pass or not depending on the time relation. Signals longer than 24µs pass in all cases.

The new input state is forwarded to the internal logic at the next 8 µs clock after the two successive comparison samples. Therefore, SCLK and DIN signals are delayed by 16 µs to 24µs. It is important to consider this delay in the software implementation.

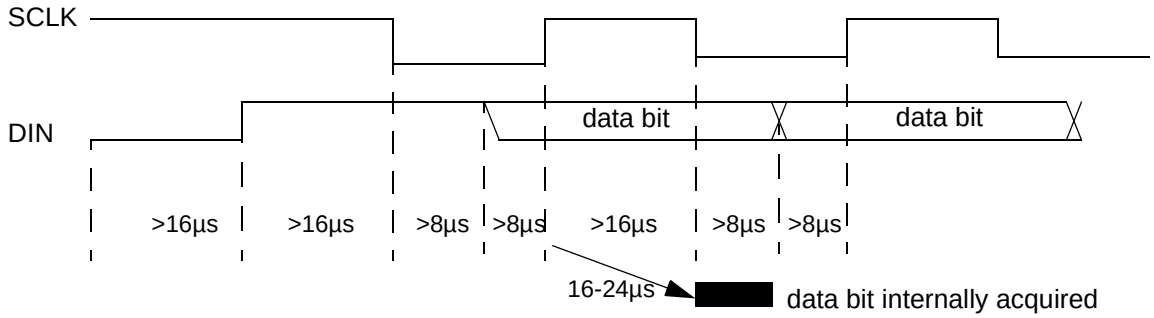



Fig.3 Serial interface reset and data transfer to the HTRC110 with glitch filters on

Due to this delay, also DOUT is delayed by 16µs to 24µs relative to SCLK.

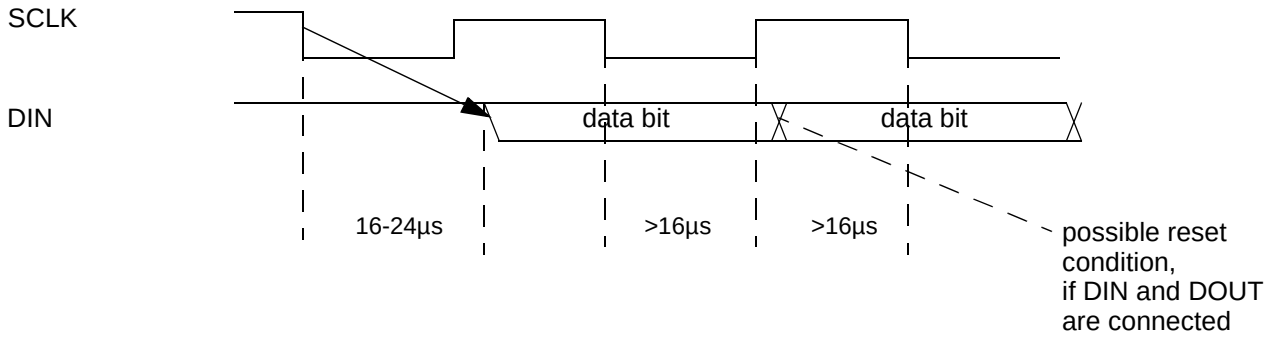



Fig.4 Data transfer from the HTRC110 to the µC with glitch filters on

Fig.4 depicts the data transfer timing from the HTRC110 to the µC. This timing can be used, if DIN and DOUT are not connected to eachother.

If DIN and DOUT are connected to eachother to from a two wire interface, it is essential to consider the DOUT delay to avoid producing an interface reset condition by the data coming out of DOUT and being fed into DIN. That means, SCLK has to be kept low for at least 24 µs in all cases, when data is coming out of DOUT (see Fig.5).

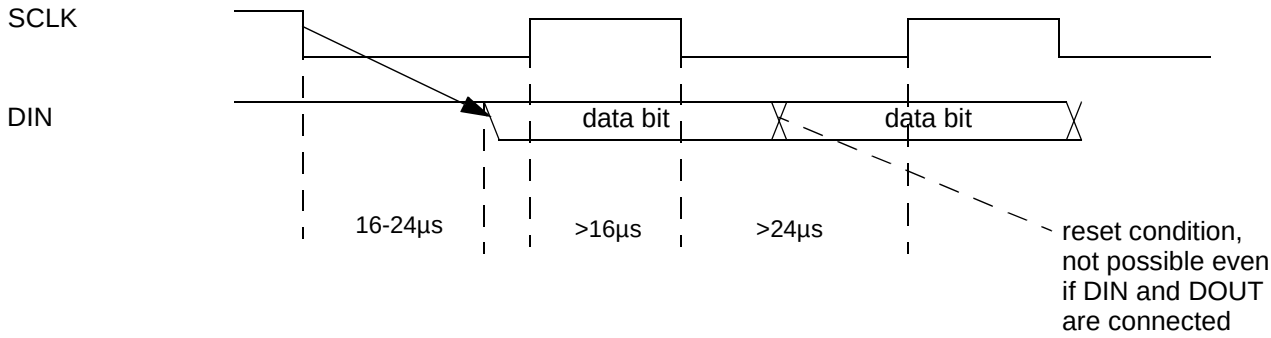



Fig.5 Data transfer from the HTRC110 to the µC with glitch filters on

From the above figures follows, that for writing data to the HTRC110 and reading data from the HTRC110 with a 3-wire interface, the minimum transmission time for one bit is 4 * 8µs = 32µs resulting in a transfer rate of 31.25 kBps.

For reading data from the HTRC110 with a two wire interface, the minimum transmission time for one bit is 5 * 8µs = 40µs resulting in a transfer rate of 25 kBps.

In practice a safety margin should be provided, e.g. in a way to assume not 8µs but 9µs sampling intervals. By this, the transmission time for one bit results in 4 * 9µs = 36µs (27.8 kbit/s). For reading data from the HTRC110 with a two wire interface, the transmission time for one bit is calculated by 5 * 9µs = 45µs (22.2 kbit/s).

### 5.1.1 Data transfer error considerations

If the HTRC110 is clocked by it's internal oscillator and this oscillator is switched off by issuing the PD_MODE command, the digital glitch filters will not pass any state changes. By this, the device is locked. As in any data

transmission systems, data transfer errors can occur. If such an error leads to the PD_MODE, the system would normally be blocked until power off. Therefore, a special backup has been implemented:

When the HTRC110 is in power down mode and SCLK is set to low plus DIN is set not equal to TXDIS, then the oscillator starts up again. This special condition should be issued for at least 10ms. Short spikes fulfilling the condition will not be able to start the oscillator.

When the oscillator starts running, the config bit PD_MODE is cleared automatically and the HTRC110 is in the idle mode afterwards. Leaving the idle mode can be done as usual by resetting the config bit PD.

A data transmission error can also lead to a wrong setting of the config pages. In normal mode this problem can easily be solved by rewriting the config pages. A wrong setting of the clock division ratio leads to longer sampling intervals in the glitch filters. If the HTRC110 clocked e.g. by a 4MHz quartz or an external 4MHz clock and the division ratio is unintentionally set according to a 16MHz clock the glitch filter sampling time is 4 times as long as normal. Therefore the maximum transmission speed is reduced to a forth of the normal speed. Rewriting the config page at this reduced speed solves the problem.

Although these transmission error related special conditions are extremely unlikely, they should be taken into consideration during the software development if a system restart by power-off, power-on is not feasible.

### 5.2 Test output

In a special configuration, during system development, MODE can also be configured to output the demodulated signal after amplification and filtering (see section 9.5).

## 6. Antenna design

Most important for a good system performance and large safety margins in wireless identification applications is a proper design of the antenna. This means a good mechanical design for achieving a long operation distance and a high coupling factor as well as the proper dimensioning of the electrical parameters of the antenna components.

The RWD antenna consists of a RLC series resonance circuitry. The antenna coil can be e.g. either circular or rectangular shaped. The coil dimension depends on the application, especially on the required operation distance. The major boundary conditions for the antenna design are:

- the maximum antenna current provided by the RWD antenna drivers
- the maximum quality factor related to the required data bandwidth
- the maximum antenna inductance resulting from the antenna current and the quality factor
- the minimum operation field strength of the applied transponder
- the minimum coupling factor required for properly demodulating the data sent to the RWD
- the antenna diameter or size

Small antenna coils provide a high field strength and coupling factor, when the transponder is positioned relatively close to the antenna. Both, the field strength and coupling factor show a strong decay when the transponder distance is increased. Therefore, small antennas are well suited for short range applications.

Large antenna coils operated at the same antenna current produce a lower field strength at zero distance and a lower coupling factor, but also the field strength is decaying much slower with increased distance.

For circular antenna coils it can be shown mathematically, that with a given maximum antenna current $\hat{I}_{antmax}$, maximum inductance $L_{amax}$ (resulting from the maximum Q) and minimum transponder operating field strength $B_{min}$ the optimum antenna radius $r_{opt}$ achieving the maximum distance not dropping below $B_{min}$ is roughly given by:

$$r_{opt} \cong \sqrt[3]{\frac{L_{max}}{c} \cdot \left(\frac{\mu_0 \hat{I}_{max}}{\hat{B}_{min}}\right)^2} \qquad c \cong 2{,}6\ \frac{\mu H}{m} \quad \text{for a 'short cylinder coil'}$$

$$\mu_0 = 4\pi \cdot 10^{-7} \frac{Vs}{Am}$$

It can be further shown, that the herewith achieved distance from the antenna plane to the transponder on the coil centre axis equals the optimized coil radius $r_{opt}$.

The optimisation which was discussed so far considered only the tag´s power requirements and supply. If the operation distance is limited by the data transmission channel, a smaller antenna radius may give better results.

## 6.1 Measuring the coupling factor

The coupling factor k describes how close the RWD antenna and the transponder antenna are coupled to each other or, in other words, “how many field lines of the RWD antenna are captured by the transponder antenna”. The coupling factor is a purely geometric parameter being independent from the antenna inductances. It only depends on the form and size of the antennas, their placement relative to each other and the materials inside or close to the coils.

The coupling factor is one of the most important parameters considering the system performance, tolerance ranges and signal to noise ratio. The relation between coupling factor and system performance is stronger than linear.

To measure the coupling factor, a transponder coil without the transponder chip is needed from the transponder manufacturer. This transponder coil is placed instead of the transponder into the antenna field. The antenna coil is excited permanently at 125 kHz by the HTRC110-RWD or by a 125 kHz sine wave frequency generator.

The voltage across the antenna coil and the transponder coil should be measured via high impedance probes or by a proper volt-meter, that is capable to handle 125 kHz correctly. It is important not to apply high resistive or capacitive loads to the relatively high impedance transponder coil by the measurement equipment for measuring the real open circuit voltage. If the HTRC110 is used for exciting the antenna, potential-free scopes or meters should be used because of the full bridge drivers. Alternatively the voltage from the antenna tap point (coil-capacitor connection) can be measured against ground via an ordinary scope or meter.

The coupling factor k results from:

$$k = \frac{U_{transponder\ coil}}{U_{antenna}} \sqrt{\frac{L_{antenna}}{L_{transponder\ coil}}}$$

## 6.2 Electrical antenna parameters

The following sections describe methods for calculating the proper electrical antenna parameters as antenna inductance, resistance and capacitance.

### 6.2.1 Minimum antenna circuitry

The minimum antenna circuitry applicable for the HTRC110 is depicted in Fig.6.

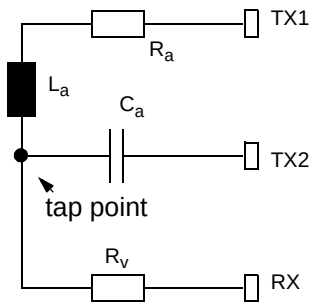



Fig.6 Minimum antenna circuitry

Normally $R_a$ is needed to adapt the antenna quality factor and by this adapt the maximum antenna current.

### 6.2.2 Antenna circuitry with driver short circuit protection

In applications, where the HTRC110 and the antenna coil together form a closed module, the so called active antenna applications, short circuit protection of the driver pins is normally not required. In other applications, were the HTRC110 and the antenna coil are separated and connected to each other via a cable, short circuit protection against VDD and VSS may be required. This can be achieved for both driver pins by dividing the resonance capacitor into two components ($C_a$ and $C_s$) as shown in Fig.7.

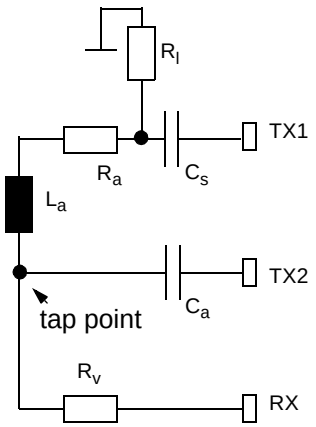



Fig.7 Antenna circuitry with driver protection

By the capacitive decoupling of the antenna coil connections, both drivers are protected against connecting to GND or to 12 V or 24 V.

It is recommended not to symmetrically divide the resonance capacitor into two components, but to use a small, low tolerance (e.g. NP0) capacitor for $C_a$ and a large, higher tolerance capacitor for $C_s$ (e.g. 100 nF).

Applying the resistor $R_l$ is strongly recommended for avoiding influence of low frequency EMI. It provides a low impedance GND-connection for low frequency signals, strayed capacitively into the antenna. Recommended values are:

$C_s$ = 100 nF, $R_l$ =1kΩ

The RX-input is protected via $R_v$ because, even in normal operation, voltages up to ±140 V are present at the antenna tap point between $L_a$ and $C_a$.

### 6.2.3 Adding additional EMI-immunity to the system

In critical applications, additional EMI*-measures may be required for rejecting RF-electromagnetic feed through. Fig.8 depicts one possibility for additional EMI-protection. This filter reduces the EMS* of the antenna.

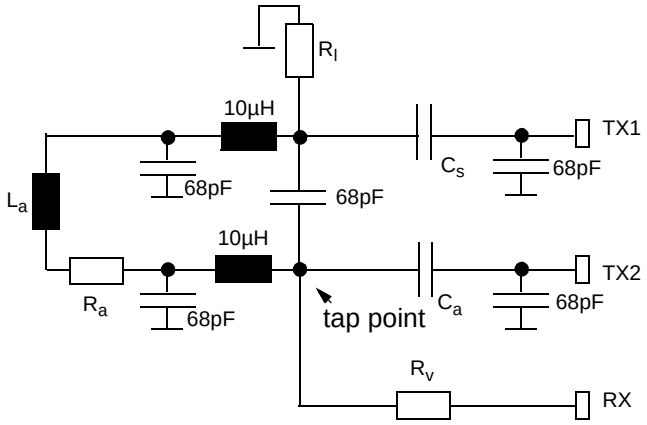



Fig.8 Additional EMI-protection

The filter capacitances and inductances should be optimized for achieving the best EMI performance for the special application. Also different EMI-filter topographies may be used, e.g. for avoiding the 10 µH coils.

### 6.2.4 Dimensioning of the antenna components

The drivers and the antenna (standard antenna shown in Fig.7) can be transformed into the following equivalent circuit diagram:

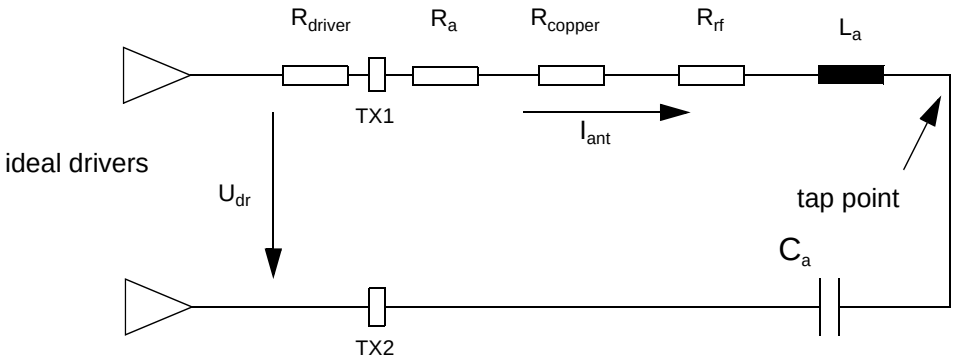



Fig.9 Antenna equivalent circuitry diagram

$R_{driver}$ stands for the driver resistance, $R_a$ for the current adapting resistor, $R_{copper}$ for the winding resistance of the antenna coil including the resistance of the antenna connection and the leads on the PCB. $R_{rf}$ is caused by eddy current losses in metal parts, that might be placed in the direct vicinity of the antenna.

* EMI...Electromagnetic Interference
EMS...Electromagnetic Susceptibility

***Antenna current adapting resistor***

The real part of the antenna impedance is:

$$R_{ant} = R_{driver} + R_a + R_{copper} + R_{rf}$$

The maximum antenna current is flowing in optimum tuned case. It equals:

$$\hat{I}_{ant_{max}} = \frac{\hat{U}_{dr}}{R_{ant}} = \frac{4}{\pi} \cdot \frac{V_{DD}}{R_{ant}}$$

The term $4/\pi$ transforms the amplitude of the rectangular driver voltage to the equivalent sine voltage, which is the fundamental of the rectangular signal.

For VDD = 5V and $I_{antmax}$ = 200 mA, $R_{ant}$ = 31.8 Ω.

If the HTRC110 is used in the burst mode with $I_{antmax}$ = 400 mA, $R_{ant}$ = 15.9 Ω.

For long range systems, external power MOSFET-transistor pairs can be connected to TX1 and TX2 to allow for even higher currents. In this case, $R_{ant}$ shall be further reduced.

For systems with high coupling factors, where the maximum achievable field strength in not needed, $R_{ant}$ can be increased to reduce the antenna current and therefore the system power consumption.

For calculating $R_a$, the other components of $R_{ant}$ have to be known. $R_{driver}$ can be set to 3.5 Ω. $R_{copper}$ can be measured with a multimeter. The sum of $R_{rf}$ and $R_{copper}$ can be measured with a network analyzer at 125 kHz.

An easier method determining $R_a$ is first setting $R_a$ to 20 Ω and running the system with this configuration (with tuned antenna). By monitoring the voltage across $L_a$ with a potential-free scope, an ordinary scope with differential probe or a battery powered multimeter (capable to handle 125 kHz) the current can be measured by calculating:

$$\hat{I}_{ant} = \frac{\hat{U}_{L_a}}{2\pi f_0 L_a}$$

where $f_0$ is the operating frequency of 125 kHz. Alternatively the voltage from the antenna tap point (coil-capacitor connection) can be measured to ground via an ordinary scope or meter.

By increasing or decreasing $R_a$, the current can be adapted to the desired antenna current.

In systems, where $R_{copper}$ is not small compared to the other $R_{ant}$-components, the temperature dependence of the copper resistance has to be taken into account. The highest antenna current flows at the lowest $R_{copper}$. This is reached at the lowest temperature in the allowed temperature range. This temperature dependence can be calculated from the room temperature resistance via the temperature coefficient of copper or measured in a climate camber. At the highest temperature in the allowed temperature range, $R_{copper}$ is the largest. Therefore the lowest antenna current flows, resulting in the lowest field strength. This has to be taken into account when measuring or simulating the system safe operation margins.

***Antenna quality factor***

The antenna quality factor Q is determined by the inductance and the resistance by:

$$Q_a = \frac{2\pi f_0 L_a}{R_{ant}}$$

With increasing Q, the data transfer bandwidth reduces. By this, an upper limit for the antenna quality factor exists. Using the HITAG-transponder family, an upper Q-limit of 20 is recommended. Smaller Q's are generally uncritical. Higher Q's can lead to reduced modulation amplitude in READ-direction and to a WRITE-pulse spreading and delay in WRITE-direction (see section 10.2). When sending data to the transponder, the field is switched off for a short time (e.g. 7 carrier periods), for modulating data onto the carrier. After switching the drivers on again, it takes some time to build up the field again. This rise time is increased with increased Q. By this, short pulses are spread. Therefore, when using high Q antennas, it is important to look at the field gap, produced by the WRITE-pulses, and to compare this to the transponder´s maximum pulse width specification. Also the READ-data rate has to be taken into consideration.

***Antenna inductance***

Choosing the antenna inductance $L_a$ is relatively uncritical.

From the formula given in the section above, the maximum antenna inductance can be directly calculated from $R_{ant}$ and Q. From this results $L_a \leq 800$ µH when operating the HTRC110 in normal mode at $\hat{I}_{antmax}$ = 200 mA and $L_a \leq 400$ µH for the burst mode at $\hat{I}_{antmax}$ = 400 mA respectively. If using an external antenna current boost stage, even lower inductances are required.

In short range systems with high coupling factors, the antenna current can be reduced by increasing $R_a$. In this case, the inductance should be also increased for achieving the optimum system performance.

***Antenna Capacitance***

The antenna capacitance can be calculated for the minimum antenna shown in Fig.6 by the following formula:

$$f_r = \frac{1}{2\pi\sqrt{L_a C_a}}$$

For the standard antenna shown in Fig.7 it is calculated by:

$$f_r = \frac{1}{2\pi\sqrt{\frac{L_a}{\frac{1}{C_s}+\frac{1}{C_a}}}}$$

In systems with low coupling factors resulting in a small tolerance range, applying a low tolerance NP0-capacitor for $C_a$ is recommended.

In practice determining $C_a$ can be easily done like follows:

- calculate $C_a$ with the above formulas and choose the closest available value,
- tune the antenna by changing the number of antenna coil windings or changing the capacitor value. Tuning measurement methods are described in section 7.

***Optimizing the demodulator input resistor***

The demodulator input resistor $R_v$, being part of the demodulator input voltage divider, should be optimized in a way, that at optimum tuning (maximum voltage at the antenna tap point) the amplitude at the RX-pin is $\hat{U}_{RXmax}$ = 7 V - 8 V relative to QGND. By this, the maximum signal-to-noise-ratio is reached.

The maximum tap point voltage is:

$$U_{tap_{max}} = 2\pi f_0 L_a I_{ant_{max}}$$

The RX-pin is internally connected to QGND (~2V) via the resistor $R_{demin}$ (see [1]). Therefore $R_v$ and this internal resistor form a voltage divider. By this, $R_v$ can be calculated by:

$$R_v = R_{demin} \cdot \left( \frac{\hat{U}_{tap_{max}}}{\hat{U}_{RX_{max}}} - 1 \right)$$

When the voltage at RX in respect to QGND becomes larger than ± 8 V, clipping will occur. By this, demodulation of the signal can be strongly disturbed. Therefore it is important not to apply a too small $R_v$. The temperature dependence of $R_{ant}$, $\hat{I}_{antmax}$ and $\hat{U}_{tapmax}$ must be considered.

The maximum value of $R_{demin}$ according to the data sheet should be used for calculating $R_v$. Another possibility for providing a safety margin is calculating $R_v$ for $\hat{U}_{RXmax}$= 7.0 V to 7.5 V instead of 8 V.

For guaranteeing the antenna diagnosis functionality, $R_v$ shall be larger than 80 kΩ. Normally it is in the range of 100 kΩ to 400 kΩ.

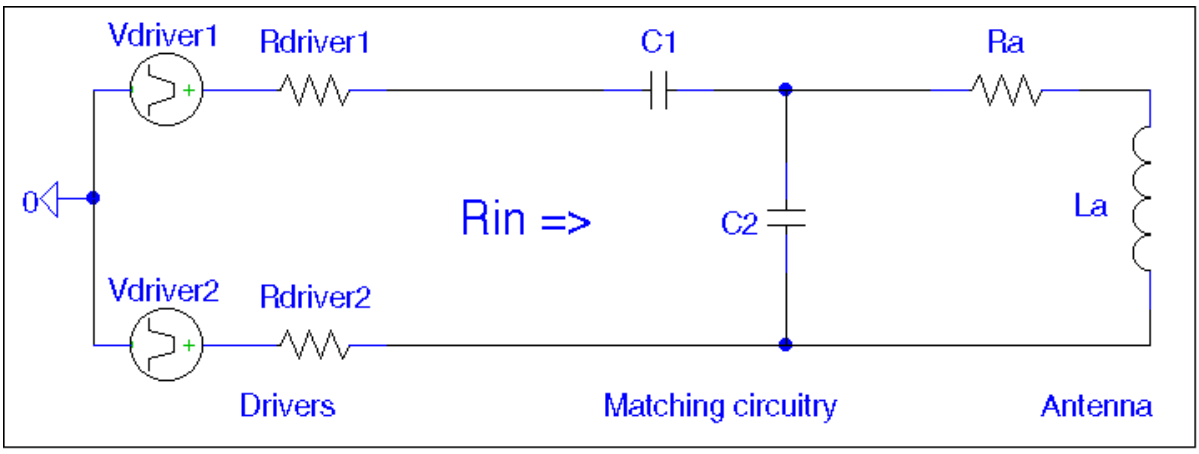
It is extraordinary important to **place $R_v$ as close as possible to the RX-pin** for optimum EMI-performance. The best is, to apply a SMD-resistor placed directly at the pin with minimum (nearly zero) lead length because the path between $R_v$ and the RX-pin is EMI-sensitive because of its relatively high impedance. A close placement of $R_v$ nearly completely avoids capacitive strew in.

In some applications it may be possible to increase the EMI performance by placing a small capacitor (in the order of 10 pF) from the RX-pin to VSS or QGND. Also this component must be close to the RX-pin. Whether it is better to connect this capacitor to VSS or to QGND should be determined by practical tests.

### 6.2.5 Matching circuitry for PCB antennas

In some wireless applications a PCB antenna is used, which usually has a low quality factor. However, these antennas also have a low antenna resistance. So it would be neccessary, to insert a resistor in order to limit the driver current. But this would decrease the quality factor of the antenna even more. The result would be a short transmission range.

Using a matching network to limit the driver current does not lower the quality factor of the antenna. The input resistance of the network can be set to the desired value by design, depending on the driver current limitation. This is done by impedance transformation. The figure below shows, how a system can be equiped with a matching circuitry.




Values for $C_1$ and $C_2$ can be found by the matched condition:

$$R_{IN} = \frac{1}{j\omega C_1} + \frac{\frac{1}{j\omega C_2} \cdot (j\omega L_A + R_A)}{\frac{1}{j\omega C_2} + j\omega L_A + R_A}$$

Equating real and imaginary parts and combining these expressions leads to the final equations for designing the matching network:

$$C_1 = \frac{1}{\omega \cdot \sqrt{R_{IN} \cdot \left( R_A - R_{IN} + \frac{\omega^2 \cdot L_A^2}{R_A} \right)}}$$

$$C_2 = \frac{R_{IN} - R_A}{\omega^2 \cdot L_A \cdot R_{IN} + \frac{R_A}{C_1}}$$

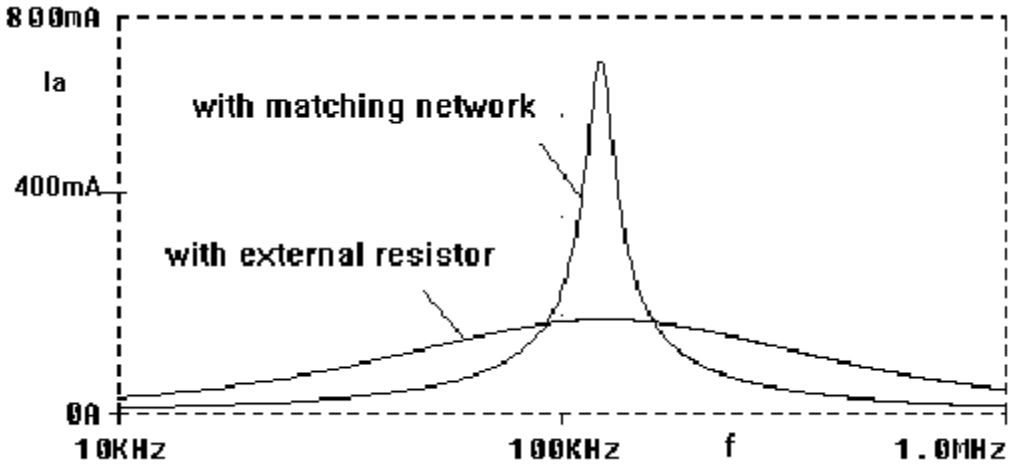
$R_{IN}$ stands for the desired input resistance at the resonance frequency $\omega$ of the antenna.

***Example:***

A PCB antenna has the following parameters: $R_A = 2\Omega$, $L_A = 20\mu H$. The carrier frequency of the system is 125kHz. The input resistance $R_{IN}$ (limited by the maximal driver current of the HTRC110) has to be $32\Omega$.

Using the derived formulas, the calculated values of the elements of the matching circuitry are: $C_1 = 23.3nF$ and $C_2 = 62.4nF$.

The figure below illustrates the advantage of the matching circuitry compared to a solution with external resistor to limit the driver current for the given example.




It can be seen, how the external resistor decreases the quality factor of antenna, whereas the matching network has no influence on the quality factor. Thus, the maximal transmission range of antenna can be achieved.

The proposed matching network consists of two capacitors. That means, that the driver current has a peak at the moment the driver switches. The maximum current is only limited by the drivers output resistors ($R_{dr,typ} = 2.5\Omega$). That would result in a peak current of 2A. For burst mode a maximum driver current $I_{dr,max}$ of 400mA is specified in the data sheet. Therefore, in applications using matching networks a resistor in series ($R_S$) to the driver outputs

should be inserted, to limit the current peak to the maximum allowed value of 400mA. The following equation shows the calculation of $R_S$:

$$R_{S,min} = \frac{U_0}{I_{dr,max}} - R_{dr} = \frac{5V}{400mA} - 2{,}5\Omega = 10\Omega$$

The desired input resistance of the matching network $R_{IN}$ is calculated as follows:

$$R_{IN} = \frac{4 \cdot U_0}{\pi \cdot I_{dr}} - R_{dr} - R_s = \frac{4 \cdot 5V}{\pi \cdot I_{dr}} - 12{,}5\Omega$$

The disadvantage of this modified matched network is, that the quality factor of antenna is changed by $R_S$. For the example above, the quality factor of the matched antenna Q is 1.26. For a circuit without matching network and an antenna resistor of 32Ω (to limit the driver current to 200mA), the quality factor drops to 0.5. Therefore, the modified matching network can still be interesting for applications using PCB antennas.

***Design flow for modified matching networks***

1) Use a serial resistor $R_S$ of 10Ω to limit the peaks in driver current to the maximum allowed value of 400mA

2) Calculate the effective input resistance of the matching network $R_{IN}$

3) Design the matching network consisting of $C_1$ and $C_2$ using the given equations

## 6.3 EMI considerations in antenna design

A wireless identification system has to meet EMI requirements given by relevant regulations. In general, there should be no difficulties to fulfil these requirements. However, the particular national regulations may vary in strictness. For this reason, this chapter shows the theoretical background to calculate the spectral components in antenna current of the HTRC110 and proposes ways to reduce higher harmonics.

To obtain the particular EMI regulations, please contact your national authority responsible for radio communications (see also [2][3][4][5]).

### 6.3.1 Antenna current of higher harmonics without filtering

The antenna current of a certain harmonic can be calculated for an antenna consisting of $L_A$, $C_A$, $R_A$ by the following complex equation:

$$\hat{I}_{AN} = \frac{\hat{U}_{AN} \cdot \omega_N \cdot C_A}{R_A \cdot \omega_N \cdot C_A + j(\omega_N^2 \cdot C_A \cdot L_A - 1)}$$

The antenna voltage $U_{AN}$ represents the spectral components of the rectangular input voltage. These values can be calculated using fourier series . The final formula for the given input voltage shape is shown below:

$$U_A(t) = \frac{4}{\pi} \cdot U_0 \cdot \sin(\omega t) + \frac{4}{3\pi} \cdot U_0 \cdot \sin(3\omega t) + \frac{4}{5\pi} \cdot U_0 \cdot \sin(5\omega t) \ldots$$

Therefore the voltage amplitudes of the particular spectral components are determined by the following equation:

$$\hat{U}_{AN} = \frac{4}{\pi \cdot N} \cdot U_0$$

Since this fourier series has only sine-terms, N can only be odd (1,3,5...).

Inserting the amplitudes found by fourier series evaluation into the complex formula for antenna current, leads to the final formula to calculate the magnitude of antenna current for a certain harmonic:

$$\left|\hat{I}_{AN}\right| = \frac{\frac{4}{\pi} \cdot U_0 \cdot \omega_0 \cdot C_A}{\sqrt{(N \cdot \omega_0 \cdot C_A \cdot R_A)^2 + (N^2 \cdot \omega_0^2 \cdot C_A \cdot L_A - 1)^2}}$$

If the antenna is optimally tuned the current of the first harmonic would be maximum and the formula simplifies to the expression as explained in chapter 6.2.4:

$$\left|I_{A1,\,Max}\right| = \frac{\frac{4}{\pi} \cdot U_0}{R_A}$$

***Example:***

An antenna consist of the following elements: $C_A$ = 4.7nF, $L_A$ = 400µH and $R_A$ = 24 Ohms. The magnitude of the rectangular voltage is $U_0$ = 5V and its frequency $f_0$ = 125kHz. Using the equation above, the current magnitudes of the first harmonics are: $I_{A1}$ = 129mA, $I_{A3}$ = 2.5mA, $I_{A5}$ = 0.85mA.

**Note:**

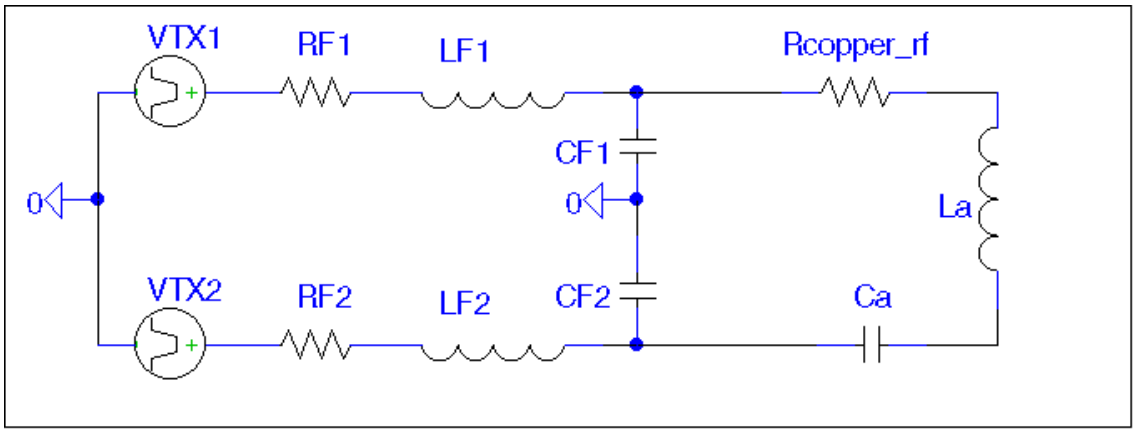
The antenna resistor $R_A$ is assumed to be constant in these calculations. In practice, the skin-effect increases the effective antenna resistor and damps the current of higher harmonics. Thus, the calculated currents of higher harmonics can be seen as worst case.

### 6.3.2 Design of EMI filters

Using the equation given in previous chapter, it is also possible to calculate the influence of antenna detuning on the harmonics of the antenna current. In general, detuning strongly effects the fundamental due to the mismatch in resonant frequency. The higher harmonics are nearly unchanged because the antenna works as a low pass filter for higher frequencies. Its cut-off frequency is not as critical as the resonance frequency of antenna for the fundamental.

The only possible way to reduce higher harmonics in antenna current is to add appropriate EMI filters. Whereas the predefined values of antenna components may not be changed.

In order to minimize the number of filter components and losses, the proposed filter uses a part of the antenna resistor $R_A$ for filter implementation. The schematic below shows the circuit consisting of drivers, filter and antenna components.




The filter is built of $R_F$, $L_F$ and $C_F$. Every element is split into two parts to design a symmetric filter with respect to ground. This is done to filter the voltage at the TAP-point with respect to both driver outputs.

For filter implementation a standard Butterworth approximation is used. This approach has the advantage, that no ripple in passband can disturb the antenna. The proposed circuit forms a 2nd order low pass filter.

To simplify the implementation, the filter is designed without taking the antenna load into account. This assumption is a good approximation for higher harmonics. For exact filter approximation the load has to be decoupled from the filter by an op-amp.

The filters cut-off frequency $f_C$ should be far below the higher harmonics but above the fundamental. For best filter performance, the cut-off frequency of the EMI filter should be set to about 200kHz (for a 125kHz system).

Analysing the filter gives the transfer function. Matching this transfer function to the Butterworth coefficients for 2nd order filters leads to the final equations for calculating the filter elements:

$$C_F = \frac{1{,}414}{2 \cdot \pi \cdot f_C \cdot R_F}$$

$$L_F = \frac{1}{(2 \cdot \pi \cdot f_C)^2 \cdot C_F}$$

***Design flow***

1) Design of the antenna as explained in this application note ($L_A$, $C_A$, $R_A$) independently of the filter

2) Use $R_F$ for EMI filter design and set the cut-off frequency to 200kHz

3) Find $L_F$ and $C_F$ by Butterworth approximation using the given equations

***Example of an EMI filter***

This example illustrates the complete design flow including antenna and EMI filter design.

$$R_{ant} = R_{copper} + R_{driver} + R_a + R_{rf} = \frac{4 \cdot U_0}{\pi \cdot \hat{I}_{ant_{max}}}$$

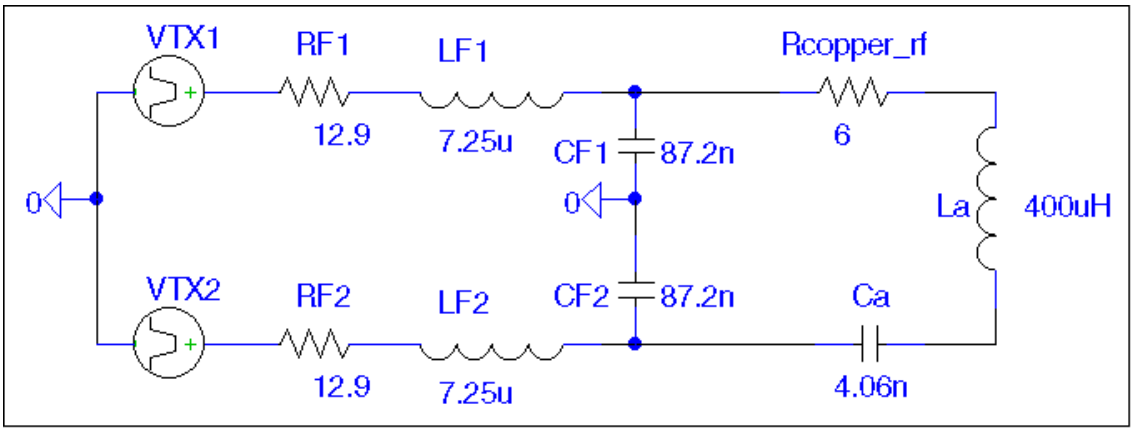
For $U_0$ = 5V and $I_{ant_{max}}$ = 200mA, $R_{ant}$ = 31.8Ω. Choosing an inductance of 400µH gives an antenna quality factor of about 10. To get the desired resonance frequency of 125kHz, the antenna capacitance has to be 4.06 nF.

Now the antenna design is done. For the proposed filter only a part of $R_{ant}$ can be used for filter implementation.

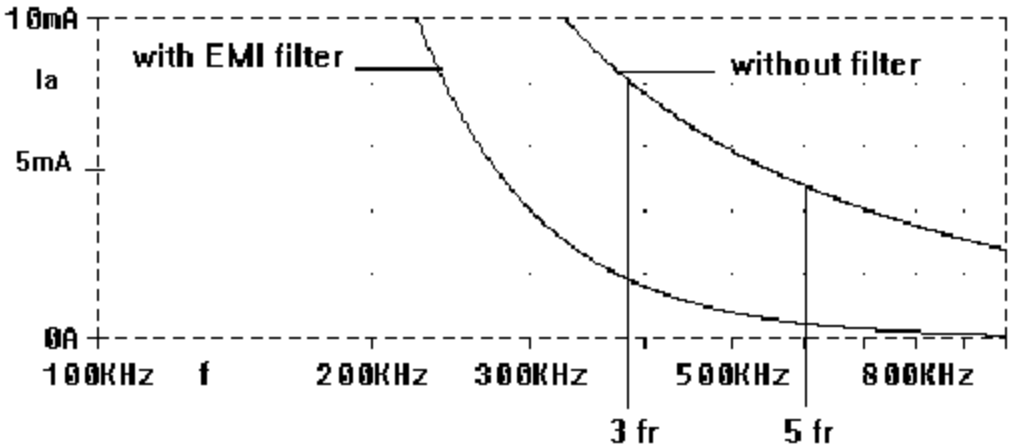
$$R_F = R_{ant} - R_{copper} - R_{rf}$$

Here $R_{copper} + R_{rf}$ is assumed to be 6Ω. So the usable resistance $R_F$ for the filter circuit is 25.8Ω. This value includes the driver resistance and the copper resistance of the filter inductance.

Inserting $R_F$ = 25.8Ω and $f_c$ = 200kHz into the implementation formulas the values for the filter components were calculated: $C_F$ = 43.6nF and $L_F$ = 14.5µH. Therefore the values of the symmetric filter are $L_{F1} = L_{F2} = L_F/2$ and $C_{F1} = C_{F2} = 2\ C_F$. The figure below shows the entire circuit.

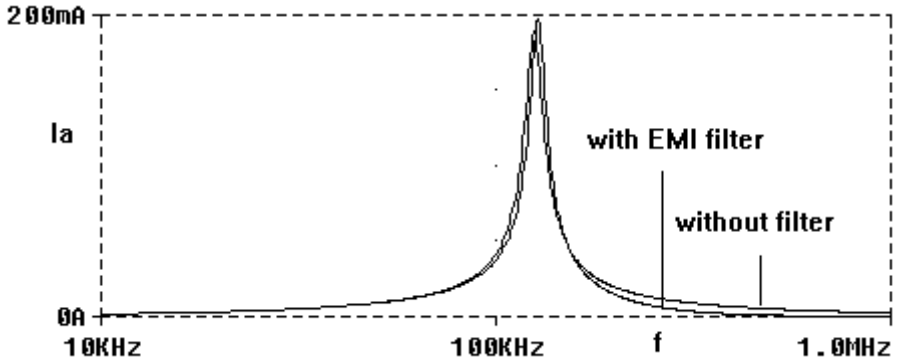



To illustrate the effect of the designed filter for the higher harmonics, an interesting part of the simulated spectrum of antenna current for AC excitation is displayed below.




Another advantage of the proposed filter is, that the resonance frequency of the antenna is almost not influenced, however the antenna should tuned including the filter as described in this application note. When using EMI filter, the offset compensation constant should be readjusted (see chapter 9.2.4).

Moreover, there are no additional resonance frequencies generated by the filter (Butterworth approach).




There are other filtering solutions possible too. In case of higher order passive filters, care should be taken of the losses in the filter elements at resonance frequency.

Active filters need power op-amps (at least for the last stage) to produce the antenna current instead of the HTRC110 and have to be very linear too, otherwise the amplifier generates higher harmonics itself (harmonc distortion).

***Hints for selecting appropriate filter components***

For best filter performance narrow tolerated filter components should be used. Elements with tolerances of 10% for $L_F$ and 5% for $C_F$ are available. Since the filter does not form a resonance circuit, the maximal voltages across the elements do not exceed the input voltage (Note: at antenna elements the voltage exceeds the input voltage by the factor Q). Moreover, the maximal nominal current of $L_F$ must stand the driver current. There are small SMD inductors available, which meet the requirements. Depending on the desired temperature range, the temperature coefficients of the elements should be as low as possible. For capacitors, components having 200ppm/K are available (e.g. Polypropylen or MKP capacitors).

### 6.3.3 Influence of cable resonances on antenna characteristic

This chapter only covers the influence of cable resonances on antenna characteristic. Other aspects like RF radiation and cable losses are out of the scope of this chapter.

Simplified, a cable can be seen as a resonance circuit consisting of distributed capacitance and inductance. For systems where the length of cable $l_c$ is much shorter than the wave lenght of the signal (here: $l_c$ << 1300m), the distributed elements can be replaced by concentrated elements. Hence, the resonance frequency $f_c$ of the cable can be approximated by the following equation:

$$f_C = \frac{1}{2 \cdot \pi \cdot l_C \cdot \sqrt{C' \cdot L'}}$$

As longer the cable as lower its resonance frequency. Thus, when using long cables from driver to antenna, the cable resonance frequency has to be concidered.

If the cable resonance frequency is near the antenna resonance frequency, the antenna will be strongly detuned by the cable. In this case, the antenna current and system performance decrease.

The cable may also increase the magnitude of higher harmonics in antenna current. This is caused by resonance effects at higher harmonics of the 125kHz carrier signal (375kHz, 625kHz...). As cable and antenna are not decoupled, the resulting resonance frequencies are not easy to calculate. The best way is to measure the current of the higher harmonics in the antenna including the entire antenna cable.

***Example:***

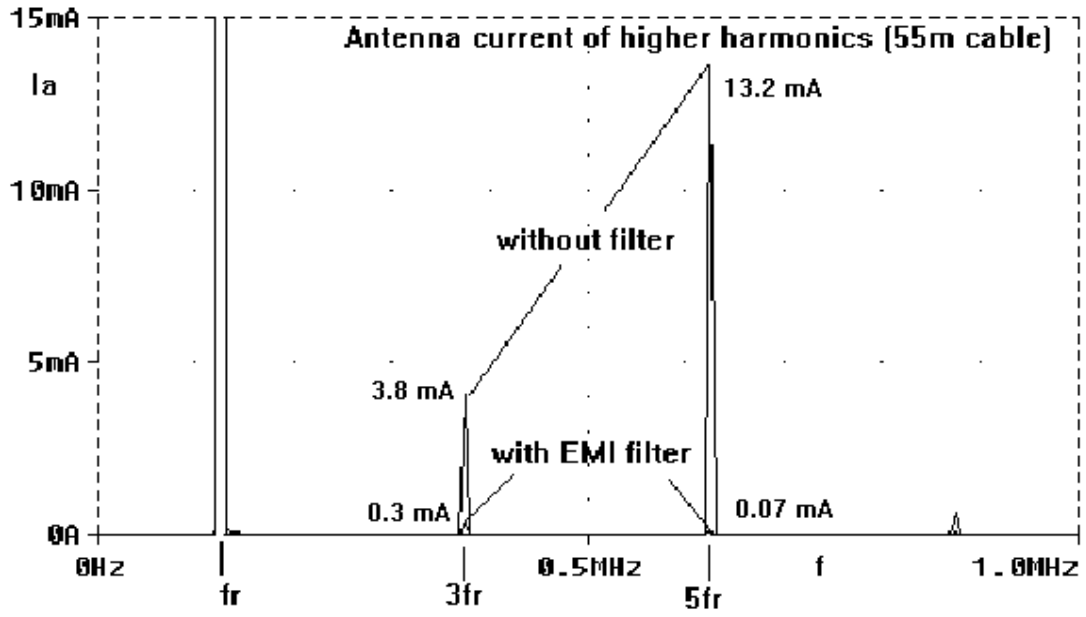
For a 125kHz system the distance between driver and antenna is $l_c$ = 55m. The cable has the parameters:

C´ = 100pF/m and L´ = 0.6µH/m.

The calculated resonance frequency of cable is therefore: $f_c$ = 374kHz. This value is close to the third harmonic of the 125kHz signal. But the resulting resonance frequency of antenna and cable is near to 625kHz, which is another higher harmonic.

This can cause EMR (electromagnetic radiation) problems. In a simulation, it can be shown, that the current at this frequency is about 10 times higher than in a system with a very short cable.

Therefore, using an EMI filter can also be very helpful in systems with long cables. The design of such filters is described in detail in chapter 6.3.2. The filter is placed between cable and antenna. For the given example, the damping characteristic of this EMI filter for the third and fifth harmonic is shown below.




In practice, the loss of longer cables must be taken into account too.

## 7. Antenna tuning

For determining the antenna capacitance and inductance as well as for the exact antenna tuning during the system design phase and the related measurements, it is important to tune the antenna to the system frequency of 125 kHz. There are two ways for tuning, that complement each other. During the system development phase, using a capacitor bank or tuneable capacitors like described in 13.1 facilitates the antenna tuning.

### 7.1 Tuning with a network analyzer

The antenna including all frequency determining components is disconnected at TX1, TX2 and RX. The TX1 and TX2 antenna terminals are connected to a network analyzer measuring the resonance frequency. By changing $L_a$ and/or $C_a$, the antenna can be tuned. The result should be checked as described in the following section.

## 7.2 In-system tuning

When the antenna is exactly tuned, the antenna drivers switch exactly at the time, when the antenna tap point sine wave has its maxima and minima. When monitoring the tap point voltage on a scope, the switching of the drivers is visible in form of small steps in the sine wave. If these steps are exactly in the maxima and minima, the system is exactly tuned. Otherwise, tuning can be done by changing $L_a$ and/or $C_a$ until the steps are adjusted to the extrema of the sine wave.

When exactly tuned, the antenna current has its maximum amplitude. Therefore, the DC system supply current consumption is at its maximum when exactly tuned. Exactly measuring the DC-supply current (with strong integration) is therefore also a method for finding the exact tuned state.

# 8. Antenna Diagnosis

## 8.1 Antenna fail detection

In some applications detection of antenna short or antenna rupture is required. The HTRC110 employs a special detection unit for these states. It is based on measuring the maximum negative voltage difference between RX and QGND.

All considerations base on the standard antenna configuration according to Fig.7. The following tap point voltages result from different antenna problems:

- antenna connections shorted to each other: $U_{tap} = \pm 2.5$ V
- antenna or antenna-connection broken: $U_{tap} = U_{QGND} \pm 2.5$ V
- tap point antenna connection shorted to VSS or +24 V: $U_{tap} \geq 0$ V

The lowest possible tap point voltage of -2.5 V results from the above.

The voltage at RX relative to QGND (~2 V) is:

$$U_{RX} - U_{QGND} = (U_{tap} - U_{QGND}) \cdot \frac{R_{demin}}{R_v + R_{demin}}$$

Assuming a minimum $R_v$ = 160 kΩ, $U_{QGND}$ = 2V, $R_{demin}$ = 33 kΩ and the most negative possible error case voltage $U_{tap}$ = -2.5V, the most negative, possible $U_{RX}$ relative to QGND therefore is:

$$U_{RXmin_{err}} - U_{QGND} = (-2,5V - 2V) \cdot \frac{R_{demin}}{160k\Omega + R_{demin}}$$

$$= -0,77V$$

In normal operation, with properly connected antenna, amplitudes of 40V up to 140 V exist at the antenna tap point in respect to VSS. This voltage is divided by $R_v$ and the internal $R_{demin}$ resistor connected to QGND (~2V). With $R_v$ optimized according to the above section the amplitude at RX is <8V with tuned antenna. When the antenna is mistuned, the amplitude at RX will be smaller, e.g. by a factor of two or three.

Assuming a maximum tap voltage amplitude of 80V that is diminished to 20V by strong mistuning. $R_{demin}$ = 17 kΩ is inserted to come out with the minimum voltage. The resulting minimum negative $\hat{U}_{RX}$ relative to QGND therefore is:

$$U_{RXmin_{norm}} - U_{QGND} = (-20V - 2V) \cdot \frac{R_{demin}}{160k\Omega + R_{demin}}$$

$$= -2,1V$$

which is sufficiently below the resulting most negative voltage in error case.

The HTRC110 tests in every carrier cycle, whether $U_{RX}$ becomes more negative, than the diagnosis level of normally DLEV = -1.15V relative to QGND. By this, antenna problems are monitored instantly.

If the diagnosis level is not crossed by $U_{RX}$ for at least one period, the ANTFAIL-bit will be set. It is automatically reset at the next crossing of the diagnosis level, e.g. when the error condition disappeared. It can be read by issuing the command GET_CONFIG_PAGE 2 or GET_CONFIG_PAGE 3. The HTRC110 does not automatically switch off the antenna drivers or invoke a power down mode when an antenna fail condition is detected (this function would strongly complicate the system development phase). Therefore, if switching off the antenna drivers at an error condition is intended, the µC can monitor the ANTFAIL-bit and switch the drivers off, if the bit is set.

If the field is not constant, e.g. in power-down modes, WRITE pulses and in settling phases, the ANTFAIL-bit is also set or is undefined. Therefore testing this bit should be done during the field is at its normal constant level.

A special case is a short connection of the $R_a$ antenna connection to VSS or +24 V. In this case, the antenna is driven in single ended mode by the driver TX2. Only half of the normal antenna current is flowing. Depending on the system safety margin, it may still work correctly. The tap point voltage strongly depends on the kind of short circuit, the antenna quality factor and other system parameters. Therefore, the output of the diagnosis circuitry is system dependent for that special case.

## 8.2 Antenna detuning detection

When the antenna resonant circuitry is properly working (not open or shorted) the ANTFAIL-bit is 0. There may be applications, where it is intended to detect, whether the antenna resonance frequency stays in between special maximum tolerance limitations. This can be done without any additional hardware by the HTRC110 phase measurement unit described in section 9.2.1 because the antenna tap point voltage phase shift is related to the antenna tuning. Checking for appropriate limits of the measured phase can be used to detect antennas not fulfilling the specified tolerance range.

# 9. Reading data from the transponder

## 9.1 Theoretical background

The data transmission from the transponder to the basestation is performed by a load modulation of the magnetic field by the transponder. The fundamental principle of this load modulation is depicted in Fig.10. Switching between the two so called clipping levels (e.g. 3V and 9V) changes the current in the transponder antenna. By this, also the current in the basestation antenna is modulated due to the inductive coupling of the two coils.This current change results in a voltage change at the antenna tap point.

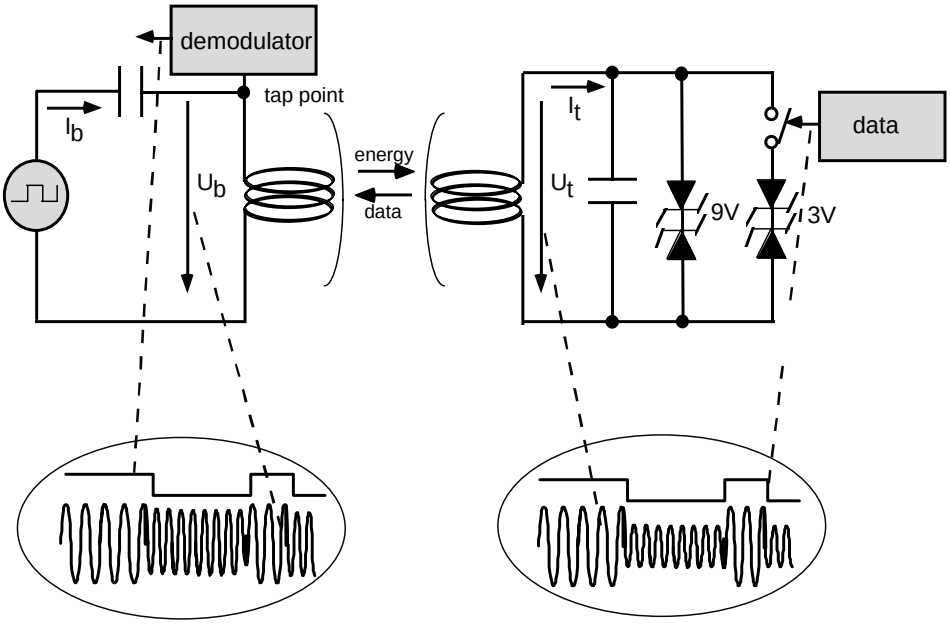



Fig.10 Data transfer from transponder to basestation

From Fig.10, on the first look, one would expect a (pure) amplitude modulation of the basestation antenna current as shown in Fig.11.

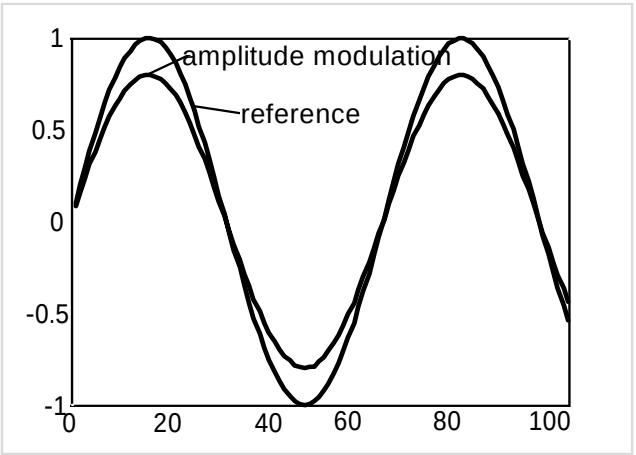



Fig.11 Pure amplitude modulation

This amplitude modulation can be detected by a very basic and simple kind of demodulator, the so called envelope demodulator:

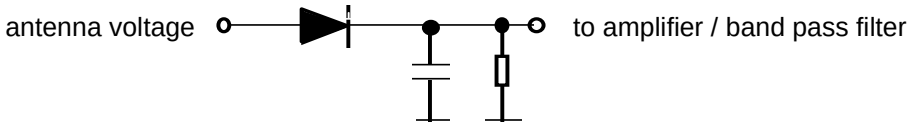



Fig.12 Envelope demodulator principle

This amplitude demodulator principle has been applied in many of the first generation immobilizer and identification systems.

Unfortunately only at optimum tuning of both, basestation and transponder antennas, relative to the oscillator frequency (125 kHz), a pure amplitude modulation of the basestation antenna current occurs. When mistuning one or both resonance circuitries, the modulation changes into a mixture of amplitude and phase modulation. At special combinations of the three frequencies, a pure phase modulation occurs.

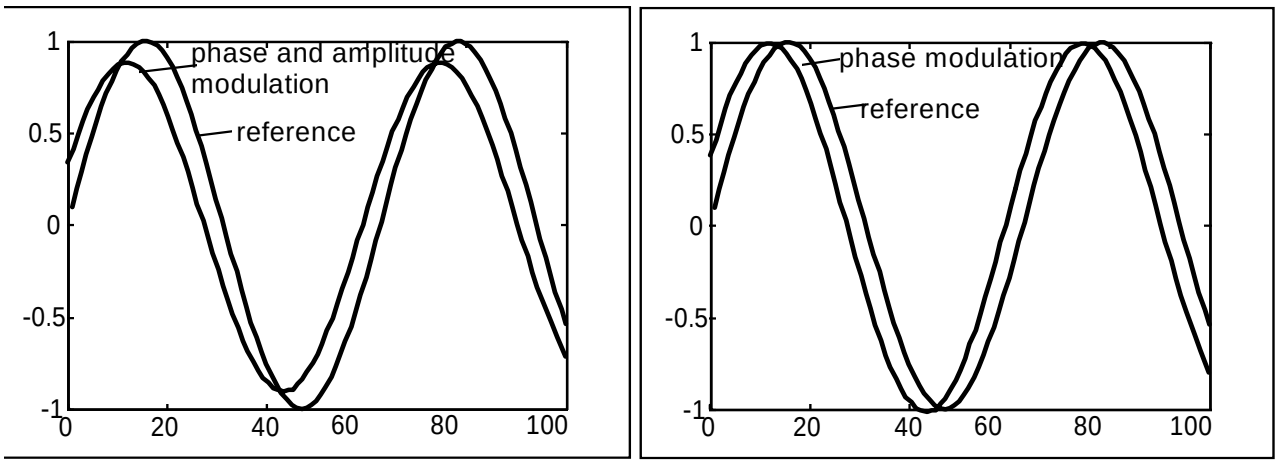



Fig.13 Mixture of amplitude and phase modulation / pure phase modulation

It can be easily seen, that at pure phase modulation, no output will be achieved with the envelope demodulator. That means absolute system failure in this case. Occurrence of pure phase modulation depends on several parameters as e.g. tuning and quality factor of both the basestation and the transponder antenna and also the coupling factor of the coils to each other. These parameters underlie fluctuations with temperature and production tolerance. The position of the pure phase modulation inside the tolerance field can be calculated and depicted in so called tolerance field diagrams. An example is shown in Fig.14. The contour lines show the demodulator output signal strength.

As expected, it is strongest in the center of the tolerance field at zero tolerance. Moving along the transponder tolerance lines, crossing of the zero lines at around 6% basestation tolerance can be seen. As the demodulator output voltage becomes small and disturbed close to zero lines, the safe operating area of this example system is limited to about 5-6% basestation antenna tolerance. This tight antenna tolerance is not easy to achieve in production. Using low tolerance NP0 capacitors and low tolerance antenna coils increases the basestation system costs.

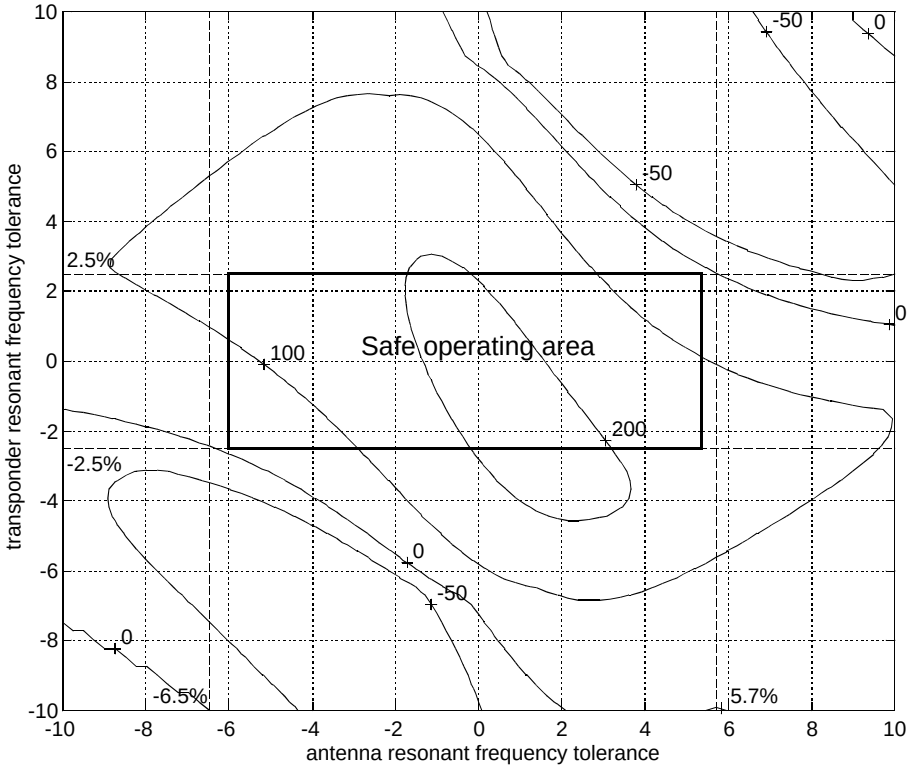



Fig.14 Example tolerance field of envelope demodulator

### 9.1.1 Sampling demodulator principle

The zero line problem can not be avoided or worked around employing amplitude demodulators. Therefore in the HTRC110 the sampling respectively synchronous demodulator principle is realized. The fundamental principle is shown in Fig.15.

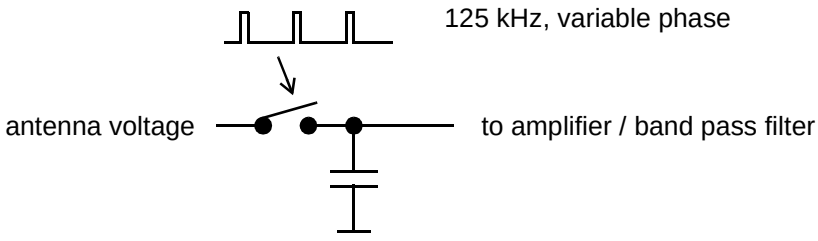



Fig.15 Sampling demodulator

The voltage at the antenna tap point (sine wave with 125 kHz) is sampled at a specific phase relative to the antenna driver signal. In the following, the sampling phase is always considered relative to the falling edge of the antenna driver signal at TX1. Fig.16 shows the dependencies between driver voltage and antenna tap point voltage if the antenna is exactly tuned. In this example, the sampling phase has been chosen to 180 deg. The sampled voltage is held in the capacitor while the switch is open. Mathematically, this sampling of the carrier is a multiplication with an equal frequency signal. By this, the carrier is removed leaving the base band as remaining signal.

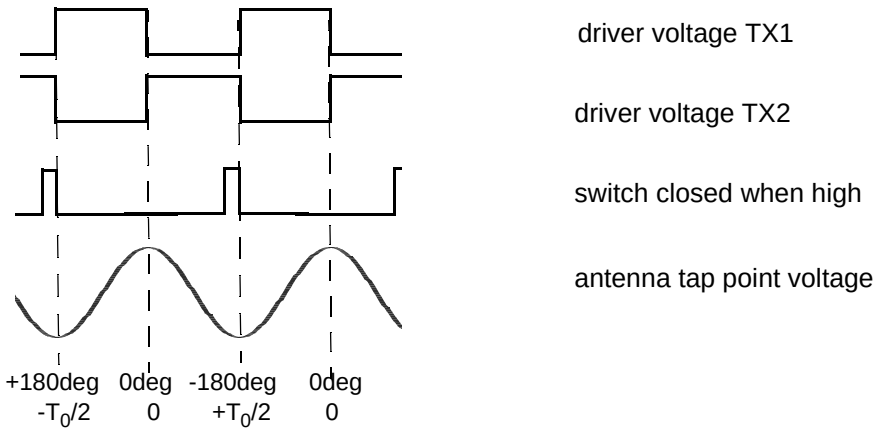



Fig.16 Phase dependencies in optimum tuned case

$T_0$ is the time of one carrier period (1/125 kHz).

Employing a synchronous demodulator, the position of the zero lines in the tolerance field additionally depends on the sampling phase. Fig.17 and Fig.18 show the zero lines with two different sampling phases at 0 deg or ±180 deg and ±90 deg.

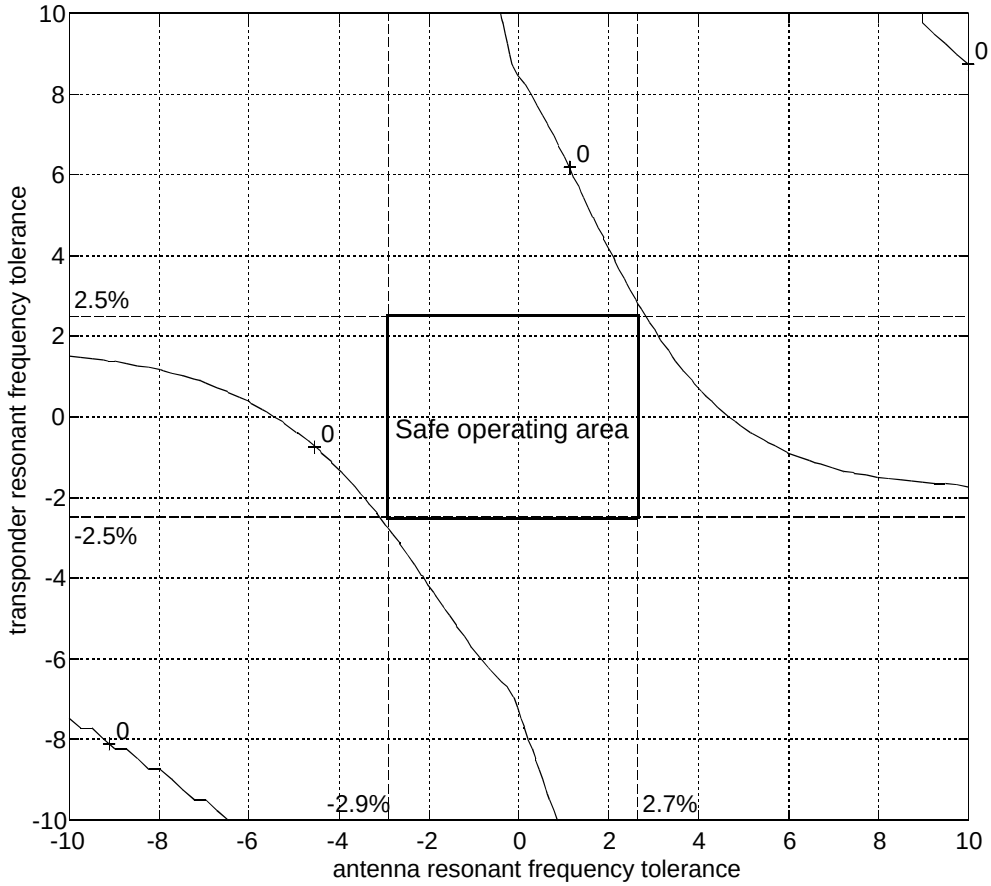



Fig.17 Example tolerance field with sampling demodulator at sample phase of 0 deg or ±180 deg.

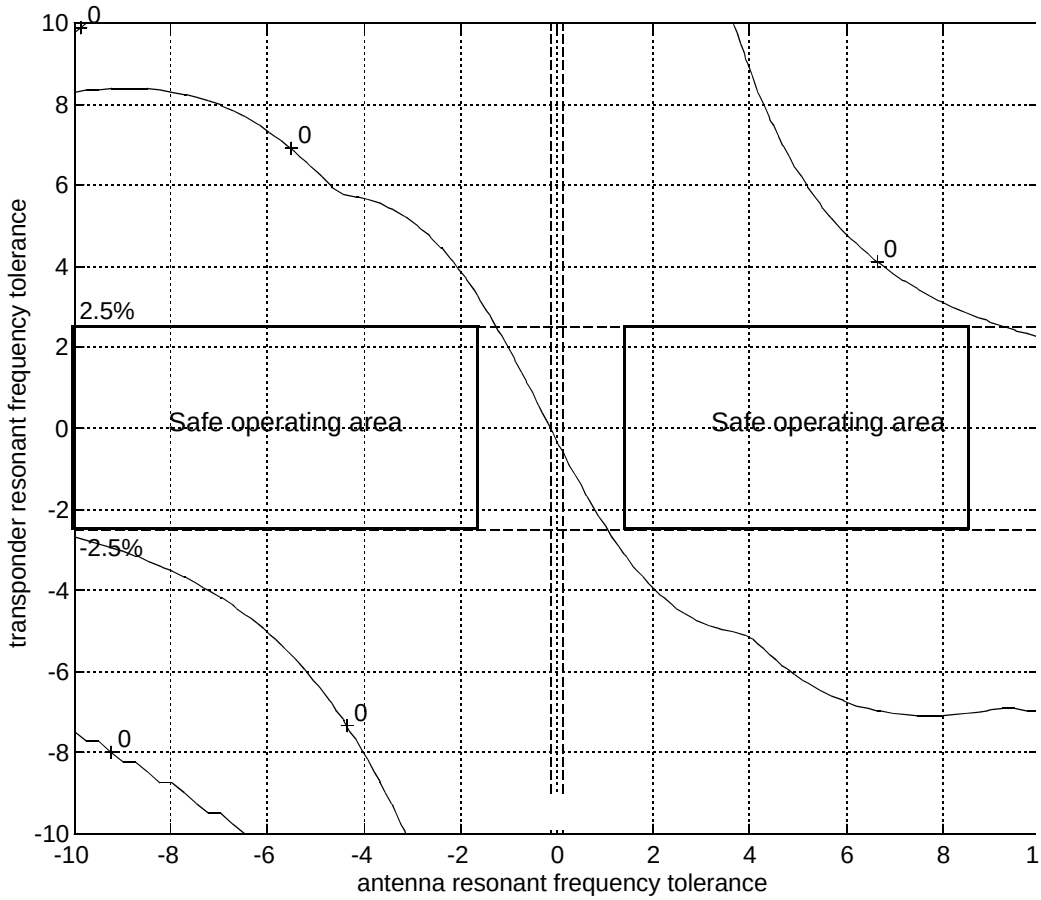



Fig.18 Example tolerance field with sampling demodulator at sample phase of ±90 deg

Due to the different zero line positions, demodulation will always be possible either with the first or second sampling phase. If a system can utilize two sampling phases (parallel or one after the other), due to the overlap of the two safe operating areas with the 90 deg. different sampling phases, the resulting safe operating area covers the full range. This holds not only for 0 deg. and 90 deg. but also for arbitrary pairs of sampling phases, that have 90 deg. difference.

In general, it can be shown mathematically, that the following is true for all pairs of sampling phases, that are 90 deg. different for arbitrary mistunings of the two resonance circuitries:

- If one of the two sampling phases results in zero demodulator output, the other sampling phase always results in a maximum demodulator output and vice versa.
- If a sampling phase results in a maximum demodulator output, a sampling phase being ±180 deg. different results also in a maximum but inverted demodulator output.

A consequence of this fact is, that for all possible mistunings of the transponder and basestation, a sampling phase can be found, that results in a maximum positive demodulator output. There always exists a second phase, that results in a maximum but inverted output. In the complete sampling phase range of 360 deg. exist two phases with maximum output and two phases with zero output. Zeros and maxima are 90 deg. apart from each other.

### 9.1.2 Adaptive-Sampling-Time (AST) principle

The idea behind the AST-method is optimizing the sampling phase based on the knowledge of the current tuning of the RWD. By this, implementing two demodulator channels can be avoided (lower costs). Another big advantage is avoiding to decode two channels simultaneously (powerful processor needed) or to switch the sampling phase after an unsuccessful data transfer attempt (needing double authentication time in worst case).

For calculating the optimum sampling phase resulting in a maximum demodulator output, it would be optimal to know the resonance frequencies of the transponder and the basestation. The current transponder resonance frequency is not available for the basestation, because there is no practically implementable measurement method for this parameter. But it is possible, to calculate an optimized sampling phase only based on the knowledge of the current basestation antenna tuning. This is sufficient for nearly all applications. The basestation antenna mistuning can be taken into account by measuring the phase shift of the antenna voltage relative to the driver signal. From this information, the sampling phase can be optimized. By this, the influence of a basestation antenna mistuning is fully compensated.

It can be shown by mathematical considerations, that the optimum sampling phases based on the phase shift measurement are:

$$\phi_s = 2\phi_{ant} \pm n \cdot 360 \text{ deg.}, \quad n = 0,1,2,..$$

$\phi_s$ = sampling phase, $\phi_{ant}$ = phase of antenna tap point voltage

Adding or subtracting 180 deg. results in a second optimum but with inverted signal polarity.

If phases are represented in form of time intervals as done in the HTRC110 phase measurement system, the formula is transposed into the following form:

$$t_s = 2t_{ant} \pm n \cdot T_0 \qquad n = 0,1,2, ...$$

$t_s$ = sampling time, $t_{ant}$ = time delay of antenna zero crossing, $T_0$ = 1/125 kHz

Adding or subtracting $T_0/2$ results in a second optimum but with inverted signal polarity.

The following picture shows the effect of the AST-principle on the zero-lines. They are typically moved outside the maximum transponder tolerances, if the coupling factor and field strength are high enough. The exact zero line position depends on several parameters, e.g. coupling factor, field strength, transponder type etc. Therefore exact measurements (see section 13.) and/or system simulations should be done during the system design phase.

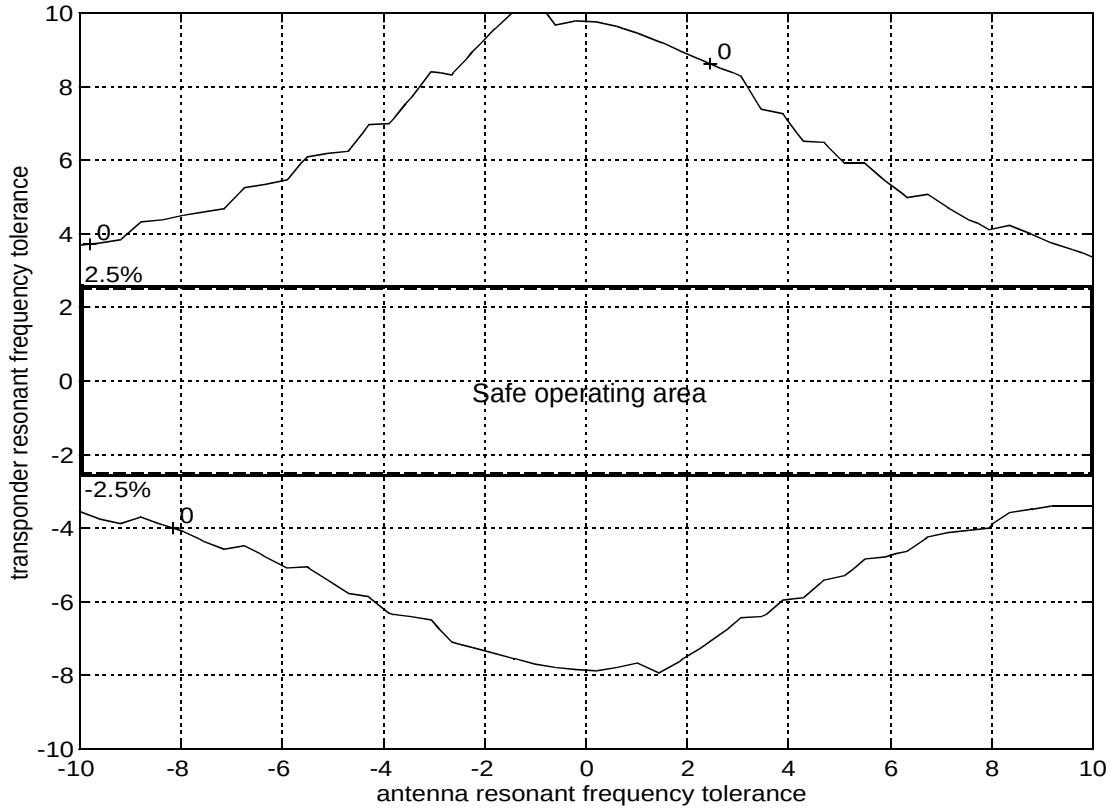



Fig.19 Example tolerance field with adapted sampling time

## 9.2 Implementation of the AST-method employing the HTRC110

The AST method is implemented employing the HTRC110 as follows:

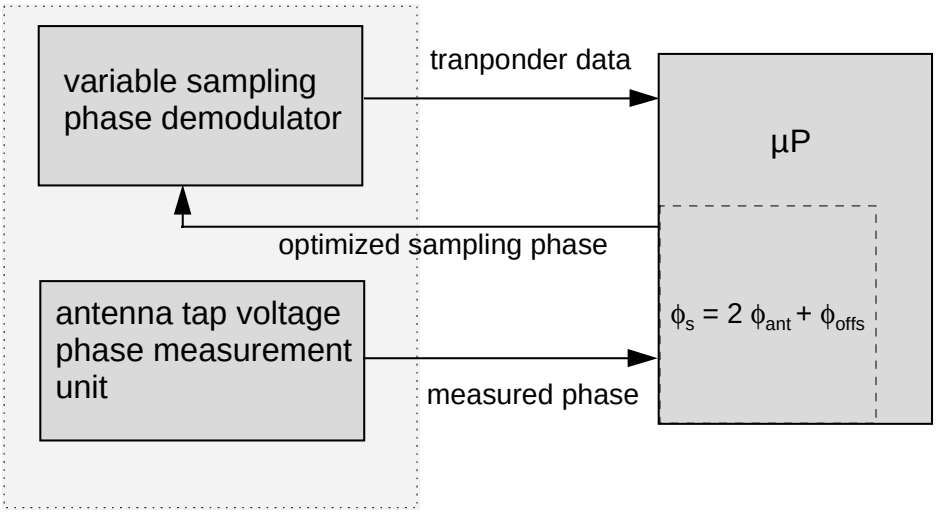



Fig.20 AST implementation

The phase respective time measurement is done by a special circuitry in the HTRC110. This measurement unit is always active. Its output is always valid if the clock oscillator (internal or external) and the antenna field are in complete settled state (see also section 11.1 and 11.2). The most recent measurement result can be read out by the µC issuing the command READ_PHASE. After calculating the optimized sampling time, the µC writes this time into a second register in the HTRC110.

### 9.2.1 Phase shift measurement system

The phase measurement system of the HTRC110 measures the time between the falling edge of the antenna driver signal at TX1 and the falling edge of a zero crossing detector connected to the antenna tap point. Therefore the phases are expressed in form of positive time intervals. A whole signal period of 360 deg. is represented as the time of one period, that is $T_0$=1/125 kHz = 8 µs. The HTRC110 phase measurement circuitry divides this period into 64 steps with a step width of 125 ns = 5.625 deg. By this, the phase respectively time is represented in a 6 bit register value. From the strictly mathematical point of view, negative phases correlate to positive time intervals. Therefore e.g. -90 deg. is represented as 2 µs = 16 * 125 ns = 10h * 125 ns.

In general the phase to measured time relation is:

$$t_{ant} = 8\mu s \ \frac{-\phi_{ant}}{360deg}$$

The register value is:

$$t_{register} = \left(40h \ \frac{-\phi_{ant}}{360deg}\right) \ mod \ \ 40h$$

Decimals are truncated.

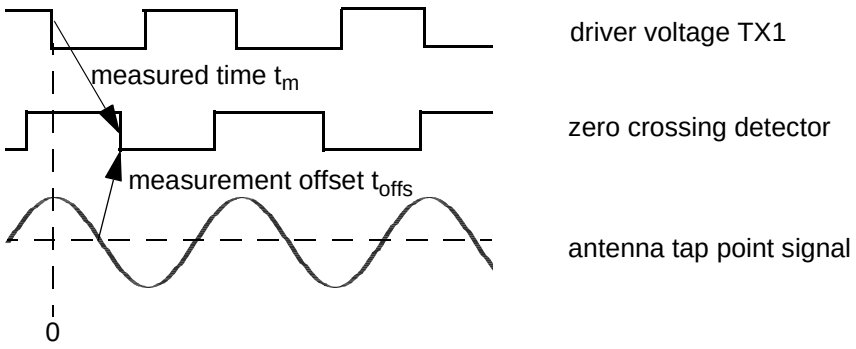



Fig.21 Phase measurement

Under optimum tuned condition, the phase between TX1 and the zero crossing detector is -90 deg. This phase is represented as 2 µs time interval which is 16 * 125 ns = 10h * 125 ns.

If the antenna is mistuned the measured phase is determined by the following formula:

$$\phi_{ant} = -90deg - \arctan(2Q\delta)$$

$$\delta = \frac{f - f_0}{f_0}$$

where Q is the antenna quality factor and $\delta$ represents the relative antenna mistuning.

In practice, the time delays in the IC-internal input filter of the RX-signal and the zero crossing detector result in an measurement offset added on this time. Also signal delays from the antenna tap point to the RX-input caused by parasitic capacitors on the PCB can cause small measurement offsets. From this results for the measured time:

$$t_m = t_{ant} + t_{offs}$$

$t_m$ = measured time; $t_{ant}$ = time between negative transition of TX1 and negative zero transition of the antenna tap point signal, $t_{offs}$ = measurement offset

In the exactly tuned state, the measured time is e.g. 10h + $3h_{offset}$ = 13h.

If the phase measurement unit is used for advanced antenna diagnosis as described in section 8.2, the measurement offset has to be taken into consideration.

### 9.2.2 Calculating and setting the sampling time

The optimum sampling time according to the AST-method can be calculated as follows:

$$t_s = (2t_m + t_{oc})$$
$$= (2t_{ant} + 2t_{offs} + t_{oc})$$

$t_{oc}$ = offset compensation constant (due to internal compensation methods not equal to $-2t_{offs}$);

By this method, the system is adjusted for offset compensation. Determining the offset compensation constant is described in section 9.2.4.

### 9.2.3 Software Implementation

The software implementation of the AST method in a microcontroller is quite easy and can be achieved in a few commands, e.g.:

| | |
|---|---|
| t_ant = READ_PHASE(); | read measured phase/time interval in 8-bit register variable |
| t_ant = t_ant << 1; | shift one bit left = multiply by 2 |
| t_ant = t_ant + t_oc; | add offset compensation constant |
| t_ant = t_ant & 0x3F; | mask bit 6 and 7 = modulo 64 = modulo $T_0$ |
| SET_SAMPLING_TIME(t_ant); | set the sampling time |

The imaginary routines READ_PHASE() and SET_SAMPLING_TIME(t_ant) implement reading respectively writing the 6-bit values.

Running this algorithm should be done after power on and settling of the quartz oscillator and the antenna field, but before the transponder has started to send data (see also section 11.). This allows to even demodulate the first data bits from the transponder correctly (see also section 12.).

After changing the sampling phase, the demodulator has to settle, which should be accelerated by a special settling procedure described in section 11.4.

In immobilizer applications, it is normally sufficient to run the AST-procedure once after power-up.

However, the AST-optimization can be repeated at any time, even if the transponder sends data. If the AST-procedure is executed during time intervals when the transponder doesn't send data, data losses can be avoided.

### 9.2.4 Determining the offset compensation constant for a specific system

The phase measurement offset mainly depends on internal filter delays. This offset component and also its temperature dependence is internally compensated. A slight influence also comes from parasitic capacitances of the antenna tap point signal on the PCB. Therefore the phase measurement offset may also depend on system related conditions. For this reason, this constant should be measured at the end of the system design phase to check whether it differs from the typical value (3Fh). If yes, the measured offset constant should be implemented. Offset constants outside 3Eh and 0h are untypical and should be carefully checked for measurement errors.

If a small capacitor is placed from RX to QGND or VSS as described in section 6.2.4, the offset compensation constant will differ more from the typical value what is normal in this case. Therefore the exact determination of the offset compensation constant is very important in this case.

If the system PCB and the basestation antenna including its connection cable is left unchanged, the measured value is valid for all reproductions of this system. By this, the offset compensation constant can be implemented as fixed constant value in the system software.

***Typical values***

Normally, the typical offset compensation constant:

$t_{oc}$ = 3Fh can be used (if no additional capacitor is connected to RX).

This results in:

$t_s = (2 * t_m + t_{oc}) \bmod T_0 = (2 * t_m + 3Fh)$ & 3Fh

In exact tuned case, $t_m$ is typically close to 13h. For this example the algorithm would calculate:

$t_s = (2 * t_m + t_{oc}) \bmod T_0 = (2 * 13h + 3Fh)$ & 3Fh = 25h.

***Exact determination of the offset compensation constant***

Measuring the exact offset compensation constant can be important for achieving the maximum possible tolerance field in a system.

As preparation for the measurement, the basestation antenna has to be exactly tuned to the system frequency (125 kHz) like described in section 7.

You also need an exactly tuned transponder. That means, a transponder that represents exactly the median in the production tolerance distribution. Normally this is 125 kHz if the transponders are delivered with a symmetric tolerance distribution having the maximum at the optimum frequency of 125 kHz. It is also possible to use a tuneable transponder. This tuneable transponder is normally build from a so called moulded coil. A moulded coil is a transponder coil in the typical transponder package with external wires connected. This moulded coil is connected in parallel to a tuneable resonance capacitor and a transponder IC in a standard (DIL) package (see also section 13.1).

Further a possibility to estimate the demodulator output signal quality is needed. The easiest way is to switch the HTRC110 into the TEST-mode ANAOUT. By this, the demodulator output can be monitored directly on the scope. With this analog signal, it is easy to find maxima and minima.

If the analog signal is not available, the digital output signal can be monitored instead. It is also possible to look at the result of the transponder reading software. Looking at the digital output or at the software reaction, it is only possible to find minima/zero lines of the demodulator output because in this case the digital output signal is corrupted and the software is not able to decode the transponder data.

Using this set up, the AST-algorithm should be repeated for all 64 possible offset compensation constants step by step. That means the sampling phase is varied across the whole range of 360 deg. Covering this range, two offset compensation constants with minimum demodulator analog output amplitude or totally corrupted digital data will be found. Looking at the analog output, also two maxima should be found. The minima and maxima are

exactly 90 deg. ~ 2 µs ~ 10h apart from each other. In practice, it's easier to exactly determine the minima. The maxima can be calculated by adding 10h to the found minima.

*Here a typical example:*

Minimum analog output amplitude or worst digital signal is detected at $t_{oc}$ ~ 2Eh and 0Eh. Because a maximum is always 90 deg. ~ 10h apart from the minimum, a maximum at 3Eh and 1Eh should be seen.

After this, the offset compensation constant related to one maximum is choosen for implementation in the system software. We recommend choosing the maximum in the interval 30h - 0 - 10h. In the example this is 3Eh.

## 9.3 Sampling time optimization

This chapter proposes a scheme to find the optimal offset compensation constant $\phi_{offs}$ for AST. The algorithm can be fully implemented in software. There is no additional hardware needed, only the built-in comparator of the HTRC110.

### 9.3.1 Principle

The AST-method is used for optimizing the sampling phase, based on the knowledge of the current tuning of the basestation only. The basic equation for AST is:

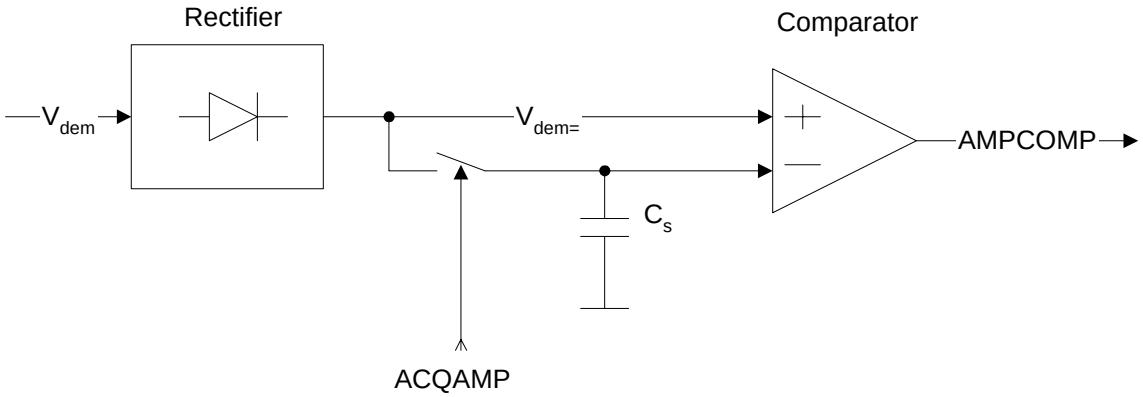
$$\phi_s = 2 \cdot \phi_{ant} + \phi_{offs}$$

The influence of the detuning by the transponder resonance frequency and coupling factor is not taken into account by AST.

However, to achieve maximum demodulator amplitude, the optimum sampling phase must be found. The HTRC110 provides the necessary circuitry.

The idea behind this method is, to vary the sampling phase $\phi_s$ and measure the corresponding amplitudes of the demodulated analog signal. The optimum sampling phase gives the maximum demodulator signal.

In order to find the maximum demodulator signal, the internal comparator of the HTRC110 can be used. The blockdiagram of this unit is shown below:




When the *ACQAMP* control bit is set by a *SET_CONFIG_PAGE* command, the actual demodulator signal amplitude $V_{dem=}$ is stored in the capacitor $C_S$. After resetting the *ACQAMP* bit, the status bit *AMPCOMP* is set, when the actual signal amplitude is larger than the stored reference otherwise it is cleared.

### 9.3.2 Algorithm

The proposed algorithm for sampling time optimization has to be implemented in the controller software for the HTRC110.

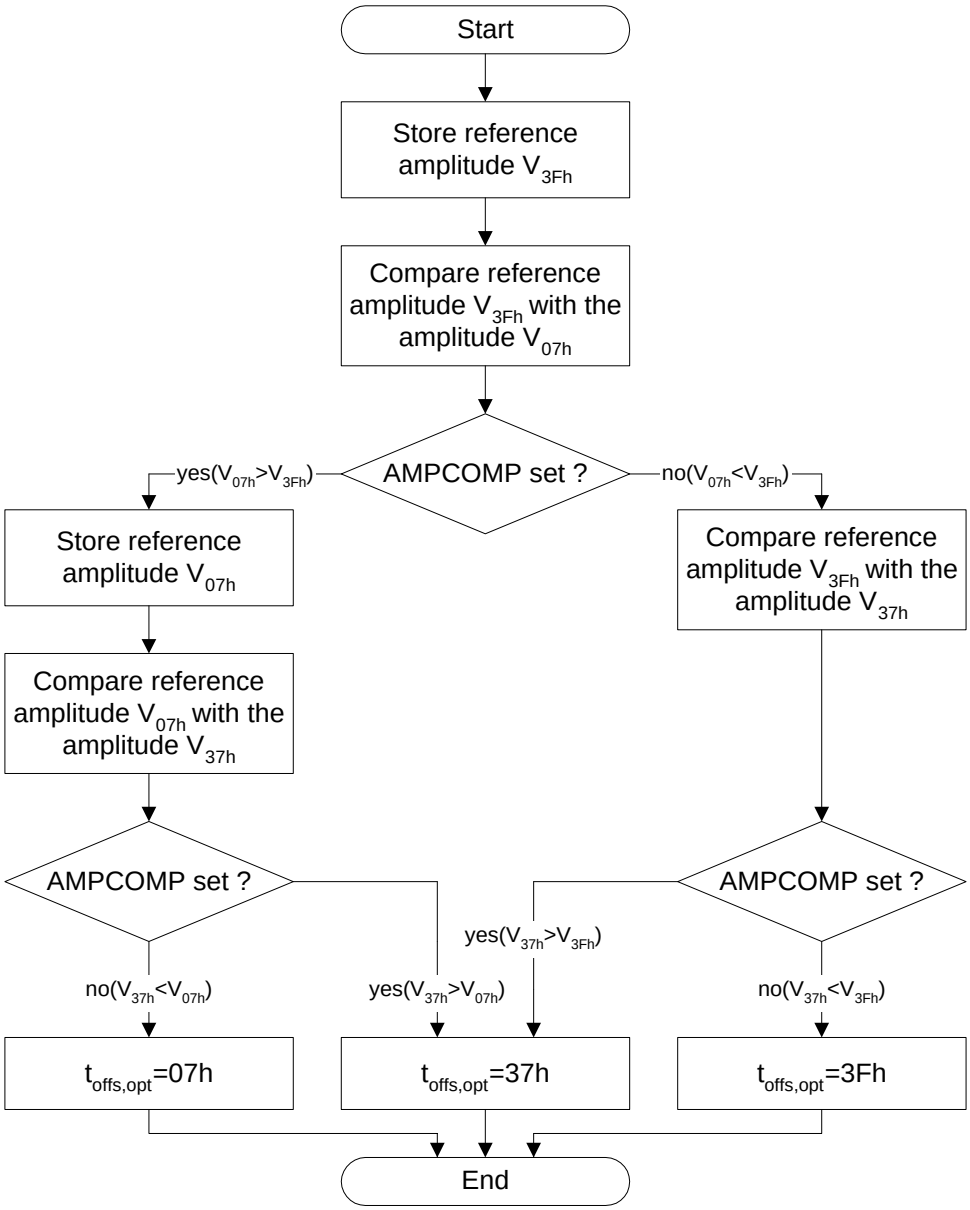
Varying the compensation constant $\phi_{offs}$ for AST has the same effect as varying the sampling phase $\phi_s$. Therefore, this method can be implemented as an extension of the AST-algorithm to find its optimum $\phi_{offs}$.

For practical application, it is important to choose compensation constants, which correspond to the maximum demodulator signal in all possible combinations of transponder and basestation detuning.

According to the theorie, a maximum of the demodulator voltage must be in this range of 90 deg. Therefore, the algorithm changes $\phi_{offs}$ in the range of 37h..07h. The number of compensation constants taken for sampling time optimization has a huge influence on the computation time this algorithm needs.

Taking all 16 compensation constants within the range (step-width of 5.625 deg) would require much time, because many read/compare operations would be necessary.

A much faster approach applies only 37h, 3Fh and 07h as compensation constants. The step-width would be 45 deg in this case. Using the built-in comparator of the HTRC110, the algorithm works as shown below:




The voltage $V_{xyh}$ denotes the measured demodulator voltage using a compensation constant of xyh. At the end of this algorithm, the optimized compensation constant $t_{offs,opt}$ is found. The number of compensation constants should be choosen in order to get a good compromise between computation speed and maximum deviation from the optimum compensation constant (e.g. n = 5,7...).

## 9.4 Additional safety backup for defect transponders or basestation antennas

According to Fig.19, for a proper designed system working with AST, the zero lines are always outside the maximum transponder tolerance range for a wide basestation tolerance range. Therefore the zero lines are never hit, if all components are inside their allowed tolerances.

If a transponder or a basestation antenna has increased tolerances e.g. due to a defect, the zero line may be hit and the system may fail. It would be a good system feature, to be able to handle this situation without a system

failure. From theory as described in section 9.1.1 follows, that if a zero line is hit at a special sampling phase, a maximum shall be at sampling phases 90 deg. apart. Therefore it is possible to implement a special backup subroutine, that does the following:

If two misreadings have been detected, e.g. by protocol violations, this routine is invoked. It sets the sampling time +10h or -10h relative to the current sampling time. After writing this sampling time to the HTRC110 and proceeding the settling sequence, a new read try is made. If the decoding software can handle both non inverted and inverted signal polarity, adding or subtracting 10h (reverse signal polarity) does not make a difference. Otherwise, a polarity dependent distinction needs to be implemented.

## 9.5 Monitoring the analog demodulator output signal

During the system and software development, it is very helpful to monitor the analog demodulator output signal on a scope. For this, the HTRC110 can be switched into a special test mode. The following circuitry should be connected to the HTRC110:

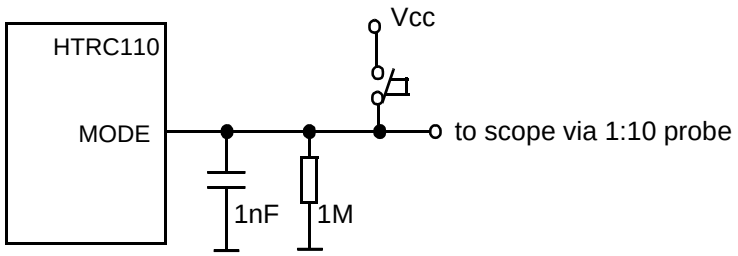



Fig.22 External circuitry for analog signal monitoring and unlocking test-mode prohibition

The HTRC110 MODE-pin is a combined input and output. For using as analog output, it has to be pulled down to VSS as shown in Fig.22

For unlocking the test-mode lock of the HTRC110, a positive pulse shall be applied once at the MODE-pin. This can be achieved by closing the switch for a period of time. After releasing the switch, the test mode can be activated by a special command:

TEST_ANAOUT: 00100001b

This command is send via the serial interface. Before sending it, an interface RESET-condition shall be issued as normal before all commands.

It is possible to switch the analog output off by the command:

TEST_OFF: 00100000b

Switching off the power supply of the HTRC110 also leaves the test mode. To reactivate it after power-up, the positive pulse has to be applied to MODE and the TEST_ANAOUT command shall be sent.

## 9.6 Adapting the demodulator to different transponders and applications by register settings

The HTRC110 demodulator can be adapted to various transponder types and basestation applications by special register settings.

### 9.6.1 Demodulator bandwidth

For achieving a high signal to noise ratio, the demodulator bandwidth should be adapted to the signal bandwidth. Therefore the internal switched capacitor filters can be adapted to different cutoff frequencies. Most transponders use biphase coding (like Manchester or CDP) for data transferred with data bit rates of 2 kbps or 4 kbps. The

power spectrum of biphase coded signals is half circular shaped. The spectral power maximum is located at the data rate. For the HITAG (4 kbps) this maximum is located at 4kHz.The optimum lowpass filter cutoff frequency therefore is 6kHz for the HITAG. The lowpass filter cutoff frequency can be adjusted by the FILTERL-bit in the configuration page 0.

Also the highpass filter cutoff frequency should be adapted to the transponder type. The HITAG does not use low frequency components and also has a factor two higher data rate. Therefore a highpass filter cutoff frequency of 160 Hz should be configured.

The highpass filter cutoff frequency can be adjusted by the FILTERH-bit in the configuration page 0. Both filter settings are configured by the following commands:

for HITAG: Set_CONFIG_PAGE 0, xx11b

For adapting to other transponder types, also the remaining two combinations of filter settings: FILTERH, FILTERL=10b, 01b are allowed. It can also be a help to look at the analog demodulator output signal, when adapting to special transponder types, that are not described here. In general, resulting from signal theory, the demodulator passband spectrum should be adapted as close as possible to the transponder data signal spectrum.

It is also possible to switch off the primary low pass filter completely by setting the DISLP1-bit in the configuration page 3 (SET_CONFIG_PAGE 3, 1xxxb). In this case the bandwidth is limited by a secondary low pass filter with an edge frequency of 15 kHz. Only special applications requiring a very high bandwidth (transponders with specially high data rate) but guaranteeing a high signal amplitude may be improved by switching this filter off. Normally it should be always on. Monitoring the analog demodulator signal is very important during the system development phase when intending to switch off this filter.

### 9.6.2 Demodulator gain

The demodulator gain can be changed by changing the gain factors GAIN0 and GAIN1 in configuration page 0 via the command SET_CONFIG_PAGE 0, $g_1g_0$xxb. The following gains can be set:

$g_1g_0$ = 00b g = 100
$g_1g_0$ = 01b g = 200
$g_1g_0$ = 10b g = 500
$g_1g_0$ = 11b g =1000

The optimum gain setting depends on the modulation amplitude at RX. In general, the gain setting is relatively uncritical because the HTRC110 demodulator is tolerant against signal clipping and in normal configuration, nearly no digitizer hysteresis is existent. During system development we recommend to start with a gain of 500. It may be possible to increase the system tolerance range by increasing or decreasing the gain. This can only be found out by tolerance field measurements (section 13.). Monitoring the analog demodulator output signal together with the digitized data output is very important for successful gain optimization.

The effect of increasing the gain might be strong signal clipping at the point of optimum tuning when the modulation is strongest. The demodulator does not run into problems because of this clipping, but settling times after WRITE-pulses may be increased.

Decreasing the gain may decrease the sensitivity for very weak signals. Therefore weak modulation signal applications need high gains if the tolerance field has to be optimized.

For all standard applications, one of the gain factors 200 or 500 should be chosen by system performance tests.

### 9.6.3 Digitizer hysteresis

The analog demodulator output signal is compared to a threshold (normally the signal mean level) for digitization. Normally, a hysteresis has to be provided to avoid jitter at the threshold crossing. As the HTRC110 employs a

very sophisticated dynamic threshold generation circuitry, this **hysteresis is not needed** in standard applications. Therefore the maximum possible sensitivity is reached.

Only in very special applications where very low frequency signals have to be demodulated, the signal and the dynamic threshold can approach each other in phases where the modulation stays constant for a long time due to the differentiating behaviour of the high pass filter. Here, the digital output may switch because of noise influence. For this case, a threshold can be activated by setting the HYSTERESIS-bit in the configuration page 1. With hysteresis on, the demodulator gain has more influence on the system sensitivity. By this, the dynamic range is strongly decreased. Therefore the influence of hysteresis setting should be tested together with the gain optimization when looking on the analog demodulator output signal together with the digital output. In normal applications with hysteresis off, this procedure is not needed.

In general, it's a better solution to handle output signal switching during long constant signal periods by a proper software implementation. This method is facilitated because the dynamic threshold guarantees, that unintended signal switching will never happen directly after the last transition and also not directly before the next transition after the constant signal period.

### 9.7 Reading out the digital data

The demodulated and digitized data is read out via DOUT. First, an interface reset condition has to be applied as usual before all serial commands [1]. After this, the three-bit command READ_TAG is issued. After sending the last of the three bits (1's), the HTRC110 switches instantly to transparent mode. So, the transponder data is directly presented at DOUT with a delay from RX to DOUT depending on the demodulator filter settings. For optimizing the WRITE-pulse positions (see section 10.2) the delay times of 310 µs for FILTERL=0 and 175 µs for FILTERL=1 shall be considered.

SCLK shall be low during that transparent mode. The transparent READ_TAG mode is terminated by a low to high transition of SCLK.

## 10. Sending data to the transponder

### 10.1 Modulation principle

Data is sent in direction from basestation to transponder by modulating the magnetic field ("On/Off-Keying", 100%-modulation) respectively switching off the field for short periods of time. During that time, the transponder energy and clock supply is provided by the transponder resonant circuitry. The data is coded into the position and/or distance of these field gaps.

A field gap is started by switching off the antenna drivers. After this, the energy stored in the basestation antenna resonant circuitry is cut down by clipping diodes in the HTRC110 driver stages. Therefore the field strength decays rapidly to zero. After switching the drivers on again, the resonance circuitry energy has to be build up again. The time needed for that depends on the quality factor of the antenna.

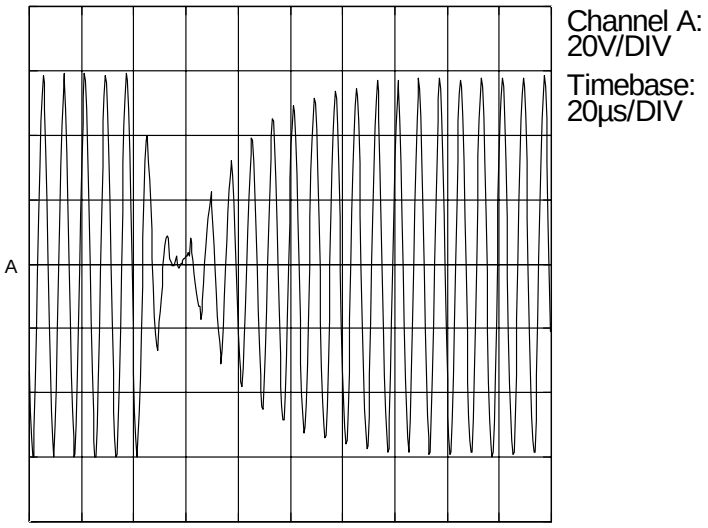



Fig.23 Typical field gap for sending data to the transponder

## 10.2 Driver-off period width and position

With high antenna quality factors, a short driver-off period can be spread to a comparatively long field gap. Therefore the antenna quality factor is limited. The shortest possible field gaps with 100% modulation can be achieved by switching off the drivers for $2t_0$ or $3t_0$, depending on the quality factor. Caused by the pulse spreading, the transponder sees longer pulses. During the system software development, the optimum driver-off period can be determined on two ways:

- If a bond-out transponder (e.g. DIL-packaged) is available, where the demodulator output can be accessed. The pulse length seen by the transponder can be directly measured. By this, the driver-off period can be optimized.
- If the transponder demodulator output is not available, the optimum driver-off period should be determined empirically by varying the driver-off period until failure. This method is sufficient for nearly all applications.

The optimum Write-pulse positions relative to the demodulated data are dependent on the demodulator delay and also on the delay of the basestation and transponder antenna resonant circuitries. One way for software optimization of the pulse position is empirically changing the relative delay in the software and by this finding the limits accepted by the transponder. If the transponder modulator and demodulator outputs are available in a bond-out version, the relative position of the WRITE-pulses in respect to the data sent from the transponder can be measured directly. This relatively complicated method is normally not needed. It may also be a help to directly monitor the field and field modulation close to the transponder. This can be done by winding some turns of thin wire around the transponder and monitoring the induced voltage on the scope together with the digital and analog basestation signals.

## 10.3 Sending data via the digital interface

Sending WRITE-pulses is done via the serial interface by the command WRITE_TAG_N, $N_3N_2N_1N_0$.

If the argument $N_3N_2N_1N_0$ does not equal 0, the command activates a mode, where the WRITE-pulse length is determined by an HTRC110 internal timer. The pulse length is determined by the binary value $N_3N_2N_1N_0$ between 1b and 1111b representing a pulse length of N * $T_0$. By this, a pulse length between 1*8µs and 15*8µs=120µs is available.

Especially if short pulses are sent, using the internal pulse length timer is a big advantage because the µC does not have to provide this high timing precision. In active antenna applications, where the HTRC110 and the µC are placed on separate PCB's connected via a cable, the transmission of short, sharp pulses may be a problem because of bandwidth limitations on the interconnection cable. This problem is also avoided by the internal timer.

After loading this command, an arbitrary number of WRITE-pulses with the fixed length can be sent. The starting position of these pulses is determined by low to high transitions of DIN.

The WRITE_TAG(_N) mode is **immediately terminated** by a low to high transition of SCLK, **even if the write pulse time has not been completed.** Therefore it is important to delay the SCLK transition in respect to the transition on DIN until the time set by the WRITE_TAG_N command is fully completed to avoid interrupting the last WRITE-pulse in a sequence.

The HTRC110 also provides a fully transparent WRITE-pulse timing method. This mode can be initialized by sending a WRITE_TAG_N command with $N_3N_2N_1N_0$ = 0000b. For transparent writing, the pulse position is determined by the low to high transitions at DIN. The pulse length is determined by the high-time of DIN. Also this mode is immediately terminated by a low to high transition of SCLK.

For allowing a very fast switching to WRITE-mode, the three bit command WRITE_TAG is provided which does not require handing over a parameter. It uses the $N_3N_2N_1N_0$ setting, previously transmitted by the last WRITE_TAG_N command. If no WRITE_TAG_N command has been transmitted before after power-up, the initial setting $N_3N_2N_1N_0$ = 0000b is used, invoking the transparent mode. For using non transparent timing with the WRITE_TAG command, at least one WRITE_TAG_N command has to be issued before.

# 11. Settling

## 11.1 Oscillator settling

After switching on the power supply of the HTRC110 or leaving the power-down mode (oscillator off), first the HTRC110 quartz oscillator has to settle. A time interval of 10 ms should be allowed for this settling. Depending on the quartz crystal, this time may be minimized during system optimization. If the HTRC110 is clocked externally e.g. by the µC, the settling time depends on the specification of this external oscillator. If the external oscillator is running during the HTRC110 is in power-down mode, no oscillator settling time is required.

## 11.2 Field settling

After reactivating the antenna field after one of the three power-down modes, a settling time of approximately 150 µs depending on the antenna quality factor should be allowed before reading out a measurement result from the phase measuring circuitry. If before an oscillator settling has taken place, the field settling is included in the oscillator setting time.

## 11.3 Demodulator settling

The demodulator of the HTRC110 contains several analog and switched capacitor filters. For generating the threshold for digitizing the analog demodulator output signal, a sophisticated circuitry has been implemented. All these function blocks need some time for settling after changing operation conditions e.g. power on, reactivating after power down modes, changing the sampling time or sending WRITE-pulses. This settling has to be completely finished before the transponder sends the first relevant data bit. Therefore special circuitries have been

implemented into the HTRC110 to accelerate settling. They are activated by the FREEZE- and the THRESET-bits in the configuration page 2.

**TABLE 1**

| FREEZE 1 | FREEZE 0 | Description |
|---|---|---|
| 0 | 0 | normal operation according to configuration page 0 |
| 0 | 1 | main low pass is frozen and main high pass is initialized to QGND |
| 1 | 0 | main low pass is frozen and the time constant of the main high pass is reduced by a factor of 16 for FILERH = 0 and by a factor of 8 for FILTERH = 1. |
| 1 | 1 | time constant of the main high pass is reduced by a factor of 16 for FILERH = 0 and by a factor of 8 for FILTERH = 1. Second high pass is initialized to QGND |

THRESET=1 switches the threshold generator to a mode, where the threshold immediately follows the demodulator output without delays. This is used to enforce a defined and sensitive start condition for the threshold.

## 11.4 General settling sequence

The following sequence should be issued by the µC when the clock is stable after power-on or leaving a power-down mode.

| | |
|---|---|
| SET_CONFIG_PAGE 2, 1011b; | THRESET=1, FREEZE1=1, FREEZE0=1 |
| Wait(4 ms); | wait 4 ms for accelerated filter and demodulator settling |
| SET_CONFIG_PAGE 2, 1000b; | THRESET=1, FREEZE1=0. FREEZE0=0 |
| Wait(1 ms); | wait 1 ms during normal filter and demodulator operation |
| SET_CONFIG_PAGE 2, 0000; | THRESET=0, FREEZE1=0 FREEZE0=0) |
| READ_TAG(); | wait for data; threshold, filter and demodulator in normal operation |

The given times are a safe basis for starting the system design. Normally, it should be possible to decrease the times if needed, without running into problems.

## 11.5 Fast settling sequence

Sending one or a series of WRITE-pulses or changing the sampling phase requires also a fast settling procedure. It starts before the first WRITE-pulse of the package or before the phase change and ends after the commands.

| | |
|---|---|
| SET_CONFIG_PAGE 2, 1001b; | THRESET=1, FREEZE1=0, FREEZE0=1 |
| Write_Data(x); / Set_sampling_Phase(x); | procedure that sends the required data to the transponder invoking the WRITE_TAG mode and leaving WRITE_TAG mode after this / setting the sampling phase |
| Wait(200 µs - $t_{transfer}$); | wait 200 µs minus transfer time of next command to HTRC110 |
| SET_CONFIG_PAGE 2, 1011b; | THRESET=1, FREEZE1=1, FREEZE0=1 |

| | |
|---|---|
| Wait(250 µs - $t_{transfer}$); | wait 250 µs minus transfer time of next command to HTRC110 for accelerated filter and demodulator settling |
| SET_CONFIG_PAGE 2, 0000; | THRESET=0, FREEZE1=0 FREEZE0=0) |
| READ_TAG(); | wait for data; threshold, filter and demodulator normal operation |

Other transponder families allow longer settling times. In this case, we recommend to increase the settling time intervals in percentage terms e.g. by a factor two or more.

Optimizing the demodulator settling (if needed in special applications) is facilitated by analyzing the analog demodulator output signal at MODE.

## 12. Power-on sequence

The following diagram shows a typical power-on sequence of an HTRC110 RWD system.

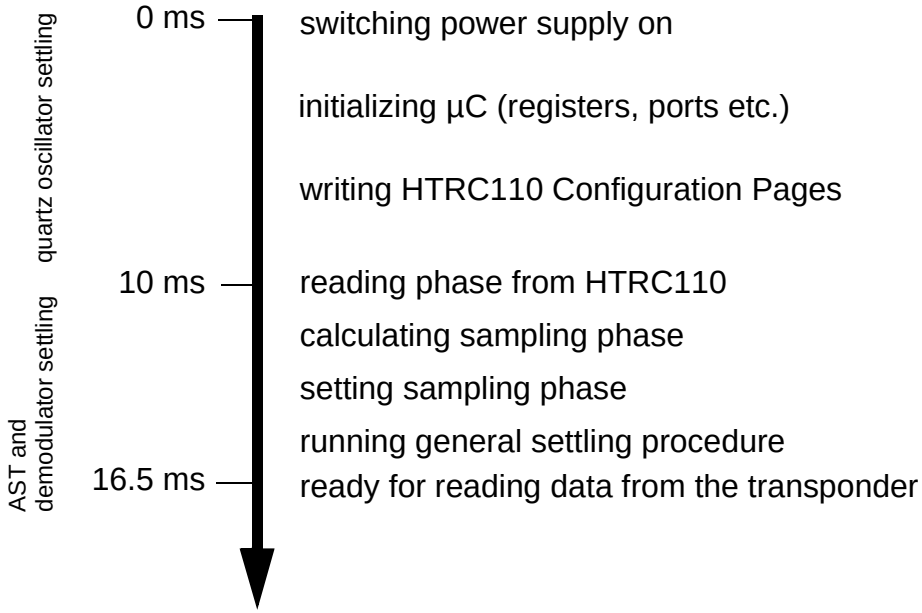



Fig.24 Example power-on sequence

## 13. Tolerance field verification

During and after the system design phase, it is important to check the system's safe operating area in means of transponder and basestation antenna tolerance. In the field, the resonance frequencies change due to production and temperature dependent tolerances. Therefore, inbetween defined limits, nearly all combinations of antenna tolerances can appear because the basestation antenna and transponder temperature can have different values. In climate chamber tests, only frequency tolerance pairs representing nearly equal antenna temperatures can be checked. By measuring or simulating independently frequency variations on basestation and transponder antenna, these operation conditions can be fully verified. Therefore, the tolerance field measurements or simulations are more expressive in this point, compared to climate chamber tests.

With a few external passive components a measurement equipment can be assembled that allows matrix measurements of the whole tolerance field. Especially the borders of the safe operation areas can easily be found.

## 13.1 Tolerance field measurement setup

Fig.25 shows an example arrangement for tolerance field measurements of a transponder - RWD system. It consists of the HTRC110 with a capacitor bank tuneable RWD antenna and a bondout transponder connected to a moulded coil $L_t$ and a tuneable capacitor.

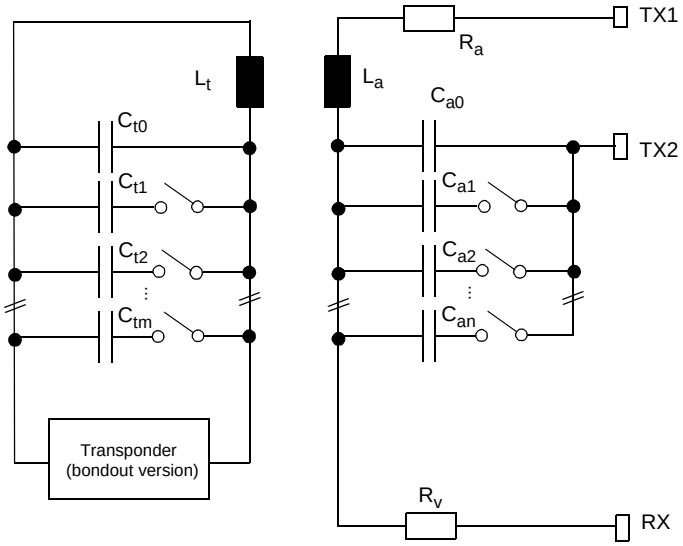



Fig.25 Tolerance field measurement circuit

With this setup, both the transponder and the basestation resonance frequencies can be adjusted. The capacitor banks should be dimensioned in a way, that resonance frequencies in a range of e.g. $f_0 \pm 15\%$ can be achieved.

The capacitor banks can be build up using DIP-switches together with SMD-capacitors. Especially for the transponder tuning capacitor bank, normally small capacitors down to 1 pf to 10 pf are needed. Therefore the stray capacitances should be taken into consideration.

Alternatively variable capacitors (trimmers) can be used to detune the transponder resonance frequency (Fig.26), but with the disadvantage of not having exactly reproducible settings.

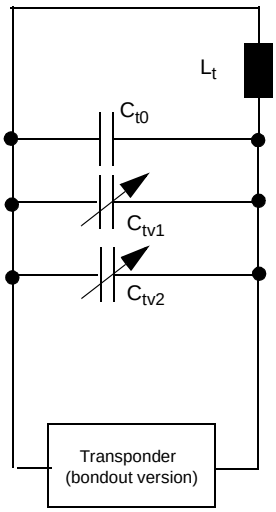



Fig.26 Transponder resonance circuit with variable capacitor

The tuned basestation antenna resonance frequency should be cross checked with a network analyzer.

The transponder resonance frequency can be measured by inductively coupling the moulded coil with a core-less solenoid, connected to a network analyzer. By monitoring the impedance and phase versus frequency, the resonance frequency can be found exactly, looking at the phase measurement negative peak. The windings number of the solenoid coil is uncritical.

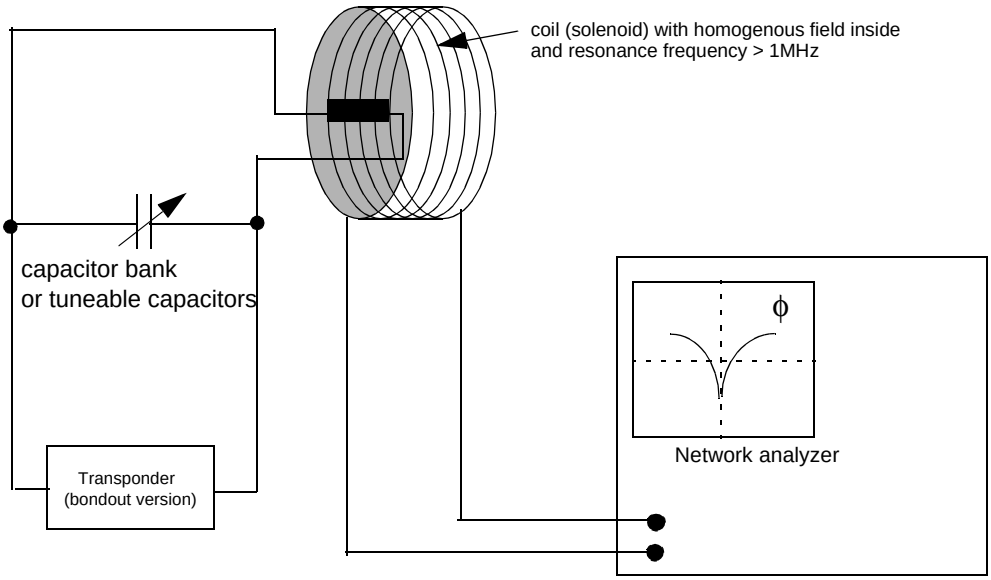



Fig.27 Contactless transponder resonance frequency measuring setup

## 13.2 Tolerance field matrix measurement

With the measurement equipment described above, dedicated points in the tolerance field of transponder and RWD detuning can be tested.

The tolerance field should be covered in form of a matrix. In each matrix point, the immobilizer system should run through its full operation, e.g. challenge/response. By monitoring the “go/nogo-output” of the system, the tolerance field is defined. Plotting the resonance frequency pairs with the appropriate answer into a diagram, depicts the measured tolerance field. If simulation diagrams are available, the calculated and measured diagrams can be overlaid with the READ- or WRITE-simulations or both.

It is important also to simulate or measure under worst case conditions to determine the exact system safety margins like e.g.:

- lowest VDD -> lowest antenna current
- highest temperature -> highest $R_{ant}$ -> lowest antenna current
- worst case transponder (normally only possible in simulation)
- worst case coupling factor

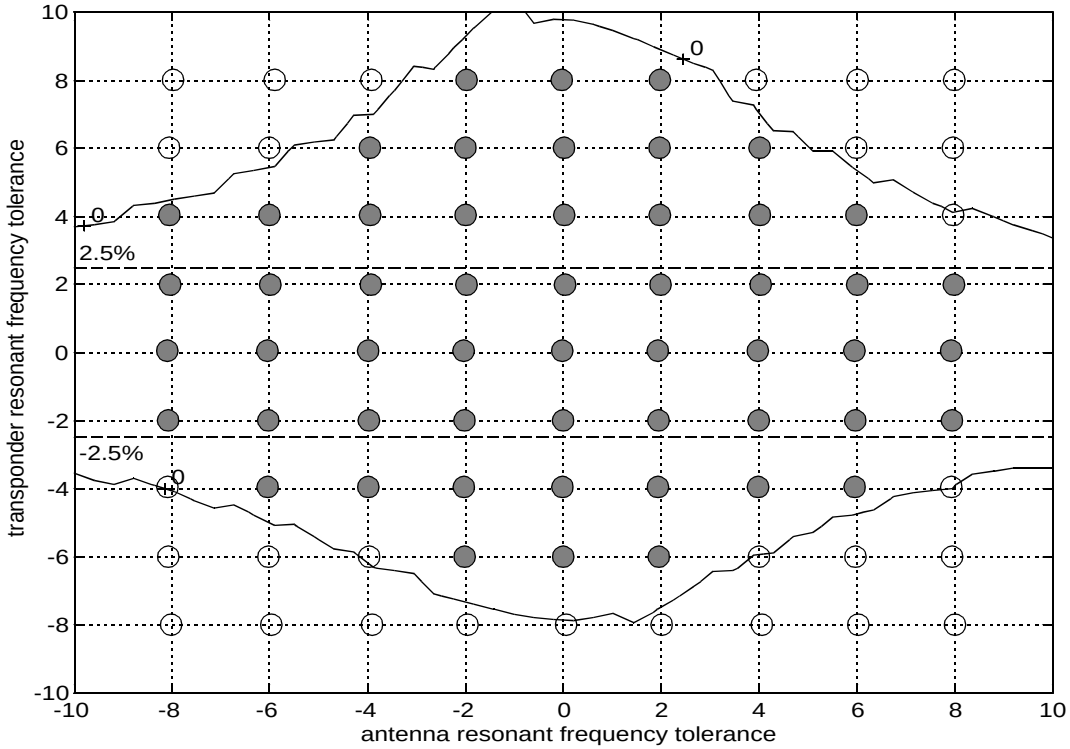



Fig.28 Matrix tolerance field measurement (gray: “go”, transparent: “nogo”)

Even more precision can be gained, if not only the “go/nogo”-information is taken. At each matrix point, the maximum possible key distance from the home position can be measured that does not lead to a system failure. The measured distances can be plotted into a three dimensional graphics for visualization.

## 14. References

[1] HTRC110 data sheet. For the latest version, please contact your local Philips Semiconductors sales office.

[2] ETSI, European Standard: EN 300 330 (Draft).
Electromagnetic compatibility and Radio spectrum Matters (ERM) Short Range Devices (SRD).

[3] USA: code of federal regulations 47: section 15 Radio Frequency Devices.

[4] Japan: Regulation for inductive communication equipment.

[5] Australia: Radiocommunications Class Licence (Low Interference Potential Devices) RCL1993/1.

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