TMS320C674x/OMAP-L1x Processor Video Port Interface (VPIF)

User's Guide

Literature Number: SPRUGJ9A
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About This Manual

This manual describes the operation of the video port interface (VPIF).

Notational Conventions

This document uses the following conventions.

- Hexadecimal numbers are shown with the suffix h. For example, the following number is 40 hexadecimal (decimal 64): 40h.
- Registers in this document are shown in figures and described in tables.
  - Each register figure shows a rectangle divided into fields that represent the fields of the register. Each field is labeled with its bit name, its beginning and ending bit numbers above, and its read/write properties below. A legend explains the notation used for the properties.
  - Reserved bits in a register figure designate a bit that is used for future device expansion.

Related Documentation From Texas Instruments

The following documents describe the TMS320C674x Digital Signal Processors (DSPs) and OMAP-L1x Applications Processors. Copies of these documents are available on the Internet at www.ti.com. *Tip:* Enter the literature number in the search box provided at www.ti.com.

The current documentation that describes the DSP, related peripherals, and other technical collateral, is available in the C6000 DSP product folder at: www.ti.com/c6000.

SPRUGM5 — ***TMS320C6742 DSP System Reference Guide.*** Describes the C6742 DSP subsystem, system memory, device clocking, phase-locked loop controller (PLLC), power and sleep controller (PSC), power management, and system configuration module.

SPRUGM6 — ***TMS320C6746 DSP System Reference Guide.*** Describes the C6746 DSP subsystem, system memory, device clocking, phase-locked loop controller (PLLC), power and sleep controller (PSC), power management, and system configuration module.

SPRUGJ7 — ***TMS320C6748 DSP System Reference Guide.*** Describes the C6748 DSP subsystem, system memory, device clocking, phase-locked loop controller (PLLC), power and sleep controller (PSC), power management, and system configuration module.

SPRUGM7 — ***OMAP-L138 Applications Processor System Reference Guide.*** Describes the System-on-Chip (SoC) including the ARM subsystem, DSP subsystem, system memory, device clocking, phase-locked loop controller (PLLC), power and sleep controller (PSC), power management, ARM interrupt controller (AINTC), and system configuration module.

SPRUFK9 — ***TMS320C674x/OMAP-L1x Processor Peripherals Overview Reference Guide.*** Provides an overview and briefly describes the peripherals available on the TMS320C674x Digital Signal Processors (DSPs) and OMAP-L1x Applications Processors.

SPRUFK5 — ***TMS320C674x DSP Megamodule Reference Guide.*** Describes the TMS320C674x digital signal processor (DSP) megamodule. Included is a discussion on the internal direct memory access (IDMA) controller, the interrupt controller, the power-down controller, memory protection, bandwidth management, and the memory and cache.

SPRUFE8 — *TMS320C674x DSP CPU and Instruction Set Reference Guide.* Describes the CPU architecture, pipeline, instruction set, and interrupts for the TMS320C674x digital signal processors (DSPs). The C674x DSP is an enhancement of the C64x+ and C67x+ DSPs with added functionality and an expanded instruction set.

SPRUG82 — *TMS320C674x DSP Cache User's Guide.* Explains the fundamentals of memory caches and describes how the two-level cache-based internal memory architecture in the TMS320C674x digital signal processor (DSP) can be efficiently used in DSP applications. Shows how to maintain coherence with external memory, how to use DMA to reduce memory latencies, and how to optimize your code to improve cache efficiency. The internal memory architecture in the C674x DSP is organized in a two-level hierarchy consisting of a dedicated program cache (L1P) and a dedicated data cache (L1D) on the first level. Accesses by the CPU to the these first level caches can complete without CPU pipeline stalls. If the data requested by the CPU is not contained in cache, it is fetched from the next lower memory level, L2 or external memory.

Video Port Interface (VPIF)

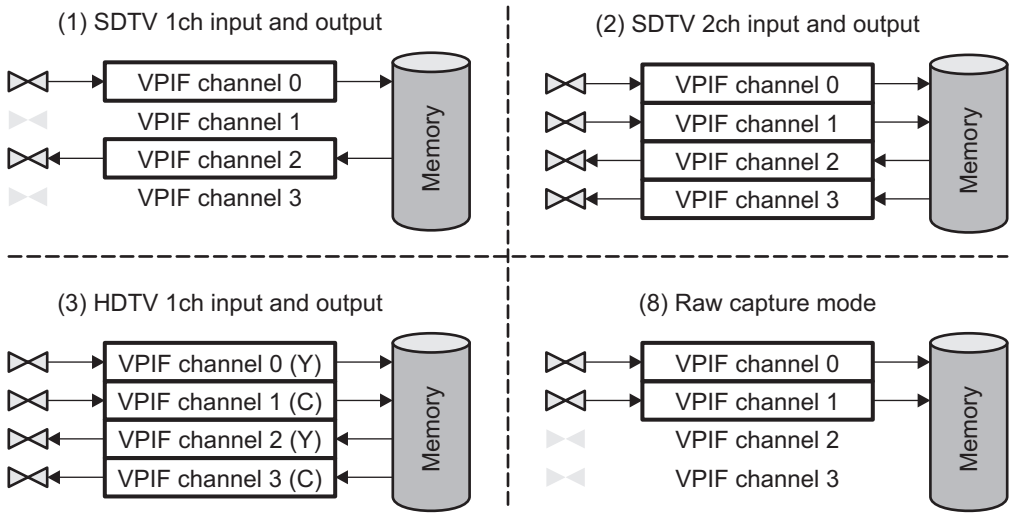
1 Introduction

This document describes the operation of the video port interface (VPIF).

1.1 Overview

The video port interface (VPIF) has two video input channels and two video output channels. Channels 0 and 1 share the same receive architecture, and channels 2 and 3 share the same transmit architecture. The input and output channel combinations of the VPIF are shown in Figure 1.

Figure 1. Input and Output Channels of VPIF



1.2 Features

The VPIF is designed to support the following features (note that some device designs may support reduced features because of system-level performance limitations):

- ITU-BT.656 format
- ITU-BT.1120 and SMTPE 296 formats
- Raw data capture
- VBI data storage
- Clipping of output data (to eliminate FFh and 00h values)

1.3 Features Not Supported

The following functions are not supported:

- ITU-BT.601 format
- Separated synchronization format (requiring vertical sync, horizontal sync, and field ID signals independent of the pixel data) is not supported (except for the raw data capture mode)

1.4 Functional Block Diagram

A block diagram of the VPIF is shown in Figure 2. A block diagram of the internal architecture of the VPIF is shown in Figure 3.

Figure 2. Video Port Interface (VPIF) Block Diagram

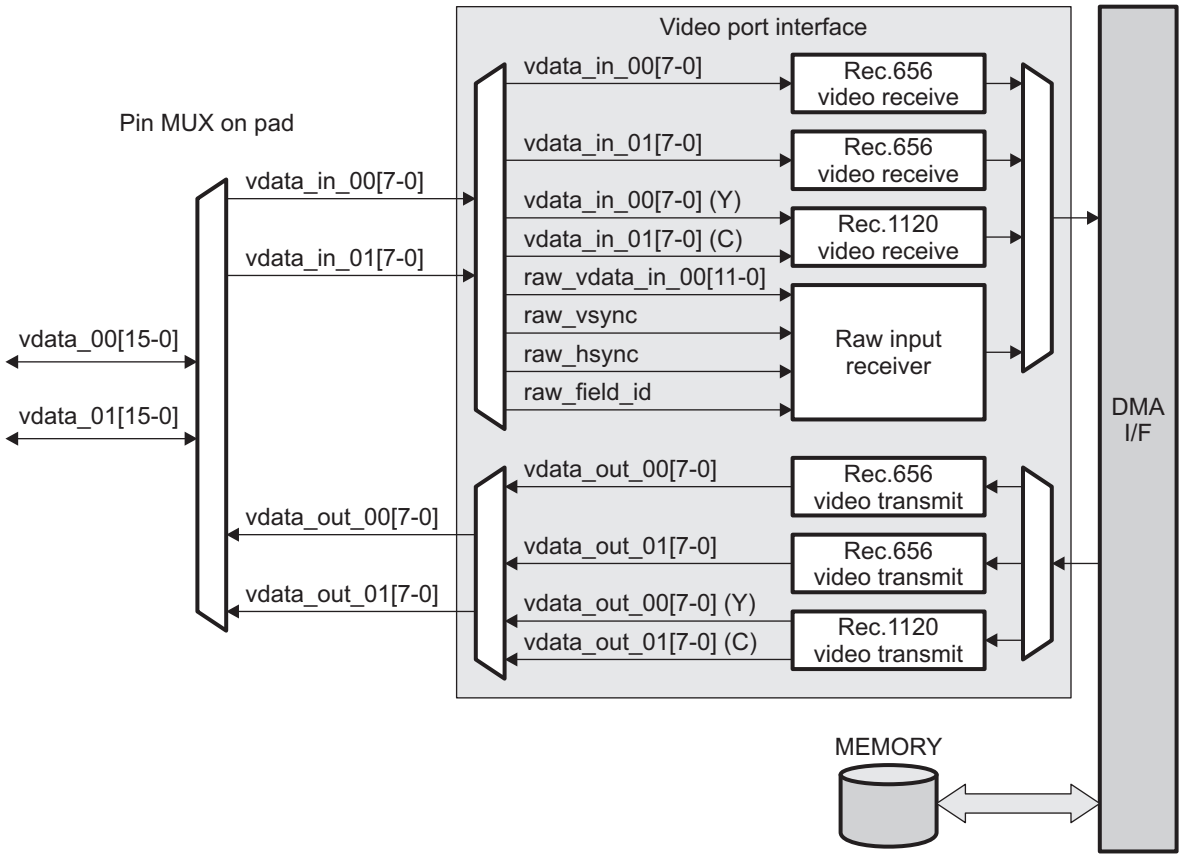
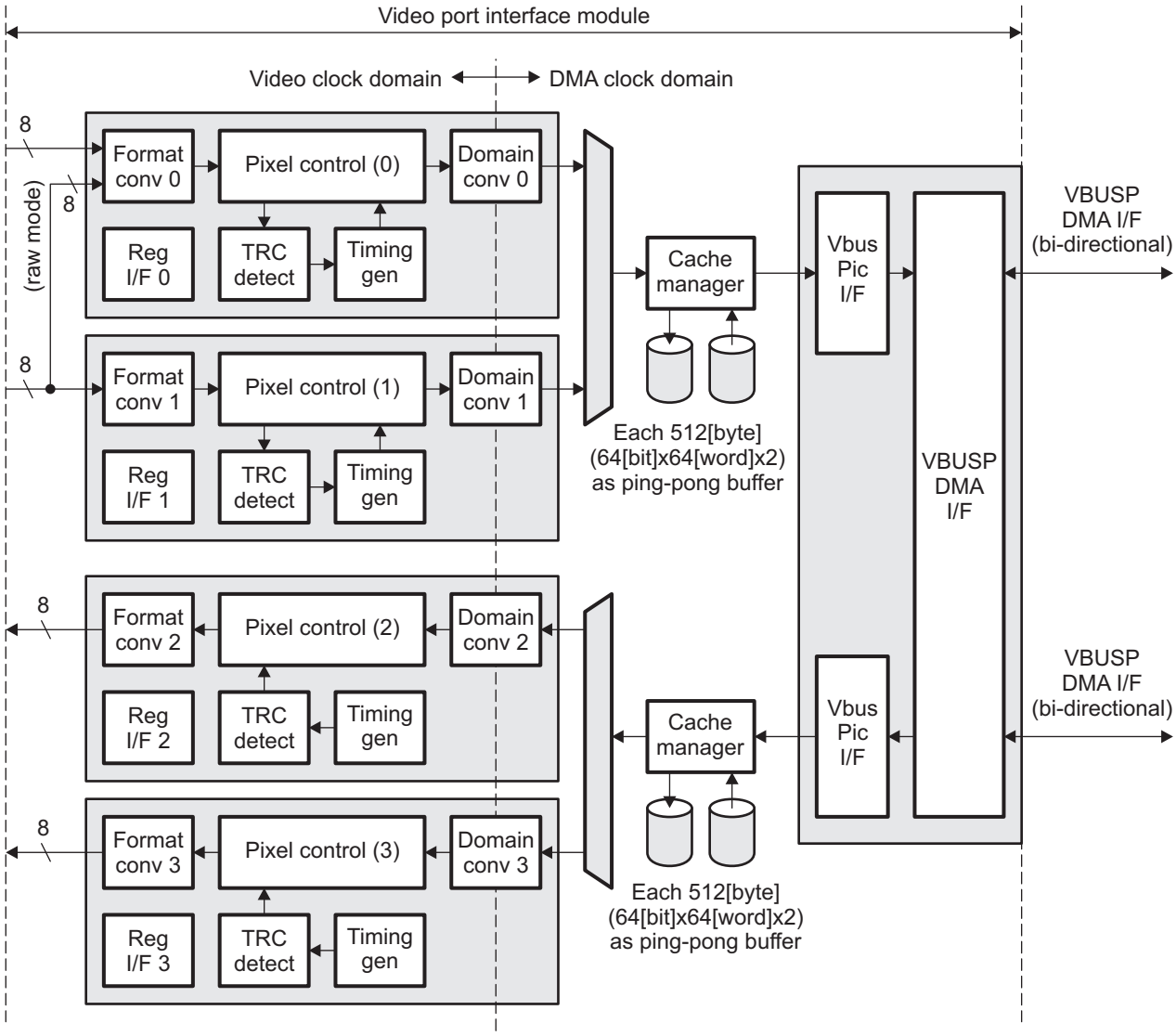


Figure 3. VPIF Architecture Block Diagram



1.5 Supported Use Cases

The following describes supported VPIF use cases. Actual VPIF performance may vary between devices designs because of system-level limitations.

The VPIF module has two input channels and two output channels. All channels can be activated simultaneously (see Table 1). The module uses four 512 byte buffers to cache data.

- Channels 0 and 1 are prepared only for input.
- Channels 2 and 3 are prepared only for output.

As shown in Table 1, both NTSC and PAL formats are supported. The supported VBI format is be based on ITU-BT.1364. Table 2 describes the usage combinations that are supported in the VPIF.

Table 1. Supported Formats on VPIF

	TV Definition Format	
TV System Format	**HDTV (rec. 1120) (no support of ancillary data)**	**SDTV (rec. 656) (ancillary data is based on BT.1364)**
NTSC	1125 line/60 field (vertical)	525 line/60 field (vertical)
	2200 pixel (horizontal)	858 pixel (horizontal)
PAL	1250 line/50 field (vertical)	625 line/50 field (vertical)
	2304 pixel (horizontal)	864 pixel (horizontal)
Square pixel common image format	1080-30p	-

Table 2. Input and Output Usage Combinations on VPIF

	Output Format		
Input Format	**HDTV Output**	**SDTV Output**	**No Output**
HDTV input (1 channel only)	√	√	√
Raw capture mode	√	√	√
SDTV input	√ (both 1-channel and 2-channel input)	√ (both 1-channel and 2-channel input/output)	√ (both 1-channel and 2-channel input)
No input	√	√ (both 1-channel and 2-channel output)	

2 Architecture

This section describes the architecture of the video port interface module (VPIF).

2.1 Clock Control

The VPIF has 4 clock input pins and 2 clock output pins. Each channel has 1 clock input pin with clock edge control using the CLKEDGE bit in the channel *n* control register (C*n*CTRL). VPIF can provide a clock for an external device on channel 2 or 3 using the CLKEN bit in the appropriate C2CTRL or C3CTRL register. The clock generated by VPIF will have the same frequency as the input clock.

2.2 Signal Descriptions

Table 3 describes the pin assignment on the VPIF for receiving video and capturing raw data. Shaded signals in Table 3 are synchronization signals that are necessary for capturing raw data.

Table 4 describes the pin assignments for transmitting video data.

Table 3. Receive Pin Multiplexing Control

Pin Name	Rec. 656	Rec. 1120	Raw Data Capture	Pin Name	Rec. 656	Rec. 1120	Raw Data Capture
DIN[0]	data0[0]	luma[0]	raw_data[0]	DIN[8]	data1[0]	chroma[0]	raw_data[8]
DIN[1]	data0[1]	luma[1]	raw_data[1]	DIN[9]	data1[1]	chroma[1]	raw_data[9]
DIN[2]	data0[2]	luma[2]	raw_data[2]	DIN[10]	data1[2]	chroma[2]	raw_data[10]
DIN[3]	data0[3]	luma[3]	raw_data[3]	DIN[11]	data1[3]	chroma[3]	raw_data[11]
DIN[4]	data0[4]	luma[4]	raw_data[4]	DIN[12]	data1[4]	chroma[4]	not used
DIN[5]	data0[5]	luma[5]	raw_data[5]	DIN[13]	data1[5]	chroma[5]	raw_field_id
DIN[6]	data0[6]	luma[6]	raw_data[6]	DIN[14]	data1[6]	chroma[6]	raw_h_valid
DIN[7]	data0[7]	luma[7]	raw_data[7]	DIN[15]	data1[7]	chroma[7]	raw_v_valid
CLKIN0	data0_clk	luma_clk	raw_data_clk	CLKIN1	data1_clk	chroma_clk	raw_data_clk

Table 4. Transmit Pin Multiplexing Control

Pin Name	Trans. 656	Trans. 1120	Pin Name	Trans. 656	Trans. 1120
DOUT[0]	data2[0]	luma[0]	DOUT[8]	data3[0]	chroma[0]
DOUT[1]	data2[1]	luma[1]	DOUT[9]	data3[1]	chroma[1]
DOUT[2]	data2[2]	luma[2]	DOUT[10]	data3[2]	chroma[2]
DOUT[3]	data2[3]	luma[3]	DOUT[11]	data3[3]	chroma[3]
DOUT[4]	data2[4]	luma[4]	DOUT[12]	data3[4]	chroma[4]
DOUT[5]	data2[5]	luma[5]	DOUT[13]	data3[5]	chroma[5]
DOUT[6]	data2[6]	luma[6]	DOUT[14]	data3[6]	chroma[6]
DOUT[7]	data2[7]	luma[7]	DOUT[15]	data3[7]	chroma[7]
CLKIN2	data2_ref_clk	luma_ref_clk	CLKIN3	data3_ref_clk	chroma_ref_clk
CLKOUT2	data2_clk	luma_clk	CLKOUT3	data3_clk	chroma_clk

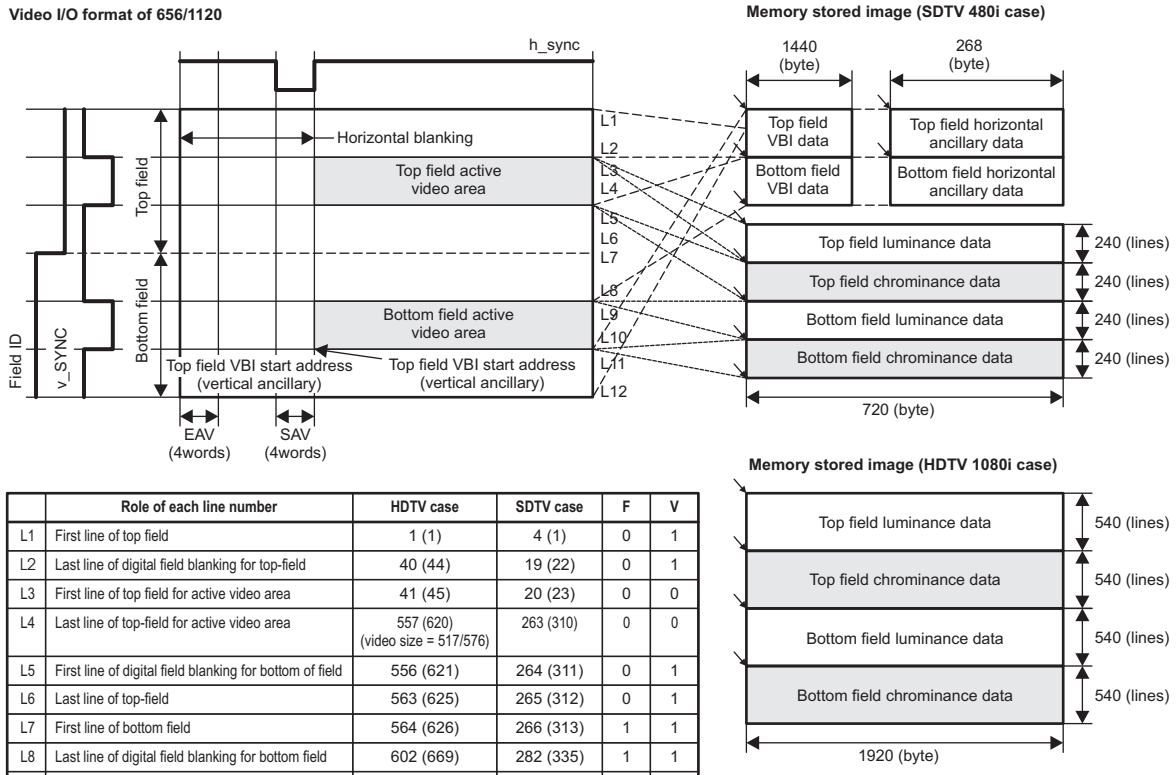
2.3 Interlaced and Progressive Video

VPIF supports both interlaced and progressive video formats.

2.3.1 Interlaced Video

The components of interlaced video are shown in Figure 4.

Figure 4. Interlaced Video



	Role of each line number	HDTV case	SDTV case	F	V
L1	First line of top field	1 (1)	4 (1)	0	1
L2	Last line of digital field blanking for top-field	40 (44)	19 (22)	0	1
L3	First line of top field for active video area	41 (45)	20 (23)	0	0
L4	Last line of top-field for active video area	557 (620) (video size = 517/576)	263 (310)	0	0
L5	First line of digital field blanking for bottom of field	556 (621)	264 (311)	0	1
L6	Last line of top-field	563 (625)	265 (312)	0	1
L7	First line of bottom field	564 (626)	266 (313)	1	1
L8	Last line of digital field blanking for bottom field	602 (669)	282 (335)	1	1
L9	First line of bottom field for active video area	603 (670)	283 (336)	1	0
L10	Last line of bottom field for active video area	1120 (1245)	525 (623)	1	0
L11	First line of digital field blanking for top-field	1121 (1246)	1 (624)	1	1
L12	Last line of bottom field	1125 (1250)	3 (625)	1	1

The values in the table are from the BT.656 and BT.1120 standards. L11 is regarded as the start line of the frame in the VPIF.

All parameters (L1 to L12) for interlaced video are configured through VPIF register settings. Values listed in Figure 4 are for NTSC and (PAL).

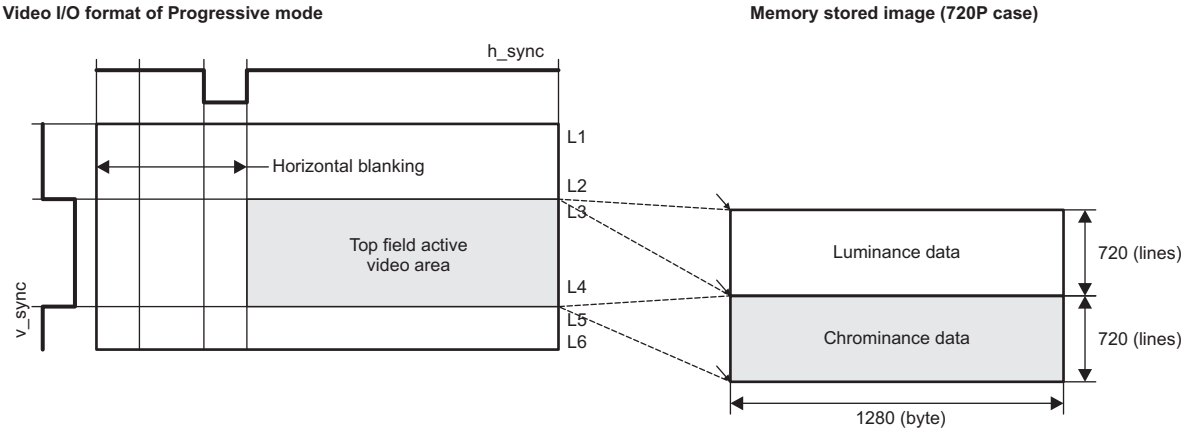
Interlaced video is divided into eight buffer spaces:

1. Top field VBI data in vertical ancillary area
2. Top field VBI data in horizontal ancillary area
3. Bottom field VBI data in vertical ancillary area
4. Bottom field VBI data in horizontal ancillary area
5. Top field luminance data
6. Top field chrominance data
7. Bottom field luminance data
8. Bottom field chrominance data

2.3.2 Progressive Video

The components of progressive video are shown in Figure 5.

Figure 5. Progressive Video



	Role of each line number	HDTV case	F	V
L1	First line of upper blanking for the frame	1	0	1
L2	Last line of upper blanking for the frame	25	0	1
L3	First line of the frame for active video area	26	0	0
L4	Last line of the frame for active video area	745	0	0
L5	First line of lower blanking for the frame	746	0	1
L6	Last line of lower blanking for the frame	750	0	1

The buffer register configurations are latched at L1 in progressive format. Data on L5 to L6 is stored into a different memory buffer from data on L1 to L2 because the base address is changed at timing of L1.

All parameters (L1 to L6) for progressive video are configured through VPIF register settings.

Progressive video is divided into four buffer spaces:

1. VBI data in vertical ancillary area
2. VBI data in horizontal ancillary area
3. Luminance data
4. Chrominance data

2.4 Memory Interface

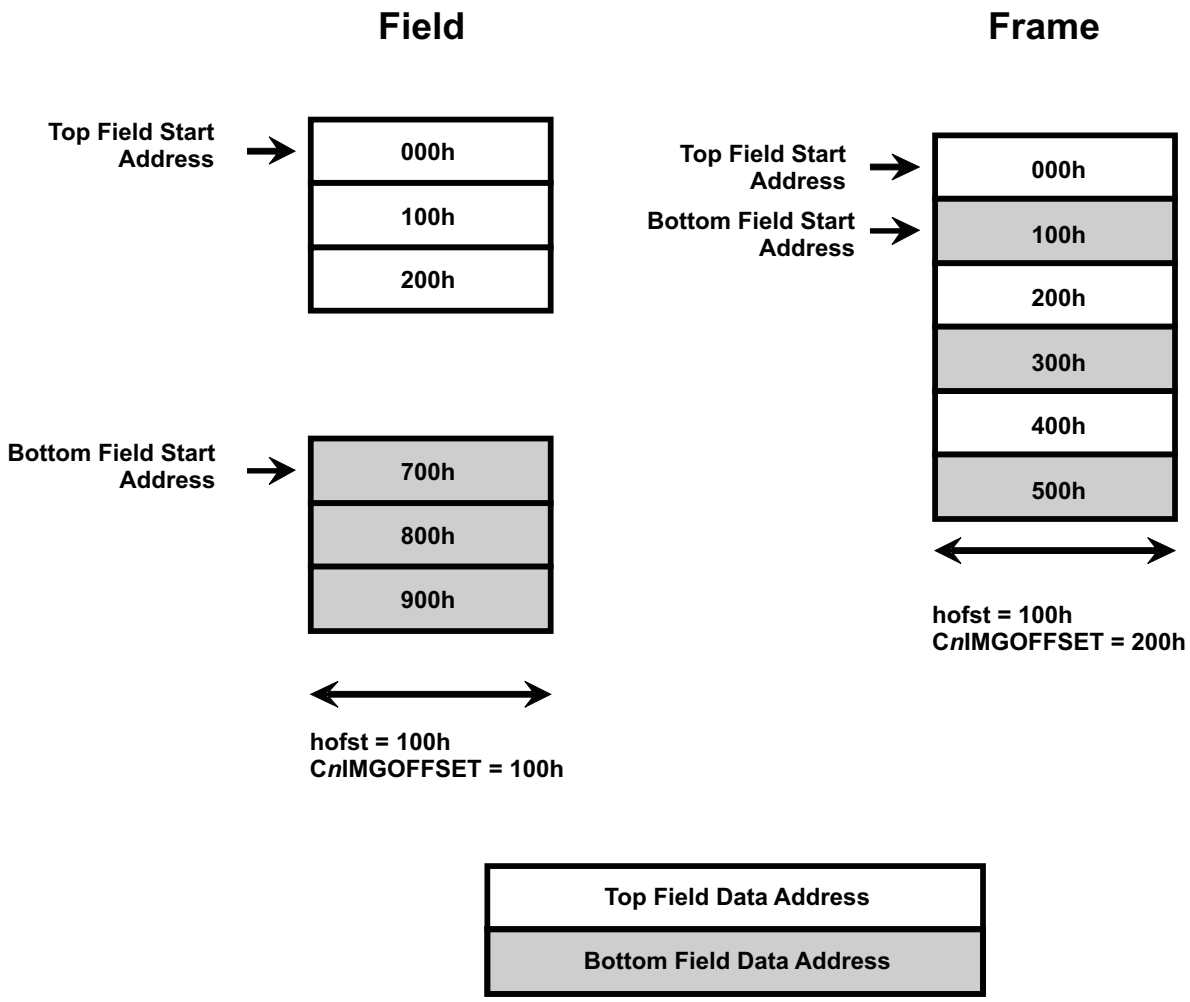
2.4.1 DMA Request Size

The DMA burst size between the VPIF module and storage memory is configured through the DMA Request Size Control Register (REQSIZE).

2.4.2 Storage Format

The VPIF supports two data buffer memory addressing modes for luminance and chrominance data: Field and Frame, as shown in Figure 6. The FIELDFRAME bit (in C0CTRL and C2CTRL) selects which storage method is used. Progressive video must use the Frame storage mode, but interlaced video can use either Field or Frame storage modes.

Figure 6. Memory Storage Modes for Interlaced Video



The storage modes are optimized for the following use conditions for interlaced video:

- Field format
  - Top- and bottom-field data-sets are stored in isolated buffers
  - Top- and bottom-field buffer start addresses are independent
  - Address offset per line of data in each top- and bottom-field buffer is equal to hofst (C*n*IMGOFFSET = hofst)
- Frame format
  - Top- and bottom-field data-sets are interlaced in memory
  - Top-field buffer start address is coupled with bottom-field buffer start address (Top Start = Bottom Start - hofst)
  - Bottom-field buffer start address is coupled with top-field buffer start address (Bottom Start = Top Start + hofst)
  - Address offset per line of data in each top- or bottom-field buffer is equal to hofst × 2 (C*n*IMGOFFSET = hofst × 2)

Note that because progressive video only uses top-field buffers, the address offset per line of data is equal to hofst (C*n*IMGOFFSET = hofst).

Note that when capturing 10-bit or 12-bit video in the raw capture mode, the offset per line of data is doubled because of bit padding.

2.5 Video Transmit

VPIF channels 2 and 3 are used for video transmit.

2.5.1 Y/C Mux

For BT.656 video, luminance (Y) and chrominance (C) values are multiplexed into a single byte-stream on one channel (either channel 2 or channel 3).

For BT.1120 video, channels 2 and 3 function as a pair without Y/C multiplexing in the following configuration:

- Channel 2 transmits Y data (C buffer settings for channel 2 are ignored)
- Channel 3 transmits C data (Y buffer settings for channel 3 are ignored)

The Y/C multiplex function for BT.656 video is enabled by setting the YCMUX bit in the channel control registers C*n*CTRL. The YCMUX bit must be the same for both channels 2 and 3.

2.5.2 Transmit Clocking

Each transmit channel uses a reference input clock (CLKIN*n*) and a video output clock (CLKOUT*n*). When transmit is enabled, VPIF will generate CLKOUT*n* with the same frequency as CLKIN*n*, and video data will be transmitted synchronously with CLKOUT*n*.

The CLKOUT*n* output signal is enabled by setting the CLKEN bit in the channel control register C*n*CTRL; the signal can also be inverted by setting the CLKEDGE bit in the C*n*CTRL register.

When transmitting BT.1120 video data, the two transmit channels operate as a pair. To ensure that video data is transmitted at the same time across both channels, the CLKIN*n* signals must share the same reference clock source.

2.5.3 Video Pixel Enable

The PIXEL bit of the C2CTRL and C3CTRL control registers enables the transmission of video data stored in memory. When the PIXEL bit is set, video data is transmitted normally. When the PIXEL bit is cleared, the VPIF will transmit blank video data (Y = 10h, C = 80h). The PIXEL bit should only be set when the associated VPIF channel is disabled, otherwise the VPIF may output corrupt data and issue an ERROR interrupt for buffer underflow.

2.6 Video Receive

VPIF channels 0 and 1 are used for video receive.

2.6.1 Y/C Mux

For BT.656 video, luminance (Y) and chrominance (C) values are multiplexed into a single byte-stream on one channel (either channel 0 or channel 1).

For BT.1120 video, channels 0 and 1 function as a pair without Y/C multiplexing in the following configuration:

- Channel 0 receives Y data (C buffer settings for channel 0 are ignored)
- Channel 1 receives C data (Y buffer settings for channel 1 are ignored)

The Y/C multiplex function for BT.656 video is enabled by setting the YCMUX bit in the channel control registers C*n*CTRL. The YCMUX bit must be the same for both channels 0 and 1.

2.6.2 Receive Clocking

Each receive channel uses an input clock (CLKIN*n*) . When receive is enabled, video data is latched synchronously with the rising edge of CLKIN*n*. The VPIF can be reconfigured to latch on the falling edge of CLKIN*n* by setting the CLKEDGE bit in the C*n*CTRL register.

When receiving BT.1120 video data, the two receive channels operate as a pair. To ensure that video data is received at the same time across both channels, the CLKIN*n* signals must share the same reference clock.

2.6.3 Capture Mode

The CAPMODE bit of the C0CTRL and C1CTRL control registers determines what data format will be captured by VPIF. The BT/YC video mode will look for video sync signals that are embedded within the video byte stream (standard for BT video). The CCD/CMOS (Raw Data Capture) mode will look for video sync signals on the dedicated VPIF sync pins (common for CCD and CMOS sensors).

When the CCD/CMOS mode is selected, channels 0 and 1 will work as a pair. Thus, both channels must be enabled before VPIF will capture receive data.

Capture mode settings must be the same for both channels 0 and 1.

2.7 Raw Data Capture

The VPIF supports raw data capturing. With this function, you can connect a camera AFE output signal directly into an input port of the CPU. Usually, the output format of the camera AFE device is in raw format that consists of an RGB component (sometimes RGrGbB format). The following functions are supported:

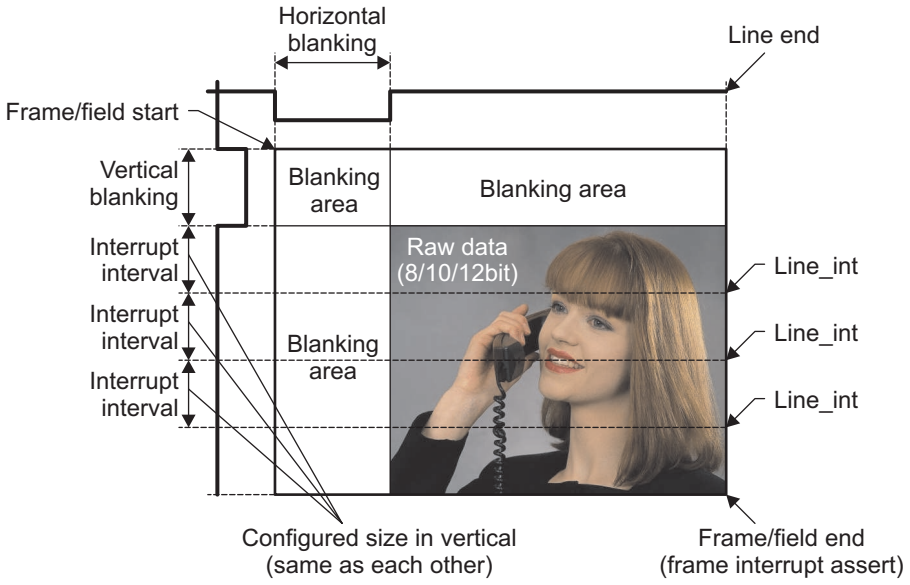
- Storing pixel data in memory (no storage of blanking data).
- Data bit widths from 8 bits/pixel, 10 bits/pixel, and 12 bits/pixel mode.
- Selectable polarity for H/V pixel valid signal and field ID signal.
- Separated field storage (top field and bottom field are stored independently) and interleaved field storage (normal frame format) support in memory storage.
- Two kinds of interrupt support. One is asserted once per each configured line size (line_interrupt) and the other is asserted at the end of the capture area (frame_interrupt). See Figure 7. Note that line_interrupt is only supported in raw mode. In other modes (BT.656, BT.1120, and SMPTE 296M), line_interrupt is not supported.

The following functions are not supported:

- No support of color space conversion from RGB to YCbCr.
- No CFA interpolation for each raw data pattern (such as Bayer or Foveon).
- No push-storage function on non-byte aligned data format (10 bits/pixel and 12 bits/pixel). Data should be stored in memory in byte-aligned format.

The active period of each synchronization signal is regarded as the blanking area and any other area is regarded as the active video area that is stored in memory. See Figure 7.

Figure 7. Functional Image of Raw Data Capturing Mode



All register configurations related to raw capture mode are reflected with the falling edge of the internal V-sync, which source is raw_v_valid, in normal polarity (low = blanking, high = data).

2.7.1 Raw Capture Mode Signals

Both interlaced and progressive interface modes are supported. The following signals are assigned to the interface signal of the raw capture mode:

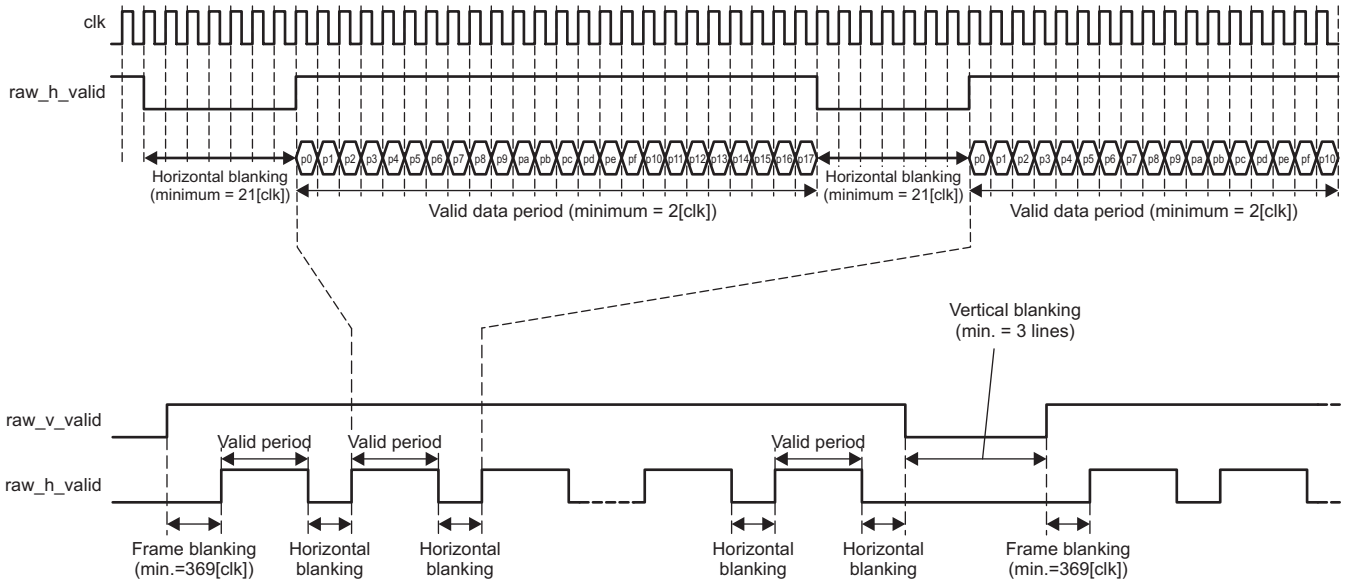
- raw_h_valid: horizontal pixel valid signal (regarded as horizontal synchronization signal)
- raw_v_valid: vertical line valid signal (regarded as vertical synchronization signal)
- raw_field_id: field ID signal
- vin_data_raw[11:0]: raw data input (8 bits/pixel, 10 bits/pixel, and 12 bits/pixel)

2.7.1.1 Progressive CCD Raw Capture Mode

The CCD Raw Capture mode is illustrated in Figure 8. In this mode, data within the active periods of both raw_v_valid and raw_h_valid is captured by VPIF. The falling edges of the two valid signals serve as the vertical and horizontal synchronization signals (the valid signal edge polarity can be configured in the C0CTRL register). You have to set the image address offset.

In this mode, without the activated period of raw_v_valid, no raw_h_valid signal is activated. Only in the period when both raw_v_valid and raw_h_valid signals are activated, the incoming data is regarded as valid data.

Figure 8. Raw Capture Progressive Mode

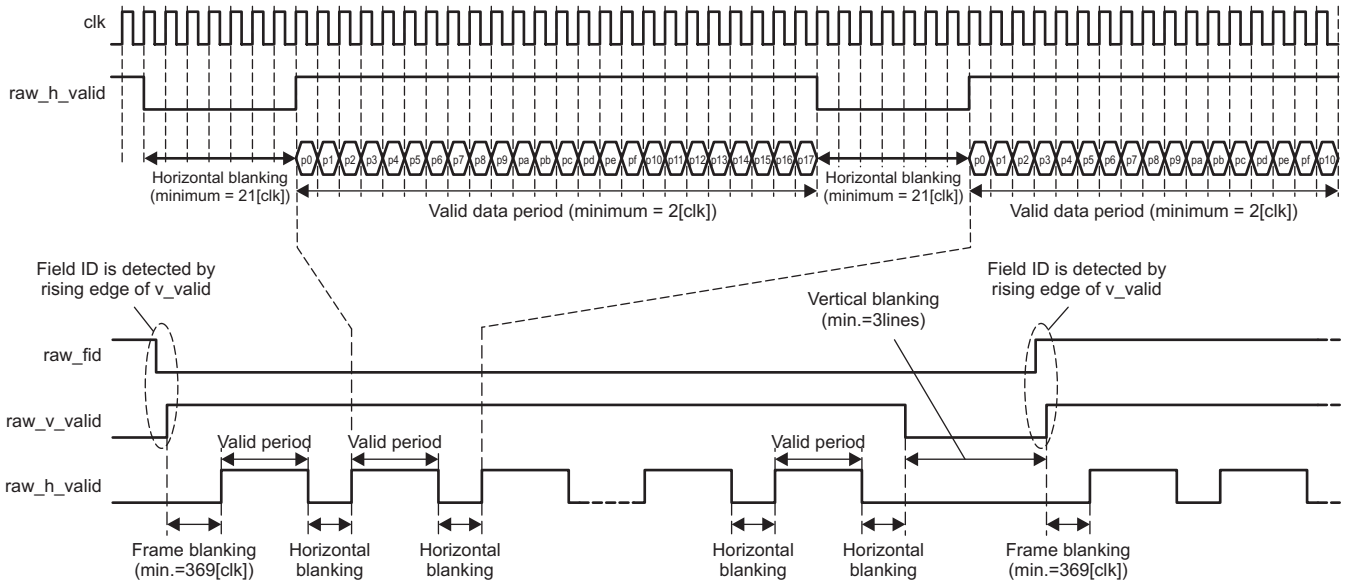


2.7.1.2 Interlaced CCD Raw Capture Mode

See Figure 9. The falling edge of the vertical valid signal (raw_v_valid) and the horizontal valid signal (raw_h_valid) is regarded as the normal vertical and horizontal synchronization signals, respectively. The field ID (raw_fid) is detected at the rising edge of the raw_v_valid signal. The description of the detail value in Figure 8 is based on the description on the Micron Image sensor device specification sheet.

In this mode, data with an active period of both of raw_v_valid and raw_h_valid is detected by the VPIF and valid data is stored in extra-VPIF memory. The falling edge of the two signals is regarded as the vertical and horizontal synchronization signals (the valid signal polarity and the field ID polarity can be configured by the channel 0 control register (C0CTRL)). You have to set the image address offset.

Figure 9. Raw Capture Interlaced Mode



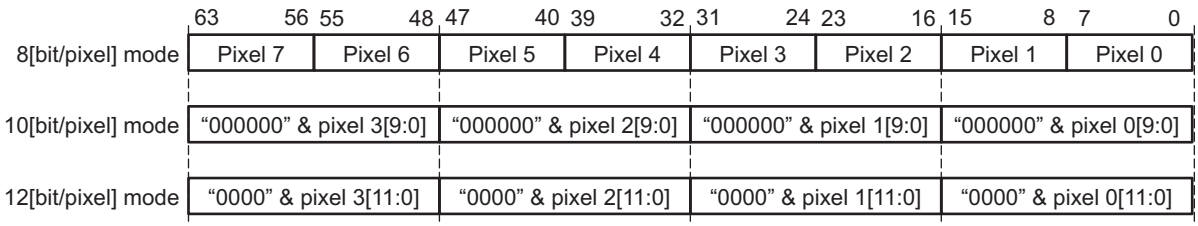
2.7.2 Configuration Settings for Raw Capture Mode

In raw capture mode, VPIF automatically detects the incoming image size by using the raw_h_valid and raw_v_valid signals. Thus, the C*n*HCFG, C*n*VCFG0, C*n*VCFG1, and C*n*VSIZE registers are not required.

2.7.3 Memory Format on Raw Capture Mode

All active video data is stored in memory outside of VPIF in byte-aligned format. Bit stuffing is performed (as shown in Figure 10) when 10 bits/pixel or 12 bits/pixel mode is selected.

Figure 10. Stuffing Manner in Storage Memory



2.8 VBI Ancillary Data

The VPIF can transmit and receive ancillary data in the video blanking interval (VBI) of BT.656 and BT.1120 video streams. The ancillary data regions are referred to as:

- Horizontal Ancillary (HANC) - Data between EAV and SAV (horizontal blanking interval), and
- Vertical Ancillary (VANC) - Data between SAV and EAV (horizontal active video area).

Transmit and receive of ancillary data is enabled by setting the HANC and VANC bits in the C0CTRL and C2CTRL control registers.

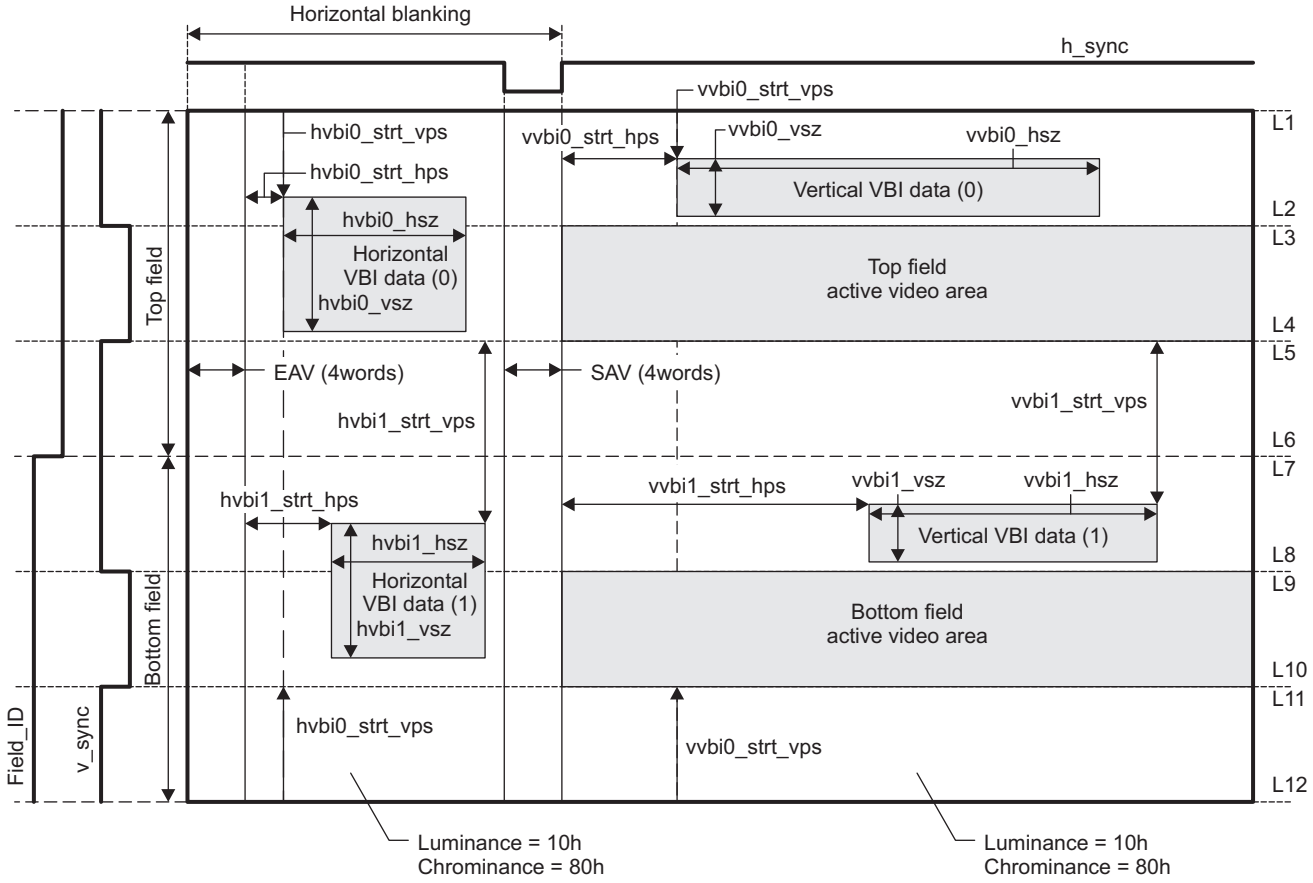
2.8.1 VBI Ancillary Data Transmit

The ancillary data to be transmitted is prepared by the user outside of VPIF. Ancillary register settings determine the origin position of the ancillary data within the VBI and how much ancillary data is to be transmitted. Note that the user is expected to place valid ancillary data in a memory buffer that is representative of the entire VBI region of interest. However, only the valid ancillary data region needs to be initialized -- the VPIF will automatically transmit blanking data (Y=10h, C=80h) for non-valid ancillary data regions.

As shown in Figure 11, the vertical-origin of each data region is offset from the falling edge of the vertical synchronization signal, and the horizontal-origin of each data region is offset from the SAV and EAV signals.

The value of the horizontal start position should be a multiple of 8 (HPOS[2:0] = 0) on both the horizontal and vertical ancillary data regions; the horizontal size can be defined as any value that does not exceed the data region.

Figure 11. VBI Result Data Transmit Image for Interlaced Image



2.8.2 VBI Ancillary Data Receive

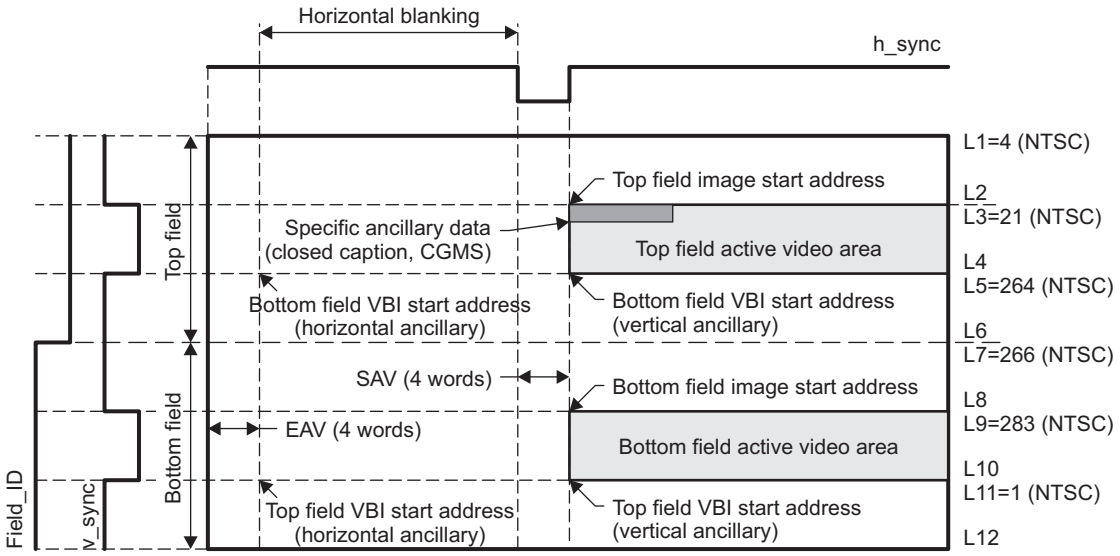
When the VBI receive function is enabled, the VPIF receives all data in the associated blanking region. The VPIF cannot selectively receive sub-regions in the VBI space. The CPU has to receive valid data from this data and you have to prepare for the correct size of data buffer. For example in the NTSC case, the horizontal ancillary data needs 268 bytes × 525 lines and the vertical ancillary data needs 1440 bytes × 38 lines buffer.

The address line offset for the vertical ancillary data uses the channel *n* image data address offset register (C*n*IMGOFFSET).

2.8.3 Processing Method for Specific Ancillary Data

The VPIF has the ability to capture/assert video ancillary data (Figure 12) that is not video image data but is VBI data. In most cases, video ancillary data is inserted in the blanking interval for either the horizontal or vertical direction. But in some cases, such as CGMS or closed-caption that is in Japanese and US applications, the line number where these kinds of ancillary data is inserted is in the active video area. In the case that ancillary data is inserted in the active video area, the VPIF regards the incoming (or stored data) as video data.

Figure 12. Image of Specific Ancillary Data on NTSC



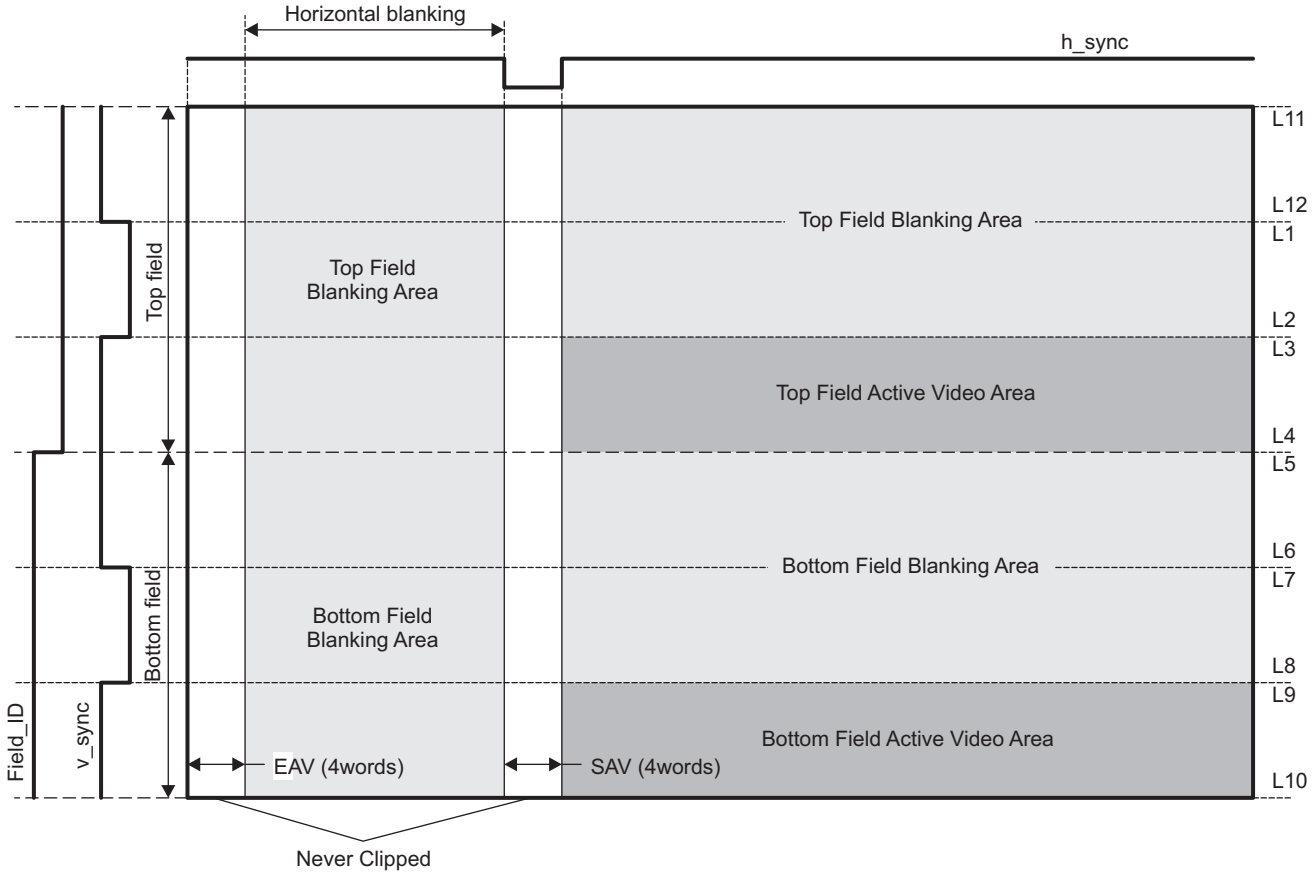
2.9 Clipping Function for Output

The clipping function is prepared for avoidance of miss-synchronization on an external device (video encoder), which receives output of the VPIF module. In some cases, the source data for the active video area has a combination of FF-00-00, which is the same as TRC (synchronization code). Some video encoders regard this combination as part of TRC and then the synchronization is failed.

In order to avoid this issue, the VPIF module is capable of clipping the output data value except the TRC within the range of 01~FEh. If this function is activated, the value 00h is clipped to 01h and the value FFh is clipped to FEh. Any other value is passed through.

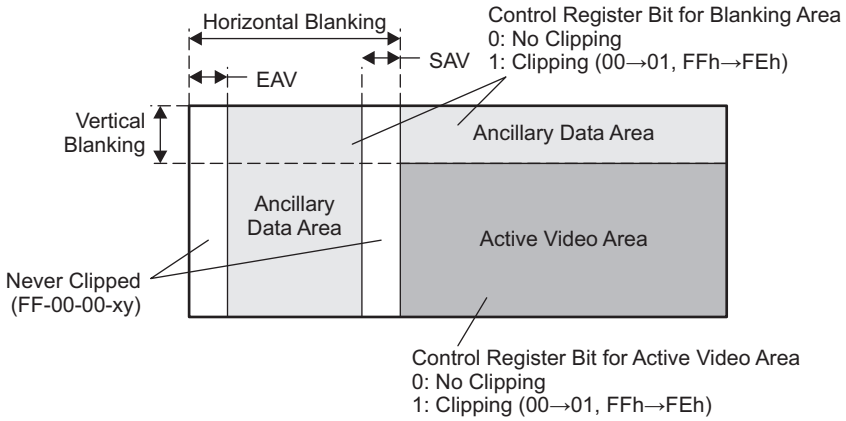
As shown in Figure 13, VPIF has two data areas other than TRC: one is blanking data (ancillary data) and the second is video image data. The clipping function can be independently enabled for each data area. Note that field-level control is not supported.

Figure 13. Data Areas and Clipping Function



The relationship between register bit assignment and the clipping function is shown in Figure 14. Control register bits in Figure 14 are prepared for both channel 2 and channel 3. Clipping on the channels is independently activated.

Figure 14. Register Bit Assignment on Clipping Function



2.10 Reset Considerations

The VPIF does not have a software reset. When a hardware reset is asserted, all VPIF registers are set to their default values.

2.11 Initialization

The general procedure for VPIF initialization is:

1. Enable the VPIF in the LPSC.
2. Program the corresponding bits in the DMA size control register (REQSIZE) and the channel *n* sub-picture configuration register (C*n*SUBPIC).
3. Program the Emulation related registers, such as the emulation suspend control register (EMUCTRL) in the VPIF and the emulation suspend source register (SUSPSRC) in the System Module (see Section 2.13 for more detail). The default values of SUSPSRC are configured to the ARM as the main processor.

2.12 Interrupt Support

2.12.1 Interrupt Events and Requests

The VPIF sends the following interrupt events to the CPU:

- FRAME0
- FRAME1
- FRAME2
- FRAME3
- ERROR

The ERROR interrupt is generated for the following reasons:

- For channels 0 or 1:
  - Internal buffer overflow
  - Length of EAV2SAV or SAV2EAV is not the same as the configured value
  - Bit error detected on 4th field of TRC
- For channels 2 or 3:
  - Internal buffer overflow

Note that the VPIF peripheral has no mechanism to reissue interrupts that may have been dropped by the CPU so care should be taken when VPIF interrupts are combined at the system level. In a combined interrupt configuration, the CPU may be busy servicing a VPIF interrupt when another VPIF interrupt arrives. If the interrupt controller has no means to count VPIF interrupts, the CPU will drop subsequent VPIF interrupts until servicing of the first VPIF interrupt is complete.

2.12.2 Field/Frame Interrupts to CPU

This section describes the conditions of the field/frame based interrupt assertion from the VPIF. The VPIF interrupt is designed to make the processor identify the timing for updating the address register of the VPIF module. The timing of the interrupt from the VPIF module is different from the timing of the V-sync. The interrupt is generated when the last data transfer between the VPIF module and the VBUS is finished.

2.12.2.1 Interrupt Condition

The interrupt signal from the VPIF described in this section means the beginning of a field (or frame). A way to indicate the beginning of a field (or a frame) varies from the function mode; normal YC receive/transmit mode and CCD/CMOS capture mode differ because of the vertical synchronization signal.

The VPIF generates the following events as conditions for interrupt assertion:

- In normal YC receive/transmit mode, EAV on line L1 (and EAV on line L7 in field interrupt for bottom field). Both L1 and L7 are described in Figure 4 and Figure 5.
- In CCD/CMOS capture mode, starting edge for first line of vertical valid pixel area.

2.12.2.2 First Interrupt from VPIF

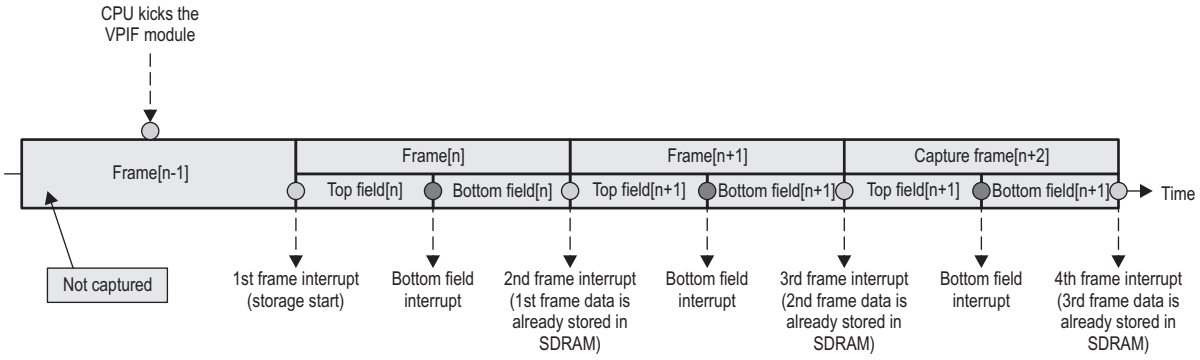
NOTE: The first vertical synchronization signal is defined as the transition from the L10 line to the L11 line in the interlace mode or from the L4 line to the L5 line in the progressive mode.

For raw capture mode, the VPIF immediately starts to capture the data if you enable middle of frame.

In channels 0 and 1, the VPIF starts to capture incoming picture data from the first vertical synchronization signal after the CPU activates the VPIF with register configuration. The interrupt signal from the VPIF is asserted when the vertical synchronization signal is received. So, no incoming data is written in memory when the first interrupt is asserted from the VPIF (Figure 15).

If the CPU uses this interrupt signal not only for the time interval between each video frame but also for the timing to read the stored data from the defined area in memory. Note that the CPU has to ignore the first interrupt signal from the VPIF.

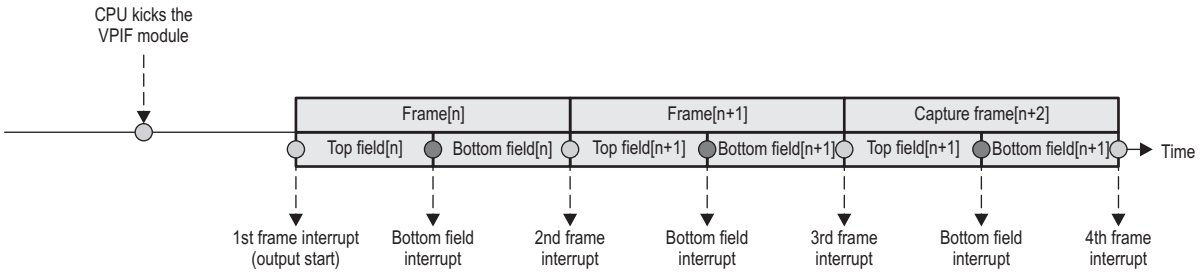
Figure 15. Relationship Between the First Interrupt and Incoming Data



In channels 2 and 3, the VPIF starts to assert displaying picture data after the CPU activates the VPIF with register configuration. The output displaying data is asserted from the VPIF just after the VPIF reads the output data from memory (Figure 16).

So, any redundant data such as the frame[n - 1] area in Figure 15 is not necessary to be prepared. The relationship between the interrupt pulse activation and the register configuration is the same as for capturing data.

Figure 16. Relationship Between the First Interrupt and Outgoing Data



If the Figure 16 described relationship with the CPU activates the VPIF and the incoming data and frame[n] start the L11 line for the interlace mode or the L5 line for the progressive mode, the VPIF starts the data store from frame[n+1] not frame[n]. The first frame interrupt happens after frame[n] (at the 2nd frame interrupt in Figure 16), because at the start of the incoming data, there is no first vertical synchronization signal.

2.12.3 Line Interrupts to CPU

In raw data capture mode (CCD/CMOS capture), VPIF will issue line-interval triggered interrupts using the field/frame interrupt signals. The line-interval is programmable in the C0CTRL register.

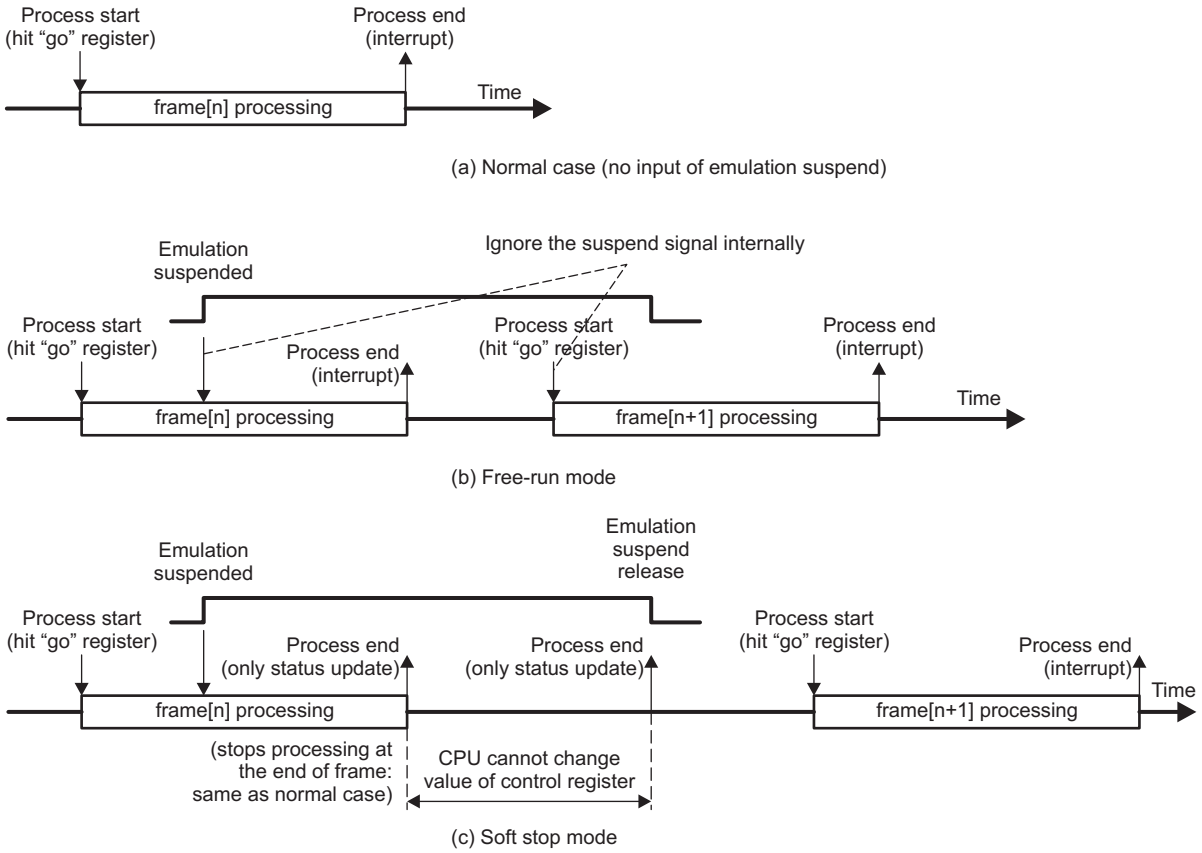
2.13 Emulation Considerations

2.13.1 Emulation Suspend Mode Support

The VPIF supports the emulation suspend signal from the CPU. The emulation suspend signal (a high signal indicates that the CPU is suspended) is asserted by the CPU when the CPU is halted with a breakpoint or any other reason during debug.

Functional performance, when the emulation suspend signal is received, is defined by the register configuration and is different for each use (receiver and transmitter). Because the VPIF has to process real-time incoming (or outgoing) data that has a unit size of 1 frame, the VPIF can be stalled at the nearest end of the present processing frame when the emulation suspend signal is received. The fundamental performance of emulation suspend is shown in Figure 17.

Figure 17. Module Performance with Emulation Suspend Signal



2.13.1.1 Receiver (Channels 0 and 1)

The VPIF receives input data from an external video device. The input format is BT.656 or BT.1120. If the emulation suspend comes from the CPU during image processing, the VPIF will first try to run at the end of the present frame and then the VPIF will be stalled (see Figure 17 (c)).

The VPIF should only have a software stop mode; the hardware stop mode is not supported. If the CPU changes the register configuration during an emulation suspended period, the new configuration should be validated at the first V-sync after the suspended period.

2.13.1.2 Transmitter (Channels 2 and 3)

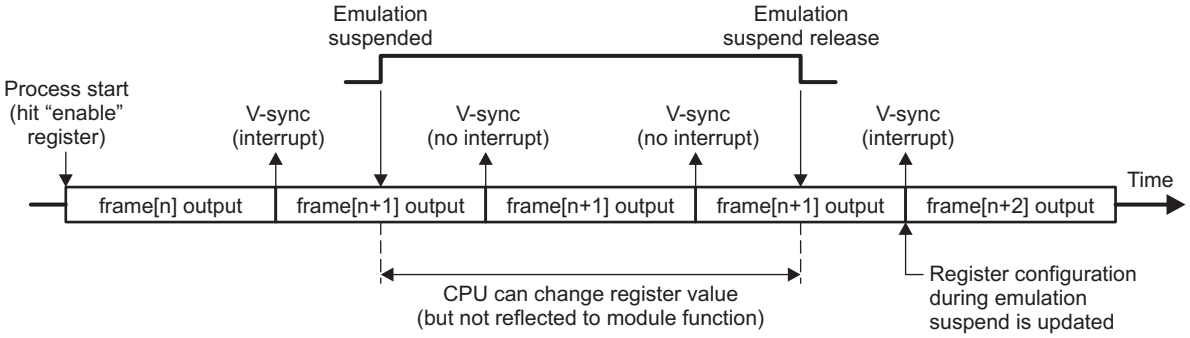
The VPIF transmits output data to an external video device. Source data for this output data is stored in SDRAM. The VPIF needs information about the start address of the source data stored in SDRAM. The output format is BT.656 or BT.1120.

In this mode, any suspend function should not be activated because you would like to see a displayed picture, taking usage of this signal into consideration. From a system's stand point, the VPIF should act in the following sequence if the emulation suspend signal is detected:

1. The VPIF continues processing at the end of the present frame.
2. If the present frame is finished, interrupt assertion is stalled.
3. At phase (b), during the active period of the emulation suspend signal, the VPIF continues reading the same frame data from SDRAM (no register change is reflected to module performance during this period).
4. After the CPU returns back to the normal state, the VPIF performs as usual. New register configurations done during an emulation suspend period are reflected in the functional performance at the first V-sync after deassertion of the suspend signal.

If the CPU changes the register configuration during an emulation suspended period, the new configuration should be validated at the first V-sync after the suspended period. Functional performance of this mode is shown in Figure 18.

Figure 18. Emulation Suspend Function on Channels 2 and 3 (Transmit)



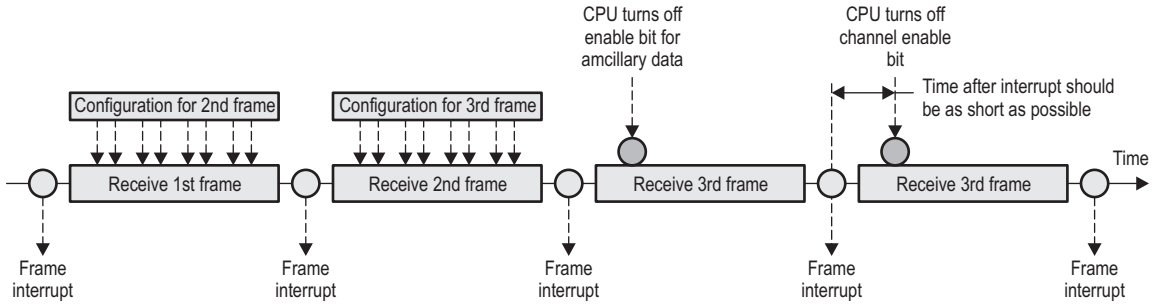
2.14 Rules for Module Control

When disabling the VPIF follow the sequence below:

1. Disable ancillary data (HANC and VANC) in the C*n*CTRL control registers.
2. Wait for frame interrupt from the active channel.
3. Clear the channel enable bit of the channel in C*n*CTRL.

The VPIF stops immediately after writing 0 to the C*n*EN bit in the channel *n* control register (C*n*CTRL). Writing to C*n*CTRL takes effect exactly at the same time you write to it, it does not wait to be latched by the VSYNC.

Figure 19. Method for Turning off Module Channel



2.15 Standard Video Modes

2.15.1 BT.656 Mode

The input clock source of 27 MHZ is used for the source clock of the video output, see Figure 20. In BT.656 mode, either channel of the input port on the VPIF is used as the actual input of the data. The VPIF can provide a 27-MHZ output to an external PLL device that provides the audio clock synchronized to the video output clock.

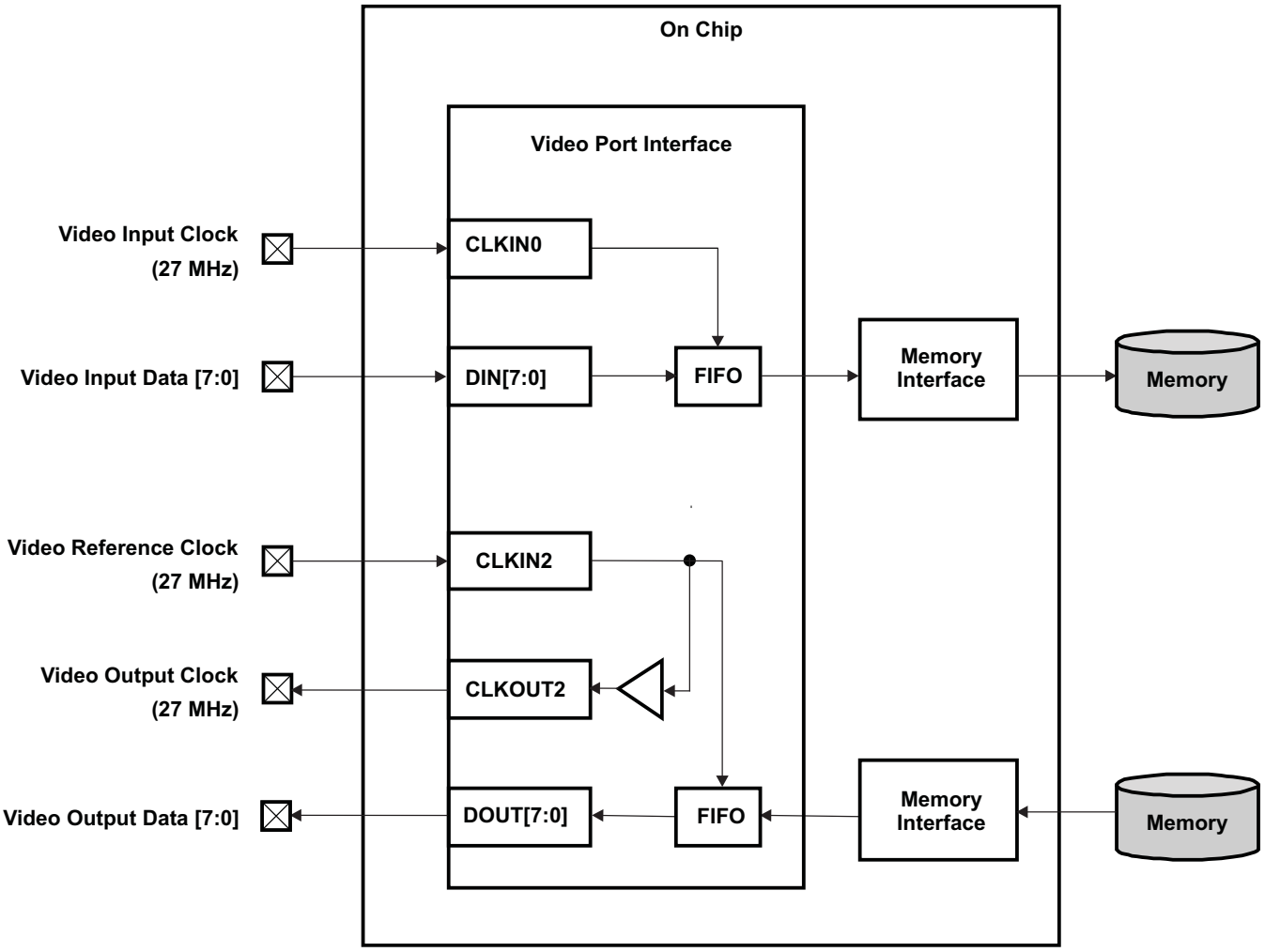
2.15.1.1 Parameter Configuration for BT.656 Mode

The configuration for each register in BT.656 mode is shown in Table 5.

Table 5. Register Configuration on BT.656 Input/Output (Unit Size = Byte in unsigned)

Parameter	Register	Bit Name	NTSC	PAL
EAV2SAV	C*n*HCFG	EAV2SAV	268	280
SAV2EAV	C*n*HCFG	SAV2EAV	1440	1440
Vertical frame size	C*n*VSIZE	VSIZE	525	625
L1	C*n*VCFG0	L1	4	1
L3	C*n*VCFG0	L3	20	23
L5	C*n*VCFG1	L5	264	311
L7	C*n*VCFG1	L7	266	313
L9	C*n*VCFG2	L9	283	336
L11	C*n*VCFG2	L11	1	624

Figure 20. Clock Control on Video Input and Output with SDTV Encoding



2.15.2 BT.1120 Mode

The BT.1120 format is necessary to support HDTV input and output for the VPIF. The BT.1120 mode requires an input clock source of 74.25 MHZ. Two VPIF channels are necessary to receive (encode) an input image and to display (local decode) the output image. The functional image and clock control is shown in Figure 21. In this case, VPIF channels 0 and 1 are used for input and VPIF channels 2 and 3 are used for output.

2.15.2.1 Parameter Configuration for BT.1120 Mode (1125/60/2:1 and 1250/50/2:1 system)

The configuration for each register in BT.1120 mode (1125/60/2:1 and 1250/50/2:1 system) is shown in Table 6.

Table 6. Register Configuration on BT.1120 (1125/60/2:1 and 1250/50/2:1 System) Input/Output (Unit Size = Byte in unsigned)

Parameter	Register	Bit Name	NTSC	PAL
EAV2SAV	C*n*HCFG	EAV2SAV	272	376
SAV2EAV	C*n*HCFG	SAV2EAV	1920	1920
Vertical frame size	C*n*VSIZE	VSIZE	1125	1250
L1	C*n*VCFG0	L1	1	1
L3	C*n*VCFG0	L3	41	45
L5	C*n*VCFG1	L5	558	621
L7	C*n*VCFG1	L7	564	626
L9	C*n*VCFG2	L9	603	670
L11	C*n*VCFG2	L11	1121	1246

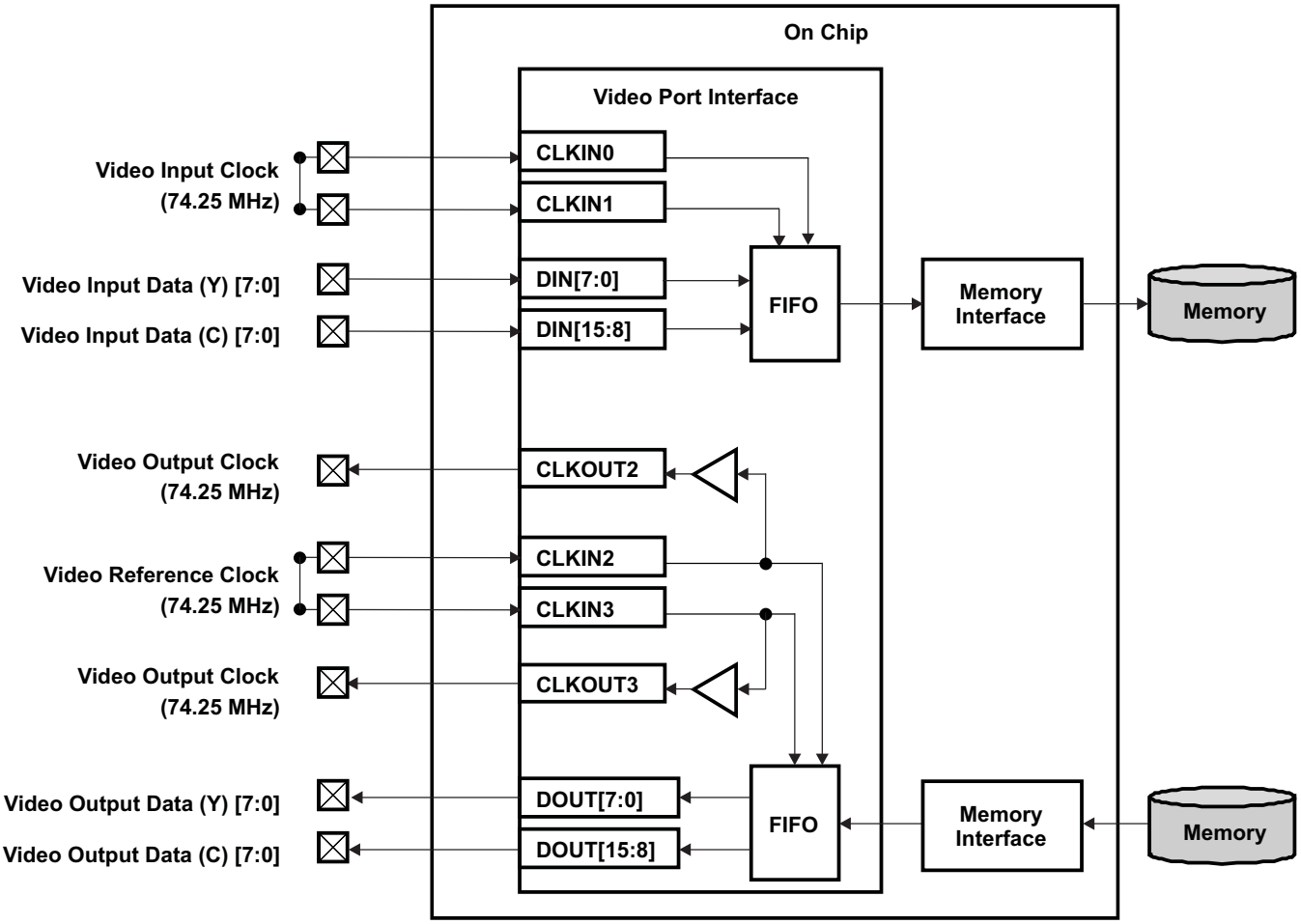
2.15.2.2 Parameter Configuration for BT.1120 Mode (1080-30p system)

The configuration for each register in BT.1120 mode (1080-30p system) is shown in Table 7.

Table 7. Register Configuration on BT.1120 (1080-30p System) Input/Output (Unit Size = Byte in unsigned)

Parameter	Register	Bit Name	Value
EAV2SAV	C*n*HCFG	EAV2SAV	272
SAV2EAV	C*n*HCFG	SAV2EAV	1920
Vertical frame size	C*n*VSIZE	VSIZE	1125
L1	C*n*VCFG0	L1	1
L3	C*n*VCFG0	L3	42
L5	C*n*VCFG1	L5	1122

Figure 21. Clock Control on Video Input and Output with HDTV Encoding



2.15.3 SMPTE 296M Mode

The SMPTE 296M mode requires the same clock control for the VPIF module as in BT.656 and BT.1120 modes. The video input clock source is 74.25 MHZ. Two VPIFs are necessary to receive an input image and to display the output image. The functional image and clock control is shown in Figure 22. In this case, VPIF channels 0 and 1 are used for input and VPIF channels 2 and 3 are used for output.

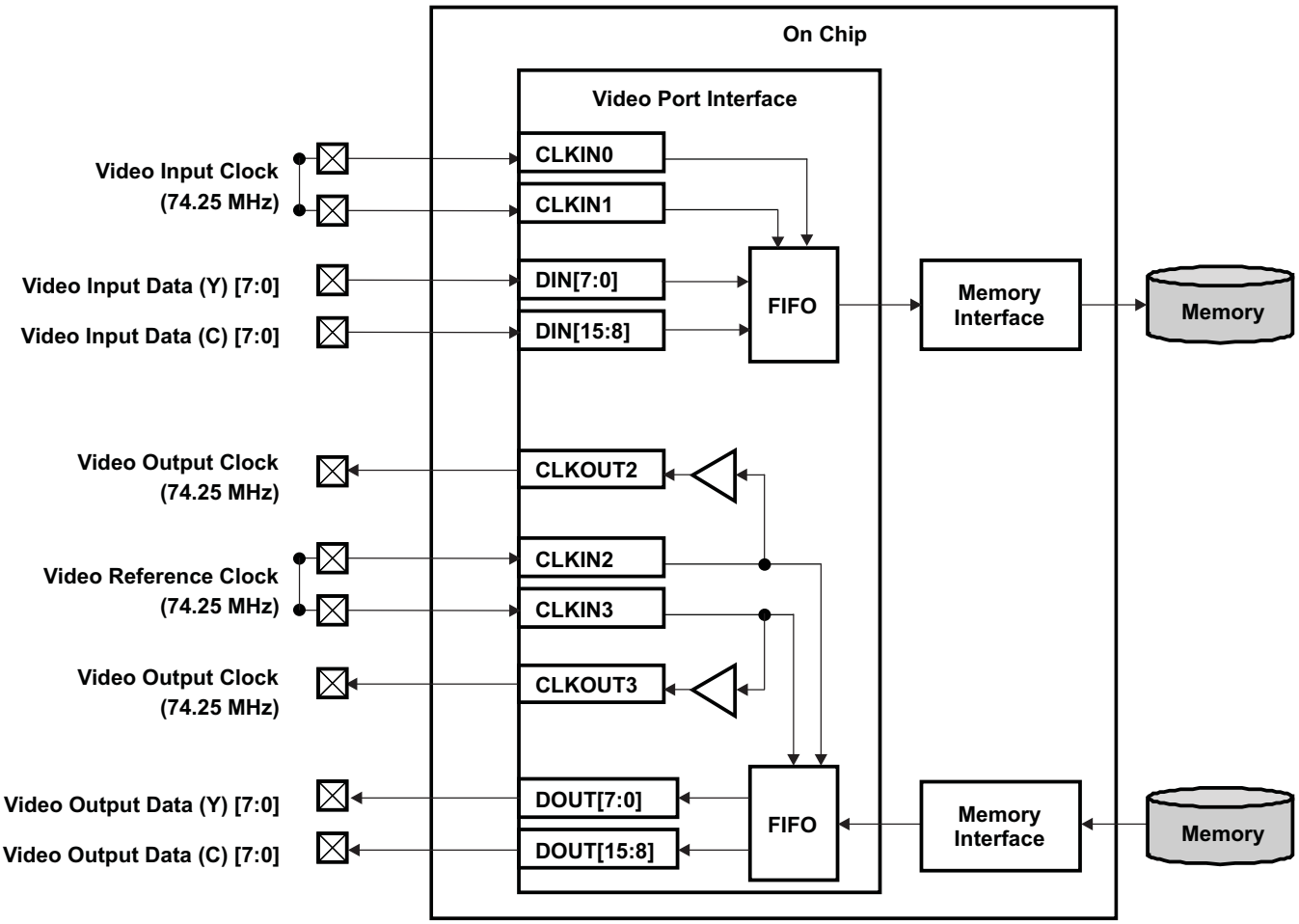
2.15.3.1 Parameter Configuration for SMPTE 296M Mode

The configuration for each register in SMPTE 296M mode is shown in Table 8.

Table 8. Register Configuration on SMPTE 296M Input/Output (Unit Size = Byte in unsigned)

Parameter	Register	Bit Name	Value
EAV2SAV	C*n*HCFG	EAV2SAV	362
SAV2EAV	C*n*HCFG	SAV2EAV	1280
Vertical frame size	C*n*VSIZE	VSIZE	750
L1	C*n*VCFG0	L1	1
L3	C*n*VCFG0	L3	26
L5	C*n*VCFG1	L5	746

Figure 22. Clock Control on Video Input and Output with HDTV Encoding



2.15.4 Raw Capture Mode

The raw capture mode requires the same input clock for VPIF channel 0 and channel 1 (clock skew has to be aligned). A single clock signal should be connected to both VP_CLKIN0 and VP_CLKIN1.

2.15.4.1 Parameter Configuration for Raw Capture Mode

When the VPIF sets the raw capture mode, the VPIF recognizes the image size automatically using the H/V valid signals. You do not need to configure the image size in the following registers:

- channel *n* horizontal data size configuration register (C*n*HCFG)
- channel *n* vertical data size configuration 0 register (C*n*VCFG0)
- channel *n* vertical data size configuration 1 register (C*n*VCFG1)
- channel *n* vertical image size register (C*n*VSIZE)

However, you still need to configure the storage memory address control related registers.

3 Registers

All register values should be configured before you set the C*n*EN bit in the channel *n* control register (C*n*CTRL) to 1. Also note that all register values except the C*n*EN bit in C*n*CTRL are detected by the first falling edge of the vertical synchronization signal on each channel as shown in Figure 23.

Table 9 lists the memory-mapped registers for the video port interface (VPIF). See the device-specific data manual for the memory address of these registers.

Figure 23. Relationship Between Register and Data Access

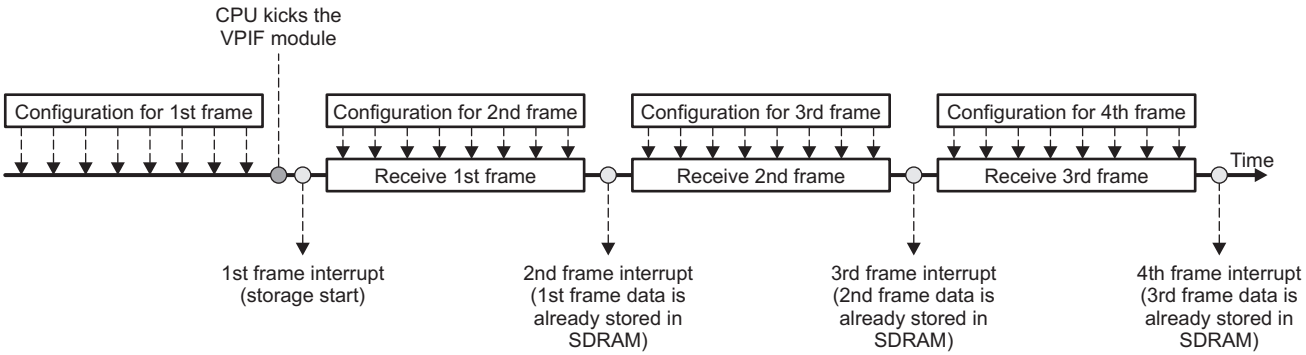


Table 9. Video Port Interface (VPIF) Registers

Offset	Acronym	Register Description	Section
0h	REVID	VPIF Revision ID Register	Section 3.1
4h	C0CTRL	Channel 0 control register	Section 3.2
8h	C1CTRL	Channel 1 control register	Section 3.3
Ch	C2CTRL	Channel 2 control register	Section 3.4
10h	C3CTRL	Channel 3 control register	Section 3.5
20h	INTEN	Interrupt enable register	Section 3.6
24h	INTSET	Interrupt enable set register	Section 3.7
28h	INTCLR	Interrupt enable clear register	Section 3.8
2Ch	INTSTAT	Interrupt status register	Section 3.9
30h	INTSTATCLR	Interrupt status clear register	Section 3.10
34h	EMUCTRL	Emulation suspend control register	Section 3.11
38h	REQSIZE	DMA size control register	Section 3.12

Table 9. Video Port Interface (VPIF) Registers (continued)

Offset	Acronym	Register Description	Section
		Channel 0	
40h	C0TLUMA	Channel 0 top field luminance address register	Section 3.13
44h	C0BLUMA	Channel 0 bottom field luminance address register	Section 3.14
48h	C0TCHROMA	Channel 0 top field chrominance address register	Section 3.15
4Ch	C0BCHROMA	Channel 0 bottom field chrominance address register	Section 3.16
50h	C0THANC	Channel 0 top field horizontal ancillary address register	Section 3.17
54h	C0BHANC	Channel 0 bottom field horizontal ancillary address register	Section 3.18
58h	C0TVANC	Channel 0 top field vertical ancillary address register	Section 3.19
5Ch	C0BVANC	Channel 0 bottom field vertical ancillary address register	Section 3.20
60h	Reserved	Reserved	
64h	C0IMGOFFSET	Channel 0 image data address offset register	Section 3.21
68h	C0HANCOFFSET	Channel 0 horizontal ancillary address offset register	Section 3.22
6Ch	C0HCFG	Channel 0 horizontal data size configuration register	Section 3.23
70h	C0VCFG0	Channel 0 vertical data size configuration 0 register	Section 3.24
74h	C0VCFG1	Channel 0 vertical data size configuration 1 register	Section 3.25
78h	C0VCFG2	Channel 0 vertical data size configuration 2 register	Section 3.26
7Ch	C0VSIZE	Channel 0 vertical image size register	Section 3.27
		Channel 1	
80h	C1TLUMA	Channel 1 top field luminance address register	Section 3.13
84h	C1BLUMA	Channel 1 bottom field luminance address register	Section 3.14
88h	C1TCHROMA	Channel 1 top field chrominance address register	Section 3.15
8Ch	C1BCHROMA	Channel 1 bottom field chrominance address register	Section 3.16
90h	C1THANC	Channel 1 top field horizontal ancillary address register	Section 3.17
94h	C1BANC	Channel 1 bottom field horizontal ancillary address register	Section 3.18
98h	C1TVANC	Channel 1 top field vertical ancillary address register	Section 3.19
9Ch	C1BVANC	Channel 1 bottom field vertical ancillary address register	Section 3.20
A0h	Reserved	Reserved	
A4h	C1IMGOFFSET	Channel 1 image data address offset register	Section 3.21
A8h	C1HANCOFFSET	Channel 1 horizontal ancillary address offset register	Section 3.22
ACh	H1HCFG	Channel 1 horizontal data size configuration register	Section 3.23
B0h	C1VCFG1	Channel 1 vertical data size configuration 0 register	Section 3.24
B4h	C1VCFG1	Channel 1 vertical data size configuration 1 register	Section 3.25
B8h	C1VCFG2	Channel 1 vertical data size configuration 2 register	Section 3.26
BCh	C1VSIZE	Channel 1 vertical image size register	Section 3.27
		Channel 2	
C0h	C2TLUMA	Channel 2 top field luminance address register	Section 3.13
C4h	C2BLUMA	Channel 2 bottom field luminance address register	Section 3.14
C8h	C2TCHROMA	Channel 2 top field chrominance address register	Section 3.15
CCh	C2BCHROMA	Channel 2 bottom field chrominance address register	Section 3.16
D0h	C2THANC	Channel 2 top field horizontal ancillary address register	Section 3.17
D4h	C2BHANC	Channel 2 bottom field horizontal ancillary address register	Section 3.18
D8h	C2TVANC	Channel 2 top field vertical ancillary address register	Section 3.19
DCh	C2BVANC	Channel 2 bottom field vertical ancillary address register	Section 3.20
E0h	Reserved	Reserved	
E4h	C2IMGOFFSET	Channel 2 image data address offset register	Section 3.21
E8h	C2HANCOFFSET	Channel 2 horizontal ancillary address offset register	Section 3.22
ECh	C2HCFG	Channel 2 horizontal data size configuration register	Section 3.28

Table 9. Video Port Interface (VPIF) Registers (continued)

Offset	Acronym	Register Description	Section
F0h	C2VCFG0	Channel 2 vertical data size configuration 0 register	Section 3.29
F4h	C2VCFG1	Channel 2 vertical data size configuration 1 register	Section 3.30
F8h	C2VCFG2	Channel 2 vertical data size configuration 2 register	Section 3.31
FCh	C2VSIZE	Channel 2 vertical image size register	Section 3.32
100h	C2THANCPOS	Channel 2 top field horizontal ancillary data insertion start position register	Section 3.33
104h	C2THANCSIZE	Channel 2 top field horizontal ancillary data size register	Section 3.34
108h	C2BHANCPOS	Channel 2 bottom field horizontal ancillary data insertion start position register	Section 3.35
10Ch	C2BHANCSIZE	Channel 2 bottom field horizontal ancillary data size register	Section 3.36
110h	C2TVANCPOS	Channel 2 top field vertical ancillary data insertion start position register	Section 3.37
114h	C2TVANCSIZE	Channel 2 top field vertical ancillary data size register	Section 3.38
118h	C2BVANCPOS	Channel 2 bottom field vertical ancillary data insertion start position register	Section 3.39
11Ch	C2BVANCSIZE	Channel 2 bottom field vertical ancillary data size register	Section 3.40
		Channel 3	
140h	C3TLUMA	Channel 3 top field luminance address register	Section 3.13
144h	C3BLUMA	Channel 3 bottom field luminance address register	Section 3.14
148h	C3TCHROMA	Channel 3 top field chrominance address register	Section 3.15
14Ch	C3BCHROMA	Channel 3 bottom field chrominance address register	Section 3.16
150h	C3THANC	Channel 3 top field horizontal ancillary address register	Section 3.17
154h	C3BHANC	Channel 3 bottom field horizontal ancillary address register	Section 3.18
158h	C3TVANC	Channel 3 top field vertical ancillary address register	Section 3.19
15Ch	C3BVANC	Channel 3 bottom field vertical ancillary address register	Section 3.20
160h	Reserved	Reserved	
164h	C3IMGOFFSET	Channel 3 image data address offset register	Section 3.21
168h	C3HANCOFFSET	Channel 3 horizontal ancillary address offset register	Section 3.22
16Ch	C3HCFG	Channel 3 horizontal data size configuration register	Section 3.28
170h	C3VCFG0	Channel 3 vertical data size configuration 0 register	Section 3.29
174h	C3VCFG1	Channel 3 vertical data size configuration 1 register	Section 3.30
178h	C3VCFG2	Channel 3 vertical data size configuration 2 register	Section 3.31
17Ch	C3VSIZE	Channel 3 vertical image size register	Section 3.32
180h	C3THANCPOS	Channel 3 top field horizontal ancillary data insertion start position register	Section 3.33
184h	C3THANCSIZE	Channel 3 top field horizontal ancillary data size register	Section 3.34
188h	C3BHANCPOS	Channel 3 bottom field horizontal ancillary data insertion start position register	Section 3.35
18Ch	C3BHANCSIZE	Channel 3 bottom field horizontal ancillary data size register	Section 3.36
190h	C3TVANCPOS	Channel 3 top field vertical ancillary data insertion start position register	Section 3.37
194h	C3TVANCSIZE	Channel 3 top field vertical ancillary data size register	Section 3.38
198h	C3BVANCPOS	Channel 3 bottom field vertical ancillary data insertion start position register	Section 3.39
19Ch	C3BVANCSIZE	Channel 3 bottom field vertical ancillary data size register	Section 3.40

3.1 VPIF Revision Register ID (REVID)

The VPIF peripheral Revision ID Register (REVID) is shown in Figure 24 and described in Table 10.

Figure 24. VPIF Revision ID Register (REVID)

31	0
REV	
R-4C08h 0A01h	

LEGEND: R = Read only; -*n* = value after reset

Table 10. VPIF Revision ID Register (REVID) Field Descriptions

Bit	Field	Value	Description
31-0	REV	4C08 0A01h	VPIF Revision

3.2 Channel 0 Control Register (C0CTRL)

The channel 0 control register (C0CTRL) is shown in Figure 25 and described in Table 11.

Figure 25. Channel 0 Control Register (C0CTRL)

31	30	29 28	27 16
CLKEDGE	Rsvd	DATAWIDTH	INTLINE
R/W-0	R-0	R/W-0	R/W-0

15	14	13	12	11	10	9	8
FIDINV	VVINV	HVINV	FIELDFRAME	Reserved	INTRPROG	VANC	HANC
R/W-0	R/W-0	R/W-0	R/W-0	R-0	R/W-0	R/W-0	R/W-0

7	6	5	4	3	2	1	0
INTFRAME		FID	Reserved	YCMUX	CAPMODE	Reserved	CHANEN
R/W-0		R-0	R-0	R/W-0	R/W-0	R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 11. Channel 0 Control Register (C0CTRL) Field Descriptions

Bit	Field	Value	Description
31	CLKEDGE		Clock edge control.
		0	Data is captured on rising edge of input clock.
		1	Data is captured on falling edge of input clock.
30	Reserved	0	Reserved
29-28	DATAWIDTH	0-3h	Data bit width. The DATAWIDTH bit is only used with the CCD/CMOS data capture mode (CAPMODE = 1h).
		0	8 bits/pixel
		1h	10 bits/pixel
		2h	12 bits/pixel
		3h	Reserved
27-16	INTLINE	0-FFFh	Line interrupt interval for CCD/CMOS capture mode. In CCD/CMOS capture mode, the frame interrupt signal is asserted to the CPU at the end of INTLINE interval lines. A value of 0 is invalid in CCD/CMOS capture mode. The INTLINE bit is only used with the CCD/CMOS capture mode (CAPMODE = 1h).
15	FIDINV		Field ID polarity inverting control bit. The FIDINV bit is only used with the CCD/CMOS data capture mode (CAPMODE = 1h).
		0	No inversion.
		1	Invert incoming field ID signal inside the VPIF.

Table 11. Channel 0 Control Register (C0CTRL) Field Descriptions (continued)

Bit	Field	Value	Description
14	VVINV		Vertical pixel valid signal polarity control. The VVINV bit is only used with the CCD/CMOS data capture mode (CAPMODE = 1h).
		0	No inversion.
		1	Invert incoming vertical pixel valid signal inside the VPIF.
13	HVINV		Horizontal pixel valid signal polarity control. The HVINV bit is only used with the CCD/CMOS data capture mode (CAPMODE = 1h).
		0	No inversion.
		1	Invert incoming horizontal pixel valid signal inside the VPIF.
12	FIELDFRAME		Memory storage mode of input picture. Note that for progressive video, only the frame-based storage method is supported.
		0	Field-based storage
		1	Frame-based storage
11	Reserved	0	Reserved
10	INTRPROG		Output display format.
		0	Interlaced
		1	Progressive
9	VANC		Channel 0 vertical ancillary data enable. Ancillary data is only supported for BT byte streams.
		0	Vertical ancillary data is disabled.
		1	Vertical ancillary data is enabled.
8	HANC		Channel 0 horizontal ancillary data enable. Ancillary data is only supported for BT byte streams.
		0	Horizontal ancillary data is disabled.
		1	Horizontal ancillary data is enabled.
7-6	INTFRAME	0-3h	Channel 0 frame interrupt to CPU for BT/YC and CCD/CMOS capture modes.
		0	Top field V-sync only.
		1h	Bottom field V-sync only. Interlaced format only.
		2h	Top and bottom field V-sync. Interlaced format only.
		3h	Reserved
5	FID		Channel 0 field identification. This bit indicates the active field ID when the FRAME0 interrupt is asserted from VPIF to the CPU.
		0	Top field
		1	Bottom field
4	Reserved	0	Reserved
3	YCMUX		Channel 0 input data format.
		0	Channel 0 Y/C non-multiplexed mode.
		1	Channel 0 Y/C multiplexed mode.
2	CAPMODE		Channel 0 data capture mode. This value must match the channel 1 data capture mode (CAPMODE bit in C1CTRL).
		0	BT video (Y/C format) capture mode.
		1	CCD/CMOS data capture mode.
1	Reserved	0	Reserved
0	CHANEN		VPIF channel 0 enable.
		0	Channel 0 is disabled.
		1	Channel 0 is enabled.

3.3 Channel 1 Control Register (C1CTRL)

The channel 1 control register (C1CTRL) is shown in Figure 26 and described in Table 12.

Figure 26. Channel 1 Control Register (C1CTRL)

31	30	16
CLKEDGE	Reserved	
R/W-0	R-0	

15	11	10	9	8
Reserved		INTRPROG	VANC	HANC
R-0		R/W-0	R/W-0	R/W-0

7	6	5	4	3	2	1	0
INTFRAME		FID	Reserved	YCMUX	CAPMODE	Reserved	CHANEN
R/W-0		R-0	R-0	R/W-0	R/W-0	R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 12. Channel 1 Control Register (C1CTRL) Field Descriptions

Bit	Field	Value	Description
31	CLKEDGE		Clock edge control.
		0	Data is captured on rising edge of input clock.
		1	Data is captured on falling edge of input clock.
30-11	Reserved	0	Reserved
10	INTRPROG		Output display format.
		0	Interlaced
		1	Progressive
9	VANC		Channel 1 vertical ancillary data enable. Ancillary data is only supported for BT byte streams.
		0	Vertical ancillary data is disabled.
		1	Vertical ancillary data is enabled.
8	HANC		Channel 1 horizontal ancillary data enable. Ancillary data is only supported for BT byte streams.
		0	Horizontal ancillary data is disabled.
		1	Horizontal ancillary data is enabled.
7-6	INTFRAME	0-3h	Channel 1 frame interrupt to CPU for BT/YC and CCD/CMOS capture modes.
		0	Top field V-sync only.
		1h	Bottom field V-sync only. Interlaced format only.
		2h	Top and bottom field V-sync. Interlaced format only.
		3h	Reserved
5	FID		Channel 1 field identification. This bit indicates the active field ID when the FRAME1 interrupt is asserted from VPIF to CPU.
		0	Top field.
		1	Bottom field.
4	Reserved	0	Reserved
3	YCMUX		Channel 1 input data format.
		0	Channel 1 Y/C non-multiplexed mode.
		1	Channel 0 Y/C multiplexed mode.
2	CAPMODE		Channel 1 data capture mode. This value must match the channel 0 data capture mode (CAPMODE bit in C0CTRL).
		0	BT video (Y/C format) capture mode.
		1	CCD/CMOS data capture mode.
1	Reserved	0	Reserved

Table 12. Channel 1 Control Register (C1CTRL) Field Descriptions (continued)

Bit	Field	Value	Description
0	CHANEN		VPIF channel 1 enable.
		0	Channel 1 is disabled.
		1	Channel 1 is enabled.

3.4 Channel 2 Control Register (C2CTRL)

The channel 2 control register (C2CTRL) is shown in Figure 27 and described in Table 13.

Figure 27. Channel 2 Control Register (C2CTRL)

31	30						16
CLKEDGE	Reserved						
R/W-0	R-0						

15	14	13	12	11	10	9	8
Reserved	CLIPANC	CLIPVID	FIELDFRAME	INTRPROG	PIXEL	VANC	HANC
R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

7	6	5	4	3	2	1	0
INTFRAME		FID	Reserved	YCMUX	Reserved	CLKEN	CHANEN
R/W-0		R-0	R-0	R/W-0	R-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 13. Channel 2 Control Register (C2CTRL) Field Descriptions

Bit	Field	Value	Description
31	CLKEDGE		Clock edge control
		0	Data is output on rising edge of output clock.
		1	Data is output on falling edge of output clock. The output clock controlled by the CLKEN bit will be inverted.
30-15	Reserved	0	Reserved
14	CLIPANC		Activates clipping function of output data in the blanking region for channel 2.
		0	Clipping in the blanking region for channel 2 is disabled.
		1	Clipping in the blanking region for channel 2 is enabled. (0 is clipped to 1; FFh is clipped to FEh)
13	CLIPVID		Activates clipping function of output data in the active region for channel 2.
		0	Clipping in the active region for channel 2 is disabled.
		1	Clipping in the active region for channel 2 is enabled. (0 is clipped to 1; FFh is clipped to FEh)
12	FIELDFRAME		Memory storage mode of output picture. Note that this bit is effective only when the INTRPROG bit is 0 (interlaced). In progressive mode, only the frame-based storage method is supported.
		0	Field-based storage
		1	Frame-based storage
11	INTRPROG		Output display format.
		0	Interlaced
		1	Progressive
10	PIXEL		Enables the display of video pixels.
		0	Pixel data is disabled. Blank pixels are displayed (Y = 10h and C = 80h).
		1	Pixel data is enabled. Pixel data from memory is displayed.
9	VANC		Channel 2 vertical ancillary data enable. Ancillary data is only supported for BT byte streams.
		0	Vertical ancillary data is disabled.
		1	Vertical ancillary data is enabled.

Table 13. Channel 2 Control Register (C2CTRL) Field Descriptions (continued)

Bit	Field	Value	Description
8	HANC		Channel 2 horizontal ancillary data enable. Ancillary data is only supported for BT byte streams.
		0	Horizontal ancillary data is disabled.
		1	Horizontal ancillary data is enabled.
7-6	INTFRAME	0-3h	Channel 2 frame level interrupt to CPU.
		0	Top field V-sync only.
		1h	Bottom field V-sync
		2h	Top and bottom field.
		3h	Reserved
5	FID		Channel 2 field identification. This bit indicates the active field ID when the FRAME2 interrupt is asserted from the VPIF to CPU.
		0	Top field.
		1	Bottom field.
4	Reserved	0	Reserved
3	YCMUX		Channel 2 output data format.
		0	Channel 2 Y/C non-multiplexed mode.
		1	Channel 2 Y/C multiplexed mode (both Y and C are in the byte stream).
2	Reserved	0	Reserved
1	CLKEN		Clock output enable control for VPIF channel 2. This bit should be set before enabling the channel and it should be cleared after deactivating the channel.
		0	VPIF channel 2 clock is disabled.
		1	VPIF channel 2 clock is enabled.
0	CHANEN		VPIF channel 2 enable.
		0	Channel 2 is disabled.
		1	Channel 2 is enabled.

3.5 Channel 3 Control Register (C3CTRL)

The channel 3 control register (C3CTRL) is shown in Figure 28 and described in Table 14.

Figure 28. Channel 3 Control Register (C3CTRL)

31	30						16
CLKEDGE	Reserved						
R/W-0	R-0						

15	14	13	12	11	10	9	8
Reserved	CLIPANC	CLIPVID	Reserved	INTRPROG	PIXEL	VANC	HANC
R-0	R/W-0	R/W-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0

7	6	5	4	3	2	1	0
INTFRAME		FID	Reserved	YCMUX	Reserved	CLKEN	CHANEN
R/W-0		R-0	R-0	R/W-0	R-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 14. Channel 3 Control Register (C3CTRL) Field Descriptions

Bit	Field	Value	Description
31	CLKEDGE		Clock edge control
		0	Data is output on rising edge of output clock.
		1	Data is output on falling edge of output clock. The output clock controlled by the CLKEN bit will be inverted.
30-15		0	Reserved
14	CLIPANC		Activates clipping function of output data in the blanking region for channel 3.
		0	Clipping in the blanking region for channel 3 is disabled.
		1	Clipping in the blanking region for channel 3 is enabled. (0 is clipped to 1; FFh is clipped to FEh)
13	CLIPVID		Activates clipping function of output data in the active region for channel 3.
		0	Clipping in the active region for channel 3 is disabled.
		1	Clipping in the active region for channel 3 is enabled. (0 is clipped to 1; FFh is clipped to FEh)
12	Reserved	0	Reserved
11	INTRPROG		Output display format.
		0	Interlaced
		1	Progressive
10	PIXEL		Enables the display of video pixels.
		0	Pixel data is disabled. Blank pixels are displayed (Y = 10h and C = 80h).
		1	Pixel data is enabled. Pixel data from memory is displayed.
9	VANC		Channel 3 vertical ancillary data enable. Ancillary data is only supported for BT byte streams.
		0	Vertical ancillary data is disabled.
		1	Vertical ancillary data is enabled.
8	HANC		Channel 3 horizontal ancillary data enable. Ancillary data is only supported for BT byte streams.
		0	Horizontal ancillary data is disabled.
		1	Horizontal ancillary data is enabled.
7-6	INTFRAME	0-3h	Channel 3 frame level interrupt to CPU.
		0	Top field V-sync only.
		1h	Bottom field V-sync.
		2h	Top and bottom field.
		3h	Reserved

Table 14. Channel 3 Control Register (C3CTRL) Field Descriptions (continued)

Bit	Field	Value	Description
5	FID		Channel 3 field identification. This bit indicates the active field ID when the FRAME3 interrupt is asserted from the VPIF to CPU.
		0	Top field.
		1	Bottom field.
4	Reserved	0	Reserved
3	YCMUX		Channel 3 output data format.
		0	Channel 3 Y/C non-multiplexed mode.
		1	Channel 3 Y/C multiplexed mode (both Y and C are in the byte stream).
2	Reserved	0	Reserved
1	CLKEN		Clock output enable control for VPIF channel 3. This bit should be set before enabling the channel and it should be cleared after deactivating the channel.
		0	VPIF channel 3 clock is disabled.
		1	VPIF channel 3 clock is enabled.
0	CHANEN		VPIF channel 3 enable.
		0	Channel 3 is disabled.
		1	Channel 3 is enabled.

3.6 Interrupt Enable Register (INTEN)

The interrupt enable register (INTEN) is shown in Figure 29 and described in Table 15.

Figure 29. Interrupt Enable Register (INTEN)

31	16
Reserved	
R-0	

15	8
Reserved	
R-0	

7	4	3	2	1	0
Reserved	ERROR	FRAME3	FRAME2	FRAME1	FRAME0
R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

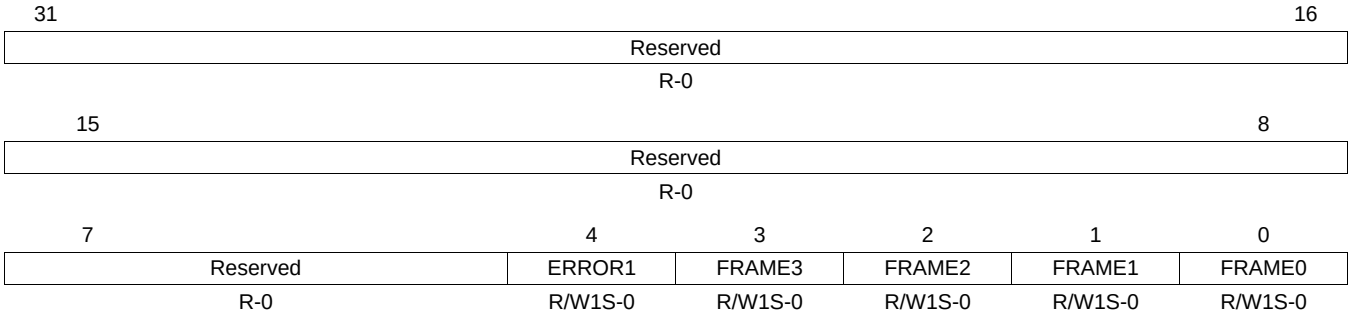
Table 15. Interrupt Enable Register (INTEN) Field Descriptions

Bit	Field	Value	Description
31-5	Reserved	0	Reserved
4	ERROR		VPIF error interrupt enable. The error interrupt is asserted when an problem is detected in any input/output byte stream data.
		0	Error interrupt is disabled.
		1	Error interrupt is enabled. The ERROR bit in the INTSET register must also be set to activate the ERROR interrupt.
3	FRAME3		Channel 3 frame interrupt enable. Enables the frame interrupt from the VPIF to CPU.
		0	Channel 3 frame interrupt is disabled.
		1	Channel 3 frame interrupt is enabled. The FRAME3 bit in the INTSET register must also be set to activate the FRAME3 interrupt.
2	FRAME2		Channel 2 frame interrupt enable. Enables the frame interrupt from the VPIF to CPU.
		0	Channel 2 frame interrupt is disabled.
		1	Channel 2 frame interrupt is enabled. The FRAME2 bit in the INTSET register must also be set to activate the FRAME2 interrupt.
1	FRAME1		Channel 1 frame interrupt enable. Enables the frame interrupt in BT/YC capture mode, or enables the line interval interrupt in CCD/CMOS capture mode.
		0	Channel 1 frame interrupt is disabled.
		1	Channel 1 frame interrupt is enabled. The FRAME1 bit in the INTSET register must also be set to activate the FRAME1 interrupt.
0	FRAME0		Channel 0 frame interrupt enable. Enables the frame interrupt in BT/YC capture mode, or enables the line interval interrupt in CCD/CMOS capture mode.
		0	Channel 0 frame interrupt is disabled.
		1	Channel 0 frame interrupt is enabled. The FRAME0 bit in the INTSET register must also be set to activate the FRAME0 interrupt.

3.7 Interrupt Enable Set Register (INTSET)

The interrupt enable set register (INTSET) is shown in Figure 30 and described in Table 16.

Figure 30. Interrupt Enable Set Register (INTSET)



LEGEND: R/WS = Read/Write 1 to Set; R = Read only; -*n* = value after reset

Table 16. Interrupt Enable Set Register (INTSET) Field Descriptions

Bit	Field	Value	Description
31-5	Reserved	0	Reserved
4	ERROR		Error interrupt enable set.
		0	Interrupt on ERROR is masked (write 0 has no effect).
		1	Interrupt on ERROR is activated.
3	FRAME3		Channel 3 frame interrupt enable set.
		0	Interrupt on FRAME3 is masked (write 0 has no effect).
		1	Interrupt on FRAME3 is activated.
2	FRAME2		Channel 2 frame interrupt enable set.
		0	Interrupt on FRAME2 is masked (write 0 has no effect).
		1	Interrupt on FRAME2 is activated.
1	FRAME1		Channel 1 frame interrupt enable set.
		0	Interrupt on FRAME1 is masked (write 0 has no effect).
		1	Interrupt on FRAME1 is activated.
0	FRAME0		Channel 0 frame interrupt enable set.
		0	Interrupt on FRAME0 is masked (write 0 has no effect).
		1	Interrupt on FRAME0 is activated.

3.8 Interrupt Enable Clear Register (INTCLR)

The interrupt enable clear register (INTCLR) is shown in Figure 31 and described in Table 17.

Figure 31. Interrupt Enable Clear Register (INTCLR)

31	16
Reserved	
R-0	

15	8
Reserved	
R-0	

7	4	3	2	1	0
Reserved	ERROR	FRAME3	FRAME2	FRAME1	FRAME0
R-0	W1C-0	W1C-0	W1C-0	W1C-0	W1C-0

LEGEND: R = Read only; W1C = Write 1 to Clear; -*n* = value after reset

Table 17. Interrupt Enable Clear Register (INTCLR) Field Descriptions

Bit	Field	Value	Description
31-5	Reserved	0	Reserved
4	ERROR		Error interrupt enable clear.
		0	No change (write 0 has no effect.).
		1	Interrupt on ERROR is masked
3	FRAME3		Channel 3 frame interrupt enable clear.
		0	No change (write 0 has no effect).
		1	Interrupt on FRAME3 is masked.
2	FRAME2		Channel 2 frame interrupt enable clear.
		0	No change (write 0 has no effect).
		1	Interrupt on FRAME2 is masked.
1	FRAME1		Channel 1 frame interrupt enable clear.
		0	No change (write 0 has no effect).
		1	Interrupt on FRAME1 is masked.
0	FRAME0		Channel 0 frame interrupt enable clear.
		0	No change (write 0 has no effect).
		1	Interrupt on FRAME0 is masked.

3.9 Interrupt Status Register (INTSTAT)

The interrupt status register (INTSTAT) is shown in Figure 32 and described in Table 18.

Figure 32. Interrupt Status Register (INTSTAT)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
R-0															

15	14	13	12	11	10	9	8
Reserved							
R-0							

7	6	5	4	3	2	1	0
Reserved			ERROR	FRAME3	FRAME2	FRAME1	FRAME0
R-0			R-0	R-0	R-0	R-0	R-0

LEGEND: R = Read only; -*n* = value after reset

Table 18. Interrupt Status Register (INTSTAT) Field Descriptions

Bit	Field	Value	Description
31-5	Reserved	0	Reserved
4	ERROR		Error interrupt status. This bit is effective even if the ERROR bit in INTEN is disabled. Use the INTSTATCLR register to clear the status.
		0	No error detected.
		1	Error detected.
3	FRAME3		Channel 3 frame interrupt status. This bit is effective even if the FRAME3 bit in INTEN is disabled. Use the INTSTATCLR register to clear the status.
		0	Frame sync on channel 3 not detected.
		1	Frame sync on channel 3 detected.
2	FRAME2		Channel 2 frame interrupt status. This bit is effective even if the FRAME2 bit in INTEN is disabled. Use the INTSTATCLR register to clear the status.
		0	Frame sync on channel 2 not detected.
		1	Frame sync on channel 2 detected.
1	FRAME1		Channel 1 frame or line interval interrupt status. This bit is effective even if the FRAME1 bit in INTEN is disabled. Use the INTSTATCLR register to clear the status.
		0	Frame sync or line interval on channel 1 not detected.
		1	Frame sync or line interval on channel 1 detected.
0	FRAME0		Channel 0 frame or line interval interrupt status. This bit is effective even if the FRAME0 bit in INTEN is disabled. Use the INTSTATCLR register to clear the status.
		0	Frame sync or line interval on channel 0 not detected.
		1	Frame sync or line interval on channel 0 detected.

3.10 Interrupt Status Clear Register (INTSTATCLR)

The interrupt status clear register (INTSTATCLR) is shown in Figure 33 and described in Table 19.

Figure 33. Interrupt Status Clear Register (INTSTATCLR)

31	16
Reserved	
R-0	

15	8
Reserved	
R-0	

7	4	3	2	1	0
Reserved	ERROR	FRAME3	FRAME2	FRAME1	FRAME0
R-0	W1C-0	W1C-0	W1C-0	W1C-0	W1C-0

LEGEND: R = Read only; W1C = Write 1 to Clear; -*n* = value after reset

Table 19. Interrupt Status Clear Register (INTSTATCLR) Field Descriptions

Bit	Field	Value	Description
31-5	Reserved	0	Reserved
4	ERROR		Error interrupt status clear.
		0	No change
		1	Clear ERROR bit in INTSTAT.
3	FRAME3		Channel 3 frame interrupt status clear.
		0	No change
		1	Clear FRAME3 bit in INTSTAT.
2	FRAME2		Channel 2 frame interrupt status clear.
		0	No change
		1	Clear FRAME2 bit in INTSTAT.
1	FRAME1		Channel 1 frame or line interval interrupt status clear.
		0	No change
		1	Clear FRAME1 bit in INTSTAT.
0	FRAME0		Channel 0 frame or line interval interrupt status clear.
		0	No change
		1	Clear FRAME0 bit in INTSTAT.

3.11 Emulation Suspend Control Register (EMUCTRL)

The emulation suspend control register (EMUCTRL) is shown in Figure 34 and described in Table 20.

Figure 34. Emulation Suspend Control Register (EMUCTRL)

31	16
Reserved	
R-0	

15	1	0
Reserved		FREE
R-0		R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 20. Emulation Suspend Control Register (EMUCTRL) Field Descriptions

Bit	Field	Value	Description
31-1	Reserved	0	Reserved
0	FREE		Controls whether the peripheral responds to the emulation suspend signal.
		0	Respond to monitoring emulation suspend signal.
		1	Ignores any emulation suspend signal (non-stop).

3.12 DMA Size Control Register (REQSIZE)

The DMA size control register (REQSIZE) is shown in Figure 35 and described in Table 21.

Figure 35. DMA Size Control Register (REQSIZE)

31	16
Reserved	
R-0	

15	9	8	0
Reserved		BYTES	
R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 21. DMA Size Control Register (REQSIZE) Field Descriptions

Bit	Field	Value	Description
31-9	Reserved	0	Reserved
8-0	BYTES	0-1FF	Request size for DMA data transfer from/to VPIF.
		0-1Fh	Reserved
		20h	32 bytes
		21h-3Fh	Reserved
		40h	64 bytes
		41h-7Fh	Reserved
		80h	128 bytes
		81h-FFh	Reserved
		100h	256 bytes
		101h-1FFh	Reserved

3.13 Channel *n* Top Field Luminance Address Register (CnTLUMA)

The Channel *n* Top Field Luminance Address Register (C*n*TLUMA) is shown in Figure 36 and described in Table 22.

NOTE: C1TLUMA and C3TLUMA registers are only used in Y/C multiplexed mode.

Figure 36. Channel *n* Top Field Luminance Address Register (C*n*TLUMA)

31	0
C*n*TLUMA	
R/W-0	

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 22. Channel *n* Top Field Luminance Address Register (C*n*TLUMA) Field Descriptions

Bit	Field	Value	Description
31-0	C*n*TLUMA	0-FFFF FFFFh	Memory address of the top field luminance buffer. The register value points to the beginning of the buffer, and the address must be a multiple of 8 (C*n*TLUMA[2:0] = 0).

3.14 Channel *n* Bottom Field Luminance Address Register (CnBLUMA)

The Channel *n* Bottom Field Luminance Address Register (C*n*BLUMA) is shown in Figure 37 and described in Table 23.

NOTE: C*n*BLUMA registers are not used in progressive video mode. C1BLUMA and C3BLUMA registers are only used in Y/C multiplexed mode.

Figure 37. Channel *n* Bottom Field Luminance Address Register (C*n*BLUMA)

31	0
C*n*BLUMA	
R/W-0	

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 23. Channel *n* Bottom Field Luminance Address Register (C*n*BLUMA) Field Descriptions

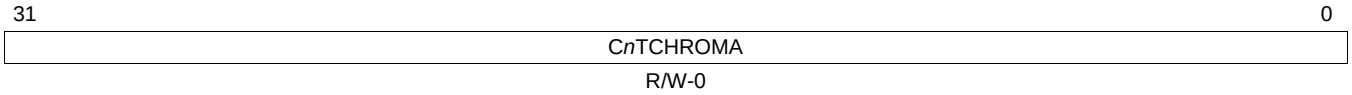
Bit	Field	Value	Description
31-0	C*n*BLUMA	0-FFFF FFFFh	Memory address of the bottom field luminance buffer. The register value points to the beginning of the buffer, and the address must be a multiple of 8 (C*n*BLUMA[2:0] = 0).

3.15 Channel *n* Top Field Chrominance Address Register (C*n*TCHROMA)

The Channel *n* Top Field Chrominance Address Register (C*n*TCHROMA) is shown in Figure 38 and described in Table 24.

NOTE: C0TCHROMA and C2TCHROMA registers are only used in Y/C multiplexed mode.

Figure 38. Channel *n* Top Field Chrominance Address Register (C*n*TCHROMA)



LEGEND: R/W = Read/Write; -*n* = value after reset

Table 24. Channel *n* Top Field Chrominance Address Register (C*n*TCHROMA) Field Descriptions

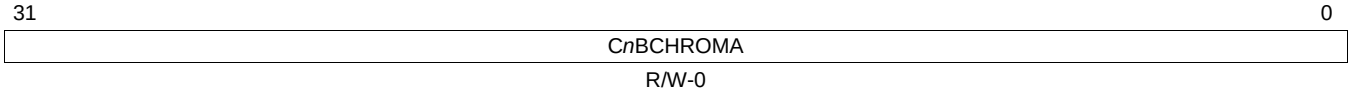
Bit	Field	Value	Description
31-0	C*n*TCHROMA	0-FFFF FFFFh	Memory address of the top field chrominance buffer. The register value points to the beginning of the buffer, and the address must be a multiple of 8 (C*n*TCHROMA[2:0] = 0).

3.16 Channel *n* Bottom Field Chrominance Address Register (C*n*BCHROMA)

The Channel *n* Bottom Field Chrominance Address Register (C*n*BCHROMA) is shown in Figure 39 and described in Table 25.

NOTE: C*n*BCHROMA registers are not used in progressive video mode. C0BCHROMA and C2BCHROMA registers are only used in Y/C multiplexed mode.

Figure 39. Channel *n* Bottom Field Chrominance Address Register (C*n*BCHROMA)



LEGEND: R/W = Read/Write; -*n* = value after reset

Table 25. Channel *n* Bottom Field Chrominance Address Register (C*n*BCHROMA) Field Descriptions

Bit	Field	Value	Description
31-0	C*n*BCHROMA	0-FFFF FFFFh	Memory address of the bottom field chrominance buffer. The register value points to the beginning of the buffer, and the address must be a multiple of 8 (C*n*BCHROMA[2:0] = 0).

3.17 Channel *n* Top Field Horizontal Ancillary Address Register (C*n*THANC)

The Channel *n* Top Field Horizontal Ancillary Address Register (C*n*THANC) is shown in Figure 40 and described in Table 26.

Figure 40. Channel *n* Top Field Horizontal Ancillary Address Register (C*n*THANC)

31	0
C*n*THANC	
R/W-0	

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 26. Channel *n* Top Field Horizontal Ancillary Address Register (C*n*THANC) Field Descriptions

Bit	Field	Value	Description
31-0	C*n*THANC	0-FFFF FFFFh	Memory address of the top field horizontal ancillary buffer. The register value points to the beginning of the buffer, and the address must be a multiple of 8 (C*n*THANC[2:0] = 0).

3.18 Channel *n* Bottom Field Horizontal Ancillary Address Register (C*n*BHANC)

The Channel *n* Bottom Field Horizontal Ancillary Address Register (C*n*BHANC) is shown in Figure 41 and described in Table 27.

NOTE: C*n*BHANC registers are not used in progressive video mode.

Figure 41. Channel *n* Bottom Field Horizontal Ancillary Address Register (C*n*BHANC)

31	0
C*n*BHANC	
R/W-0	

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 27. Channel *n* Bottom Field Horizontal Ancillary Address Register (C*n*BHANC) Field Descriptions

Bit	Field	Value	Description
31-0	C*n*BHANC	0-FFFF FFFFh	Memory address of the bottom field horizontal ancillary buffer. The register value points to the beginning of the buffer, and the address must be a multiple of 8 (C*n*BHANC[2:0] = 0).

3.19 Channel *n* Top Field Vertical Ancillary Address Register (C*n*TVANC)

The Channel *n* Top Field Vertical Ancillary Address Register (C*n*TVANC) is shown in Figure 42 and described in Table 28.

Figure 42. Channel *n* Top Field Vertical Ancillary Address Register (C*n*TVANC)

31	0
C*n*TVANC	
R/W-0	

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 28. Channel *n* Top Field Vertical Ancillary Address Register (C*n*TVANC) Field Descriptions

Bit	Field	Value	Description
31-0	C*n*TVANC	0-FFFF FFFFh	Memory address of the top field vertical ancillary buffer. The register value points to the beginning of the buffer, and the address must be a multiple of 8 (C*n*TVANC[2:0] = 0).

3.20 Channel *n* Bottom Field Vertical Ancillary Address Register (C*n*BVANC)

The Channel *n* Bottom Field Vertical Ancillary Address Register (C*n*BVANC) is shown in Figure 43 and described in Table 29.

NOTE: C*n*BVANC registers are not used in progressive video mode.

Figure 43. Channel *n* Bottom Field Vertical Ancillary Data Buffer Start Address Register (C*n*BVANC)

31	0
C*n*BVANC	
R/W-0	

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 29. Channel *n* Bottom Field Vertical Ancillary Data Buffer Start Address Register (C*n*BVANC) Field Descriptions

Bit	Field	Value	Description
31-0	C*n*BVANC	0-FFFF FFFFh	Memory address of the bottom field vertical ancillary buffer. The register value points to the beginning of the buffer, and the address must be a multiple of 8 (C*n*BVANC[2:0] = 0).

3.21 Channel *n* Image Address Offset Register (C*n*IMGOFFSET)

The Channel *n* Image Address Offset Register (C*n*IMGOFFSET) is shown in Figure 44 and described in Table 30.

Figure 44. Channel *n* Image Address Offset Register (C*n*IMGOFFSET)

31	0
C*n*IMGOFFSET	
R/W-0	

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 30. Channel *n* Image Address Offset Register (C*n*IMGOFFSET) Field Descriptions

Bit	Field	Value	Description
31-0	C*n*IMGOFFSET	0-FFFF FFFFh	Memory address offset of each line of image data. Value is given in bytes, note that the 3 LSBs must be 0. Address calculation method on line[x] is written in the following equation: Address = C*n*IMG_STRT_ADD + C*n*IMGOFFSET × line[x] line[x] = current_line – L3: top field or L9: bottom field Note that this value is valid only if SDRAM storage mode is raster scanning format. In sub-picture mode, this value is ignored. For vertical ancillary data, the address line offset value is automatically calculated by hardware with the configuration of the C*n*YC_MUX bit in C*n*CTRL. In Y/C mux mode, the actual address offset is C*n*IMGOFFSET × 2. In Y/C separate mode, the actual address offset is C*n*IMGOFFSET. See Section 2.4.2 for more information.

3.22 Channel *n* Horizontal Ancillary Address Offset Register (C*n*HANCOFFSET)

The Channel *n* Horizontal Ancillary Address Offset Register (C*n*HANCOFFSET) is shown in Figure 45 and described in Table 31.

Figure 45. Channel *n* Horizontal Ancillary Address Offset Register (C*n*HANCOFFSET)

31	0
C*n*HANCOFFSET	
R/W-0	

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 31. Channel *n* Horizontal Ancillary Address Offset Register (C*n*HANCOFFSET) Field Descriptions

Bit	Field	Value	Description
31-0	C*n*HANCOFFSET	0-FFFF FFFFh	Memory address line-offset for the horizontal ancillary buffers. C*n*HANCOFFSET is given in bytes. Hanc_Address[Line] = Hanc_Buffer_Start_Address + (C*n*HANCOFFSET × Line) The offset value must be a multiple of 8 (C*n*HANCOFFSET[2:0] = 0).

3.23 Channel *n* Horizontal Size Configuration Register (C0HCFG and C1HCFG)

The Channel *n* Horizontal Size Configuration Register (C*n*HCFG) is shown in Figure 48 and described in Table 32.

The C*n*HCFG Register determines the number of bytes in the active (SAV2EAV) and inactive (EAV2SAV) video regions. In the BT/YC mode (Figure 46), the video regions are delimited by the embedded EAV and SAV codes (the region size does not include the 4-byte EAV and SAV codes). In the CCD/CMOS mode (Figure 47), the regions are delimited by the synchronous raw_h_valid capture signal.

Figure 46. Horizontal Distance in Y/C Mode

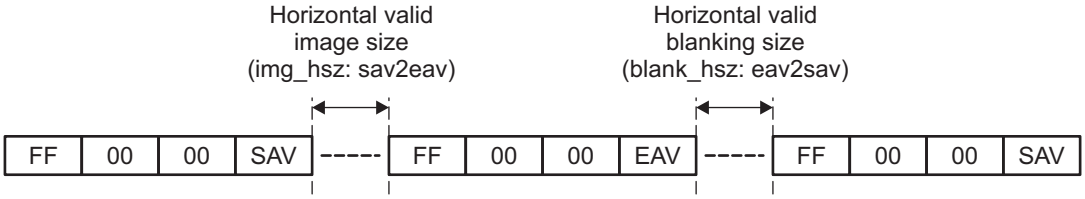


Figure 47. Horizontal Distance in CCD/CMOS Mode

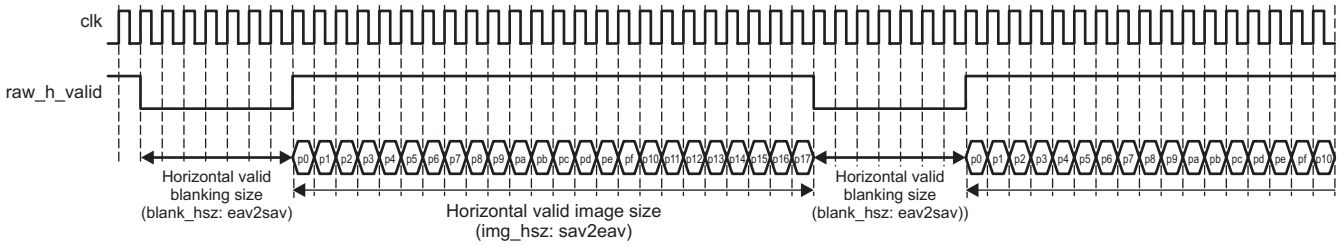


Figure 48. Channel *n* Horizontal Size Configuration Register (C*n*HCFG)

31	29	28	16
Reserved		EAV2SAV	
R-0		R/W-0	

15	13	12	0
Reserved		SAV2EAV	
R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 32. Channel *n* Horizontal Size Configuration Register (C*n*HCFG) Field Descriptions

Bit	Field	Value	Description
31-29	Reserved	0	Reserved
28-16	EAV2SAV	0-1FFFh	Number of bytes in the EAV2SAV region. The EAV2SAV value must be even (EAV2SAV[0:0] = 0)
15-13	Reserved	0	Reserved
12-0	SAV2EAV	0-1FFFh	Number of bytes in the SAV2EAV region. The SAV2EAV value must be even (SAV2EAV[0:0] = 0)

3.24 Channel *n* Vertical Size Configuration 0 Register (C0VCFG0 and C1VCFG0)

The Channel *n* Vertical Size Configuration 0 Register (C*n*VCFG0) is shown in Figure 49 and described in Table 33.

Figure 49. Channel *n* Vertical Size Configuration 0 Register (C*n*VCFG0)

31	28	27	16
Reserved		L1	
R-0		R/W-0	

15	12	11	0
Reserved		L3	
R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 33. Channel *n* Vertical Size Configuration 0 Register (C*n*VCFG0) Field Descriptions

Bit	Field	Value	Description
31-28	Reserved	0	Reserved
27-16	L1	0-FFFh	Enumerated line number for the L1 field position (see Section 2.3).
15-12	Reserved	0	Reserved
11-0	L3	0-FFFh	Enumerated line number for the L3 field position (see Section 2.3).

3.25 Channel *n* Vertical Size Configuration 1 Register (C0VCFG1 and C1VCFG1)

The Channel *n* Vertical Size Configuration 1 Register (C*n*VCFG1) is shown in Figure 50 and described in Table 34.

Figure 50. Channel *n* Vertical Data Size Configuration 1 Register (C*n*VCFG1)

31	28	27	16
Reserved		L5	
R-0		R/W-0	

15	12	11	0
Reserved		L7	
R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 34. Channel *n* Vertical Size Configuration 1 Register (C*n*VCFG1) Field Descriptions

Bit	Field	Value	Description
31-28	Reserved	0	Reserved
27-16	L5	0-FFFh	Enumerated line number for the L5 field position (see Section 2.3).
15-12	Reserved	0	Reserved
11-0	L7	0-FFFh	Enumerated line number for the L7 field position (see Section 2.3). Note that L7 is not used with the progressive video mode.

3.26 Channel *n* Vertical Size Configuration 2 Register (C0VCFG2 and C1VCFG2)

NOTE: The C*n*VCFG2 registers are not used with the progressive video mode.

The Channel *n* Vertical Size Configuration 2 Register (C*n*VCFG2) is shown in Figure 51 and described in Table 35.

Figure 51. Channel *n* Vertical Size Configuration 2 Register (C*n*VCFG2)

31	28	27	16
Reserved		L9	
R-0		R/W-0	

15	12	11	0
Reserved		L11	
R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 35. Channel *n* Vertical Size Configuration 2 Register (C*n*VCFG2) Field Descriptions

Bit	Field	Value	Description
31-28	Reserved	0	Reserved
27-16	L9	0-FFFh	Enumerated line number for the L9 field position (see Section 2.3).
15-12	Reserved	0	Reserved
11-0	L11	0-FFFh	Enumerated line number for the L11 field position (see Section 2.3).

3.27 Channel *n* Vertical Image Size Register (C0VSIZE and C1VSIZE)

The Channel *n* Vertical Image Size Register (C*n*VSIZE) is shown in Figure 52 and described in Table 36.

Figure 52. Channel *n* Vertical Image Size Register (C*n*VSIZE)

31	16
Reserved	
R-0	

15	12	11	0
Reserved		VSIZE	
R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 36. Channel *n* Vertical Image Size Register (C*n*VSIZE) Field Descriptions

Bit	Field	Value	Description
31-12	Reserved	0	Reserved
11-0	VSIZE	0-FFFh	Vertical size of image (total number of lines).

3.28 Channel *n* Horizontal Size Configuration Register (C2HCFG and C3HCFG)

The Channel *n* Horizontal Size Configuration Register (C*n*HCFG) is shown in Figure 53 and described in Table 37.

The C*n*HCFG Register determines the number of bytes in the active (SAV2EAV) and inactive (EAV2SAV) video regions. In the BT/YC mode (Figure 46), the video regions are delimited by the embedded EAV and SAV codes (the region size does not include the 4-byte EAV and SAV codes). In the CCD/CMOS mode (Figure 47), the regions are delimited by the synchronous raw_h_valid capture signal.

Figure 53. Channel *n* Horizontal Size Configuration Register (C*n*HCFG)

31	27	26	16
Reserved		EAV2SAV	
R-0		R/W-0	

15	11	10	0
Reserved		SAV2EAV	
R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 37. Channel *n* Horizontal Size Configuration Register (C*n*HCFG) Field Descriptions

Bit	Field	Value	Description
31-27	Reserved	0	Reserved
26-16	EAV2SAV	0-7FFh	Number of bytes in the EAV2SAV region. The EAV2SAV value must be even (EAV2SAV[0:0] = 0)
15-11	Reserved	0	Reserved
10-0	SAV2EAV	0-7FFh	Number of bytes in the SAV2EAV region. The SAV2EAV value must be even (SAV2EAV[0:0] = 0)

3.29 Channel *n* Vertical Size Configuration 0 Register (C2VCFG0 and C3VCFG0)

The Channel *n* Vertical Size Configuration 0 Register (C*n*VCFG0) is shown in Figure 54 and described in Table 38.

Figure 54. Channel *n* Vertical Size Configuration 0 Register (C*n*VCFG0)

31	27	26	16
Reserved		L1	
R-0		R/W-0	

15	11	10	0
Reserved		L3	
R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 38. Channel *n* Vertical Size Configuration 0 Register (C*n*VCFG0) Field Descriptions

Bit	Field	Value	Description
31-27	Reserved	0	Reserved
26-16	L1	0-7FFh	Enumerated line number for the L1 field position (see Section 2.3).
15-11	Reserved	0	Reserved
10-0	L3	0-7FFh	Enumerated line number for the L3 field position (see Section 2.3).

3.30 Channel *n* Vertical Size Configuration 1 Register (C2VCFG1 and C3VCFG1)

The Channel *n* Vertical Size Configuration 1 Register (C*n*VCFG1) is shown in Figure 55 and described in Table 39.

Figure 55. Channel *n* Vertical Size Configuration 1 Register (C*n*VCFG1)

31	27	26	16
Reserved		L5	
R-0		R/W-0	

15	11	10	0
Reserved		L7	
R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 39. Channel *n* Vertical Size Configuration 1 Register (C*n*VCFG1) Field Descriptions

Bit	Field	Value	Description
31-27	Reserved	0	Reserved
26-16	L5	0-7FFh	Enumerated line number for the L5 field position (see Section 2.3).
15-11	Reserved	0	Reserved
10-0	L7	0-7FFh	Enumerated line number for the L5 field position (see Section 2.3). Note that L7 is not used with the progressive video mode.

3.31 Channel *n* Vertical Size Configuration 2 Register (C2VCFG2 and C3VCFG2)

NOTE: The C*n*VCFG2 registers are not used with progressive video mode.

The Channel *n* Vertical Size Configuration 2 Register (C*n*VCFG2) is shown in Figure 56 and described in Table 40.

Figure 56. Channel *n* Vertical Size Configuration 2 Register (C*n*VCFG2)

31	27	26	16
Reserved		L9	
R-0		R/W-0	

15	11	10	0
Reserved		L11	
R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 40. Channel *n* Vertical Size Configuration 2 Register (C*n*VCFG2) Field Descriptions

Bit	Field	Value	Description
31-27	Reserved	0	Reserved
26-16	L9	0-7FFh	Enumerated line number for the L9 field position (see Section 2.3).
15-11	Reserved	0	Reserved
10-0	L11	0-7FFh	Enumerated line number for the L11 field position (see Section 2.3).

3.32 Channel *n* Vertical Image Size Register (C2VSIZE and C3VSIZE)

The Channel *n* Vertical Image Size Register (C*n*VSIZE) is shown in Figure 57 and described in Table 41.

Figure 57. Channel *n* Vertical Image Size Register (C*n*VSIZE)

31	16
Reserved	
R-0	

15	11	10	0
Reserved		VSIZE	
R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 41. Channel *n* Vertical Image Size Register (C*n*VSIZE) Field Descriptions

Bit	Field	Value	Description
31-11	Reserved	0	Reserved
10-0	VSIZE	0-7FFh	Vertical size of image (total number of lines)

3.33 Channel *n* Top Field Horizontal Ancillary Position Register (C2THANCPOS and C3THANCPOS)

The Channel *n* Top Field Horizontal Ancillary Position Register (C*n*THANCPOS) is shown in Figure 58 and described in Table 42.

Figure 58. Channel *n* Top Field Horizontal Ancillary Position Register (C*n*THANCPOS)

31	27	26	16
Reserved		VPOS	
R-0		R/W-0	

15	11	10	0
Reserved		HPOS	
R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 42. Channel *n* Top Field Horizontal Ancillary Position Register (C*n*THANCPOS) Field Descriptions

Bit	Field	Value	Description
31-27	Reserved	0	Reserved
26-16	VPOS	0-7FFh	Vertical position (line-count) of valid data within the top field horizontal ancillary blanking region. Line positions are enumerated beginning with 1.
15-11	Reserved	0	Reserved
10-0	HPOS	0-7FFh	Horizontal position (byte-count) of valid data within the top field horizontal ancillary blanking region. Byte positions are enumerated beginning with 0. The value of HPOS must be a multiple of 8 (HPOS[2:0] = 0).

3.34 Channel *n* Top Field Horizontal Ancillary Size Register (C2THANCSIZE and C3THANCSIZE)

The Channel *n* Top Field Horizontal Ancillary Size Register (C*n*THANCSIZE) is shown in Figure 59 and described in Table 43.

Figure 59. Channel *n* Top Field Horizontal Ancillary Size Register (C*n*THANCSIZE)

31	27	26	16
Reserved		VSIZE	
R-0		R/W-0	

15	11	10	0
Reserved		HSIZE	
R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 43. Channel *n* Top Field Horizontal Ancillary Size Register (C*n*THANCSIZE) Field Descriptions

Bit	Field	Value	Description
31-27	Reserved	0	Reserved
26-16	VSIZE	0-7FFh	Vertical size (line-count) of valid top field horizontal ancillary data beginning at VPOS of the C*n*THANCPOS register.
15-11	Reserved	0	Reserved
10-0	HSIZE	0-7FFh	Horizontal size (byte-count) of valid top field horizontal ancillary data beginning at HPOS of the C*n*THANCPOS register. The value of HSIZE must be a multiple of 8 (HPOS[2:0] = 0).

3.35 Channel *n* Bottom Field Horizontal Ancillary Position Register (C2BHANCPOS and C3BHANCPOS)

The Channel *n* Bottom Field Horizontal Ancillary Position Register (C*n*BHANCPOS) is shown in Figure 60 and described in Table 44.

Figure 60. Channel *n* Bottom Field Horizontal Ancillary Position Register (C*n*BHANCPOS)

31	27	26	16
Reserved		VPOS	
R-0		R/W-0	

15	11	10	0
Reserved		HPOS	
R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 44. Channel *n* Bottom Field Horizontal Ancillary Position Register (C*n*BHANCPOS) Field Descriptions

Bit	Field	Value	Description
31-27	Reserved	0	Reserved
26-16	VPOS	0-7FFh	Vertical position (line-count) of valid data within the bottom field horizontal ancillary blanking region. Line positions are enumerated beginning with 1.
15-11	Reserved	0	Reserved
10-0	HPOS	0-7FFh	Horizontal position (byte-count) of valid data within the bottom field horizontal ancillary blanking region. Byte positions are enumerated beginning with 0. The value of HPOS must be a multiple of 8 (HPOS[2:0] = 0).

3.36 Channel *n* Bottom Field Horizontal Ancillary Size Register (C2BHANCSIZE and C3BHANCSIZE)

The Channel *n* Bottom Field Horizontal Ancillary Size Register (C*n*BHANCSIZE) is shown in Figure 61 and described in Table 45.

Figure 61. Channel *n* Bottom Field Horizontal Ancillary Size Register (C*n*BHANCSIZE)

31	27	26	16
Reserved		VSIZE	
R-0		R/W-0	

15	11	10	0
Reserved		HSIZE	
R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 45. Channel *n* Bottom Field Horizontal Ancillary Size Register (C*n*BHANCSIZE) Field Descriptions

Bit	Field	Value	Description
31-27	Reserved	0	Reserved
26-16	VSIZE	0-7FFh	Vertical size (line-count) of valid bottom field horizontal ancillary data beginning at VPOS of the C*n*BHANCPOS register.
15-11	Reserved	0	Reserved
10-0	HSIZE	0-7FFh	Horizontal size (byte-count) of valid bottom field horizontal ancillary data beginning at HPOS of the C*n*BHANCPOS register. The value of HSIZE must be a multiple of 8 (HSIZE[2:0] = 0).

3.37 Channel *n* Top Field Vertical Ancillary Position Register (C2TVANCPOS and C3TVANCPOS)

The Channel *n* Top Field Vertical Ancillary Position Register (C*n*TVANCPOS) is shown in Figure 62 and described in Table 46.

Figure 62. Channel *n* Top Field Vertical Ancillary Position Register (C*n*TVANCPOS)

31	27	26	16
Reserved		VPOS	
R-0		R/W-0	

15	11	10	0
Reserved		HPOS	
R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 46. Channel *n* Top Field Vertical Ancillary Position Register (C*n*TVANCPOS) Field Descriptions

Bit	Field	Value	Description
31-27	Reserved	0	Reserved
26-16	VPOS	0-7FFh	Vertical position (line-count) of valid data within the top field vertical ancillary blanking region. Line positions are enumerated beginning with 1.
15-11	Reserved	0	Reserved
10-0	HPOS	0-7FFh	Horizontal position (byte-count) of valid data within the top field vertical ancillary blanking region. Byte positions are enumerated beginning with 0. The value of HPOS must be a multiple of 8 (HPOS[2:0] = 0).

3.38 Channel *n* Top Field Vertical Ancillary Size Register (C2TVANCSIZE and C3TVANCSIZE)

The Channel *n* Top Field Vertical Ancillary Size register (C*n*TVANCSIZE) is shown in Figure 63 and described in Table 47.

Figure 63. Channel *n* Top Field Vertical Ancillary Size Register (C*n*TVANCSIZE)

31	27	26	16
Reserved		VSIZE	
R-0		R/W-0	

15	11	10	0
Reserved		HSIZE	
R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 47. Channel *n* Top Field Vertical Ancillary Size Register (C*n*TVANCSIZE) Field Descriptions

Bit	Field	Value	Description
31-27	Reserved	0	Reserved
26-16	VSIZE	0-7FFh	Vertical size (line-count) of valid top field verticall ancillary data beginning at VPOS of the C*n*TVANCPOS register.
15-11	Reserved	0	Reserved
10-0	HSIZE	0-7FFh	Horizontal size (byte-count) of valid top field vertical ancillary data beginning at HPOS of the C*n*TVANCPOS register. The value of HSIZE must be a multiple of 8 (HSIZE[2:0] = 0).

3.39 Channel *n* Bottom Field Vertical Ancillary Position Register (C2BVANCPOS and C3BVANCPOS)

The Channel *n* Bottom Field Vertical Ancillary Position Register (C*n*BVANCPOS) is shown in Figure 64 and described in Table 48.

Figure 64. Channel *n* Bottom Field Vertical Ancillary Position Register (C*n*BVANCPOS)

31	27	26	16
Reserved		VPOS	
R-0		R/W-0	

15	11	10	0
Reserved		HPOS	
R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 48. Channel *n* Bottom Field Vertical Ancillary Position Register (C*n*BVANCPOS) Field Descriptions

Bit	Field	Value	Description
31-27	Reserved	0	Reserved
26-16	VPOS	0-7FFh	Vertical position (line-count) of valid data within the bottom field vertical ancillary blanking region. Line positions are enumerated beginning with 1.
15-11	Reserved	0	Reserved
10-0	HPOS	0-7FFh	Horizontal position (byte-count) of valid data within the bottom field vertical ancillary blanking region. Byte positions are enumerated beginning with 0. The value of HPOS must be a multiple of 8 (HPOS[2:0] = 0).

3.40 Channel *n* Bottom Field Vertical Ancillary Size Register (C2BVANCSIZE and C3BVANCSIZE)

The Channel *n* Bottom Field Vertical Ancillary Size Register (C*n*BVANCSIZE) is shown in Figure 65 and described in Table 49.

Figure 65. Channel *n* Bottom Field Vertical Ancillary Size Register (C*n*BVANCSIZE)

31	27	26	16
Reserved		VSIZE	
R-0		R/W-0	

15	11	10	0
Reserved		HSIZE	
R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 49. Channel *n* Bottom Field Vertical Ancillary Size Register (C*n*BVANCSIZE) Field Descriptions

Bit	Field	Value	Description
31-27	Reserved	0	Reserved
26-16	VSIZE	0-7FFh	Vertical size (line-count) of valid bottom field verticall ancillary data beginning at VPOS of the C*n*BVANCPOS register.
15-11	Reserved	0	Reserved
10-0	HSIZE	0-7FFh	Horizontal size (byte-count) of valid bottom field vertical ancillary data beginning at HPOS of the C*n*BVANCPOS register. The value of HSIZE must be a multiple of 8 (HSIZE[2:0] = 0).

Appendix A Revision History

Table 50 lists the changes made since the previous version of this document.

Table 50. Document Revision History

Reference	Additions/Modifications/Deletions
Section 2.4.2	Added last paragraph.
Figure 25	Changed bit 1 to Reserved.
Table 11	Changed Description of INTFRAME bit.
	Changed Description of CAPMODE bit.
Figure 26	Changed bit 1 to Reserved.
Table 12	Changed Description of INTFRAME bit.
	Changed Description of CAPMODE bit.
Table 21	Changed Description of BYTES bit.
Table 30	Added last paragraph to Description.

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