TMS320C674x/OMAP-L1x Processor DDR2/mDDR Memory Controller

User's Guide

Literature Number: SPRUGJ4
June 2009

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Read This First

About This Manual

Describes the operation of the DDR2/mobile DDR memory controller.

Notational Conventions

This document uses the following conventions.

- Hexadecimal numbers are shown with the suffix h. For example, the following number is 40 hexadecimal (decimal 64): 40h.
- Registers in this document are shown in figures and described in tables.
  - Each register figure shows a rectangle divided into fields that represent the fields of the register. Each field is labeled with its bit name, its beginning and ending bit numbers above, and its read/write properties below. A legend explains the notation used for the properties.
  - Reserved bits in a register figure designate a bit that is used for future device expansion.

Related Documentation From Texas Instruments

The following documents describe the TMS320C674x Digital Signal Processors (DSPs) and OMAP-L1x Applications Processors. Copies of these documents are available on the Internet at www.ti.com. *Tip:* Enter the literature number in the search box provided at www.ti.com.

The current documentation that describes the DSP, related peripherals, and other technical collateral, is available in the C6000 DSP product folder at: www.ti.com/c6000.

SPRUGM5 — ***TMS320C6742 DSP System Reference Guide.*** Describes the C6742 DSP subsystem, system memory, device clocking, phase-locked loop controller (PLLC), power and sleep controller (PSC), power management, and system configuration module.

SPRUGJ0 — ***TMS320C6743 DSP System Reference Guide.*** Describes the System-on-Chip (SoC) including the C6743 DSP subsystem, system memory, device clocking, phase-locked loop controller (PLLC), power and sleep controller (PSC), power management, and system configuration module.

SPRUFK4 — ***TMS320C6745/C6747 DSP System Reference Guide.*** Describes the System-on-Chip (SoC) including the C6745/C6747 DSP subsystem, system memory, device clocking, phase-locked loop controller (PLLC), power and sleep controller (PSC), power management, and system configuration module.

SPRUGM6 — ***TMS320C6746 DSP System Reference Guide.*** Describes the C6746 DSP subsystem, system memory, device clocking, phase-locked loop controller (PLLC), power and sleep controller (PSC), power management, and system configuration module.

SPRUGJ7 — ***TMS320C6748 DSP System Reference Guide.*** Describes the C6748 DSP subsystem, system memory, device clocking, phase-locked loop controller (PLLC), power and sleep controller (PSC), power management, and system configuration module.

SPRUG84 — ***OMAP-L137 Applications Processor System Reference Guide.*** Describes the System-on-Chip (SoC) including the ARM subsystem, DSP subsystem, system memory, device clocking, phase-locked loop controller (PLLC), power and sleep controller (PSC), power management, ARM interrupt controller (AINTC), and system configuration module.

SPRUGM7 — *OMAP-L138 Applications Processor System Reference Guide.* Describes the System-on-Chip (SoC) including the ARM subsystem, DSP subsystem, system memory, device clocking, phase-locked loop controller (PLLC), power and sleep controller (PSC), power management, ARM interrupt controller (AINTC), and system configuration module.

SPRUFK9 — *TMS320C674x/OMAP-L1x Processor Peripherals Overview Reference Guide.* Provides an overview and briefly describes the peripherals available on the TMS320C674x Digital Signal Processors (DSPs) and OMAP-L1x Applications Processors.

SPRUFK5 — *TMS320C674x DSP Megamodule Reference Guide.* Describes the TMS320C674x digital signal processor (DSP) megamodule. Included is a discussion on the internal direct memory access (IDMA) controller, the interrupt controller, the power-down controller, memory protection, bandwidth management, and the memory and cache.

SPRUFE8 — *TMS320C674x DSP CPU and Instruction Set Reference Guide.* Describes the CPU architecture, pipeline, instruction set, and interrupts for the TMS320C674x digital signal processors (DSPs). The C674x DSP is an enhancement of the C64x+ and C67x+ DSPs with added functionality and an expanded instruction set.

SPRUG82 — *TMS320C674x DSP Cache User's Guide.* Explains the fundamentals of memory caches and describes how the two-level cache-based internal memory architecture in the TMS320C674x digital signal processor (DSP) can be efficiently used in DSP applications. Shows how to maintain coherence with external memory, how to use DMA to reduce memory latencies, and how to optimize your code to improve cache efficiency. The internal memory architecture in the C674x DSP is organized in a two-level hierarchy consisting of a dedicated program cache (L1P) and a dedicated data cache (L1D) on the first level. Accesses by the CPU to the these first level caches can complete without CPU pipeline stalls. If the data requested by the CPU is not contained in cache, it is fetched from the next lower memory level, L2 or external memory.

DDR2/mDDR Memory Controller

1 Introduction

This document describes the DDR2/mobile DDR memory controller.

1.1 Purpose of the Peripheral

The DDR2/mDDR memory controller is used to interface with JESD79D-2A standard compliant DDR2 SDRAM devices and standard mobile DDR (mDDR) SDRAM devices. Memories types such as DDR1 SDRAM, SDR SDRAM, SBSRAM, and asynchronous memories are not supported. The DDR2/mDDR memory is the major memory location for program and data storage.

1.2 Features

The DDR2/mDDR memory controller supports the following features:

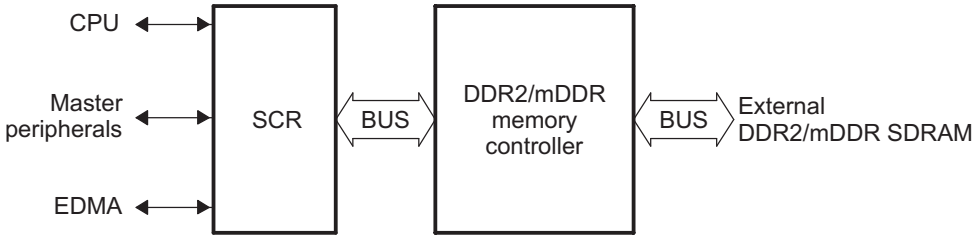
- JESD79D-2A standard compliant DDR2 SDRAM
- Standard compliant mobile DDR (mDDR)
- Data bus width of 16 bits
- CAS latencies:
  - DDR2: 2, 3, 4, and 5
  - mDDR: 2 and 3
- Internal banks:
  - DDR2: 1, 2, 4, and 8
  - mDDR: 1, 2, and 4
- Burst length: 8
- Burst type: sequential
- 1 CS signal
- Page sizes: 256, 512, 1024, and 2048
- SDRAM auto-initialization
- Self-refresh mode
- Partial array self-refresh (for mDDR)
- Power-down mode
- Prioritized refresh
- Programmable refresh rate and backlog counter
- Programmable timing parameters
- Little-endian mode

1.3 Functional Block Diagram

The DDR2/mDDR memory controller is the main interface to external DDR2/mDDR memory. Figure 1 displays the general data paths to on-chip peripherals and external DDR2/mDDR SDRAM.

Master peripherals, EDMA, and the CPU can access the DDR2/mDDR memory controller through the switched central resource (SCR).

Figure 1. Data Paths to DDR2/mDDR Memory Controller



1.4 Supported Use Case Statement

The DDR2/mDDR memory controller supports JESD79D-2A DDR2 SDRAM memories and mobile DDR (mDDR) SDRAM memories utilizing 16 bits of the DDR2/mDDR memory controller data bus. See Section 3 for more details.

1.5 Industry Standard(s) Compliance Statement

The DDR2/mDDR memory controller is compliant with the JESD79D-2A DDR2 SDRAM standard and mobile DDR (mDDR) standard with the following exception:

- On-Die Termination (ODT). The DDR2/mDDR memory controller does not include any on-die terminating resistors. Furthermore, the on-die terminating resistors of the DDR2/mDDR SDRAM device must be disabled by tying the ODT input pin of the DDR2/mDDR SDRAM to ground.

2 Architecture

This section describes the architecture of the DDR2/mDDR memory controller as well as how it is structured and how it works within the context of the system-on-a-chip. The DDR2/mDDR memory controller can gluelessly interface to most standard DDR2/mDDR SDRAM devices and supports such features as self-refresh mode and prioritized refresh. In addition, it provides flexibility through programmable parameters such as the refresh rate, CAS latency, and many SDRAM timing parameters. The following sections include details on how to interface and properly configure the DDR2/mDDR memory controller to perform read and write operations to externally-connected DDR2/mDDR SDRAM devices. Also, Section 3 provides a detailed example of interfacing the DDR2/mDDR memory controller to a common DDR2/mDDR SDRAM device.

2.1 Clock Control

The DDR2/mDDR memory controller receives two input clocks from internal clock sources, VCLK and 2X_CLK (Figure 2). VCLK is a divided-down version of the PLL0 clock. 2X_CLK is the PLL1 clock. 2X_CLK should be configured to clock at the frequency of the desired data rate, or stated similarly, it should operate at twice the frequency of the desired DDR2/mDDR memory clock. DDR_CLK and $\overline{\text{DDR\_CLK}}$ are the two output clocks of the DDR2/mDDR memory controller providing the interface clock to the DDR2/mDDR SDRAM memory. These two clocks operate at a frequency of 2X_CLK/2.

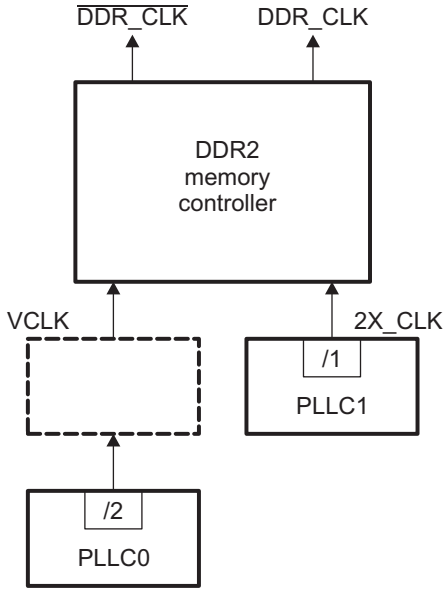
2.1.1 Clock Source

VCLK and 2X_CLK are sourced from two independent PLLs (Figure 2). VCLK is sourced from PLL controller 0 (PLLC0) and 2X_CLK is sourced from PLL controller 1 (PLLC1).

VCLK is clocked at a fixed divider ratio of PLL0. This divider is fixed at 2, meaning VCLK is clocked at a frequency of PLL0/2.

The clock from PLLC1 is not divided before reaching 2X_CLK. PLLC1 should be configured to supply 2X_CLK at the desired frequency. For example, if a 138-MHz DDR2/mDDR interface clock (DDR_CLK) is desired, then PLLC1 must be configured to generate a 276-MHz clock on 2X_CLK.

Figure 2. DDR2/mDDR Memory Controller Clock Block Diagram



2.1.2 Clock Configuration

The frequency of 2X_CLK is configured by selecting the appropriate PLL multiplier. The PLL multiplier is selected by programming registers within PLLC1. The PLLC1 divider ration is fixed at 1. For information on programming the PLL controllers, see your device-specific *System Reference Guide*. For information on supported clock frequencies, see your device-specific data manual.

Note: PLLC1 should be configured and a stable clock present on 2X_CLK before releasing the DDR2/mDDR memory controller from reset.

2.1.3 DDR2/mDDR Memory Controller Internal Clock Domains

There are two clock domains within the DDR2/mDDR memory controller. The two clock domains are driven by VCLK and a divided-down by 2 version of 2X_CLK called MCLK. The command FIFO, write FIFO, and read FIFO described in Section 2.6 are all on the VCLK domain. From this, VCLK drives the interface to the peripheral bus.

The MCLK domain consists of the DDR2/mDDR memory controller state machine and memory-mapped registers. This clock domain is clocked at the rate of the external DDR2/mDDR memory, 2X_CLK/2.

To conserve power within the DDR2/mDDR memory controller, VCLK, MCLK, and 2X_CLK may be stopped. See Section 2.16 for proper clock stop procedures.

2.2 Signal Descriptions

The DDR2/mDDR memory controller signals are shown in Figure 3 and described in Table 1. The following features are included:

- The maximum data bus is 16-bits wide.
- The address bus is 14-bits wide with an additional three bank address pins.
- Two differential output clocks driven by internal clock sources.
- Command signals: Row and column address strobe, write enable strobe, data strobe, and data mask.
- One chip select signal and one clock enable signal.

Figure 3. DDR2/mDDR Memory Controller Signals

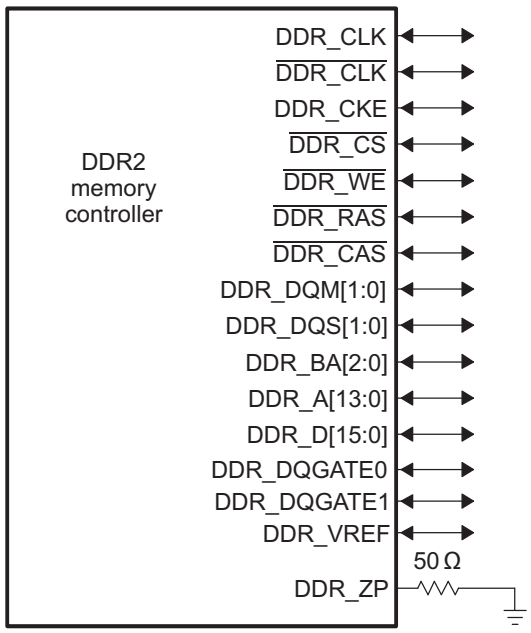


Table 1. DDR2/mDDR Memory Controller Signal Descriptions

Pin	Type[1]	Description
DDR_CLK, $\overline{\text{DDR\_CLK}}$	O/Z	**Clock:** Differential clock outputs.
DDR_CKE	O/Z	**Clock enable:** Active high.
$\overline{\text{DDR\_CS}}$	O/Z	**Chip select:** Active low.
$\overline{\text{DDR\_WE}}$	O/Z	**Write enable strobe:** Active low, command output.
$\overline{\text{DDR\_RAS}}$	O/Z	**Row address strobe:** Active low, command output.
$\overline{\text{DDR\_CAS}}$	O/Z	**Column address strobe:** Active low, command output.
DDR_DQM[1:0]	O/Z	**Data mask**: Output mask signal for write data.
DDR_DQS[1:0]	I/O/Z	**Data strobe:** Active high, bi-directional signals. Output with write data, input with read data.
DDR_BA[2:0]	O/Z	**Bank select:** Output, defining which bank a given command is applied.
DDR_A[13:0]	O/Z	**Address:** Address bus.
DDR_D[15:0]	I/O/Z	**Data:** Bi-directional data bus. Input for read data, output for write data.
DDR_DQGATE0	O/Z	**Strobe Enable:** Active high
DDR_DQGATE1	I/O/Z	**Strobe Enable Delay:** Loopback signal for timing adjustment (DQS gating). Route from DDR_DQGATE0 to DDR device and back to DDR_DQGATE1 with same constraints as used for DDR clock and data.
DDR_ZP	I/O/Z	**Output drive strength reference:** Reference output for drive strength calibration of N and P channel outputs. Tie to ground via 50 ohm .5% tolerance 1/16th watt resistor (49.9 ohm .5% tolerance is acceptable).
DDR_VREF	pwr	**Voltage reference input:** Voltage reference input for the SSTL_18 I/O buffers. Note even in the case of mDDR an external resistor divider connected to this pin is necessary.

(1) Legend: I = input, O = Output, Z = high impedance, pwr = power

2.3 Protocol Description(s)

The DDR2/mDDR memory controller supports the DDR2/mDDR SDRAM commands listed in Table 2. Table 3 shows the signal truth table for the DDR2/mDDR SDRAM commands.

Table 2. DDR2/mDDR SDRAM Commands

Command	Function
ACTV	Activates the selected bank and row.
DCAB	Precharge all command. Deactivates (precharges) all banks.
DEAC	Precharge single command. Deactivates (precharges) a single bank.
DESEL	Device Deselect.
EMRS	Extended Mode Register set. Allows altering the contents of the mode register.
MRS	Mode register set. Allows altering the contents of the mode register.
NOP	No operation.
Power Down	Power-down mode.
READ	Inputs the starting column address and begins the read operation.
READ with autoprecharge	Inputs the starting column address and begins the read operation. The read operation is followed by a precharge.
REFR	Autorefresh cycle.
SLFREFR	Self-refresh mode.
WRT	Inputs the starting column address and begins the write operation.
WRT with autoprecharge	Inputs the starting column address and begins the write operation. The write operation is followed by a precharge.

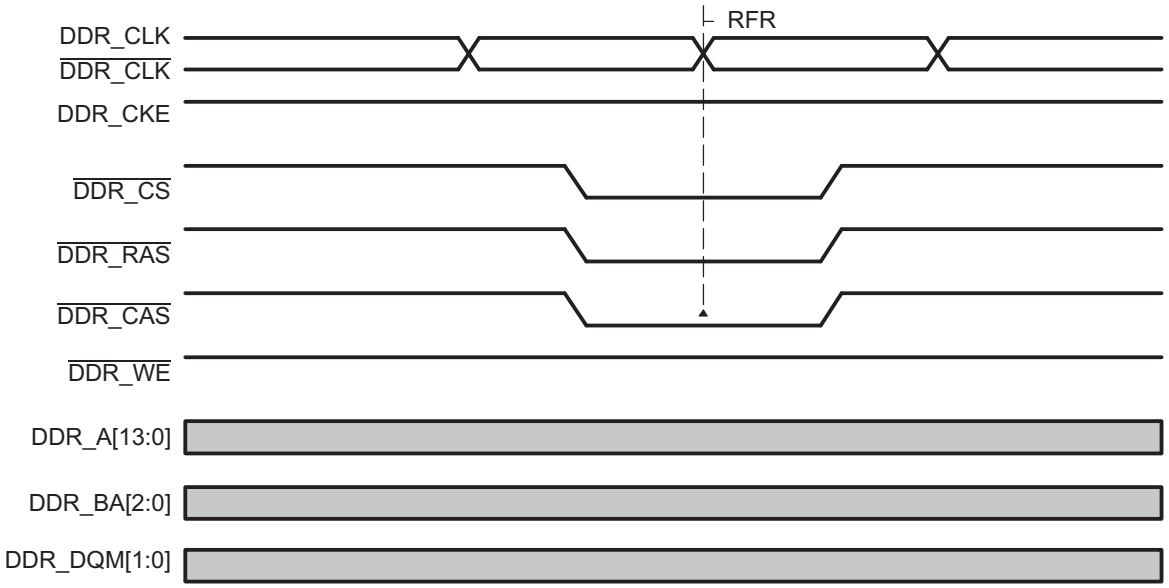
Table 3. Truth Table for DDR2/mDDR SDRAM Commands

DDR2/mDDR SDRAM:	CKE		$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BA[2:0]	A[13:11, 9:0]	A10
DDR2/mDDR memory controller:	DDR_CKE Previous Cycles	DDR_CKE Current Cycle	$\overline{DDR\_CS}$	$\overline{DDR\_RAS}$	$\overline{DDR\_CAS}$	$\overline{DDR\_WE}$	DDR_BA[2:0]	DDR_A[13:11, 9:0]	DDR_A[10]
ACTV	H	H	L	L	H	H	Bank	Row Address	
DCAB	H	H	L	L	H	L	X	X	H
DEAC	H	H	L	L	H	L	Bank	X	L
MRS	H	H	L	L	L	L	BA	OP Code	
EMRS	H	H	L	L	L	L	BA	OP Code	
READ	H	H	L	H	L	H	BA	Column Address	L
READ with precharge	H	H	L	H	L	H	BA	Column Address	H
WRT	H	H	L	H	L	L	BA	Column Address	L
WRT with precharge	H	H	L	H	L	L	BA	Column Address	H
REFR	H	H	L	L	L	H	X	X	X
SLFREFR entry	H	L	L	L	L	H	X	X	X
SLFREFR exit	L	H	H	X	X	X	X	X	X
			L	H	H	H	X	X	X
NOP	H	X	L	H	H	H	X	X	X
DESEL	H	X	H	X	X	X	X	X	X
Power Down entry	H	L	H	X	X	X	X	X	X
			L	H	H	H	X	X	X
Power Down exit	L	H	H	X	X	X	X	X	X
			L	H	H	H	X	X	X

2.3.1 Refresh Mode

The DDR2/mDDR memory controller issues refresh commands to the DDR2/mDDR SDRAM memory (Figure 4). REFR is automatically preceded by a DCAB command, ensuring the deactivation of all CE spaces and banks selected. Following the DCAB command, the DDR2/mDDR memory controller begins performing refreshes at a rate defined by the refresh rate (RR) bit in the SDRAM refresh control register (SDRCR). Page information is always invalid before and after a REFR command; thus, a refresh cycle always forces a page miss. This type of refresh cycle is often called autorefresh. Autorefresh commands may not be disabled within the DDR2/mDDR memory controller. See Section 2.7 for more details on REFR command scheduling.

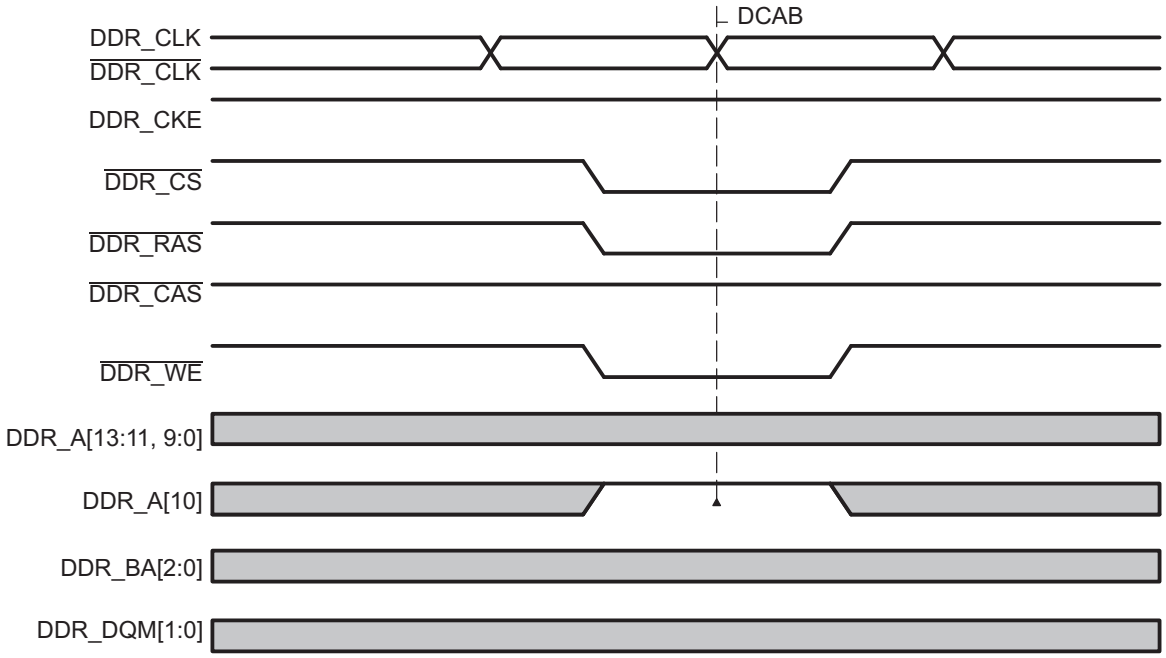
Figure 4. Refresh Command



2.3.2 Deactivation (DCAB and DEAC)

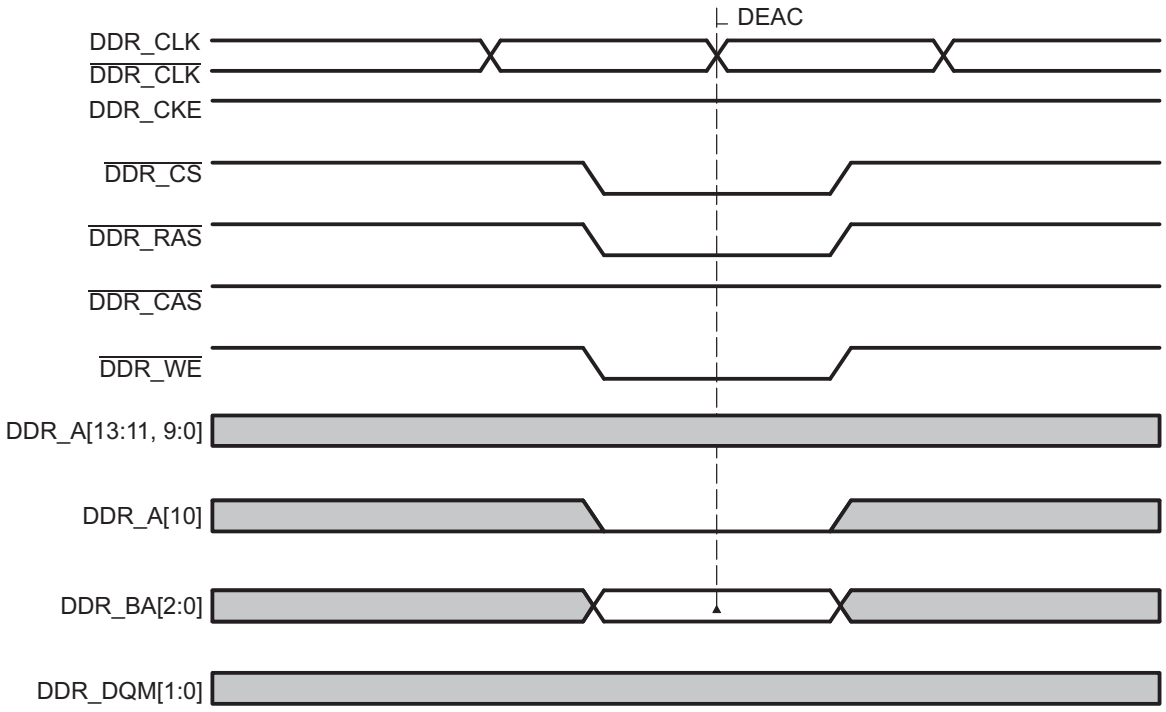
The precharge all banks command (DCAB) is performed after a reset to the DDR2/mDDR memory controller or following the initialization sequence. DDR2/mDDR SDRAMs also require this cycle prior to a refresh (REFR) and mode set register commands (MRS and EMRS). During a DCAB command, DDR_A[10] is driven high to ensure the deactivation of all banks. Figure 5 shows the timing diagram for a DCAB command.

Figure 5. DCAB Command



The DEAC command closes a single bank of memory specified by the bank select signals. Figure 6 shows the timings diagram for a DEAC command.

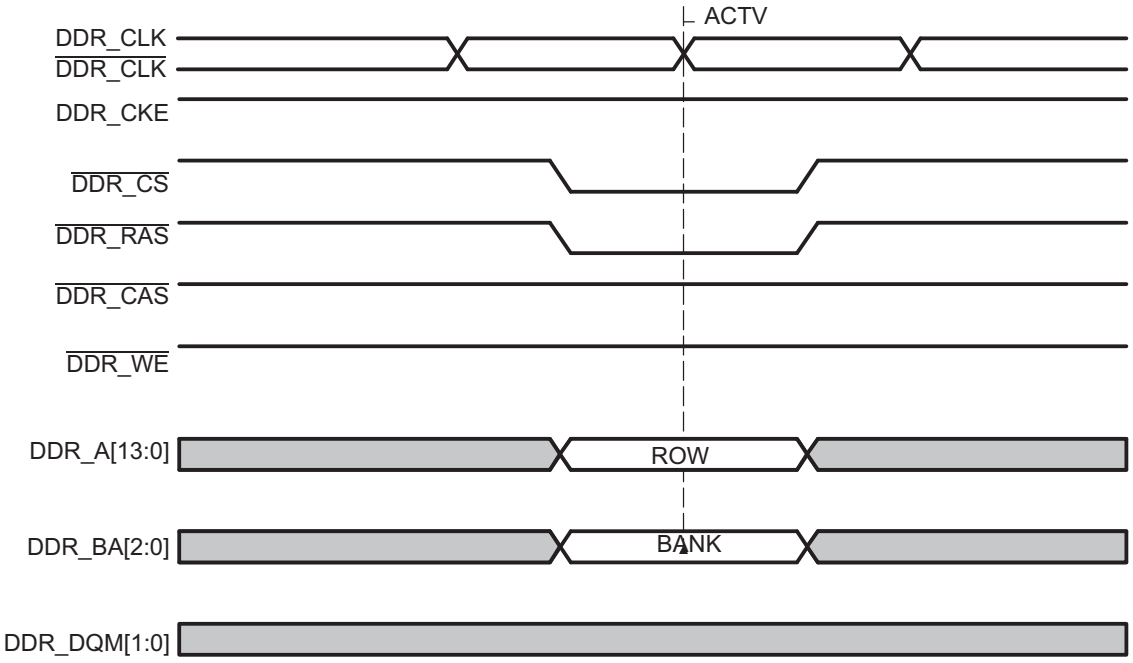
Figure 6. DEAC Command



2.3.3 Activation (ACTV)

The DDR2/mDDR memory controller automatically issues the activate (ACTV) command before a read or write to a closed row of memory. The ACTV command opens a row of memory, allowing future accesses (reads or writes) with minimum latency. The value of DDR_BA[2:0] selects the bank and the value of DDR_A[13:0] selects the row. When the DDR2/mDDR memory controller issues an ACTV command, a delay of t_{RCD} is incurred before a read or write command is issued. Figure 7 shows an example of an ACTV command. Reads or writes to the currently active row and bank of memory can achieve much higher throughput than reads or writes to random areas because every time a new row is accessed, the ACTV command must be issued and a delay of t_{RCD} incurred.

Figure 7. ACTV Command

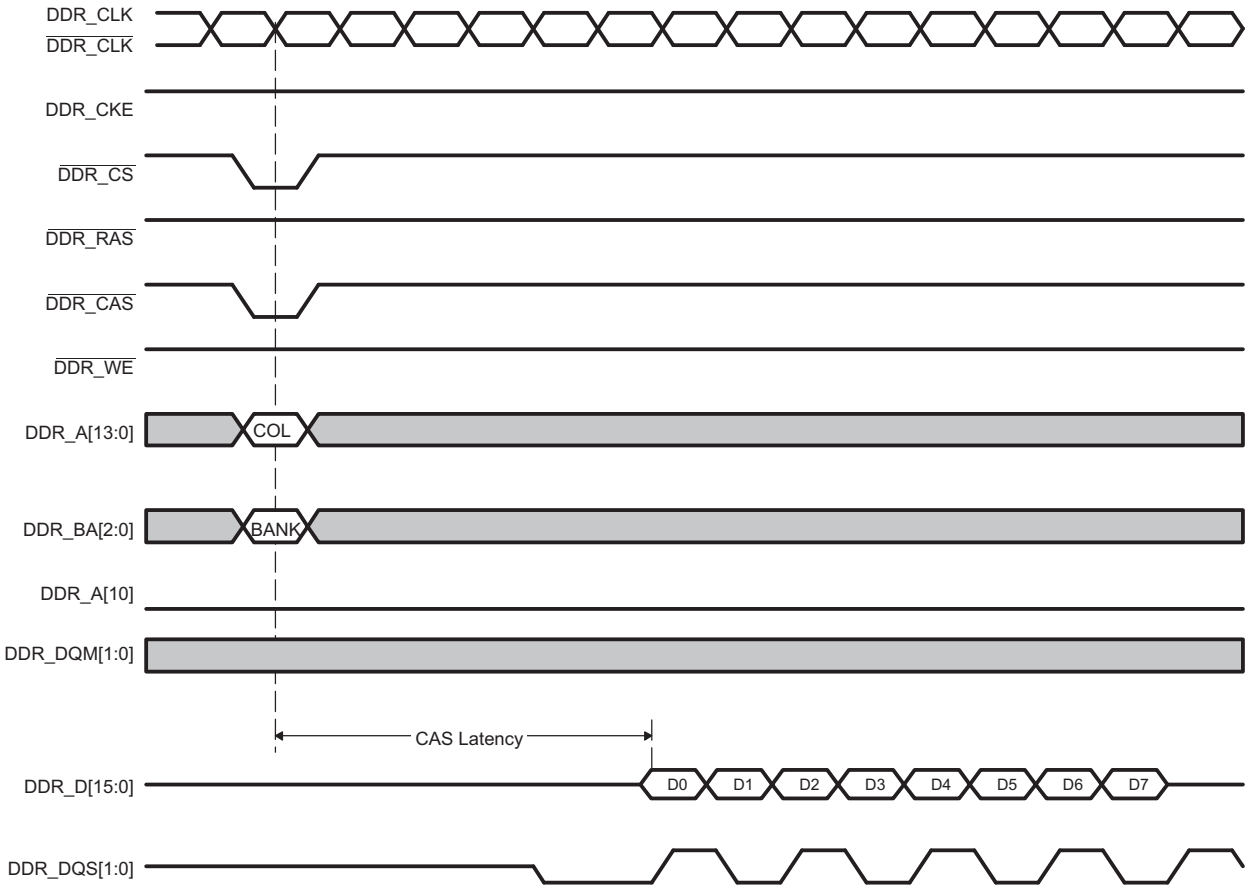


2.3.4 READ Command

Figure 8 shows the DDR2/mDDR memory controller performing a read burst from DDR2/mDDR SDRAM. The READ command initiates a burst read operation to an active row. During the READ command, DDR_CAS drives low, DDR_WE and DDR_RAS remain high, the column address is driven on DDR_A[13:0], and the bank address is driven on DDR_BA[2:0].

The DDR2/mDDR memory controller uses a burst length of 8, and has a programmable CAS latency of 2, 3, 4, or 5. The CAS latency is three cycles in Figure 8. Read latency is equal to CAS latency plus additive latency. The DDR2/mDDR memory controller always configures the memory to have an additive latency of 0, so read latency equals CAS latency. Since the default burst size is 8, the DDR2/mDDR memory controller returns 8 pieces of data for every read command. If additional accesses are not pending to the DDR2/mDDR memory controller, the read burst completes and the unneeded data is disregarded. If additional accesses are pending, depending on the scheduling result, the DDR2/mDDR memory controller can terminate the read burst and start a new read burst. Furthermore, the DDR2/mDDR memory controller does not issue a DAB/DEAC command until page information becomes invalid.

Figure 8. DDR2/mDDR READ Command



2.3.5 Write (WRT) Command

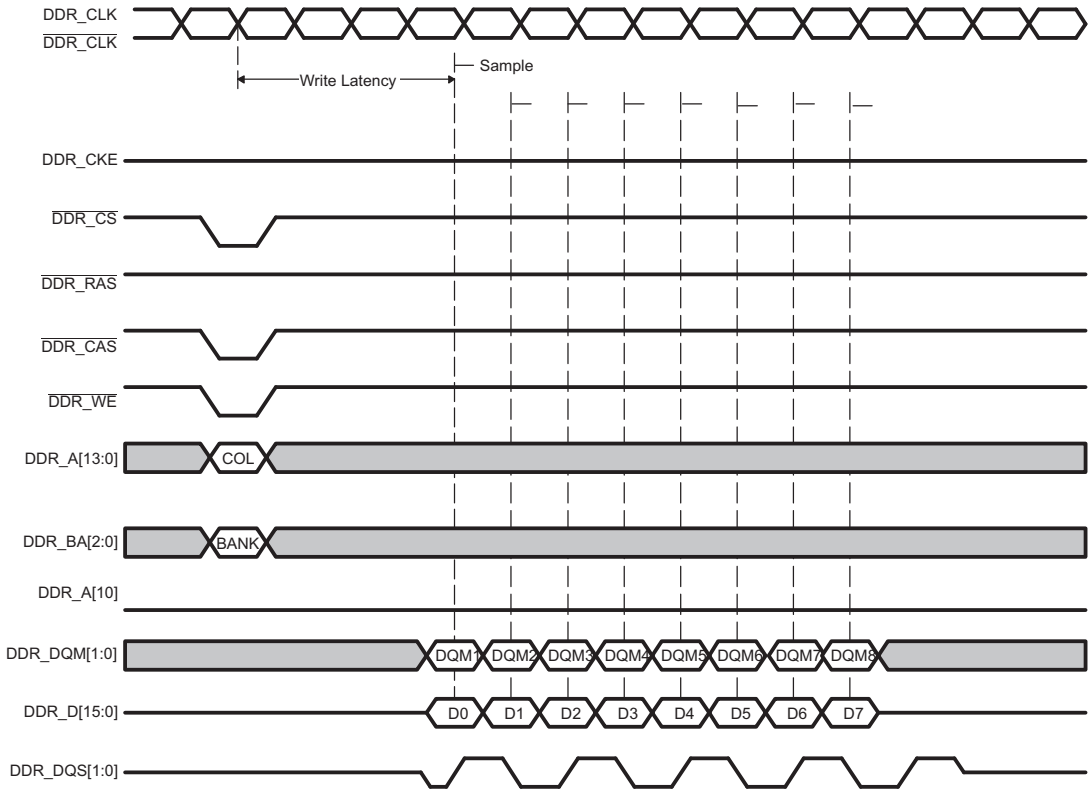
Prior to a WRT command, the desired bank and row are activated by the ACTV command. Following the WRT command, a write latency is incurred. For DDR2, write latency is equal to CAS latency minus 1 cycles. For mDDR, write latency is equal to 1 cycle, always. All writes have a burst length of 8. The use of the DDR_DQM outputs allows byte and halfword writes to be executed. Figure 9 shows the timing for a DDR2 write on the DDR2/mDDR memory controller.

If the transfer request is for less than 8 words, depending on the scheduling result and the pending commands, the DDR2/mDDR memory controller can:

- Mask out the additional data using DDR_DQM outputs
- Terminate the write burst and start a new write burst

The DDR2/mDDR memory controller does not perform the DEAC command until page information becomes invalid.

Figure 9. DDR2/mDDR WRT Command



NOTE: This diagrams shows write latency for DDR2. For mDDR, write latency is always equal to 1 cycle.

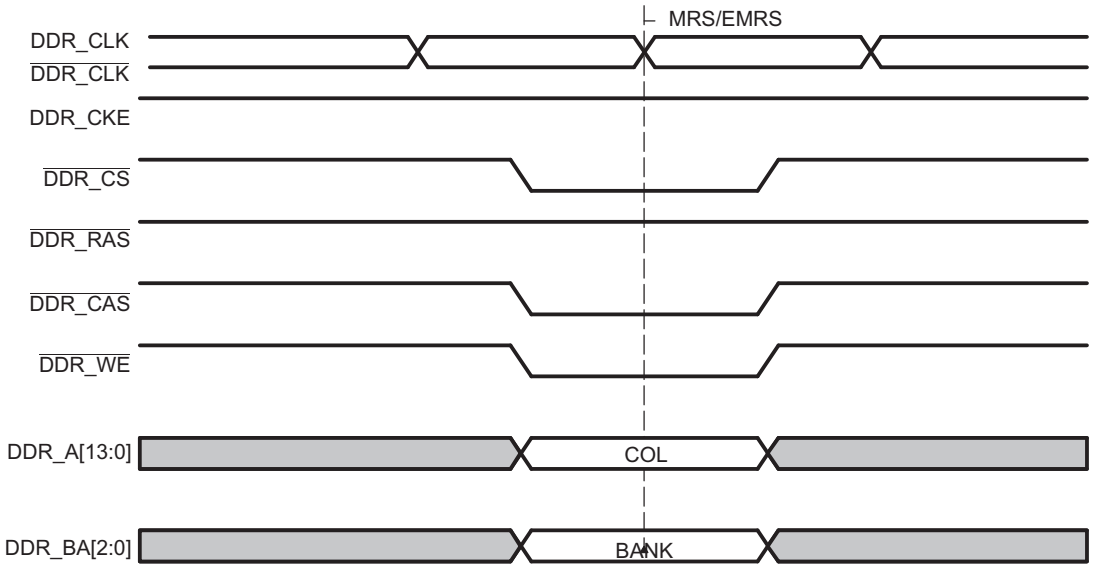
2.3.6 Mode Register Set (MRS and EMRS)

DDR2/mDDR SDRAM contains mode and extended mode registers that configure the DDR2/mDDR memory for operation. These registers control burst type, burst length, CAS latency, DLL enable/disable (on DDR2/mDDR device), single-ended strobe, differential strobe etc.

The DDR2/mDDR memory controller programs the mode and extended mode registers of the DDR2/mDDR memory by issuing MRS and EMRS commands. When the MRS or EMRS command is executed, the value on DDR_BA[2:0] selects the mode register to be written and the data on DDR_A[13:0] is loaded into the register. Figure 10 shows the timing for an MRS and EMRS command.

The DDR2/mDDR memory controller only issues MRS and EMRS commands during the DDR2/mDDR memory controller initialization sequence. See Section 2.13 for more information.

Figure 10. DDR2/mDDR MRS and EMRS Command



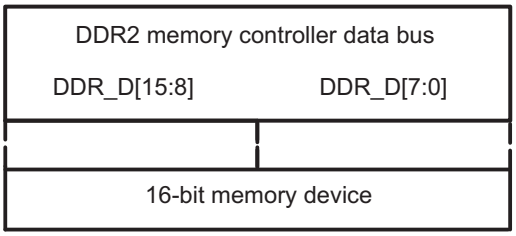
2.4 Memory Width and Byte Alignment

The DDR2/mDDR memory controller supports memory widths of 16 bits. Table 4 summarizes the addressable memory ranges on the DDR2/mDDR memory controller. Only little-endian format is supported. Figure 11 shows the byte lanes used on the DDR2/mDDR memory controller. The external memory is always right aligned on the data bus.

Table 4. Addressable Memory Ranges

Memory Width	Maximum addressable bytes per CS space	Description
×16	512 Mbytes	Halfword address

Figure 11. Byte Alignment



2.5 Address Mapping

The memory controller views the DDR2/mDDR SDRAM device as one continuous block of memory. The memory controller receives memory access requests with a 32-bit logical address, and it uses the logical address to generate a row, column, and bank address for accessing the DDR2/mDDR SDRAM device.

The memory controller supports two address mapping schemes: normal address mapping and special address mapping. Special address mapping is typically used only with mDDR devices using partial array self-refresh.

When the internal bank position (IBANKPOS) bit in the SDRAM configuration register (SDCR) is cleared, the memory controller operates with normal address mapping. In this case, the number of column and bank address bits is determined by the IBANK and PAGESIZE fields in SDCR. The number of row address bits is determined by the number of valid address pins for the device and does not need to be set in a register.

When IBANKPOS is set to 1, the memory controller operates with special address mapping. In this case, the number of column, row, and bank address bits is determined by the PAGESIZE, ROWSIZE, and IBANK fields. The ROWSIZE field is in the SDRAM configuration register 2 (SDCR2). See Table 5 for a descriptions of these bit fields.

Table 5. Configuration Register Fields for Address Mapping

Bit Field	Bit Value	Bit Description
IBANK		Defines the number of internal banks in the external DDR2/mDDR memory.
	0	1 bank
	1h	2 banks
	2h	4 banks
	3h	8 banks
PAGESIZE		Defines the page size of each page in the external DDR2/mDDR memory.
	0	256 words (requires 8 column address bits)
	1h	512 words (requires 9 column address bits)
	2h	1024 words (requires 10 column address bits)
	3h	2048 words (requires 11 column address bits)
ROWSIZE		Defines the row size of each row in the external DDR2/mDDR memory
	0	512 (requires 9 row address bits)
	1h	1024 (requires 10 row address bits)
	2h	2048 (requires 11 row address bits)
	3h	4096 (requires 12 row address bits)
	4h	8192 (requires 13 row address bits)
	5h	16384 (requires 14 row address bits)

2.5.1 Normal Address Mapping (IBANKPOS = 0)

As stated in Table 5, the IBANK and PAGESIZE fields of SDCR control the mapping of the logical, source address of the DDR2/mDDR memory controller to the DDR2/mDDR SDRAM row, column, and bank address bits. The DDR2/mDDR memory controller logical address always contains up to 14 row address bits, whereas the number of column and bank bits are determined by the IBANK and PAGESIZE fields. Table 6 show how the logical address bits map to the DDR2/mDDR SDRAM row, column, and bank bits for combinations of IBANK and PAGESIZE values. The same DDR2/mDDR memory controller pins provide the row and column address to the DDR2/mDDR SDRAM, thus the DDR2/mDDR memory controller appropriately shifts the address during row and column address selection.

Figure 12 shows how this address-mapping scheme organizes the DDR2/mDDR SDRAM rows, columns, and banks into the device memory-map. Note that during a linear access, the DDR2/mDDR memory controller increments the column address as the logical address increments. When the DDR2/mDDR memory controller reaches a page/row boundary, it moves onto the same page/row in the next bank. This movement continues until the same page has been accessed in all banks. To the DDR2/mDDR SDRAM, this process looks as shown in Figure 13.

By traversing across banks while remaining on the same row/page, the DDR2/mDDR memory controller maximizes the number of activated banks for a linear access. This results in the maximum number of open pages when performing a linear access being equal to the number of banks. Note that the DDR2/mDDR memory controller never opens more than one page per bank.

Ending the current access is not a condition that forces the active DDR2/mDDR SDRAM row to be closed. The DDR2/mDDR memory controller leaves the active row open until it becomes necessary to close it. This decreases the deactivate-reactivate overhead.

Table 6. Logical Address-to-DDR2/mDDR SDRAM Address Map for 16-bit SDRAM

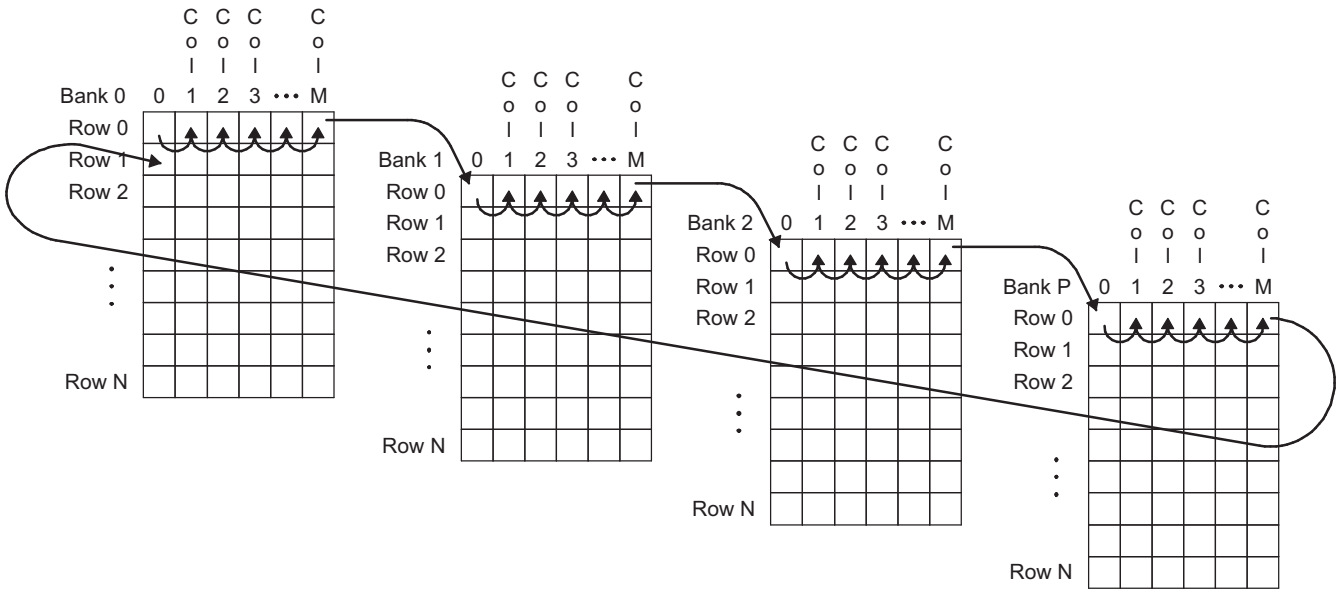
SDCR Bit		Logical Address																		
IBANK	PAGESIZE	31	30	29	28	27	26	25	24	23	22	21:15	14	13	12	11	10	9	8:1	0
0	0	-									nrb=14								ncb=8	
1	0	-								nrb=14								nbb=1	ncb=8	
2h	0	-							nrb=14								nbb=2		ncb=8	
3h	0	-						nrb=14								nbb=3			ncb=8	
0	1	-								nrb=14								ncb=9		
1	1	-							nrb=14								nbb=1	ncb=9		
2h	1	-						nrb=14								nbb=2		ncb=9		
3h	1	-					nrb=14								nbb=3			ncb=9		
0	2h	-							nrb=14								ncb=10			
1	2h	-						nrb=14								nbb=1	ncb=10			
2h	2h	-					nrb=14								nbb=2		ncb=10			
3h	2h	-				nrb=14								nbb=3			ncb=10			
0	3h	-						nrb=14								ncb=11				
1	3h	-					nrb=14								nbb=1	ncb=11				
2h	3h	-				nrb=14								nbb=2		ncb=11				
3h	3h	-			nrb=14								nbb=3			ncb=11				

Figure 12. Logical Address-to-DDR2/mDDR SDRAM Address Map

Col. 0	Col. 1	Col. 2	Col. 3	Col. 4	• • •	Col. M−1	Col. M	
					• • •			Row 0, bank 0
					• • •			Row 0, bank 1
					• • •			Row 0, bank 2
•	•	•	•	•	• • •	•	•	•
•	•	•	•	•	• • •	•	•	•
•	•	•	•	•	• • •	•	•	•
					• • •			Row 0, bank P
					• • •			Row 1, bank 0
					• • •			Row 1, bank 1
					• • •			Row 1, bank 2
•	•	•	•	•	• • •	•	•	•
•	•	•	•	•	• • •	•	•	•
•	•	•	•	•	• • •	•	•	•
					• • •			Row 1, bank P
					• • •			•
					• • •			•
					• • •			•
					• • •			Row N, bank 0
					• • •			Row N, bank 1
					• • •			Row N, bank 2
•	•	•	•	•	• • •	•	•	•
•	•	•	•	•	• • •	•	•	•
•	•	•	•	•	• • •	•	•	•
					• • •			Row N, bank P

NOTE: M is number of columns (as determined by PAGESIZE) minus 1, P is number of banks (as determined by IBANK) minus 1, and N is number of rows (as determined by both PAGESIZE and IBANK) minus 1.

Figure 13. DDR2/mDDR SDRAM Column, Row, and Bank Access



NOTE: M is number of columns (as determined by PAGESIZE) minus 1, P is number of banks (as determined by IBANK) minus 1, and N is number of rows (as determined by both PAGESIZE and IBANK) minus 1.

2.5.2 Special Address Mapping (IBANKPOS = 1)

When the internal bank position (IBANKPOS) bit is set to 1, the PAGESIZE, ROWSIZE, and IBANK fields control the mapping of the logical source address of the memory controller to the column, row, and bank address bits of the SDRAM device. Table 7 shows which source address bits map to the SDRAM column, row, and bank address bits for all combinations of PAGESIZE, ROWSIZE, and IBANK.

When IBANKPOS is set to 1, the effect of the address-mapping scheme is that as the source address increments across an SDRAM page boundary, the memory controller proceeds to the next page in the same bank. This movement along the same bank continues until all the pages have been accessed in the same bank. The memory controller then proceeds to the next bank in the device. This sequence is shown in Figure 14 and Figure 15.

Since, in this address mapping scheme, the memory controller can keep only one bank open, this scheme is lower in performance than the case when IBANKPOS is cleared to 0. Therefore, this case is only recommended to be used with Partial Array Self-refresh for mDDR SDRAM where performance may be traded-off for power savings.

Table 7. Address Mapping Diagram for 16-Bit SDRAM (IBANKPOS = 1)

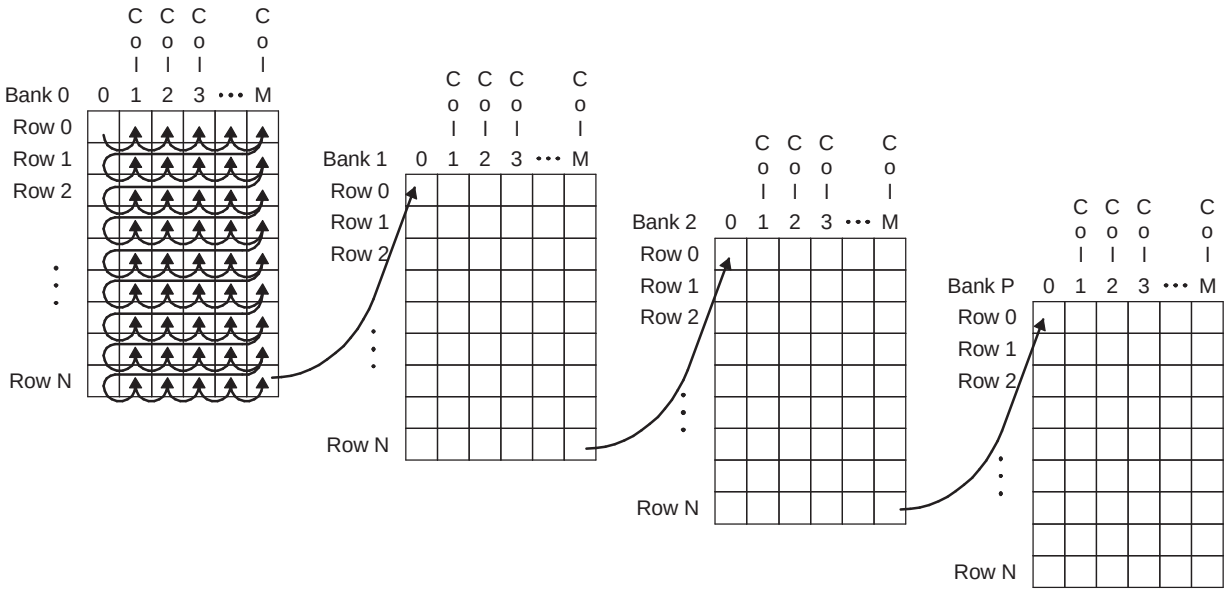
31	Source Address	1
Bank Address	**Row Address**	**Column Address**
Number of bank bits is defined by IBANK nbb = 1, 2, or 3	Number of row bits is defined by ROWSIZE: nrb = 9, 10, 11, 12, 13, or 14	Number of column bits is defined by PAGESIZE: ncb = 8, 9, 10, or 11

Figure 14. Address Mapping Diagram (IBANKPOS = 1)

Col. 0	Col. 1	Col. 2	Col. 3	Col. 4	• • •	Col. M−1	Col. M	
					• • •			Row 1, bank 0
					• • •			Row 2, bank 0
					• • •			Row 3, bank 0
•	•	•	•	•	• • •	•	•	•
•	•	•	•	•	• • •	•	•	•
•	•	•	•	•	• • •	•	•	•
					• • •			Row N, bank 0
					• • •			Row 1, bank 1
					• • •			Row 2, bank 1
					• • •			Row 3, bank 1
•	•	•	•	•	• • •	•	•	•
•	•	•	•	•	• • •	•	•	•
•	•	•	•	•	• • •	•	•	•
					• • •			Row N, bank 1
					• • •			•
					• • •			•
					• • •			•
					• • •			Row 1, bank P
					• • •			Row 2, bank P
					• • •			Row 3, bank P
•	•	•	•	•	• • •	•	•	•
•	•	•	•	•	• • •	•	•	•
•	•	•	•	•	• • •	•	•	•
					• • •			Row N, bank P

NOTE: M is number of columns (as determined by PAGESIZE) minus 1, P is number of banks (as determined by IBANK) minus 1, and N is number of rows (as determined by ROWSIZE) minus 1.

Figure 15. SDRAM Column, Row, Bank Access (IBANKPOS = 1)



NOTE: M is number of columns (as determined by PAGESIZE) minus 1, P is number of banks (as determined by IBANK) minus 1, and N is number of rows (as determined by ROWSIZE) minus 1.

2.6 DDR2/mDDR Memory Controller Interface

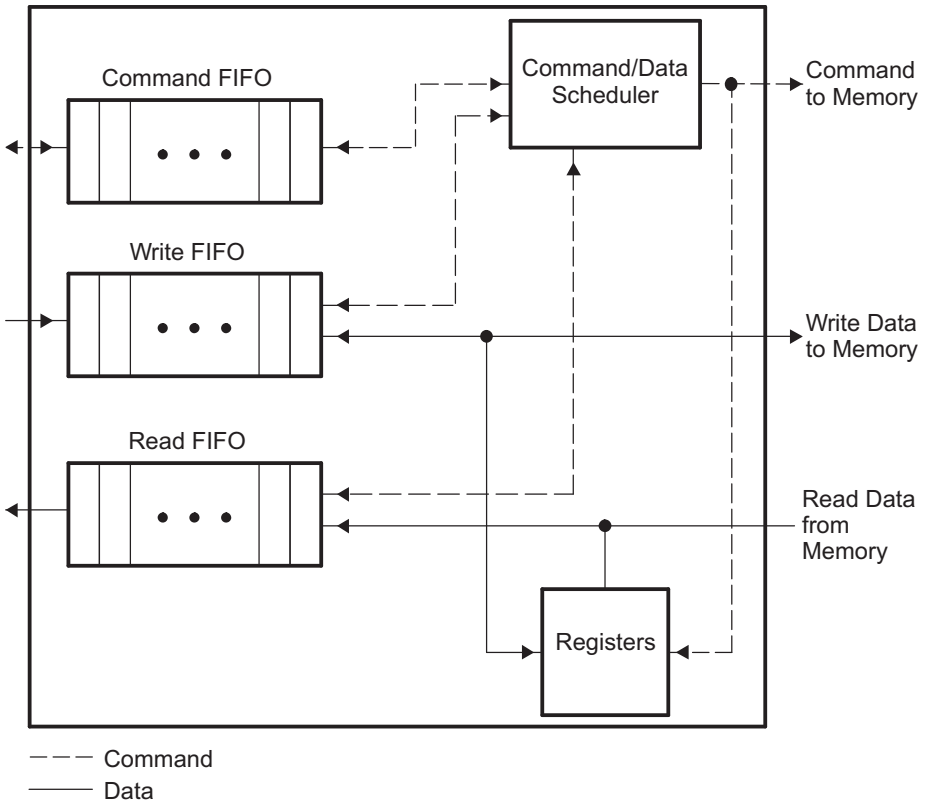
To move data efficiently from on-chip resources to external DDR2/mDDR SDRAM memory, the DDR2/mDDR memory controller makes use of a command FIFO, a write FIFO, a read FIFO, and command and data schedulers. Table 8 describes the purpose of each FIFO.

Figure 16 shows the block diagram of the DDR2/mDDR memory controller FIFOs. Commands, write data, and read data arrive at the DDR2/mDDR memory controller parallel to each other. The same peripheral bus is used to write and read data from external memory as well as internal memory-mapped registers.

Table 8. DDR2/mDDR Memory Controller FIFO Description

FIFO	Description	Depth (64-bit doublewords)
Command	Stores all commands coming from on-chip requestors	7
Write	Stores write data coming from on-chip requestors to memory	11
Read	Stores read data coming from memory to on-chip requestors	17

Figure 16. DDR2/mDDR Memory Controller FIFO Block Diagram



2.6.1 Command Ordering and Scheduling, Advanced Concept

The DDR2/mDDR memory controller performs command re-ordering and scheduling in an attempt to achieve efficient transfers with maximum throughput. The goal is to maximize the utilization of the data, address, and command buses while hiding the overhead of opening and closing DDR2/mDDR SDRAM rows. Command re-ordering takes place within the command FIFO.

Typically, a given master issues commands on a single priority. EDMA transfer controller read and write ports are different masters. The DDR2/mDDR memory controller first reorders commands from each master based on the following rules:

- Selects the oldest command (first command in the queue)
- Selects a read before a write if:
  - The read is to a different block address (2048 bytes) than the write
  - The read has greater or equal priority

The second bullet above may be viewed as an exception to the first bullet. This means that for an individual master, all of its commands will complete from oldest to newest, with the exception that a read may be advanced ahead of an older, lower or equal priority write. Following this scheduling, each master may have one command ready for execution.

Next, the DDR2/mDDR memory controller examines each of the commands selected by the individual masters and performs the following reordering:

- Among all pending reads, selects reads to rows already open. Among all pending writes, selects writes to rows already open.
- Selects the highest priority command from pending reads and writes to open rows. If multiple commands have the highest priority, then the DDR2/mDDR memory controller selects the oldest command.

The DDR2/mDDR memory controller may now have a final read and write command. If the Read FIFO is not full, then the read command will be performed before the write command, otherwise the write command will be performed first.

Besides commands received from on-chip resources, the DDR2/mDDR memory controller also issues refresh commands. The DDR2/mDDR memory controller attempts to delay refresh commands as long as possible to maximize performance while meeting the SDRAM refresh requirements. As the DDR2/mDDR memory controller issues read, write, and refresh commands to DDR2/mDDR SDRAM memory, it adheres to the following rules:

1. Refresh request resulting from the Refresh Must level of urgency being reached
2. Read request without a higher priority write (selected from above reordering algorithm)
3. Refresh request resulting from the Refresh Need level of urgency being reached
4. Write request (selected from above reordering algorithm)
5. Refresh request resulting from Refresh May level of urgency being reached
6. Request to enter self-refresh mode

The following results from the above scheduling algorithm:

- All writes from a single master will complete in order
- All reads from a single master will complete in order
- From the same master, any read to the same location (or within 2048 bytes) as a previous write will complete in order

2.6.2 Command Starvation

The reordering and scheduling rules listed above may lead to command starvation, which is the prevention of certain commands from being processed by the DDR2/mDDR memory controller. Command starvation results from the following conditions:

- A continuous stream of high-priority read commands can block a low-priority write command
- A continuous stream of DDR2/mDDR SDRAM commands to a row in an open bank can block commands to the closed row in the same bank.

To avoid these conditions, the DDR2/mDDR memory controller can momentarily raises the priority of the oldest command in the command FIFO after a set number of transfers have been made. The PR_OLD_COUNT bit in the peripheral bus burst priority register (PBBPR) sets the number of the transfers that must be made before the DDR2/mDDR memory controller will raise the priority of the oldest command.

2.6.3 Possible Race Condition

A race condition may exist when certain masters write data to the DDR2/mDDR memory controller. For example, if master A passes a software message via a buffer in DDR2/mDDR memory and does not wait for indication that the write completes, when master B attempts to read the software message it may read stale data and therefore receive an incorrect message. In order to confirm that a write from master A has landed before a read from master B is performed, master A must wait for the write completion status from the DDR2/mDDR memory controller before indicating to master B that the data is ready to be read. If master A does not wait for indication that a write is complete, it must perform the following workaround:

1. Perform the required write.
2. Perform a dummy write to the DDR2/mDDR memory controller SDRAM status register.
3. Perform a dummy read to the DDR2/mDDR memory controller SDRAM status register.
4. Indicate to master B that the data is ready to be read after completion of the read in step 3. The completion of the read in step 3 ensures that the previous write was done.

The EDMA peripheral does not need to implement the above workaround. The above workaround is required for all other peripherals. See your device-specific data manual for more information.

2.7 Refresh Scheduling

The DDR2/mDDR memory controller issues autorefresh (REFR) commands to DDR2/mDDR SDRAM devices at a rate defined in the refresh rate (RR) bit field in the SDRAM refresh control register (SDRCR). A refresh interval counter is loaded with the value of the RR bit field and decrements by 1 each cycle until it reaches zero. Once the interval counter reaches zero, it reloads with the value of the RR bit. Each time the interval counter expires, a refresh backlog counter increments by 1. Conversely, each time the DDR2/mDDR memory controller performs a REFR command, the backlog counter decrements by 1. This means the refresh backlog counter records the number of REFR commands the DDR2/mDDR memory controller currently has outstanding.

The DDR2/mDDR memory controller issues REFR commands based on the level of urgency. The level of urgency is defined in Table 9. Whenever the refresh must level of urgency is reached, the DDR2/mDDR memory controller issues a REFR command before servicing any new memory access requests. Following a REFR command, the DDR2/mDDR memory controller waits T_RFC cycles, defined in the SDRAM timing register 1 (SDTIMR1), before rechecking the refresh urgency level.

In addition to the refresh counter previously mentioned, a separate backlog counter ensures the interval between two REFR commands does not exceed 8× the refresh rate. This backlog counter increments by 1 each time the interval counter expires and resets to zero when the DDR2/mDDR memory controller issues a REFR command. When this backlog counter is greater than 7, the DDR2/mDDR memory controller issues four REFR commands before servicing any new memory requests.

The refresh counters do not operate when the DDR2/mDDR memory is in self-refresh mode.

Table 9. Refresh Urgency Levels

Urgency Level	Description
Refresh May	Backlog count is greater than 0. Indicates there is a backlog of REFR commands, when the DDR2/mDDR memory controller is not busy it will issue the REFR command.
Refresh Release	Backlog count is greater than 3. Indicates the level at which enough REFR commands have been performed and the DDR2/mDDR memory controller may service new memory access requests.
Refresh Need	Backlog count is greater than 7. Indicates the DDR2/mDDR memory controller should raise the priority level of a REFR command above servicing a new memory access.
Refresh Must	Backlog count is greater than 11. Indicates the level at which the DDR2/mDDR memory controller should perform a REFR command before servicing new memory access requests.

2.8 Self-Refresh Mode

Clearing the self refresh/low power (SR_PD) bit to 0 and then setting the low power mode enable (LPMODEN) bit to 1 in the SDRAM refresh control register (SDRCR) , forces the DDR2/mDDR memory controller to place the external DDR2/mDDR SDRAM in a low-power mode (self refresh), in which the DDR2/mDDR SDRAM maintains valid data while consuming a minimal amount of power. When the LPMODEN bit is set to 1, the DDR2/mDDR memory controller continues normal operation until all outstanding memory access requests have been serviced and the refresh backlog has been cleared. At this point, all open pages of DDR2/mDDR SDRAM are closed and a self-refresh (SLFRFR) command (an autorefresh command with self refresh/low power) is issued.

The memory controller exits the self-refresh state when a memory access is received, when the LPMODEN bit in SDRCR is cleared to 0, or when the SR_PD bit in SDRCR changed to 1. While in the self-refresh state, if a request for a memory access is received, the DDR2/mDDR memory controller services the memory access request, returning to the self-refresh state upon completion. The DDR2/mDDR memory controller will not wake up from the self-refresh state (whether from a memory access request, from clearing the LPMODEN bit, or from clearing the SR_PD bit) until T_CKE + 1 cycles have expired since the self-refresh command was issued. The value of T_CKE is defined in the SDRAM timing register 2 (SDTIMR2).

In the case of DDR2, after exiting from the self-refresh state, the memory controller will not immediately start executing commands. Instead, it will wait T_SXNR + 1 clock cycles before issuing non-read/write commands and T_SXRD + 1 clock cycles before issuing read or write commands. The SDRAM timing register 2 (SDTIMR2) programs the values of T_SXNR and T_SXRD.

In the case of mDDR, after exiting from the self-refresh state, the memory controller will not immediately start executing commands. Instead, it will wait T_SXNR+1 clock cycles and then execute auto-refresh command before issuing any other commands. The SDRAM timing register 2 (SDTIMR2) programs the value of T_SXNR.

Once in self-refresh mode, the DDR2/mDDR memory controller input clocks (VCLK and 2X_CLK) may be gated off or changed in frequency. Stable clocks must be present before exiting self-refresh mode. See Section 2.16 for more information describing the proper procedure to follow when shutting down DDR2/mDDR memory controller input clocks.

See Section 2.16.1 for a description of the self-refresh programming sequence.

2.9 Partial Array Self Refresh for Mobile DDR

For additional power savings during self-refresh, the partial array self-refresh (PASR) feature of the mDDR allows you to select the amount of memory that will be refreshed during self-refresh. Use the partial array self-refresh (PASR) bit field in the SDRAM configuration register 2 (SDCR2) to select the amount of memory to refresh during self-refresh. As shown in Table 10 you may select either 4, 2, 1, 1/2, or 1/4 bank(s). The PASR bits are loaded into the extended mode register of the mDDR device, during autoinitialization (see Section 2.13).

The mDDR performs bank interleaving when the internal bank position (IBANKPOS) bit in SDRAM configuration register (SDCR) is cleared to 0. Since the SDRAM banks are only partially refreshed during partial array self-refresh, it is recommended that you set IBANKPOS to 1 to avoid bank interleaving. When IBANKPOS is cleared to 0, it is the responsibility of software to move critical data into the banks that are to be refreshed during partial array self-refresh. Refer to Section 2.5.2 for more information on IBANKPOS and addressing mapping in general.

Table 10. Configuration Bit Field for Partial Array Self-refresh

Bit Field	Bit Value	Bit Description
PASR		Partial array self refresh.
	0	Refresh banks 0, 1, 2, and 3
	1h	Refresh banks 0 and 1
	2h	Refresh bank 0
	5h	Refresh 1/2 of bank 0
	6h	Refresh 1/4 of bank 0

2.10 Power-Down Mode

Setting the self-refresh/low power (SR_PD) bit and the low-power mode enable (LPMODEN) bit in the SDRAM refresh control register (SDRCR) to 1, forces the DDR2/mDDR memory controller to place the external DDR2 SDRAM in the power-down mode. When the LPMODEN bit is asserted, the DDR2/mDDR memory controller continues normal operation until all outstanding memory access requests have been serviced and the refresh backlog has been cleared. At this point, all open pages of DDR2 SDRAM are closed and a Power Down command (same as NOP command but driving DDR_CKE low on the same cycle) is issued.

The DDR2/mDDR memory controller exits the power-down state when a memory access is received, when a Refresh Must level is reached, when the LPMODEN bit in SDRCR is cleared to 0, or when the SR_PD bit in SDRCR changed to 0. While in the power-down state, if a request for a memory access is received, the DDR2/mDDR memory controller services the memory access request, returning to the power-down state upon completion. The DDR2/mDDR memory controller will not wake-up from the power-down state (whether from a memory access request, from reaching a Refresh Must level, from clearing the LPMODEN bit, or from clearing the SR_PD bit) until T_CKE + 1 cycles have expired since the power-down command was issued. The value of T_CKE is defined in the SDRAM timing register 2 (SDTIMR2).

After exiting from the power-down state, the DDR2/mDDR memory controller will drive DDR_CKE high and then not immediately start executing commands. Instead, it will wait T_XP + 1 clock cycles before issuing commands. The SDRAM timing register 2 (SDTIMR2) programs the values of T_XP.

See Section 2.16.1 for a description of the power-down mode programming sequence.

Note: Power-down mode is best suited as a power savings mode when SDRAM is being used intermittently and the system requires power savings as well as a short recovery time. You may use self-refresh mode if you desire additional power savings from disabling clocks.

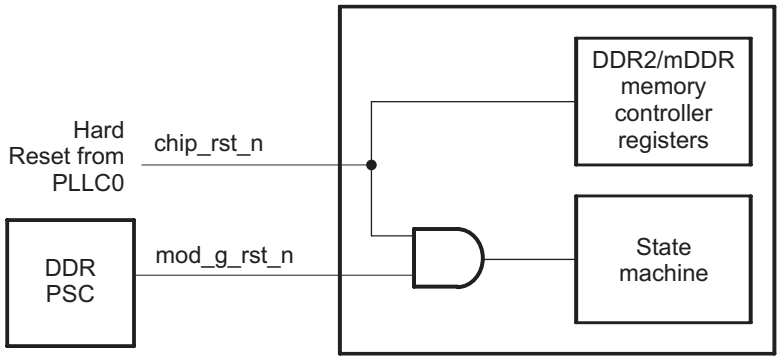
2.11 Reset Considerations

The DDR2/mDDR memory controller has two reset signals, chip_rst_n and mod_g_rst_n. The chip_rst_n is a module-level reset that resets both the state machine as well as the DDR2/mDDR memory controller memory-mapped registers. The mod_g_rst_n resets the state machine only; it does not reset the controller's registers, which allows soft reset (from PSC or WDT) to reset the module without resetting the configuration registers and reduces the programming overhead for setting up access to the DDR2/mDDR device. If the DDR2/mDDR memory controller is reset independently of other peripherals, the user's software should not perform memory, as well as register accesses, while chip_rst_n or mod_g_rst_n are asserted. If memory or register accesses are performed while the DDR2/mDDR memory controller is in the reset state, other masters may hang. Following the rising edge of chip_rst_n or mod_g_rst_n, the DDR2/mDDR memory controller immediately begins its initialization sequence. Command and data stored in the DDR2/mDDR memory controller FIFOs are lost. Table 11 describes the different methods for asserting each reset signal. The Power and Sleep Controller (PSC) acts as a master controller for power management for all of the peripherals on the device. For detailed information on power management procedures using the PSC, see your device-specific *System Reference Guide*. Figure 17 shows the DDR2/mDDR memory controller reset diagram.

Table 11. Reset Sources

Reset Signal	Reset Source
chip_rst_n	Hardware/device reset
mod_g_rst_n	Power and sleep controller

Figure 17. DDR2/mDDR Memory Controller Reset Block Diagram



2.12 VTP IO Buffer Calibration

The DDR2/mDDR memory controller is able to control the impedance of the output IO. This feature allows the DDR2/mDDR memory controller to tune the output impedance of the IO to match that of the PCB board. Control of the output impedance of the IO is an important feature because impedance matching reduces reflections, creating a cleaner board design. Calibrating the output impedance of the IO will also reduce the power consumption of the DDR2/mDDR memory controller. The calibration is performed with respect to voltage, temperature, and process (VTP). The VTP information obtained from the calibration is used to control the output impedance of the IO.

The impedance of the output IO is selected by the value of a reference resistor connected to pin DDR_ZP. The DDR2/mDDR reference design requires the reference resistor to be a 50 ohm, 0.5% tolerance, 1/16th watt resistor (49.9 ohm, 0.5% tolerance is acceptable).

The VTP IO control register (VTPIO_CTL) is written to begin the calibration process. The VTP calibration process is described in the DDR2/mDDR initialization sequence in Section 2.13.2.

Note: VTP IO calibration must be performed following device power up and device reset. If the DDR2/mDDR memory controller is reset via the Power and Sleep Controller (PSC) and the VTP input clock is disabled, accesses to the DDR2/mDDR memory controller will not complete. To re-enable accesses to the DDR2/mDDR memory controller, enable the VTP input clock and then perform the VTP calibration sequence again.

2.13 Auto-Initialization Sequence

The DDR2/mDDR SDRAM contains mode and extended mode registers that configure the DDR2/mDDR memory for operation. These registers control burst type, burst length, CAS latency, DLL enable/disable (on the DDR2/mDDR device), single-ended strobe, differential strobe, etc. The DDR2/mDDR memory controller programs the mode and extended mode registers of the DDR2/mDDR memory by issuing MRS and EMRS commands during the initialization sequence. The SDRAMEN, MSDRAMEN, DDREN, and DDR2EN bits in the SDRAM configuration register (SDCR) determine if the DDR2/mDDR memory controller will perform a DDR2 or mobile DDR initialization sequence. Set these bits as follows for DDR2: SDRAMEN = 1, MSDRAMEN = 0, DDREN = 1, DDR2EN = 1. Set these bits as follow for mDDR: SDRAMEN = 1, MSDRAMEN = 1, DDREN = 1, DDR2EN = 0. The DDR2 initialization sequence performed by the DDR2/mDDR memory controller is compliant with the JESDEC79-2A specification and the mDDR initialization sequence is compliant with mDDR. The DDR2/mDDR memory controller performs an initialization sequence under the following conditions:

- Following reset (rising edge of chip_rst_n or mod_g_rst_n)
- Following a write to the DDRDRIVE, CL, IBANK, or PAGESIZE bit fields in the SDRAM configuration register (SDCR)

During the initialization sequence, the memory controller issues MRS and EMRS commands that configure the DDR2/mobile DDR SDRAM mode register and extended mode register 1. The register values for DDR2 are described in Table 12 and Table 13, and the register values for mDDR are described in Table 14 and Table 15. The extended mode registers 2 and 3 are configured with a value of 0h. At the end of the initialization sequence, the memory controller performs an autorefresh cycle, leaving the memory controller in an idle state with all banks deactivated.

When a reset occurs, the DDR2/mDDR memory controller immediately begins the initialization sequence. Under this condition, commands and data stored in the DDR2/mDDR memory controller FIFOs will be lost. However, when the initialization sequence is initiated by a write to the two least-significant bytes in SDCR, data and commands stored in the DDR2/mDDR memory controller FIFOs will not be lost and the DDR2/mDDR memory controller will ensure read and write commands are completed before starting the initialization sequence.

Table 12. DDR2 SDRAM Configuration by MRS Command

Memory Controller Address Bus	Value	DDR2/mDDR SDRAM Register Bit	DDR2/mDDR SDRAM Field	Function Selection
DDR_A[12]	0	12	Power Down Exit	Fast exit
DDR_A[11:9]	t_WR	11:9	Write Recovery	Write recovery from autoprecharge. Value of 2, 3, 4, 5, or 6 is programmed based on value of the T_WR bit in the SDRAM timing register 1 (SDTIMR1).
DDR_A[8]	0	8	DLL Reset	Out of reset
DDR_A[7]	0	7	Mode: Test or Normal	Normal mode
DDR_A[6:4]	CL bit	6:4	CAS Latency	Value of 2, 3, 4, or 5 is programmed based on value of the CL bit in the SDRAM configuration register (SDCR).
DDR_A[3]	0	3	Burst Type	Sequential
DDR_A[2:0]	3h	2:0	Burst Length	Value of 8

Table 13. DDR2 SDRAM Configuration by EMRS(1) Command

Memory Controller Address Bus	Value	DDR2/mDDR SDRAM Register Bit	DDR2/mDDR SDRAM Field	Function Selection
DDR_A[12]	0	12	Output Buffer Enable	Output buffer enable
DDR_A[11]	0	11	RDQS Enable	RDQS disable
DDR_A[10]	1	10	$\overline{\text{DQS}}$ enable	Disables differential DQS signaling.
DDR_A[9:7]	0	9:7	OCD Calibration Program	Exit OCD calibration
DDR_A[6]	0	6	ODT Value (Rtt)	Cleared to 0 to select 75 ohms. This feature is not supported because the DDR_ODT signal is not pinned out.
DDR_A[5:3]	0	5:3	Additive Latency	0 cycles of additive latency
DDR_A[2]	1	2	ODT Value (Rtt)	Set to 1 to select 75 ohms. This feature is not supported because the DDR_ODT signal is not pinned out.
DDR_A[1]	DDRDRIVE[0]	1	Output Driver Impedance	Value of 0 or 1 is programmed based on value of DDRDRIVE0 bit in SDRAM configuration register (SDCR).
DDR_A[0]	0	0	DLL enable	DLL enable

Table 14. Mobile DDR SDRAM Configuration by MRS Command

Memory Controller Address Bus	Value	mDDR SDRAM Register Bit	mDDR SDRAM Field	Function Selection
DDR_A[11:7]	0	11:7	Operating mode	Normal operating mode
DDR_A[6:4]	CL bit	6:4	CAS Latency	Value of 2 or 3 is programmed based on value of CL bit in SDRAM configuration register (SDCR).
DDR_A[3]	0	3	Burst Type	Sequential
DDR_A[2:0]	3h	2:0	Burst Length	Value of 8

Table 15. Mobile DDR SDRAM Configuration by EMRS(1) Command

Memory Controller Address Bus	Value	mDDR SDRAM Register Bit	mDDR SDRAM Field	Function Selection
DDR_A[11:7]	0	11:7	Operating Mode	Normal operating mode
DDR_A[6:5]	DDRDRIVE[1:0]	6:5	Output Driver Impedance	Value of 0, 1, 2, or 3 is programmed based on value of DDRDRIVE[1:0] bits in SDRAM configuration register (SDCR).
DDR_A[4:3]	0	4:3	Temperature Compensated Self Refresh	Value of 0
DDR_A[2:0]	PASR bits	2:0	Partial Array Self Refresh	Value of 0, 1, 2, 5, or 6 is programmed based on value of PASR bits in SDRAM configuration register 2 (SDCR2).

2.13.1 Initializing Configuration Registers

Perform the following steps when configuring the DDR2/mDDR memory controller memory-mapped registers:

1. Program the read latency (RL) bit in the DDR PHY control register (DRPYC1R) to the desired value.
2. Program the SDRAM configuration register (SDCR) with BOOTUNLOCK bit set to 1 (unlocked).
3. Program the SDRAM configuration register (SDCR) to the desired value with the BOOTUNLOCK cleared to 0 and the TIMUNLOCK bit set to 1 (unlocked).
4. For mDDR only, program the SDRAM configuration register 2 (SDCR2) to the desired value.
5. Program the SDRAM timing register 1 (SDTIMR1) and SDRAM timing register 2 (SDTIMR2) to the desired values to meet the DDR2/mDDR SDRAM memory data sheet specification.
6. Program SDCR to the desired value with the TIMUNLOCK bit cleared to 0 (locked).
7. Program the RR bit in the SDRAM refresh control register (SDRCR) to the desired value to meet the refresh requirements of the DDR2/mDDR SDRAM memory.

Note: Before accessing the DDR2/mDDR memory controller registers, you must complete VTP initialization. Accessing the DDR2/mDDR memory controller registers prior to VTP initialization will result in a bus lock-up condition. See Section 2.13.2 for the overall initialization sequence.

2.13.2 Initializing Following Device Power Up and Device RESET

Following device power up, the DDR2/mDDR memory controller is held in reset with the internal clocks to the module gated off. Before releasing the DDR2/mDDR memory controller from reset, the clocks to the module must be turned on. Perform the following steps when turning the clocks on and initializing the module:

1. Program PLLC1 registers to start 2X_CLK. For information on programming PLLC1, see your device-specific *System Reference Guide*.
2. Program Power and Sleep Controller (PSC) to enable the DDR2/mDDR memory controller VCLK.
3. Perform VTP IO calibration
   a. Clear CLKRZ, LOCK, and POWERDN bits in the VTP IO control register (VTPIO_CTL) and wait at least 1 reference clock cycle. You must wait at least 1 reference clock cycle for the CLKRZ to take affect. The reference clock is the clock at MXI/MXO.
   b. Set CLKRZ bit in VTPIO_CTL.
   c. Poll READY bit in VTPIO_CTL until it changes to logic-high.
   d. Set IOPWRDN bit in VTPIO_CTL.
   e. Set LOCK bit in VTPIO_CTL.
   f. Set POWERDN bit in VTPIO_CTL to save power. VTP is locked and no dynamic calibration will happen.
4. Configure the DDR PHY control register 1 (DRPYC1R). All of the following steps may be done in a single register write to DRPYC1R.
   a. Set the EXT_STRBEN bit to 1 to select external DQS strobe gating.
   b. Program the RL bit to the required value.
5. Program the Power and Sleep Controller (PSC) to reset (synchReset) the DDR2/mDDR memory controller.
6. Configure the peripheral bus burst priority register (PBBPR). You must change its default value. See Section 4.8.
7. Follow the register initialization procedure described in Section 2.13.1 to complete the DDR2/mDDR memory controller configuration.

Note: If the DDR2/mDDR memory controller is reset via the Power and Sleep Controller (PSC) and the VTP input clock is disabled, accesses to the DDR2/mDDR memory controller will not complete. To re-enable accesses to the DDR2/mDDR memory controller, enable the VTP input clock and then perform the VTP calibration sequence again.

2.14 Interrupt Support

The DDR2/mDDR memory controller supports two addressing modes, linear incrementing and cache line wrap. Upon receipt of an access request for an unsupported addressing mode, the DDR2/mDDR memory controller generates an interrupt by setting the LT bit in the interrupt raw register (IRR). The DDR2/mDDR memory controller will then treat the request as a linear incrementing request.

This interrupt is called the line trap interrupt and is the only interrupt the DDR2/mDDR memory controller supports. It is an active-high interrupt and is enabled by the LTMSET bit in the interrupt mask set register (IMSR). This interrupt is mapped to the CPU and is muxed with RTCINT.

2.15 DMA Event Support

The DDR2/mDDR memory controller is a DMA slave peripheral and therefore does not generate DMA events. Data read and write requests may be made directly by masters and by the DMA.

2.16 Power Management

Power dissipation from the DDR2/mDDR memory controller may be managed by the following methods:

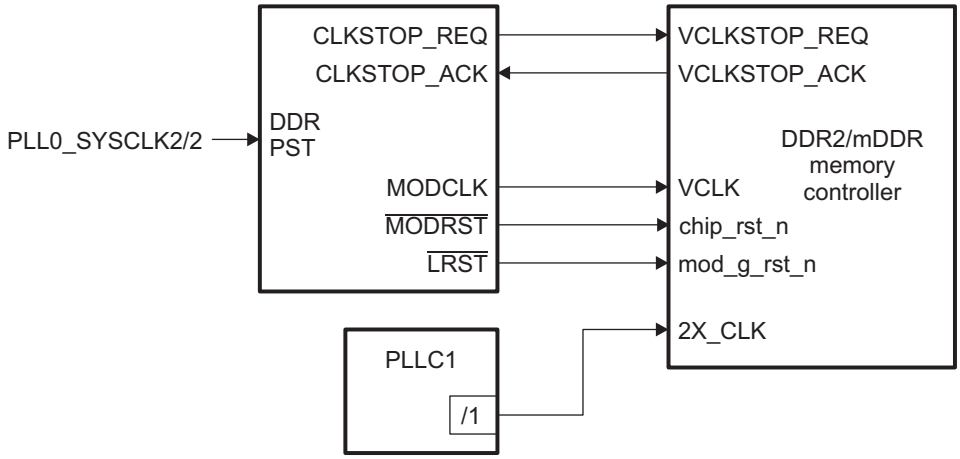
- Self-refresh mode (see Section 2.8)
- Power-down mode (see Section 2.10)
- Disabling the DDR PHY to reduce power

  The DDR2/mDDR memory controller supports low-power modes where the DLL internal to the PHY and the receivers at the I/O pins can be disabled. These functions are controlled through the DDR2/mDDR memory controller. Even if the PHY is active, the receivers can be configured to disable whenever writes are in progress and the receivers are not needed.
- Gating input clocks to the module off

  Gating input clocks off to the DDR2/mDDR memory controller achieves higher power savings when compared to the power savings of self-refresh mode and power-down mode. The input clocks are turned off outside of the DDR2/mDDR memory controller through the use of the Power and Sleep Controller (PSC) and the PLL controller 1 (PLLC1). Figure 18 shows the connections between the DDR2/mDDR memory controller, PSC, and PLLC1. For detailed information on power management procedures using the PSC, see your device-specific *System Reference Guide*.

  Before gating clocks off, the DDR2/mDDR memory controller must place the DDR2/mDDR SDRAM memory in self-refresh mode. If the external memory requires a continuous clock, the DDR2/mDDR memory controller clock provided by PLLC1 must not be turned off because this may result in data corruption. See the following subsections for the proper procedures to follow when stopping the DDR2/mDDR memory controller clocks. Once the clocks are stopped, to re-enable the clocks follow the clock stop procedure in each respective subsection in reverse order.

Figure 18. DDR2/mDDR Memory Controller Power Sleep Controller Diagram



2.16.1 DDR2/mDDR Memory Controller Clock Stop Procedure

Note: If a data access occurs to the DDR2/mDDR memory after completing steps 1-4, the DLL will wake up and lock, then the MCLK will turn on and the access will be performed. Following steps 5 and 6, in which the clocks are disabled , all DDR2/mDDR memory accesses are not possible until the clocks are reenabled.

In power-down mode, the DDR2/mDDR memory controller input clocks (VCLK and 2X_CLK) may not be gated off. This is a limitation of the DDR2/mDDR controller. For this reason, power-down mode is best suited as a power savings mode when SDRAM is being used intermittently and the system requires power savings as well as a short recovery time. You may use self-refresh mode if you desire additional power savings from disabling clocks.

To achieve maximum power savings VCLK, MCLK, 2X_CLK, DDR_CLK, and $\overline{\text{DDR\_CLK}}$ should be gated off. The procedure for clock gating is described in the following steps.

1. Allow software to complete the desired DDR transfers.
2. Change the SR_PD bit to 0 and set the LPMODEN bit in the DDR2 SDRAM refresh control register (SDRCR) to enable self-refresh mode. The DDR2/mDDR memory controller will complete any outstanding accesses and backlogged refresh cycles and then place the external DDR2/mDDR memory in self-refresh mode.
3. Set the MCLKSTOPEN bit in SDRCR. This enables the DDR2/mDDR memory controller to shut off the MCLK.
4. Poll the PHYRDY bit in the SDRAM status register (SDRSTAT) to be a logic-low indicating that the MCLK has been stopped.
5. Program the PSC to disable the DDR2/mDDR memory controller VCLK. You must not disable VCLK in power-down mode; use only for self-refresh mode (see notes in this section).
6. Program PLLC1 registers to stop 2X_CLK to DDR2/mDDR memory controller, as well as DDR_CLK and $\overline{\text{DDR\_CLK}}$. You must note disable 2X_CLK in power-down mode; use only for self-refresh mode (see notes in this section). For information on programming PLLC1, see your device-specific *System Reference Guide*.

To turn clocks back on:

1. Program PLLC1 registers to start 2X_CLK to the DDR2/mDDR memory controller.
2. Once 2X_CLK is stable, program the PSC to enable VCLK.
3. Clear the MCLKSTOPEN bit in SDRCR to 0.
4. Clear the LPMODEN bit in the DDR2 SDRAM refresh control register (SDRCR) to 0.

2.17 Emulation Considerations

The DDR2/mDDR memory controller will remain fully functional during emulation halts to allow emulation access to external memory.

Note: VTP IO calibration must be performed before emulation tools attempt to access the register or data space of the DDR2/mDDR memory controller. A bus lock-up condition will occur if the emulation tool attempts to access the register or data space of the DDR2/mDDR memory controller before completing VTP IO calibration. See Section 2.12 for information on VTP IO calibration.

3 Supported Use Cases

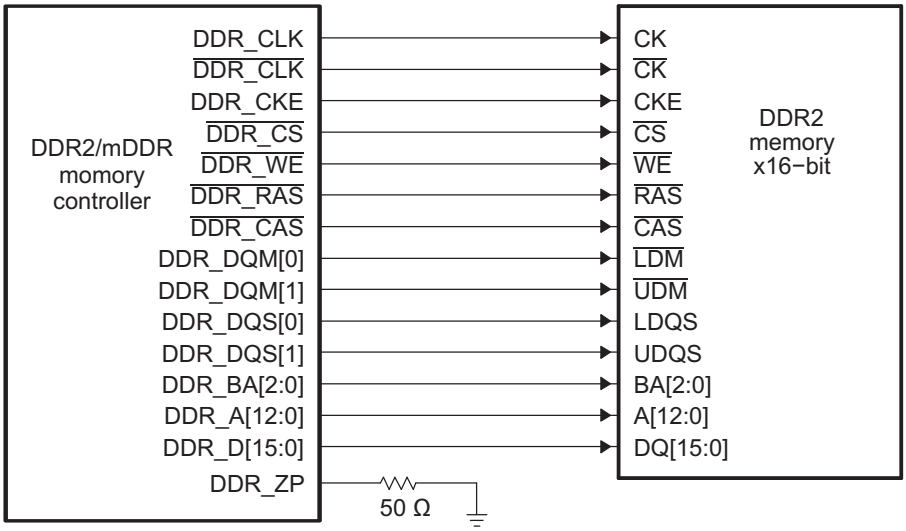
The DDR2/mDDR memory controller allows a high degree of programmability for shaping DDR2/mDDR accesses. The programmability inherent to the DDR2/mDDR memory controller provides the DDR2/mDDR memory controller with the flexibility to interface with a variety of DDR2/mDDR devices. By programming the SDRAM configuration register (SDCR), SDRAM refresh control register (SDRCR), SDRAM timing register 1 (SDTIMR1), and SDRAM timing register 2 (SDTIMR2), the DDR2/mDDR memory controller can be configured to meet the data sheet specification for JESD79D-2A compliant DDR2 SDRAM as well as mDDR memory devices.

This section presents an example describing how to interface the DDR2 memory controller to a JESD79D DDR2/mDDR-400 512-Mbyte device. The DDR2/mDDR memory controller is assumed to be operating at 150 MHz. A similar procedure can be followed when interfacing to a mDDR memory device.

3.1 Connecting the DDR2/mDDR Memory Controller to DDR2/mDDR Memory

Figure 19 shows how to connect the DDR2/mDDR memory controller to a DDR2 device. Figure 19 displays a 16-bit interface; you can see that all signals are point-to-point connection.

Figure 19. Connecting DDR2/mDDR Memory Controller to a 16-Bit DDR2 Memory



3.2 Configuring Memory-Mapped Registers to Meet DDR2 Specification

As previously stated, four memory-mapped registers must be programmed to configure the DDR2/mDDR memory controller to meet the data sheet specification of the attached DDR2/mDDR device. The registers are:

- SDRAM configuration register (SDCR)
- SDRAM refresh control register (SDRCR)
- SDRAM timing register 1 (SDTIMR1)
- SDRAM timing register 2 (SDTIMR2)

In addition to these registers, the DDR PHY control register (DRPYC1R) must also be programmed. The configuration of DRPYC1R is not dependent on the DDR2 device specification but rather on the board layout.

The following sections describe how to configure each of these registers. See Section 4 for more information on the DDR2/mDDR memory controller registers.

Note: When interfacing the DDR2/mDDR memory controller to a mDDR device, the SDRAM configuration register 2 (SDCR2) must be programmed in addition to the registers mentioned above.

3.2.1 Configuring SDRAM Configuration Register (SDCR)

The SDRAM configuration register (SDCR) contains register fields that configure the DDR2/mDDR memory controller to match the data bus width, CAS latency, number of banks, and page size of the attached memory. In this example, we assume the following DDR2 configuration:

- Data bus width = 16 bits
- CAS latency = 3
- Number of banks = 8
- Page size = 1024 words

Table 16 shows the resulting SDCR configuration. Note that the value of the TIMING_UNLOCK field is dependent on whether or not it is desirable to unlock SDTIMR1 and SDTIMR2. The TIMING_UNLOCK bit should only be set to 1 when the SDTIMR1 and SDTIMR2 needs to be updated.

Table 16. SDCR Configuration

Field	Value	Function Selection
TIMING_UNLOCK	x	Set to 1 to unlock the SDRAM timing register 1 and SDRAM timing register 2. Cleared to 0 to lock the SDRAM timing register 1 and SDRAM timing register 2.
NM	1h	To configure the DDR2/mDDR memory controller for a 16-bit data bus width.
CL	3h	To select a CAS latency of 3.
IBANK	3h	To select 8 internal DDR2 banks.
PAGESIZE	2h	To select 1024-word page size.

3.2.2 Configuring SDRAM Refresh Control Register (SDRCR)

The SDRAM refresh control register (SDRCR) configures the DDR2/mDDR memory controller to meet the refresh requirements of the attached memory device. SDRCR also allows the DDR2/mDDR memory controller to enter and exit self refresh and enable and disable the MCLK stopping. In this example, we assume that the DDR2/mDDR memory controller is not is in self-refresh mode or power-down mode and that MCLK stopping is disabled.

The RR field in SDRCR is defined as the rate at which the attached memory device is refreshed in DDR2/mDDR cycles. The value of this field may be calculated using the following equation:

RR = DDR2/mDDR clock frequency $\times$ *DDR2/mDDR memory refresh period*

Table 17 displays the DDR2-400 refresh rate specification.

Table 17. DDR2 Memory Refresh Specification

Symbol	Description	Value
t_{REF}	Average Periodic Refresh Interval	7.8 µs

Therefore, the following results assuming 150 MHz DDR2/mDDR clock frequency.

RR = 150 MHz $\times$ 7.8 µs = 1170

Therefore, RR = 1170 = 492h.

Table 18 shows the resulting SDRCR configuration.

Table 18. SDRCR Configuration

Field	Value	Function Selection
LPMODEN	0	DDR2/mDDR memory controller is not in power-down mode.
MCLKSTOP_EN	0	MCLK stopping is disabled.
SR_PD	0	Leave a default value.
RR	492h	Set to 492h DDR2 clock cycles to meet the DDR2/mDDR memory refresh rate requirement.

3.2.3 Configuring SDRAM Timing Registers (SDTIMR1 and SDTIMR2)

The SDRAM timing register 1 (SDTIMR1) and SDRAM timing register 2 (SDTIMR2) configure the DDR2/mDDR memory controller to meet the data sheet timing parameters of the attached memory device. Each field in SDTIMR1 and SDTIMR2 corresponds to a timing parameter in the DDR2/mDDR data sheet specification. Table 19 and Table 20 display the register field name and corresponding DDR2 data sheet parameter name along with the data sheet value. These tables also provide a formula to calculate the register field value and displays the resulting calculation. Each of the equations include a minus 1 because the register fields are defined in terms of DDR2/mDDR clock cycles minus 1. See Section 4.5 and Section 4.6 for more information.

Table 19. SDTIMR1 Configuration

Register Field Name	DDR2 Data Manual Parameter Name	Description	Data Manual Value (nS)	Formula (Register field must be ≥)	Register Value
T_RFC	t_{RFC}	Refresh cycle time	127.5	$(t_{RFC} \times f_{DDR2/mDDR\_CLK}) - 1$	19
T_RP	t_{RP}	Precharge command to refresh or activate command	15	$(t_{RP} \times f_{DDR2/mDDR\_CLK}) - 1$	2
T_RCD	t_{RCD}	Activate command to read/write command	15	$(t_{RCD} \times f_{DDR2/mDDR\_CLK}) - 1$	2
T_WR	t_{WR}	Write recovery time	15	$(t_{WR} \times f_{DDR2/mDDR\_CLK}) - 1$	2
T_RAS	t_{RAS}	Active to precharge command	40	$(t_{RAC} \times f_{DDR2/mDDR\_CLK}) - 1$	5
T_RC	t_{RC}	Activate to Activate command in the same bank	55	$(t_{RC} \times f_{DDR2/mDDR\_CLK}) - 1$	8
T_RRD(1)	t_{RRD}	Activate to Activate command in a different bank	10	$((4 \times t_{RRD}) + (2 \times t_{CK}))/(4 \times t_{CK}) - 1$	1
T_WTR	t_{WTR}	Write to read command delay	10	$(t_{WTR} \times f_{DDR2/mDDR\_CLK}) - 1$	1

(1) The formula for the T_RRD field applies only for 8 bank DDR2/mDDR memories; when interfacing to DDR2/mDDR memories with less than 8 banks, the T_RRD field should be calculated using the following formula: $(t_{RRD} \times f_{DDR2/mDDR\_CLK}) - 1$.

Table 20. SDTIMR2 Configuration

Register Field Name	DDR2 Data Manual Parameter Name	Description	Data Manual Value	Formula (Register field must be ≥)	Register Value
T_RASMAX	t_{RAS}(MAX)	Active to precharge command	70 µs	$t_{RAS}(MAX)/_{DDR\ refresh\ rate}$ - 1	8
T_XP	t_{XP}	Exit power down to a non-read command	2(t_{CK} cycles)	If $t_{XP} > t_{CKE}$, then T_XP = t_{XP} - 1, else T_XP = t_{CKE} - 1	2
T_XSNR	t_{XSNR}	Exit self refresh to a non-read command	137.5 nS	($t_{XSNR} \times f_{DDR2/mDDR\_CLK}$) - 1	18
T_XSRD	t_{XSRD}	Exit self refresh to a read command	200 (t_{CK} cycles)	t_{XSRD} - 1	199
T_RTP	t_{RTP}	Read to precharge command delay	15 nS	($t_{RTP} \times f_{DDR2/mDDR\_CLK}$) - 1	1
T_CKE	t_{CKE}	CKE minimum pulse width	3 (t_{CK} cycles)	t_{CKE} - 1	2

3.2.4 Configuring DDR PHY Control Register (DRPYC1R)

The DDR PHY control register (DRPYC1R) contains a read latency (RL) field that helps the DDR2/mDDR memory controller determine when to sample read data. The RL field should be programmed to a value equal to the CAS latency plus the round trip board delay minus 1. The minimum RL value is CAS latency plus 1 and the maximum RL value is CAS latency plus 2 (again, the RL field would be programmed to these values minus 1). Table 21 shows the resulting DRPYC1R configuration.

When calculating round trip board delay the signals of primary concern are the differential clock signals (DDR_CLK and DDR_CLK) and data strobe signals (DDR_DQS). For these signals, calculate the round trip board delay from the DDR memory controller to the memory and then choose the maximum delay to determine the RL value. In this example, we will assume the round trip board delay is one DDR_CLK cycle; therefore, RL can be calculated as:

RL = CAS latency + round trip board delay – 1 = 4 + 1 – 1 = 4

Table 21. DRPYC1R Configuration

Field	Value	Function Selection
EXT_STRBEN	1h	Programs to select external strobe gating
RL	4h	Read latency is equal to CAS latency plus round trip board delay for data minus 1
PWRDNEN	0	Programmed to power up the DDR2/mDDR memory controller receivers

4 Registers

Table 22 lists the memory-mapped registers for the DDR2/mDDR memory controller. Note that the VTP IO control register (VTPIO_CTL) resides in the System Configuration Module.

Table 22. DDR2/mDDR Memory Controller Registers

Address Offset	Acronym	Register Description	Section
0h	REVID	Revision ID Register	Section 4.1
4h	SDRSTAT	SDRAM Status Register	Section 4.2
8h	SDCR	SDRAM Configuration Register	Section 4.3
Ch	SDRCR	SDRAM Refresh Control Register	Section 4.4
10h	SDTIMR1	SDRAM Timing Register 1	Section 4.5
14h	SDTIMR2	SDRAM Timing Register 2	Section 4.6
1Ch	SDCR2	SDRAM Configuration Register 2	Section 4.7
20h	PBBPR	Peripheral Bus Burst Priority Register	Section 4.8
40h	PC1	Performance Counter 1 Register	Section 4.9
44h	PC2	Performance Counter 2 Register	Section 4.10
48h	PCC	Performance Counter Configuration Register	Section 4.11
4Ch	PCMRS	Performance Counter Master Region Select Register	Section 4.12
50h	PCT	Performance Counter Time Register	Section 4.13
C0h	IRR	Interrupt Raw Register	Section 4.14
C4h	IMR	Interrupt Masked Register	Section 4.15
C8h	IMSR	Interrupt Mask Set Register	Section 4.16
CCh	IMCR	Interrupt Mask Clear Register	Section 4.17
E4h	DRPYC1R	DDR PHY Control Register 1	Section 4.18
01E2 C000h(1)	VTPIO_CTL	VTP IO Control Register	Section 4.19

(1) VTPIO_CTL resides in the register space of the System Configuration Module. It is listed in the register space of the DDR2/mDDR controller because it is applicable to the DDR2/mDDR controller.

4.1 Revision ID Register (REVID)

The revision ID register (REVID) contains the current revision ID for the DDR2/mDDR memory controller. The REVID is shown in Figure 20 and described in Table 23.

Figure 20. Revision ID Register (REVID)

31	0
REV	
R-4031 1B1Fh	

LEGEND: R = Read only; -*n* = value after reset

Table 23. Revision ID Register (REVID) Field Descriptions

Bit	Field	Value	Description
31-0	REV	4031 1B1Fh	Revision ID value of the DDR2/mDDR memory controller.

4.2 SDRAM Status Register (SDRSTAT)

The SDRAM status register (SDRSTAT) is shown in Figure 21 and described in Table 24.

Figure 21. SDRAM Status Register (SDRSTAT)

31	30	29	16
Rsvd	DUALCLK	Reserved	
R-0	R-1	R-0	

15	3	2	1	0
Reserved		PHYRDY	Reserved	
R-0		R-0	R-0	

LEGEND: R = Read only; -*n* = value after reset

Table 24. SDRAM Status Register (SDRSTAT) Field Descriptions

Bit	Field	Value	Description
31	Reserved	0	Reserved
30	DUALCLK		Dual clock. Specifies whether the VCLK and MCLK inputs are asynchronous. This bit should always be read as 1.
		0	VCLK and MCLK are not asynchronous.
		1	VCLK and MCLK are asynchronous.
29-3	Reserved	0	Reserved
2	PHYRDY		DDR2/mDDR memory controller DLL ready. Specifies whether the DDR2/mDDR memory controller DLL is powered up and locked.
		0	DLL is not ready, either powered down, in reset, or not locked.
		1	DLL is powered up, locked, and ready for operation.
1-0	Reserved	0	Reserved

4.3 SDRAM Configuration Register (SDCR)

The SDRAM configuration register (SDCR) contains fields that program the DDR2/mDDR memory controller to meet the specification of the attached DDR2/mDDR memory. These fields configure the DDR2/mDDR memory controller to match the data bus width, CAS latency, number of internal banks, and page size of the attached DDR2/mDDR memory. Writing to the DDRDRIVE[1:0], CL, IBANK, and PAGESIZE bit fields causes the DDR2/mDDR memory controller to start the DDR2/mDDR SDRAM initialization sequence. The SDCR is shown in Figure 22 and described in Table 25.

Figure 22. SDRAM ConfigurationRegister (SDCR)

31	28	27	26	25	24
Reserved		DDR2TERM1	IBANK_POS	MSDRAMEN	DDRDRIVE1
R-0		R/W-1	R/W-0	R/W-0	R/W-0

23	22	21	20	19	18	17	16
BOOTUNLOCK	DDR2DDQS	DDR2TERM0	DDR2EN	DDRDLL_DIS	DDRDRIVE0	DDREN	SDRAMEN
R/W-0	R/W-0	R/W-0	R/W-1	R/W-0	R/W-0	R/W-1	R/W-1

15	14	13	12	11	9	8
TIMUNLOCK	NM	Reserved		CL		Reserved
R/W-0	R/W-1	R-0		R/W-5h		R-0

7	6	4	3	2	0
Reserved	IBANK		Reserved	PAGESIZE	
R-0	R/W-2h		R-0	R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 25. SDRAM Configuration Register (SDCR) Field Descriptions

Bit	Field	Value	Description
31-28	Reserved	0	Reserved
27	DDR2TERM1	0-3h	DDR2 termination resistor value. This bit is used in conjunction with the DDR2TERM0 bit to make a 2-bit field. This bit is writeable only when the BOOTUNLOCK bit is unlocked. See the DDR2TERM0 bit. Note that the reset value of DDR2TERM[1:0] = 10, these bits must be cleared and forced to 00 to disable the termination because the ODT feature is not supported.
26	IBANK_POS		Internal Bank position.
		0	Normal addressing
		1	Special addressing. Typically used with mobile DDR partial array self-refresh.
25	MSDRAMEN		Mobile SDRAM enable. Use this bit in conjunction with DDR2EN, DDREN, and SDRAMEN to enable/disable mobile SDRAM. To change this bit value, use the following sequence: 1. Write a 1 to the BOOTUNLOCK bit. 2. Write a 0 to the BOOTUNLOCK bit along with the desired value of the MSDRAMEN bit.
		0	Disable mobile SDRAM
		1	Enable mobile SDRAM
24	DDRDRIVE1	0-3h	SDRAM drive strength. This bit is used in conjunction with the DDRDRIVE0 bit to make a 2-bit field. This bit is writeable only when the BOOTUNLOCK bit is unlocked. See the DDRDRIVE0 bit.

Table 25. SDRAM Configuration Register (SDCR) Field Descriptions (continued)

Bit	Field	Value	Description
23	BOOTUNLOCK		Boot Unlock. Controls the write permission settings for the DDR2TERM[1:0], MSDRAMEN, DDRDRIVE[1:0], DDR2DDQS, DDR2EN, DDRDLL_DIS, DDREN and SDRAMEN bit fields. To change these bits, use the following sequence: 1. Write a 1 to the BOOTUNLOCK bit. 2. Write a 0 to the BOOTUNLOCK bit along with the desired value of the DDR2TERM[1:0], MSDRAMEN, DDRDRIVE[1:0], DDR2DDQS, DDR2EN, DDRDLL_DIS, DDREN and SDRAMEN bits.
		0	DDR2TERM[1:0], MSDRAMEN, DDRDRIVE[1:0], DDR2DDQS, DDR2EN, DDRDLL_DIS, DDREN and SDRAMEN bit fields may not be changed.
		1	DDR2TERM[1:0], MSDRAMEN, DDRDRIVE[1:0], DDR2DDQS, DDR2EN, DDRDLL_DIS, DDREN and SDRAMEN bit fields may be changed.
22	DDR2DDQS		DDR2 SDRAM differential DQS enable. This bit is writeable only when the BOOTUNLOCK bit is unlocked. To change this bit value, use the following sequence: 1. Write a 1 to the BOOTUNLOCK bit. 2. Write a 0 to the BOOTUNLOCK bit along with the desired value of the DDR2DDQS bit.
		0	Single-ended DQS
		1	Differential DQS
21	DDR2TERM0	0-3h	DDR2 termination resistor value. This bit is used in conjunction with the DDR2TERM1 bit to make a 2-bit field. This bit is writeable only when the BOOTUNLOCK bit is unlocked. To change this bit value, use the following sequence: 1. Write a 1 to the BOOTUNLOCK bit. 2. Write a 0 to the BOOTUNLOCK bit along with the desired value of the DDR2TERM[1:0] bits. Note that the reset value of DDR2TERM[1:0] = 10, these bits must be cleared and forced to 00 to disable the termination because the ODT feature is not supported.
		0	Disable termination
		1h-3h	Reserved
20	DDR2EN		DDR2 enable. This bit is used in conjunction with the DDREN and SDRAMEN bits to enable/disable DDR2. This bit is writeable only when the BOOTUNLOCK bit is unlocked. To change this bit value, use the following sequence: 1. Write a 1 to the BOOTUNLOCK bit. 2. Write a 0 to the BOOTUNLOCK bit along with the desired value of the DDR2EN bit.
		0	Disable DDR2
		1	Enable DDR2
19	DDRDLL_DIS		DLL disable for DDR SDRAM. This bit is writeable only when the BOOTUNLOCK bit is unlocked. To change this bit value, use the following sequence: 1. Write a 1 to the BOOTUNLOCK bit. 2. Write a 0 to the BOOTUNLOCK bit along with the desired value of the DDRDLL_DIS bit.
		0	Enable DLL
		1	Disable DLL inside DDR SDRAM
18	DDRDRIVE0	0-3h	SDRAM drive strength. This bit is used in conjunction with the DDRDRIVE1 bit to make a 2-bit field. The DDRDRIVE[1:0] bits configure the output driver impedance control value of the SDRAM memory. This bit is writeable only when the BOOTUNLOCK bit is unlocked. To change this bit value, use the following sequence: 1. Write a 1 to the BOOTUNLOCK bit. 2. Write a 0 to the BOOTUNLOCK bit along with the desired value of the DDRDRIVE[1:0] bits.
		0	For DDR2, normal drive strength. For mobile DDR, full drive strength.
		1h	For DDR2, weak drive strength. For mobile DDR, 1/2 drive strength.
		2h	For DDR2, reserved. For mobile DDR, 1/4 drive strength.
		3h	For DDR2, reserved. For mobile DDR, 1/8 drive strength.

Table 25. SDRAM Configuration Register (SDCR) Field Descriptions (continued)

Bit	Field	Value	Description
17	DDREN		DDR enable. This bit is used in conjunction with the DDR2EN and SDRAMEN bits to enable/disable DDR. This bit is writeable only when the BOOTUNLOCK bit is unlocked. To change this bit value, use the following sequence: 1. Write a 1 to the BOOTUNLOCK bit. 2. Write a 0 to the BOOTUNLOCK bit along with the desired value of the DDREN bit.
		0	Disable DDR
		1	Enable DDR
16	SDRAMEN		SDRAM enable. This bit is used in conjunction with the DDR2EN and DDREN bits to enable/disable SDRAM. This bit is writeable only when the BOOTUNLOCK bit is unlocked. To change this bit value, use the following sequence: 1. Write a 1 to the BOOTUNLOCK bit. 2. Write a 0 to the BOOTUNLOCK bit along with the desired value of the SDRAMEN bit.
		0	Disable SDRAM
		1	Enable SDRAM
15	TIMUNLOCK		Timing unlock. Controls the write permission settings for the CL bit field, and the SDRAM timing register 1 (SDTIMR1) and the SDRAM timing register 2 (SDTIMR2) bit fields. To change these bits, use the following sequence: 1. Write a 1 to the TIMUNLOCK bit. 2. Write a 0 to the TIMUNLOCK bit along with the desired value of the CL bit and SDTIMR1 and SDTIMR2 bit fields.
		0	CL bit, and SDTIMR1 and SDTIMR2 bit fields may not be changed.
		1	CL bit, and SDTIMR1 and SDTIMR2 bit fields may be changed.
14	NM		SDRAM data bus width.
		0	Reserved
		1	16-bit bus width.
13-12	Reserved	0	Reserved
11-9	CL	0-7h	SDRAM CAS latency. This bit is writeable only when the TIMUNLOCK bit is unlocked. To change this bit value, use the following sequence: 1. Write a 1 to the TIMUNLOCK bit. 2. Write a 0 to the TIMUNLOCK bit along with the desired value of the CL bit.
		0-1h	Reserved
		2h	CAS Latency = 2
		3h	CAS Latency = 3
		4h	CAS Latency = 4
		5h	CAS Latency = 5
		6h-7h	Reserved
8-7	Reserved	0	Reserved
6-4	IBANK	0-7h	Internal SDRAM bank setup. Defines the number of internal banks on the external SDRAM device.
		0	1 bank
		1h	2 banks
		2h	4 banks
		3h	8 banks
		4h-7h	Reserved
3	Reserved	0	Reserved
2-0	PAGESIZE	0-7h	Page Size. Defines the page size of the SDRAM device.
		0	256-word page requiring 8 column address bits.
		1h	512-word page requiring 9 column address bits.
		2h	1024-word page requiring 10 column address bits.
		3h	2048-word page requiring 11 column address bits.
		4h-7h	Reserved

4.4 SDRAM Refresh Control Register (SDRCR)

The SDRAM refresh control register (SDRCR) is used to configure the DDR2/mDDR memory controller to:

- Enter and Exit the self-refresh and power-down states.
- Enable and disable MCLK, stopping when in the self-refresh state.
- Meet the refresh requirement of the attached DDR2/mDDR device by programming the rate at which the DDR2/mDDR memory controller issues autorefresh commands.

The SDRCR is shown in Table 26 and described in Figure 23.

Figure 23. SDRAM Refresh Control Register (SDRCR)

31	30	29 24	23	22 16
LPMODEN	MCLKSTOPEN	Reserved	SR_PD	Reserved
R/W-0	R/W-0	R-0	R/W-0	R-0

15 0
RR
R/W-884h

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 26. SDRAM Refresh Control Register (SDRCR) Field Descriptions

Bit	Field	Value	Description
31	LPMODEN		Low-power mode enable.
		0	Disable low-power mode.
		1	Enable low-power mode. The state of bit SR_PD selects either self-refresh or power-down mode.
30	MCLKSTOPEN		MCLK stop enable.
		0	Disables MCLK stopping, MCLK may not be stopped.
		1	Enables MCLK stopping, MCLK may be stopped. The LPMODEN bit must be set to 1 before setting the MCLKSTOPEN bit to 1.
29-24	Reserved	0	Reserved
23	SR_PD		Self-refresh or Power-down select. This bit is ignored when the LPMODEN bit is cleared to 0.
		0	When LPMODEN = 1, self-refresh mode.
		1	When LPMODEN = 1, power-down mode.
22-16	Reserved	0	Reserved
15-0	RR	0-FFFFh	Refresh rate. Defines the rate at which the attached SDRAM devices will be refreshed. The value of this field may be calculated with the following equation: *RR = SDRAM frequency/SDRAM refresh rate* where *SDRAM refresh rate* is derived from the SDRAM data sheet.

4.5 SDRAM Timing Register 1 (SDTIMR1)

The SDRAM timing register 1 (SDTIMR1) configures the DDR2/mDDR memory controller to meet many of the AC timing specification of the DDR2/mDDR memory. The SDTIMR1 is programmable only when the TIMUNLOCK bit is set to 1 in the SDRAM configuration register (SDCR). Note that DDR_CLK is equal to the period of the DDR_CLK signal. See the DDR2/mDDR memory data sheet for information on the appropriate values to program each field. The SDTIMR1 is shown in Figure 24 and described in Table 27.

Figure 24. SDRAM Timing Register 1 (SDTIMR1)

31–25	24–22	21–19	18–16
T_RFC	T_RP	T_RCD	T_WR
R/W-Fh	R/W-2h	R/W-2h	R/W-2h

15–11	10–6	5–3	2	1–0
T_RAS	T_RC	T_RRD	Rsvd	T_WTR
R/W-6h	R/W-9h	R/W-1	R-0	R/W-1

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 27. SDRAM Timing Register 1 (SDTIMR1) Field Descriptions

Bit	Field	Value	Description
31-25	T_RFC	0-7Fh	Specifies the minimum number of DDR_CLK cycles from a refresh or load mode command to a refresh or activate command, minus 1. Corresponds to the t_{rfc} AC timing parameter in the DDR2/mDDR data sheet. Calculate by: T_RFC = (t_{rfc}/DDR_CLK) - 1
24-22	T_RP	0-7h	Specifies the minimum number of DDR_CLK cycles from a precharge command to a refresh or activate command, minus 1. Corresponds to the t_{rp} AC timing parameter in the DDR2/mDDR data sheet. Calculate by: T_RP = (t_{rp}/DDR_CLK) - 1
21-19	T_RCD	0-7h	Specifies the minimum number of DDR_CLK cycles from an activate command to a read or write command, minus 1. Corresponds to the t_{rcd} AC timing parameter in the DDR2/mDDR data sheet. Calculate by: T_RCD = (t_{rcd}/DDR_CLK) - 1
18-16	T_WR	0-7h	Specifies the minimum number of DDR_CLK cycles from the last write transfer to a precharge command, minus 1. Corresponds to the t_{wr} AC timing parameter in the DDR2/mDDR data sheet. Calculate by: T_WR = (t_{wr}/DDR_CLK) - 1 When the value of this field is changed from its previous value, the initialization sequence will begin.
15-11	T_RAS	0-1Fh	Specifies the minimum number of DDR_CLK cycles from an activate command to a precharge command, minus 1. Corresponds to the t_{ras} AC timing parameter in the DDR2/mDDR data sheet. Calculate by: T_RAS = (t_{ras}/DDR_CLK) - 1 T_RAS must be greater than or equal to T_RCD.
10-6	T_RC	0-1Fh	Specifies the minimum number of DDR_CLK cycles from an activate command to an activate command, minus 1. Corresponds to the t_{rc} AC timing parameter in the DDR2/mDDR data sheet. Calculate by: T_RC = (t_{rc}/DDR_CLK) - 1
5-3	T_RRD	0-7h	Specifies the minimum number of DDR_CLK cycles from an activate command to an activate command in a different bank, minus 1. Corresponds to the t_{rrd} AC timing parameter in the DDR2/mDDR data sheet. Calculate by: T_RRD = (t_{rrd}/DDR_CLK) - 1 For an 8 bank DDR2/mDDR device, this field must be equal to (($4 \times t_{RRD}$) + ($2 \times t_{CK}$)) / ($4 \times t_{CK}$) - 1.
2	Reserved	0	Reserved

Table 27. SDRAM Timing Register 1 (SDTIMR1) Field Descriptions (continued)

Bit	Field	Value	Description
1-0	T_WTR	0-3h	Specifies the minimum number of DDR_CLK cycles from the last write to a read command, minus 1. Corresponds to the t_{wtr} AC timing parameter in the DDR2/mDDR data sheet. Calculate by: T_WTR = (t_{wtr}/DDR_CLK) - 1

4.6 SDRAM Timing Register 2 (SDTIMR2)

Like the SDRAM timing register 1 (SDTIMR1), the SDRAM timing register 2 (SDTIMR2) also configures the DDR2/mDDR memory controller to meet the AC timing specification of the DDR2/mDDR memory. The SDTIMR2 is programmable only when the TIMUNLOCK bit is set to 1 in the SDRAM configuration register (SDCR). Note that DDR_CLK is equal to the period of the DDR_CLK signal. See the DDR2/mDDR data sheet for information on the appropriate values to program each field. SDTIMR2 is shown in Figure 25 and described in Table 28.

Figure 25. SDRAM Timing Register 2 (SDTIMR2)

31	30 27	26 25	24 23	22 16
Rsvd	T_RASMAX	T_XP	T_ODT	T_XSNR
R-0	R/W-8h	R/W-2h	R/W-2h	R/W-32h

15 8	7 5	4 0
T_XSRD	T_RTP	T_CKE
R/W-A7h	R/W-1	R/W-2h

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 28. SDRAM Timing Register 2 (SDTIMR2) Field Descriptions

Bit	Field	Value	Description
31	Reserved	0	Any writes to these bit(s) must always have a value of 0.
30-27	T_RASMAX	0-Fh	Specifies the maximum number of refresh rate intervals from Activate to Precharge command. Corresponds to the t_{ras} AC timing parameter and the refresh rate in the DDR2/mDDR data sheet. Calculate by: T_RASMAX = (t_{ras}max/refresh_rate) - 1 Round down to the nearest cycle.
26-25	T_XP	0-3h	Specifies the minimum number of DDR_CLK cycles from Power Down exit to any other command except a read command, minus 1. Corresponds to the t_{xp} or t_{cke} AC timing parameter in the DDR2/mDDR data sheet. This field must satisfy the greater of t_{XP} or t_{CKE}. If $t_{xp} > t_{cke}$, then calculate by T_XP = t_{xp} - 1 If $t_{xp} < t_{cke}$, then calculate by T_XP = t_{cke} - 1
24-23	T_ODT	0-3h	Specifies the minimum number of DDR_CLK cycles from ODT enable to write data driven for DDR2 SDRAM. T_ODT must be equal to (CAS latency - tAOND -1). T_ODT must be less than CAS latency minus 1. This feature is not supported because the DDR_ODT signal is not pinned out.
22-16	T_XSNR	0-7Fh	Specifies the minimum number of DDR_CLK cycles from a self_refresh exit to any other command except a read command, minus 1. Corresponds to the t_{xsnr} AC timing parameter in the DDR2/mDDR data sheet. Calculate by: T_XSNR = (t_{xsnr}/DDR_CLK) - 1
15-8	T_XSRD	0-FFh	Specifies the minimum number of DDR_CLK cycles from a self_refresh exit to a read command, minus 1. Corresponds to the t_{xsrd} AC timing parameter in the DDR2/mDDR data sheet. Calculate by: T_XSRD = t_{xsrd} - 1
7-5	T_RTP	0-7h	Specifies the minimum number of DDR_CLK cycles from a last read command to a precharge command, minus 1. Corresponds to the t_{rtp} AC timing parameter in the DDR2/mDDR data sheet. Calculate by: T_RTP = (t_{rtp}/DDR_CLK) - 1
4-0	T_CKE	0-1Fh	Specifies the minimum number of DDR_CLK cycles between transitions on the DDR_CKE pin, minus 1. Corresponds to the t_{cke} AC timing parameter in the DDR2/mDDR data sheet. Calculate by: T_CKE = t_{cke} - 1

4.7 SDRAM Configuration Register 2 (SDCR2)

The SDRAM configuration register 2 (SDCR2) contains fields to configure partial array self-refresh and rowsize of the mDDR. This register is applicable only when the IBANK_POS bit in the SDRAM configuration register (SDCR) is set to 1 for special addressing. Writing to the PASR and ROWSIZE bit fields will cause the DDR2/mDDR memory controller to start the DDR2/mDDR SDRAM initialization sequence. SDCR2 is shown in Figure 26 and described in Table 29.

Figure 26. SDRAM Configuration Register 2 (SDCR2)

31	19	18	16
Reserved		PASR	
R-0		R/W-0	

15	3	2	0
Reserved		ROWSIZE	
R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 29. SDRAM Configuration Register 2 (SDCR2) Field Descriptions

Bit	Field	Value	Description
31-19	Reserved	0	Reserved
18-16	PASR	0-7h	Partial array self-refresh.
		0	4 banks will be refreshed.
		1h	2 banks will be refreshed.
		2h	1 bank will be refreshed.
		3h-4h	Reserved
		5h	1/2 bank will be refreshed.
		6h	1/4 bank will be refreshed.
		7h	Reserved
15-3	Reserved	0	Reserved
2-0	ROWSIZE	0-7h	Row size. Defines the number of row address bit for DDR device.
		0	9 row address bits
		1h	10 row address bits
		2h	11 row address bits
		3h	12 row address bits
		4h	13 row address bits
		5h	14 row address bits
		6h	15 row address bits
		7h	16 row address bits

4.8 Peripheral Bus Burst Priority Register (PBBPR)

The peripheral bus burst priority register (PBBPR) helps prevent command starvation within the DDR2/mDDR memory controller. To avoid command starvation, the DDR2/mDDR memory controller momentarily raises the priority of the oldest command in the command FIFO after a set number of transfers have been made. The PR_OLD_COUNT bit sets the number of transfers that must be made before the DDR2/mDDR memory controller raises the priority of the oldest command. See Section 2.6.2 for more details on command starvation.

Proper configuration of the PBBPR is critical to correct system operation. The DDR2/mDDR memory controller always prioritizes accesses to open rows as highest, if there is any bank conflict regardless of master priority. This is done to allow most efficient utilization of the DDR2/mDDR. However, it could lead to excessive blocking of high priority masters. If the PR_OLD_COUNT bits are cleared to 00h, then the DDR2/mDDR memory controller always honors the master priority, regardless of open row/bank status. For most systems, the PBBPR should be set to a moderately low value to provide an acceptable balance of DDR2/mDDR efficiency and latency for high priority masters (for example, 10h or 20h).

The PBBPR is shown in Figure 27 and described in Table 30.

Figure 27. Peripheral Bus Burst Priority Register (PBBPR)

31	16
Reserved	
R-0	

15	8	7	0
Reserved		PR_OLD_COUNT	
R-0		R/W-FFh	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 30. Peripheral Bus Burst Priority Register (PBBPR) Field Descriptions

Bit	Field	Value	Description
31-8	Reserved	0	Any writes to these bit(s) must always have a value of 0.
7-0	PR_OLD_COUNT	0-FFh	Priority raise old counter. Specifies the number of memory transfers after which the DDR2/mDDR memory controller will elevate the priority of the oldest command in the command FIFO. Clearing to 00h will ensure master priority is strictly honored (at the cost of decreased DDR2/mDDR memory controller efficiency, as open row will always be closed immediately if any bank conflict occurs). Recommended setting for typical system operation is between 10h and 20h.
		0	1 memory transfer
		1h	2 memory transfers
		2h	3 memory transfers
		3h-FFh	4 to 256 memory transfers

4.9 Performance Counter 1 Register (PC1)

For debug or gathering performance statistics, the PC1 and PC2 counters and associated configuration registers are provided. These are intended for debug and analysis only. By configuring the performance counter configuration register (PCC) to define the type of statistics to gather and configuring the performance counter master region select register (PCMRS) to filter accesses only to specific chip select regions, performing system applications and then reading these counters, different statistics can be gathered. To reset the counters, you must reset (mod_g_rst_n) the DDR2/mDDR memory controller through the PSC. For details on the PSC, see your device-specific *System Reference Guide*.

The performance counter 1 register (PC1) is shown in Figure 28 and described in Table 31.

Figure 28. Performance Counter 1 Register (PC1)

31	0
Counter1	
R-0	

LEGEND: R = Read only; -*n* = value after reset

Table 31. Performance Counter 1 Register (PC1) Field Descriptions

Bit	Field	Value	Description
31-0	Counter1	0-FFFF FFFFh	32-bit counter that can be configured as specified in the performance counter configuration register (PCC) and the performance counter master region select register (PCMRS).

4.10 Performance Counter 2 Register (PC2)

The performance counter 2 register (PC2) is shown in Figure 29 and described in Table 32.

Figure 29. Performance Counter 2 Register (PC2)

31	0
Counter2	
R-0	

LEGEND: R = Read only; -*n* = value after reset

Table 32. Performance Counter 2 Register (PC2) Field Descriptions

Bit	Field	Value	Description
31-0	Counter2	0-FFFF FFFFh	32-bit counter that can be configured as specified in the performance counter configuration register (PCC) and the performance counter master region select register (PCMRS).

4.11 Performance Counter Configuration Register (PCC)

The performance counter configuration register (PCC) is shown in Figure 30 and described in Table 33.

Table 34 shows the possible filter configurations for the two performance counters. These filter configurations can be used in conjunction with a Master ID and/or an external chip select to obtain performance statistics for a particular master and/or an external chip select.

Figure 30. Performance Counter Configuration Register (PCC)

31	30	29 20	19 16
CNTR2_MSTID_EN	CNTR2_REGION_EN	Reserved	CNTR2_CFG
R/W-0	R/W-0	R-0	R/W-1

15	14	13 4	3 0
CNTR1_MSTID_EN	CNTR1_REGION_EN	Reserved	CNTR1_CFG
R/W-0	R/W-0	R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 33. Performance Counter Configuration Register (PCC) Field Descriptions

Bit	Field	Value	Description
31	CNTR2_MSTID_EN		Master ID filter enable for performance counter 2 register (PC2). Refer to Table 34 for details.
		0	Master ID filter is disabled. PC2 counts accesses from all masters to DDR2/mDDR SDRAM.
		1	Master ID filter is enabled. PC2 counts accesses from the master, corresponding to the Master ID value in the MST_ID2 bit field of the performance counter master region select register (PCMRS).
30	CNTR2_REGION_EN		Chip select filter enable for performance counter 2 register (PC2). Refer to Table 34 for details.
		0	Chip select filter is disabled. PC2 counts total number of accesses (DDR2/mDDR SDRAM + DDR2/mDDR memory controller memory-mapped register accesses). The REGION_SEL2 bit field value in the performance counter master region select register (PCMRS) is a don't care.
		1	Chip select filter is enabled. If the REGION_SEL2 bit field value in the performance counter master region select register (PCMRS) is: **REGION_SEL2 = 0:** PC2 counts accesses to DDR2/mDDR SDRAM memory. **REGION_SEL2 = 7h:** PC2 counts accesses to DDR2/mDDR memory controller memory-mapped registers.
29-20	Reserved	0	Any writes to these bit(s) must always have a value of 0.
19-16	CNTR2_CFG	0-Fh	Filter configuration for performance counter 2 register (PC2). Refer to Table 34 for details.
15	CNTR1_MSTID_EN		Master ID filter enable for performance counter 1 register (PC1). Refer to Table 34 for details.
		0	Master ID filter is disabled. PC1 counts accesses from all masters to DDR2/mDDR SDRAM.
		1	Master ID filter is enabled. PC1 counts accesses from the master, corresponding to the Master ID value in the MST_ID1 bit field of the performance counter master region select register (PCMRS).
14	CNTR1_REGION_EN		Chip select filter enable for performance counter 1 register (PC1). Refer to Table 34 for details.
		0	Chip select filter is disabled. PC1 counts total number of accesses (DDR2/mDDR SDRAM + DDR2/mDDR memory controller memory-mapped register accesses). The REGION_SEL1 bit field value in the performance counter master region select register (PCMRS) is a don't care.
		1	Chip select filter is enabled. If the REGION_SEL1 bit field value in the performance counter master region select register (PCMRS) is: **REGION_SEL1 = 0:** PC1 counts accesses to DDR2/mDDR SDRAM memory. **REGION_SEL1 = 7h:** PC1 counts accesses to DDR2/mDDR memory controller memory-mapped registers.
13-4	Reserved	0	Any writes to these bit(s) must always have a value of 0.

Table 33. Performance Counter Configuration Register (PCC) Field Descriptions (continued)

Bit	Field	Value	Description
3-0	CNTR1_CFG	0-Fh	Filter configuration for performance counter 1 register (PC1). Refer to Table 34 for details.

Table 34. Performance Counter Filter Configuration

Performance Counter Configuration Register (PCC) Bit			
CNTR*n*_CFG	**CNTR*n*_REGION_EN**	**CNTR*n*_MSTID_EN**	**Description**
0	0	0 or 1	**Counts the total number of READ/WRITE commands the external memory controller receives.** The size of counter increments are determines by the size of the transfer and the default burst size (DBS). The counter breaks up transfers into sizes according to DBS. Therefore, counter increments for transfers aligned to DBS are equal to the transfer size divided by the DBS.
1h	0	0	**Counts the total number of ACTIVATE commands the external memory controller issues to DDR2/mDDR memory.** The counter increments by a value of 1 for every request to read/write data to a closed bank in DDR2/mDDR memory by the external memory controller.
2h	0 or 1	0 or 1	**Counts the total number of READ commands (read accesses) the DDR2/mDDR memory controller receives.** Counter increments for transfers aligned to the default burst size (DBS) are equal to the transfer size divided by the DBS.
3h	0 or 1	0 or 1	**Counts the total number of WRITE commands the DDR2/mDDR memory controller receives.** Counter increments for transfers aligned to the default burst size (DBS) are equal to the transfer size of data written to the DDR2/mDDR memory controller divided by the DBS.
4h	0	0	**Counts the number of external memory controller cycles (DDR_CLK cycles) that the command FIFO is full.** Use the following to calculate the counter value as a percentage: *% = counter value / total DDR_CLK cycles in a sample period* As the value of this counter approaches 100%, the DDR2/mDDR memory controller is approaching a congestion point where the command FIFO is full 100% of the time and a command will have to wait at the SCR to be accepted in the command FIFO.
5h-7h	0	0	Reserved
8h	0 or 1	0 or 1	**Counts the number of commands (requests) in the command FIFO that require a priority elevation.** To avoid command starvation, the DDR2/mDDR memory controller can momentarily raise the priority of the oldest command in the command FIFO after a set number of transfers have been made. The PR_OLD_COUNT bit field in the peripheral bus burst priority register (PBBPR) sets the number of the transfers that must be made before the DDR2/mDDR memory controller will raise the priority of the oldest command.
9h	0	0	**Counts the number of DDR2/mDDR memory controller cycles (DDR_CLK cycles) that a command is pending in the command FIFO.** This counter increments every cycle the command FIFO is not empty. Use the following to calculate the counter value as a percentage: *% = counter value / total DDR_CLK cycles in sample period* As the value of this counter approaches 100%, the number of cycles the DDR2/mDDR memory controller has a command in the command FIFO to service approaches 100%.
Ah-Fh	0	0	Reserved

4.12 Performance Counter Master Region Select Register (PCMRS)

The performance counter master region select register (PCMRS) is shown in Figure 31 and described in Table 35.

Figure 31. Performance Counter Master Region Select Register (PCMRS)

31	24	23	20	19	16
MST_ID2		Reserved		REGION_SEL2	
R/W-0		R-0		R/W-0	

15	8	7	4	3	0
MST_ID1		Reserved		REGION_SEL1	
R/W-0		R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

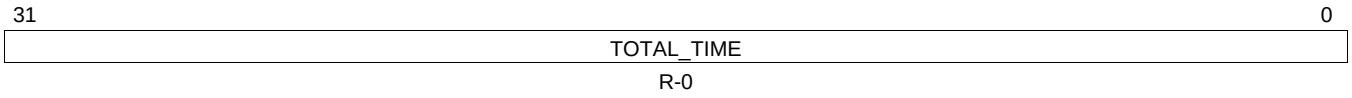
Table 35. Performance Counter Master Region Select Register (PCMRS) Field Descriptions

Bit	Field	Value	Description
31-24	MST_ID2	0-FFh	Master ID for performance counter 2 register (PC2). For the Master ID value for master peripherals in the device, see your device-specific *System Reference Guide*.
23-20	Reserved	0	Any writes to these bit(s) must always have a value of 0.
19-16	REGION_SEL2	0-Fh	Region select for performance counter 2 register (PC2).
		0	PC2 counts total DDR2/mDDR accesses.
		1h-6h	Reserved
		7h	PC2 counts total DDR2/mDDR memory controller memory-mapped register accesses.
		8h-Fh	Reserved
15-8	MST_ID1	0-FFh	Master ID for performance counter 1 register (PC1). For the Master ID value for master peripherals in the device, see your device-specific *System Reference Guide*.
7-4	Reserved	0	Any writes to these bit(s) must always have a value of 0.
3-0	REGION_SEL1	0-Fh	Region select for performance counter 1 register (PC1).
		0	PC1 counts total DDR2/mDDR accesses.
		1h-6h	Reserved
		7h	PC1 counts total DDR2/mDDR memory controller memory-mapped register accesses.
		8h-Fh	Reserved

4.13 Performance Counter Time Register (PCT)

The performance counter time register (PCT) is shown in Figure 32 and described in Table 36.

Figure 32. Performance Counter Time Register (PCT)



LEGEND: R = Read only; -*n* = value after reset

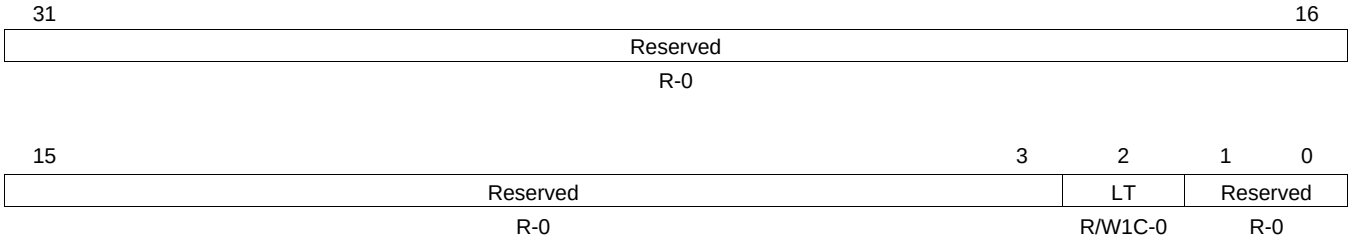
Table 36. Performance Counter Time Register (PCT) Field Description

Bit	Field	Value	Description
31-0	TOTAL_TIME	0-FFFF FFFFh	32-bit counter that continuously counts number for DDR_CLK cycles elapsed after the DDR2/mDDR memory controller is brought out of reset.

4.14 Interrupt Raw Register (IRR)

The interrupt raw register (IRR) displays the raw status of the interrupt. If the interrupt condition occurs, the corresponding bit in IRR is set independent of whether or not the interrupt is enabled. The IRR is shown in Figure 33 and described in Table 37.

Figure 33. Interrupt Raw Register (IRR)



LEGEND: R/W = Read/Write; R = Read only; W1C = Write 1 to clear (writing 0 has no effect); -*n* = value after reset

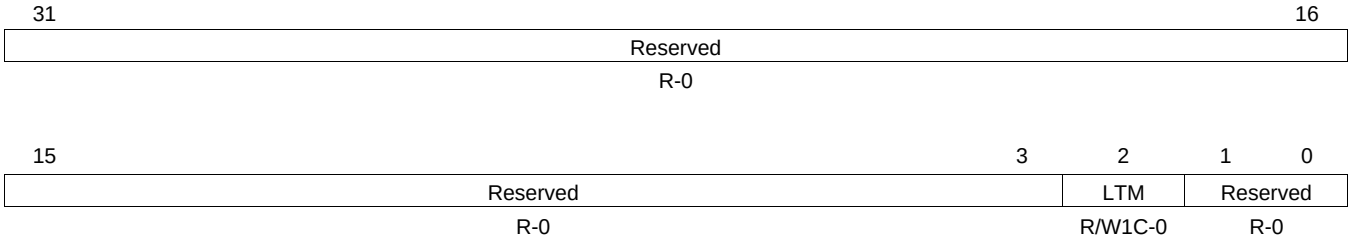
Table 37. Interrupt Raw Register (IRR) Field Descriptions

Bit	Field	Value	Description
31-3	Reserved	0	Reserved
2	LT		Line trap. Write a 1 to clear LT and the LTM bit in the interrupt masked register (IMR); a write of 0 has no effect.
		0	A line trap condition has not occurred.
		1	Illegal memory access type. See Section 2.14 for more details.
1-0	Reserved	0	Reserved

4.15 Interrupt Masked Register (IMR)

The interrupt masked register (IMR) displays the status of the interrupt when it is enabled. If the interrupt condition occurs and the corresponding bit in the interrupt mask set register (IMSR) is set, then the IMR bit is set. The IMR bit is not set if the interrupt is not enabled in IMSR. The IMR is shown in Figure 34 and described in Table 38.

Figure 34. Interrupt Masked Register (IMR)



LEGEND: R/W = Read/Write; R = Read only; W1C = Write 1 to clear (writing 0 has no effect); -*n* = value after reset

Table 38. Interrupt Masked Register (IMR) Field Descriptions

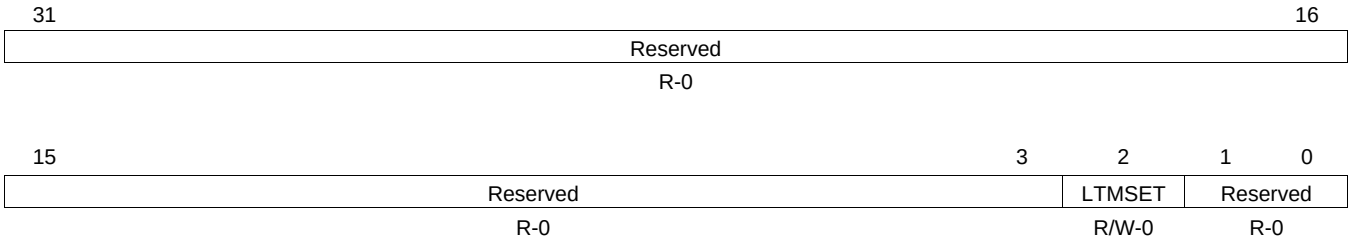
Bit	Field	Value	Description
31-3	Reserved	0	Reserved
2	LTM		Line trap masked. Write a 1 to clear LTM and the LT bit in the interrupt raw register (IRR); a write of 0 has no effect.
		0	A line trap condition has not occurred.
		1	Illegal memory access type (only set if the LTMSET bit in IMSR is set). See Section 2.14 for more details.
1-0	Reserved	0	Reserved

4.16 Interrupt Mask Set Register (IMSR)

The interrupt mask set register (IMSR) enables the DDR2/mDDR memory controller interrupt. The IMSR is shown in Figure 35 and described in Table 39.

Note: If the LTMSET bit in IMSR is set concurrently with the LTMCLR bit in the interrupt mask clear register (IMCR), the interrupt is not enabled and neither bit is set to 1.

Figure 35. Interrupt Mask Set Register (IMSR)



LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 39. Interrupt Mask Set Register (IMSR) Field Descriptions

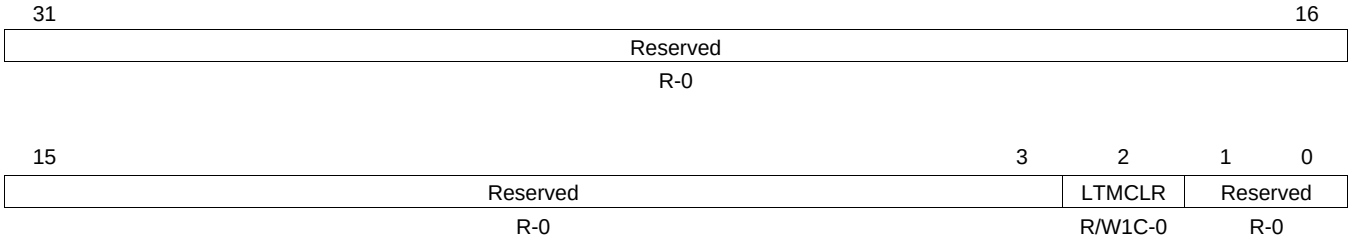
Bit	Field	Value	Description
31-3	Reserved	0	Reserved
2	LTMSET		Line trap interrupt set. Write a 1 to set LTMSET and the LTMCLR bit in the interrupt mask clear register (IMCR); a write of 0 has no effect.
		0	Line trap interrupt is not enabled; a write of 1 to the LTMCLR bit in IMCR occurred.
		1	Line trap interrupt is enabled.
1-0	Reserved	0	Reserved

4.17 Interrupt Mask Clear Register (IMCR)

The interrupt mask clear register (IMCR) disables the DDR2/mDDR memory controller interrupt. Once an interrupt is enabled, it may be disabled by writing a 1 to the IMCR bit. The IMCR is shown in Figure 36 and described in Table 40.

Note: If the LTMCLR bit in IMCR is set concurrently with the LTMSET bit in the interrupt mask set register (IMSR), the interrupt is not enabled and neither bit is set to 1.

Figure 36. Interrupt Mask Clear Register (IMCR)



LEGEND: R/W = Read/Write; R = Read only; W1C = Write 1 to clear (writing 0 has no effect); -*n* = value after reset

Table 40. Interrupt Mask Clear Register (IMCR) Field Descriptions

Bit	Field	Value	Description
31-3	Reserved	0	Reserved
2	LTMCLR		Line trap interrupt clear. Write a 1 to clear LTMCLR and the LTMSET bit in the interrupt mask set register (IMSR); a write of 0 has no effect.
		0	Line trap interrupt is not enabled.
		1	Line trap interrupt is enabled; a write of 1 to the LTMSET bit in IMSR occurred.
1-0	Reserved	0	Reserved

4.18 DDR PHY Control Register (DRPYC1R)

The DDR PHY control register 1 (DRPYC1R) configures the DDR2/mDDR memory controller read latency. The DRPYC1R is shown in Figure 37 and described in Table 41.

Figure 37. DDR PHY Control Register 1 (DRPYC1R)

31	16
Reserved	
R-0	

15	8	7	6	5	3	2	0
Reserved		EXT_STRBEN	PWRDNEN	Reserved		RL	
R-0		R/W-0	R/W-1	R-0		R/W-6h	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 41. DDR PHY Control Register 1 (DRPYC1R) Field Descriptions

Bit	Field	Value	Description
31-8	Reserved	0	Reserved
7	EXT_STRBEN		Internal/External strobe gating.
		0	Internal strobe gating mode.
		1	External strobe gating mode.
6	PWRDNEN		Power down receivers.
		0	Receivers powered up.
		1	Receivers powered down.
5-3	Reserved	0	Reserved
2-0	RL	0-7h	Read latency. Read latency is equal to CAS latency plus round trip board delay for data minus 1. The maximum value of read latency that is supported is CAS latency plus 2. The minimum read latency value that is supported is CAS latency plus 1. The read latency value is defined in number of MCLK/DDR_CLK cycles.

4.19 VTP IO Control Register (VTPIO_CTL)

The VTP IO control register (VTPIO_CTL) is used to control the calibration of the DDR2/mDDR memory controller I/Os with respect to voltage, temperature, and process (VTP). The voltage, temperature, and process information is used to control the I/O's output impedance. The VTPIO_CTL is shown in Figure 38 and described in Table 42. Note that the VTPIO_CTL resides in the register space of the System Control Module.

Figure 38. VTP IO Control Register (VTPIO_CTL)

31							24
Reserved							
R-0							

23						19	18	17	16
Reserved							VREFEN	VREFTAP	
R-0							R/W-0	R/W-0	

15	14	13	12	11	10	9	8
READY	IOPWRDN	CLKRZ	FORCEDNP	FORCEDNN	FORCEUPP	FORCEUPN	PWRSAVE
R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

7	6	5	4	3	2	1	0
LOCK	POWERDN	D0	D1	D2	F0	F1	F2
R/W-0	R/W-1	R/W-1	R/W-1	R/W-0	R/W-1	R/W-1	R/W-1

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 42. VTP IO Control Register (VTPIO_CTL) Field Descriptions

Bit	Field	Value	Description
31-19	Reserved	0	Reserved
18	VREFEN		Internal DDR I/O Vref enable.
		0	Connected to pad, external reference.
		1	Connected to internal reference.
17-16	VREFTAP	0-3h	Selection for internal reference voltage level.
		0	Vref = 50.0% of VDDS
		1h	Vref = 47.5% of VDDS
		2h	Vref = 52.5% of VDDS
		3h	Reserved
15	READY		VTP Ready status
		0	VTP is not ready.
		1	VTP is ready.
14	IOPWRDN		Power down enable for DDR input buffer.
		0	Disable power down control by the PWRDNEN bit in the DDR PHY control register 1 (DRPYC1R).
		1	Enable power down control by the PWRDNEN bit in the DDR PHY control register 1 (DRPYC1R).
13	CLKRZ	0	VTP clear. Write 0 to clear VTP flops.
12	FORCEDNP	0	Force decrease PFET drive.
11	FORCEDNN	0	Force decrease NFET drive.
10	FORCEUPP	0	Force increase PFET drive.
9	FORCEUPN	0	Force increase PFET drive.

Table 42. VTP IO Control Register (VTPIO_CTL) Field Descriptions (continued)

Bit	Field	Value	Description
8	PWRSAVE		VTP power save mode.
		0	Disable power save mode.
		1	Enable power save mode.
7	LOCK		VTP impedance lock.
		0	Unlock impedance.
		1	Lock impedance.
6	POWERDN		VTP power down.
		0	Disable power down.
		1	Enable power down.
5	D0	1	Drive strength control bit.
4	D1	1	Drive strength control bit.
3	D2	0	Drive strength control bit.
2	F0	1	Digital filter control bit.
1	F1	1	Digital filter control bit.
0	F2	1	Digital filter control bit.

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