Features

- Complete Data Transmission on Power Line functions
- High Maximum Input Voltage: 30V
- Integrated Low Dropout Voltage Regulator
- Integrated Voltage Detector for Power Supply Monitoring
- Open drain NMOS drivers for flexible interfacing
- Power and Reset Protection Features
- 8-pin SOP package type
- Minimal external component requirements

General Description

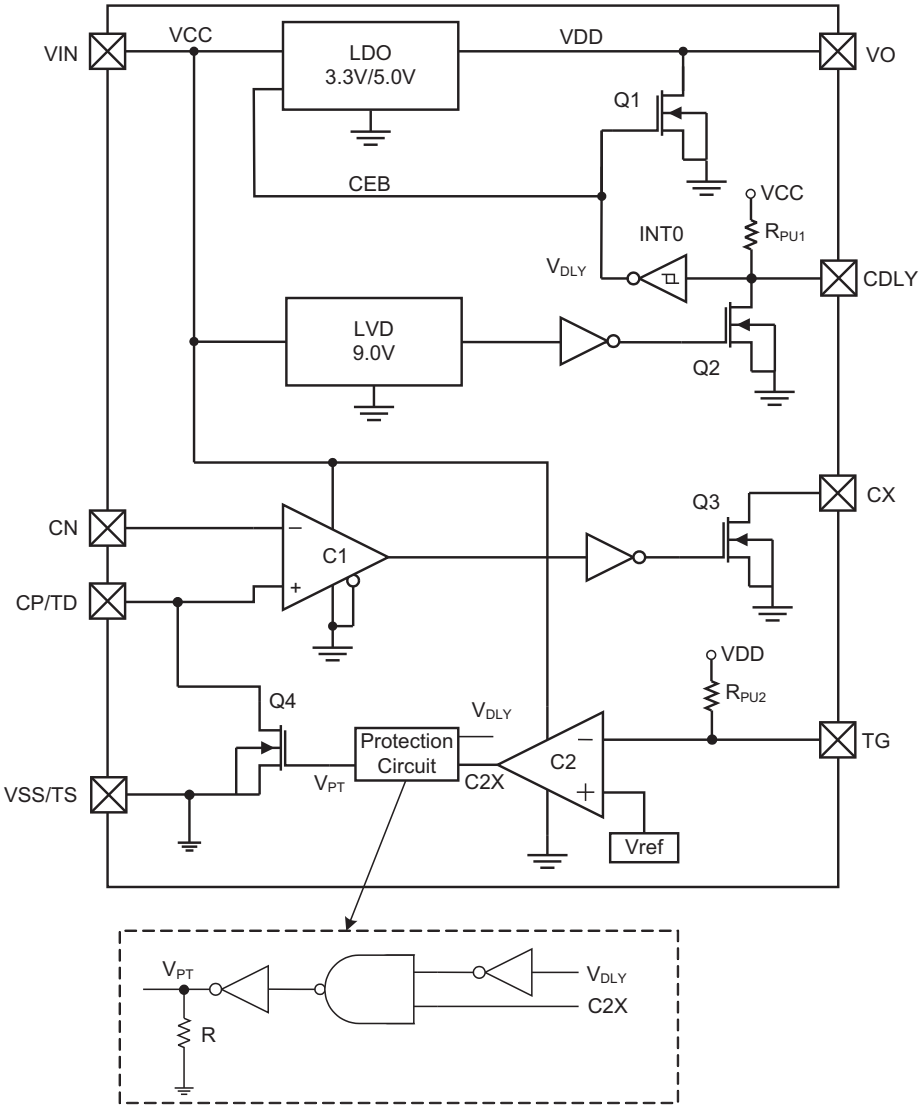
In systems where a master controller controls a number of individual interconnected subsystems such as found in smoke detector systems, water metering systems, solar energy system etc., the cost of the lengthy interconnecting cabling can be a major factor. By sending data along the power supply lines, the interconnecting cables can be reduced to a simple two line type, thus greatly reducing both cable and installation costs.

With a the addition of a few external components, this power line data transceiver device contains all the internal components required to provide users with a system for power line data transmission and reception. Data is modulated onto the power line by the simple reduction of the power line voltage for a specific period of time. Power supply voltage changes can be initiated by the master controller for data reception or initiated by the HT71D0x devices for data transmission. An internal voltage regulator within the device ensures that a constant voltage power supply is provided to the interconnected subsystem units while an internal voltage detector monitors the power line voltage level.

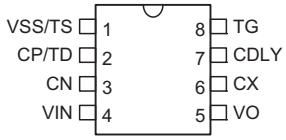
Selection Guide

Part No.	LDO Voltage	Detect Voltage	Package
HT71D02	3.3V	9.0V	8SOP
HT71D04	5.0V	9.0V	8SOP

Block Diagram



Pin Assignment



HT71D02/HT71D04
8 SOP-A

Pin Description

Pin Name	I/O	Pin-Shared Mapping
VIN	—	Input voltage
CN	I	Comparator Negative Terminal Input
CP/TD	I	Comparator positive input - CP
	O	NMOS Driver Drain Terminal - TD
VSS/TS	—	Ground pin - VSS
	O	NMOS Driver Source Terminal - TS
TG	I	NMOS Gate Input
CX	O	Comparator NMOS output
CDLY	O	LDO Output Control - delay time determined by external capacitor
VO	—	LDO Output Voltage

CP and TD share the same pin

Absolute Maximum Ratings

Maximum Input Supply Voltage 33V
Operating Temperature.....–40°C to 85°C
Storage Temperature .....–55°C to 150°C
Maximum Junction Temperature .....150°C

Note: These are stress ratings only. Stresses exceeding the range specified under "Absolute Maximum Ratings" may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

D.C. Characteristics

Ta=25°C

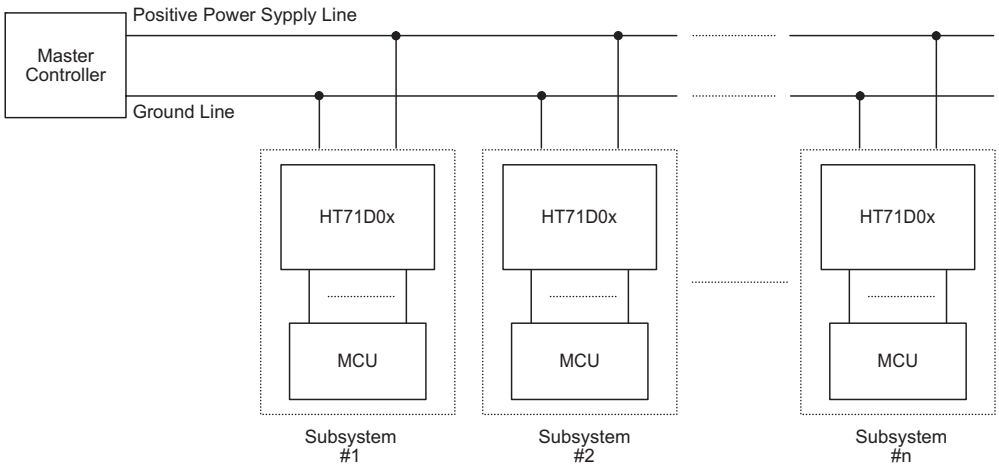
Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
V_{IN}	Operating Voltage	—	—	10	—	30	V
I_{CC}	Operating current of VIN	—	V_{IN}=24V , CP=5V, CN=2V, No Load	—	30	85	μA
I_{OL1}	Output Sink Current (Q1, VO pin)	—	V_{IN}=5V, V_{OL} =0.5V	0.8	—	—	mA
I_{OL2}	Output Sink Current (Q2,CDLY pin)	—	V_{IN}=5V, V_{OL} =0.5V	250	500	—	μA
I_{OL3}	Output Sink Current (Q3,CX pin)	—	V_{IN}=5V, V_{OL} =0.5V	0.8	—	—	mA
I_{OL4}	Output Sink Current (Q4,TS pin) (NMOS driver)	—	V_{GS}=18V, V_{DS} =1V	90	—	—	mA
R_{PU1}	Pull-up resistor 1	—	V_{IN}=10V	-50%	5	+50%	MΩ
R_{PU2}	Pull-up resistor 2	—	V_{IN}=10V	-30%	50	+30%	kΩ

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
Inverter 0 (INT) Schmitt Trigger Window							
V_{SW} (note)	V_H	—	V_{IN}=24V	-20%	13.7	+20%	V
	V_L			-20%	7.16	+20%	V
	V_H	—	V_{IN}=10V	-20%	5.83	+20%	V
	V_L			-20%	3.07	+20%	V
Inverter 0 (INT) Schmitt Trigger Window							
V_{OUT}	LDO Output Voltage	3.3V	V_{IN}=10V, I_{OUT}=10mA	3.201	3.300	3.399	V
		5.0V		4.850	5.000	5.150	V
I_{OUT}	LDO Output Current	—	V_{IN}=10V, ΔV_{OUT}=3% (Note1)	60	—	—	mA
ΔV_{LOAD}	Load Regulation	—	V_{IN}=10V, 1mA≤I_{OUT}≤30mA	—	60	100	mV
ΔV_{LINE}	Line Regulation	—	I_{OUT}=1mA, 10V≤V_{IN}≤24V	—	0.2	—	%/V
t_{SU}	Startup Time (Falling Egde of CE to V_{OUT} Within Specification)	—	V_{IN}=10V, I_{OUT}=10mA, C_L=10μF	—	3.3	5.0	ms
		—	V_{IN}=10V, I_{OUT}=10mA, C_L=0.1μF	—	700	1400	μs
$\frac{\Delta V_{OUT}}{\Delta T_a}$	Temperature Coefficient	3.3V	I_{OUT}=10mA, -40°C < Ta < +85°C	—	±0.50	—	mV/°C
		5.0V		—	±0.75	—	mV/°C
Voltage Detector							
V_{DET}	Detection Voltage	—	V_{LVD}=9.0V	V_{LVD}-0.3	V_{LVD}	V_{LVD}+0.3	V
V_{HYS}	Hysteresis Width	—	—	—	0.05 V_{DET}	—	V
$\frac{\Delta V_{DET}}{\Delta T_a}$	Temperature Coefficient	—	-40°C < Ta < +85°C	—	±0.9	—	mV/°C
Comparator							
t_{RES}	Response Time	—	—	—	—	10	μs
V_{HC}	hysteresis Window	—	—	—	0.15	—	V
V_{COM}	Common-Mode Input Range	—	—	V_{SS}+1.5	—	V_{IN}-1	V

Note: 1. ΔV_{OUT} is calculated as the difference between the output voltage under testing and the output voltage which is measured at I_{OUT} =10mA.
2. V_{IO} specification is design guaranteed.

Functional Description

These devices provide a way to transmit and receive data on the common power lines of an interconnected array of microcontroller based subsystems. By having one of these devices inside each subsystem, the shared power and data cabling can be reduced to a simple two line type, offering major installation cost reductions.



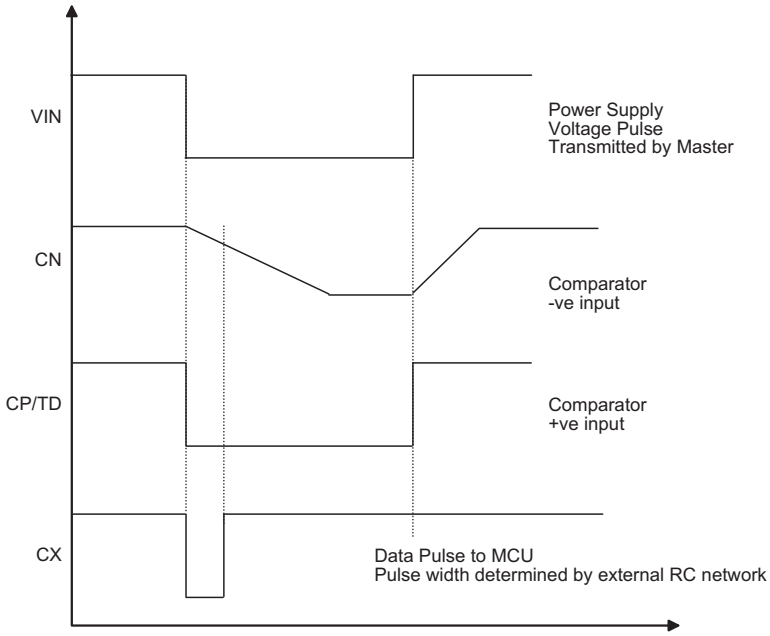
System Block Diagram

Shared Power Line

All microcontroller based subsystems are connected together via the same two line power connection. The ground line is hardwired to each subsystem while the positive power line is connected to the VIN pin on each of the HT71D0x devices. An internal Low Dropout Voltage Regulator within the HT71D0x devices, converts this input power supply voltage to a fixed voltage level which is supplied to the subsystem microcontroller and other circuit components. In this way when the power line voltage is changed due to the transmission or reception of data the subsystem circuits still continue to receive a regulated power supply.

Data Transmission

Refer to the application circuit when reading the following description. Data information can be transmitted onto the positive power line by reducing the voltage level for a short time duration. As the devices include a voltage regulator which is used as the power supply to the subsystem units, then the subsystem power supply voltage will not be affected as long as the regulator minimum dropout voltage is maintained. However a reduction in the power supply will be detected by the C1 internal comparators. The output of this comparator is connected to an open drain NMOS transistor, Q1, whose open drain output on pin CX can be connected to a microcontroller input for use as a data signal.



Power Line Data Reception

Data Reception

Refer to the application circuit when reading the following description. The individual subsystems can transmit data to the master controller along the power supply line by using one of its I/O lines to reduce the positive power line supply line voltage level for a short time duration. An output line on the subsystem microcontroller should be connected to the TG pin. An internal comparator, C2, whose positive input is connected to an internal voltage reference, will detect if this pin is pulled low. The comparator output is connected to an internal open drain NMOS transistor, Q4, which will pull the CP/TD line low. By connecting a suitable value resistor between the CP/TD pin and the power supply line, the correct value of power supply voltage reduction can be implemented.

Protection Circuits

The devices include an internal Voltage Detector function which monitors the power supply input voltage. Should the input power supply voltage fall below a safe level specified by the voltage detector level, then the voltage detector output will change state and disable the internal regulator thus removing the power supply source to the subsystem circuits. An internal NMOS transistor whose drain is connected to the output power supply line, VO will also turn on keeping the VO level close to zero. This ensures that the subsystem microcontroller receives the proper power on reset conditions. When power is applied an external capacitor, connected to pin CDLY, together with an internal resistor, RPU1, implement a power on delay time for the internal LDO.

Application Considerations

It is envisaged that the devices will be used together with microcontroller based subsystems which will be required to provide two I/O pins for data transmission and reception. The MCU pin connected to the TG pin must be setup as an output while the MCU pin connected to the CX pin must be setup as an input.

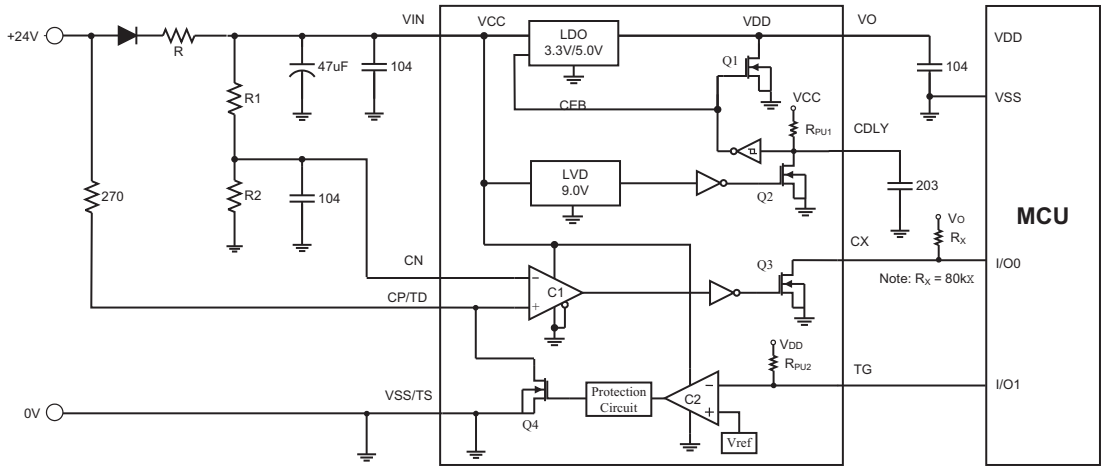
The power supply impedence will play an important role in applications using these devices and must be well defined for reliable data transmission and reception.

The external components connected to the CP/TD pin must be chosen carefully to ensure that an adequate pulse duration on pin CX is generated.

The usual decoupling precautions must be taken to ensure reliable operation.

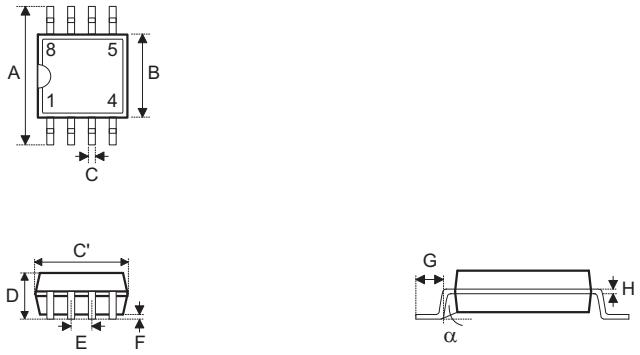
Application Circuits

The following application circuit shows the device used in conjunction with a microcontroller.



Package Information

8-pin SOP (150mil) Outline Dimensions

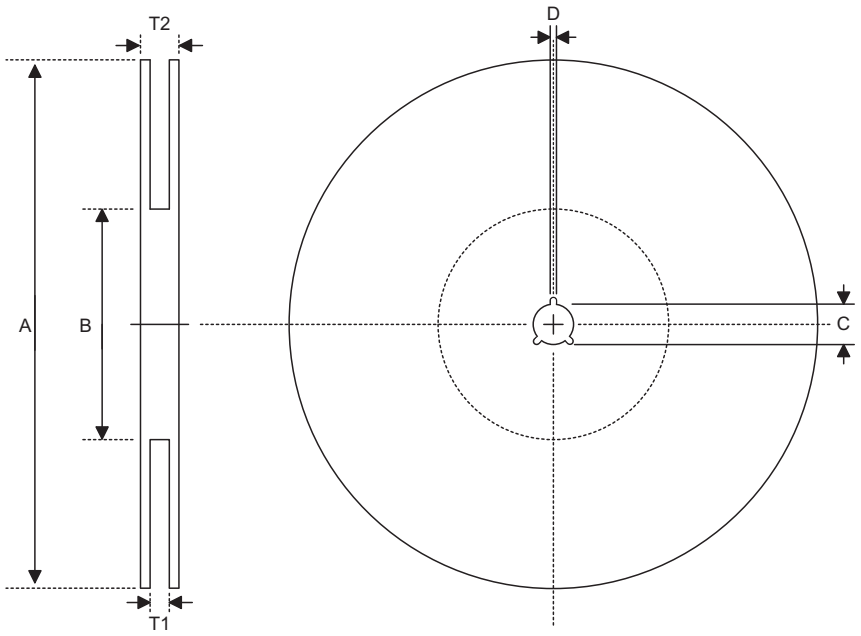


MS-012

Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	0.228	—	0.244
B	0.150	—	0.157
C	0.012	—	0.020
C′	0.188	—	0.197
D	—	—	0.069
E	—	0.050	—
F	0.004	—	0.010
G	0.016	—	0.050
H	0.007	—	0.010
α	0°	—	8°

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	5.79	—	6.20
B	3.81	—	3.99
C	0.30	—	0.51
C′	4.78	—	5.00
D	—	—	1.75
E	—	1.27	—
F	0.10	—	0.25
G	0.41	—	1.27
H	0.18	—	0.25
α	0°	—	8°

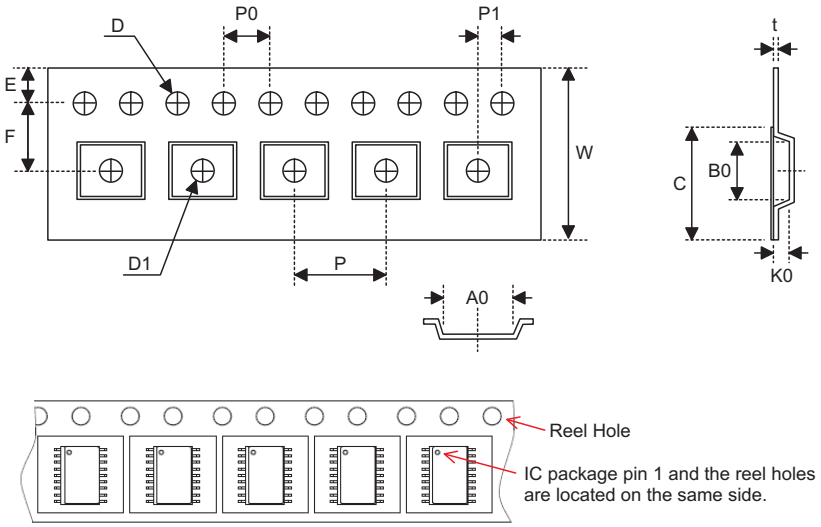
Reel Dimensions



SOP 8N

Symbol	Description	Dimensions in mm
A	Reel Outer Diameter	330.0±1.0
B	Reel Inner Diameter	100.0±1.5
C	Spindle Hole Diameter	$13.0^{+0.5/-0.2}$
D	Key Slit Width	2.0±0.5
T1	Space Between Flange	$12.8^{+0.3/-0.2}$
T2	Reel Thickness	18.2±0.2

Carrier Tape Dimensions



SOP 8N

Symbol	Description	Dimensions in mm
W	Carrier Tape Width	12.0 $^{+0.3/-0.1}$
P	Cavity Pitch	8.0±0.1
E	Perforation Position	1.75±0.1
F	Cavity to Perforation (Width Direction)	5.5±0.1
D	Perforation Diameter	1.55±0.1
D1	Cavity Hole Diameter	1.50 $^{+0.25/-0.00}$
P0	Perforation Pitch	4.0±0.1
P1	Cavity to Perforation (Length Direction)	2.0±0.1
A0	Cavity Length	6.4±0.1
B0	Cavity Width	5.2±0.1
K0	Cavity Depth	2.1±0.1
t	Carrier Tape Thickness	0.30±0.05
C	Cover Tape Width	9.3±0.1

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