



SiRFstarIII GPS Architecture GSC3 Family High Performance GPS Single Chip

ARCHITECTURE HIGHLIGHTS

Next Generation GPS Performance

- High sensitivity for indoor fixes
- Extremely fast TTFFs at low signal levels
- Real-time navigation for location-based services
- Low 100 ms interrupt load on microprocessor for easy IP implementation
- SBAS (WAAS and EGNOS) support

SiRFLoc™ Client AGPS Support

- SiRF's patented end-to-end solution
- Multi-modes: mobile centric to network centric
- Multi-standard support: 3GPP, 3GPP2, PDC, iDEN, and TIA-916
- Supports A13 and F interfaces

GSW3 - Modular Software Support

- API compatible with GSW2
- RTOS friendly

GSC3 PRODUCT HIGHLIGHTS

GSC3 - Digital and RF Single Chip

- 200,000+ effective correlators for fast TTFF and high sensitivity acquisitions
- 20-Channel GPS receiver
- Digital and RF in a single package
- Small 7 mm x 10 mm x 1.4 mm BGA package
- ARM7TDMI CPU and SRAM to enable user tasks
- Accepts seven reference frequencies between 13 MHz to 33 MHz
- Extensive GPS receiver peripherals: 2 UARTS, high speed serial bus, battery-backed SRAM, and 14 GPIOs

Built On Proven Experience

- IP integration experience
- Highly developed design tools
- FCC E911 compliance experience

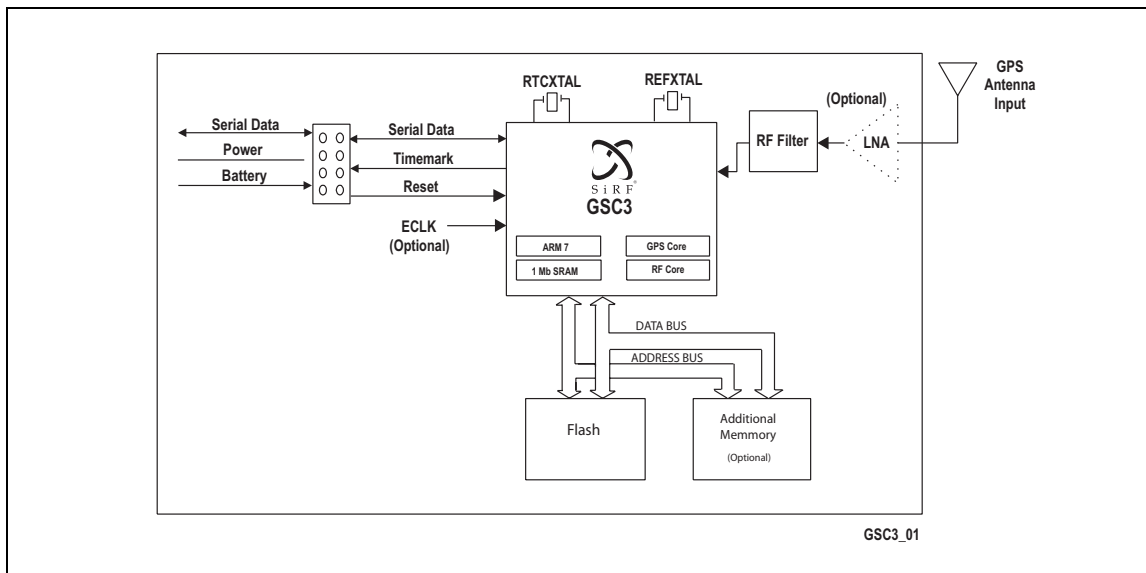


Figure 1. Sample Architecture Diagram

SiRFstarIII ARCHITECTURE DESCRIPTION

Wireless and handheld applications make rigorous demands on GPS; receivers are pushed to get fixes in places never before expected and in times measured in only seconds. SiRF Technology has risen to the challenge with the SiRFstarIII; a GPS architecture based on three generations of experience. This experience includes getting customers from design to production in the shortest time possible, developing IP solutions based on production-worthy silicon, and creating a chipset that goes far beyond the FCC's E911 mandate.

The SiRFstarIII has the performance required to meet the industry's toughest challenges. With 200,000+ effective correlators, the SiRFstarIII can acquire in only seconds even at low signal levels. As part of SiRF's patented multi-mode GPS, the SiRFstarIII can track signal levels as low as -159 dBm. The SiRFstarIII supports real-time navigation in urban canyons as well as high sensitivity acquisition needed for indoor environments. With power management and low power silicon, the SiRFstarIII can get a fix in a fraction of a joule.

For very high volume customers, the SiRFstarIII and software is designed in modular blocks specifically to make IP integration easier. It is an RTOS friendly design and supports power management and user task integration.

GSC3 DESCRIPTION

The GSC3 is SiRF's advanced SiRFstarIII receiver in a single package. Both the baseband and the RF are integrated into the 7mm x 10mm package making for an extremely compact design. The GSC3 includes a powerful GPS DSP integrated with an ARM7TDMI microprocessor and 1 Mb of SRAM. The GSC3 architecture uses an FFT and Matched Filter that delivers performance equivalent to more than 200,000 correlators. This represents a quantum leap forward in GPS performance. While some A-GPS receivers can acquire at low signal levels, the SiRFstarIII's architecture enables unmatched TTFF at low signal levels. This allows a richer user experience, which is important since slow or poorly performing applications often fail in the market place.

The GSC3's RF section is the most highly integrated lowest-power SiRF RF silicon to date. The RF section integrates an RTC and monitor circuitry as well as many components that were previously on the board into the silicon while reducing RF current consumption to 13 mA. The GSC3 can share an RTC and the reference oscillator supports different input frequencies. This means that designs can be simpler and smaller, and batteries can be smaller and last longer.

The small form factor of the GSC3 in combination with the frequency sharing abilities of the RF section allows for very compact receiver designs. The sensitivity of the GSC3 can also be used to help overcome a high loss antenna such as the type often required by small consumer designs.

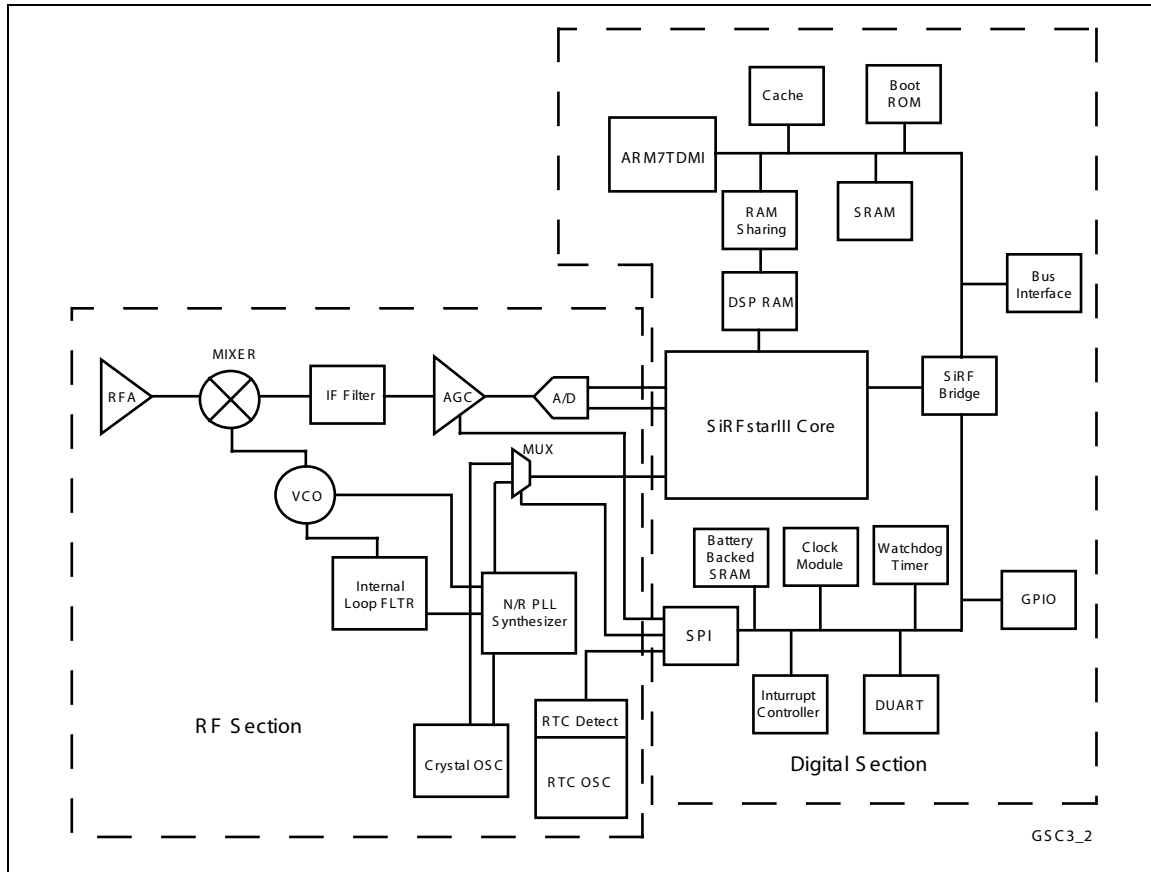


Figure 2. GSC3 Internal Block Diagram

FUNCTIONAL DESCRIPTION

The GSC3 is optimized for location applications requiring high performance in a small form factor. The single chip solution is offered as a 140-pin (7 mm x 10 mm) BGA with integrated digital and RF sections. The GSC3 contains a powerful GPS engine built on a low power 0.13 μ CMOS process with a 1.5 V core. The chip can run on a single 2.85 V power using internal voltage regulators to create the smallest form factor. Alternatively, these regulators can be bypassed for lower power consumption if 1.5 V power is already available in the system. The internal functions of the digital section are split into two main parts that are defined by the buses that run them. The ARM System Bus (ASB) has all the core CPU components and the SiRF IP bus (SIPB) contains all the GPS and other DSP peripherals. The ARM and DSP share memory for a more cost effective and gate efficient design.

The digital section is described first followed by the RF section.

DIGITAL SECTION DESCRIPTION

SiRFstarIII Core

The SiRFstarIII core is built around a reconfigurable high-output segmented matched filter in conjunction with an FFT processor, which can search all 1023 chips of the GPS code simultaneously over a wide frequency range for fast initial acquisition with large uncertainties. The flexibility of the core allows the core processing engine and memory to be reconfigured to track more than 20 satellites using the same hardware. This flexibility makes the SiRFstarIII a highly efficient engine for a wide variety of location applications. The SiRFstarIII core contains a built-in sequencer, which handles all the high-rate interrupts for GPS and SBAS (WAAS, EGNOS) tracking and acquisitions. After initialization, the core handles all the time critical and

low latency acquisition, tracking and reacquisition tasks of GPS and SBAS autonomously. The core provides interrupts, which in turn provides measurement data to the CPU for computation of the navigation solution.

The SiRFstarIII core also provides time and frequency management. This includes the basic clock counters, alarms, edge-aligned ratio counters (EARC) and synchronization blocks used to provide the system time line and to transfer accurate time and frequency into and out of the system. An EARC is an improved (SiRF patented) type of ratio counter used to transfer frequency accuracy among asynchronous clocks using a stroboscopic edge-alignment technique to capture measurements when the clock edges are closely aligned in time.

ARM7TDMI

The ARM7TDMI is an ideal core providing high performance and low power consumption. The ARM7TDMI CPU can run at speeds up to 50 MHz and is supported by a wide variety of development tools. Because the SiRFstarIII core eliminates the need for the CPU to service high-rate interrupts, it is easier than ever to use the ARM processing power for user tasks.

The ARM7TDMI includes a JTAG interface, which provides a standard development/ debugging interface that connects to a variety of off-the-shelf emulators. This provides single-step, trap and access to all the internal registers of the digital section of the GSC3.

Battery-Backed SRAM (BB-SRAM)

The GSC3 contains a small block of battery-backed SRAM which contains all necessary GPS information for hot starts and a small amount for user configuration variables.

Boot ROM

The Boot ROM contains a small code set that can load a set of user code through the dual UART into the SRAM and execute it. This allows the GSC3, for example, to update Flash.

Bus Interface Unit

The Bus Interface Unit (BIU) provides an external 16-bit interface for memory or peripherals. Byte, half-word and word transactions are supported. Each chip select addresses a 2-Mb address space with an independent start address. The external source for Boot code memory must be selected by CS0. The number of wait states for each chip select can be independently set with a maximum of seven.

Cache

A two-way 8 KB associative instruction/data cache provides a fast access memory for $\overline{\text{CS0}}$ only.

Clock Module

This block manages the four major internal clocks: Acquisition (ACQ) Clock, Signal Processing (SP) Clock, Bus (B) Clock, and RTC. These clocks run the SiRFstarIII DSP and ARM and control the various power management modes allowing for maximum power savings and system flexibility.

Default Memory Map Configuration

Address(19:0)	Signal	Description
43FF FFFF ... 4300 0000	CS3	Available
42FF FFFF ... 4200 0000	CS2	Available
41FF FFFF ... 4100 0000	CS1	Available
40FF FFFF ... 4000 0000	CS0	External Memory

DUART

The GSC3 contains two full duplex serial ports. One port is normally used for GPS data reports and receiver control and the second serial port is used for the reception of differential corrections (RTCM). The transmit and receive side of each port contains a 16-byte deep FIFO with selectable bit rates ranging from 1.2 to 115.2 Kbps.

GPIO Unit

The GSC3 supports a variety of peripherals through 14 GPIO lines. The GPIO unit centralizes management of all GPIO lines and provides a simple software interface for their control.

Interrupt Controller

The Interrupt Controller manages all possible internal or external sources of interrupts. These include the SiRFstarIII core, SBAS, DSP, DUART and external user interrupts.

SiRF Bridge Unit

The SiRF Bridge Units (SBU1 and SBU2) provide low power access to peripherals. SBU1 provides access to general purpose ARM peripherals such as the serial port UARTS, RTC and interrupt controller. SBU2 provides access to the DSP core and its associated memory. The DSP core also uses this bus for internal communications. The ARM is able to perform byte, half-word and word transactions via the 32-bit peripheral busses.

SRAM

The on-chip SRAM size is 1 Mbit (32Kx32) memory that can be used for instructions or data. In many applications, it completely eliminates the need for external data memory. The SRAM is designed for a combination of low power and high speed, and can support single cycle reads for all bus speeds.

Synchronous Peripheral Interface

The Synchronous Peripheral Interface (SPI) port handles communication, such as reference frequency selection, AGC, and power control, between the digital

and RF sections. The RF section acts in slave mode and can only be controlled by the digital section using SiRF software. The SPI port consists of: SPI_CLK, SPI_DI, SPI_DO and SPI_CEB for the RF section, and corresponds to SK, SI, SO and CEB in the digital section. The SPI port does not support additional SPI devices. Figure 3. illustrates the timing of waveforms of the SPI port.

DSP RAM and RAM Sharing

The GSC3 includes RAM for the use of the DSP and RAM which can be shared between the ARM and DSP core. This keeps the overall size of the chip down while maximizing the availability of memory.

Factory Testing

The GSC3 uses a memory built-in self-test called MEMBIST to provide complete coverage of all the memory during chip testing and qualification. This is combined with the SCAN block using Automatic Test Pattern Generation (ATPG) at the wafer level to provide functional test coverage. (These functions are not available to customers.)

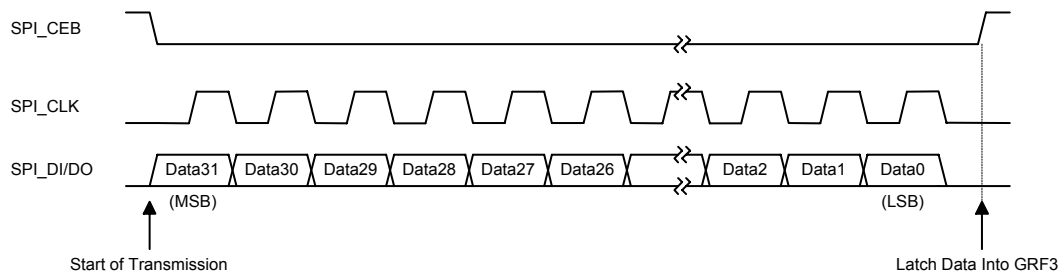


Figure 3. SPI Port Timing Waveforms

GSC3 RF SECTION DESCRIPTION

RFA

The RF section receives the GPS L1 signal via an external antenna. The L1 input signal is a Direct Sequence Spread Spectrum (DSSS) signal at 1575.42 MHz with a 1.023 Mbps Bi-Phase Shift Keying (BPSK) modulated code. Since the input signal power at the antenna is nominally -130 dBm (spread over 2 MHz), the desired signal is below the thermal noise floor. With a front-end input compression point of -65 dBm, rejection of large out-of-band signals is possible given filtering in the IF section. The RFA uses a single-ended RF input for ease of use.

Image-Reject Mixer

The image-reject mixer is a double balanced design, which significantly reduces common mode interference. The Image Reject Mixer block also contains an I-Q phase shift combiner. This circuit properly phase shifts and sums the I and Q outputs internal to the image reject mixer to a single channel and achieves an RF image suppression in excess of 20 dB. By using an image reject mixer, an inexpensive pre-select RF filter may be used. The Mixer and on-chip 1571.424 MHz VCO produce an IF center frequency of 3.996 MHz.

IF Filter

An IF filter is required between the Mixer and AGC Amplifier to provide an anti-aliasing function before A/D conversion. In the RF section, the IF filter has been integrated on-chip, thus minimizing the number of external parts on the board. This filter provides typically >20 dB roll-off at the alias frequency (located at $F_S - F_{IF}$, where F_S is the ADC sample rate) which makes the contribution of C/No degradation due to Nyquist noise folding insignificant. Thus, the combined effects of IF noise aliasing and RF image conversion have a negligible impact to C/No performance.

AGC Amplifier and Control Block

The AGC amplifier provides the additional gain needed to optimally load the signal range of the 2-bit A/D Converter. The AGC IF gain is digitally controlled by an AGC Control block, which loads and registers digital gain setting words from GSC3 via the four wire SPI interface. The 5-bit AGC Control register allows the SiRFstarIII receiver to compensate for roughly 50 dB variation in system gain for all causes including temperature front-end configuration, and process variations.

A/D Converter

The AGC amplifier output drives a 2-bit A/D Converter which provides sign and magnitude output bits to the Interface block. The combination of 2-bit quantization and oversampling in the SiRFstarIII architecture provides significant improvement in C/No and CW jamming immunity over 1-bit systems.

RTC Oscillator

This circuit is designed to drive a 32-KHz crystal. This oscillator is operational during the sleep cycle of the RF section. The main section is specifically designed using a pseudo-inverter topology that provides sufficient gain to start oscillation of the crystal with minimum startup time and minimum current consumption. The crystal is connected between the input and output of this inverter. An internal differential stage followed by a series of inverters is included to convert and drive the oscillation amplitude to CMOS levels. The RTC oscillator circuit also includes a start-up circuitry for the bias section to guarantee fast and reliable startup.

RTC Detector

During sleep mode special circuitry is used to monitor the output of the RTC oscillator and indicate the status of the RTC clock upon request from the baseband once the chip is back in normal operation. If during the sleep

mode the RTC oscillator output is lost for at least ten periods, the RF section flags the baseband via the SPI that the RTC clock is not valid. This feature guards against failure due to temporary disconnection of the crystal, lowering of the supply voltage below the functional level or temporary loss of the power.

Reference Oscillator

The Reference Oscillator circuit is designed to drive a 13 to 33.6 MHz crystal (optimal performance is achieved using a TCXO). The main section is specially designed using a pseudo-inverter topology that provides sufficient gain to start oscillation of the crystal with minimum start-up time and minimum current consumption. The crystal is connected between the input and output of this inverter. An internal differential stage followed by a series of inverters is included to convert and drive the oscillation amplitude to CMOS levels. The reference oscillator circuit also includes a start-up circuitry for the bias section to guarantee fast and reliable start-up.

Frequency Synthesizer

The RF section's GPS down-converter includes an N/R synthesizer that will allow the use of a range of reference oscillators. The synthesizer generates the local oscillator signal for the image reject mixer and also generates the CLKACQ. If the reference crystal is chosen to be 16.369 MHz, the CLKACQ can also be generated from reference crystal directly (this is the default).

The synthesizer is programmed by software using "N" and "R" words. "N" represents the division ratio of the loop and "R" represents division ratio of the reference signal.

$$[f_{out} / f_{ref}] = N / R$$

N and R inputs are determined by the baseband controller using configuration straps at start-up. The frequencies supported are shown in Table 1.

Table 1. Supported Frequencies

F _{ref} MHz
13
16.369
16.8
19.2
24.5535
26
33.6

The local oscillator and sample clock (CLKACQ) are derived from an on-chip PLL synthesizer block. The VCO, dividers and phase detector are provided in the chip.

Internal Loop Filter

Internal loop filter has been implemented in RF section to reduce pin count and improve noise immunity on the control node of the VCO. The internal loop filter is adjusted automatically for each input crystal reference frequency to optimize the poles and zeros to achieve optimum loop stability. The loop filter of the RF section synthesizer is an on-chip RC filter.

Clock_Mux

If the system crystal is 16.369 MHz then the Clock Mux circuitry allows additional power saving modes by switching off the PLL and using the system as the source of the system clock. To avoid glitches, the transition is made by forcing the output low until the switch is completed. The selection of the clock is programmed by the digital section through the SPI interface.

SAMPLE CONNECTION DIAGRAM

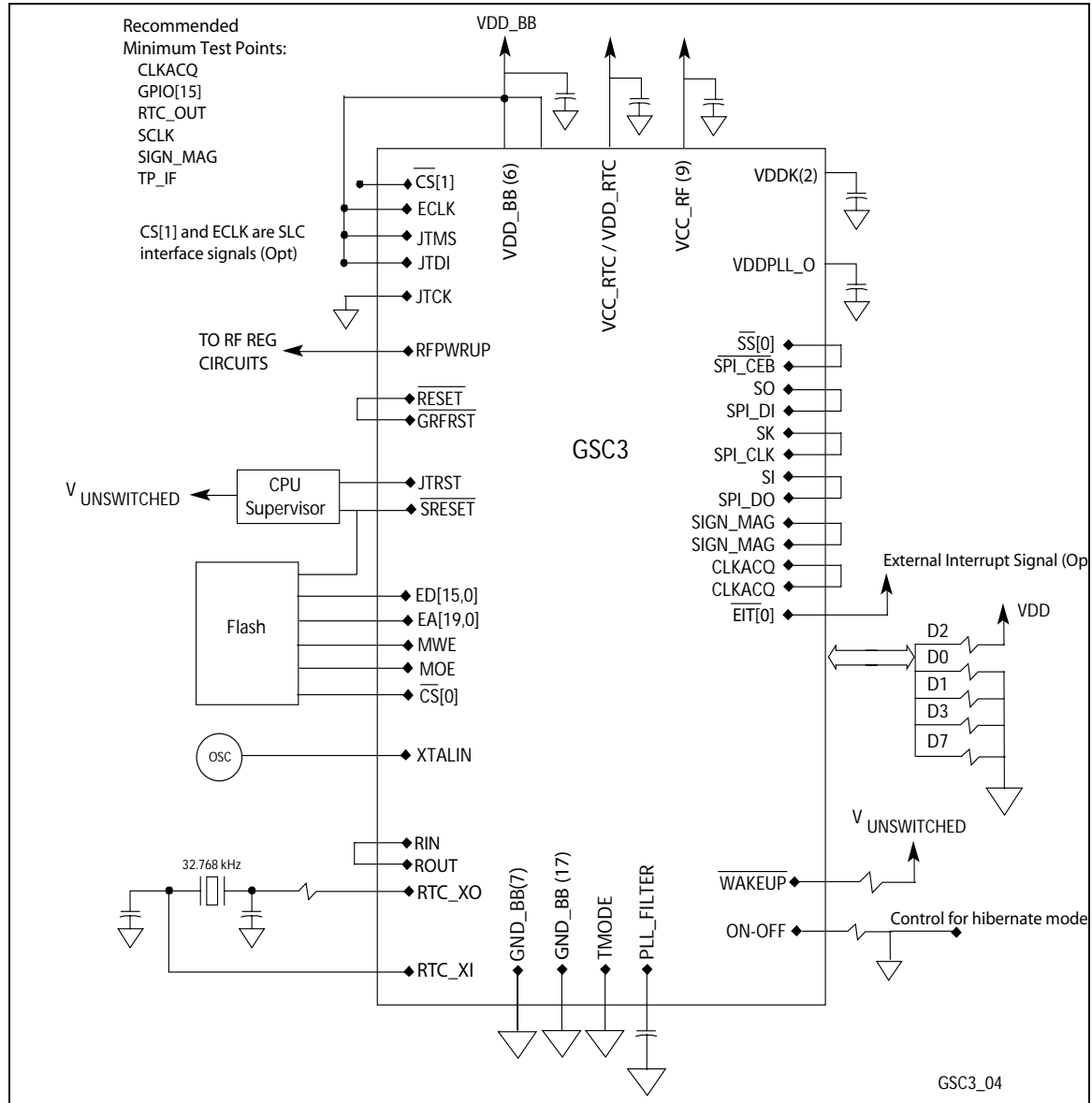


Figure 4. 7871 Series – 24.5535 MHz Configuration

	1	2	3	4	5	6	7	8	9	10
A	GND_BB	ODO	Reserved	GPIO[0]	RXA	TXA	ECLK	SCLK	EA[0]	VDDPLL_O
B	RFPWRUP	$\overline{\text{MWE}}$	VDD_FLASH	VDD_RTC	$\overline{\text{EIT}}[0]$	EA[4]	TXB	Reserved	EA[1]	VDDK
C	$\overline{\text{CS}}[2]$	ED[1]	ED[10]	VDD_REG	VDD_PLL	TIMEMARK	RXB	Reserved	EA[3]	VDDK
D	$\overline{\text{MOE}}$	ED[4]	$\overline{\text{CS}}[0]$	VDD_BB	GND_BB	GND_BB	E[A2]	EA[5]	EA[6]	TMODE
E	$\overline{\text{CS}}[3]$	ED[9]	ED[8]	VDD_BB	GND_BB	GND_BB	$\overline{\text{WAKEUP}}$	EA[7]	EA[8]	ROUT
F	$\overline{\text{CS}}[1]$	ED[3]	ED[2]	VDD_BB	GND_BB	GND_BB	VDD_REG	EA[18]	EA[19]	RIN
G	ED[0]	ED[12]	ED[11]	ED[14]	EA[16]	EA[15]	EA[13]	EA[11]	EA[9]	ON_OFF
H	$\overline{\text{SS}}[1]$	ED[5]	ED[13]	ED[6]	EA[17]	PLL_FILTER	EA[14]	EA[12]	EA[10]	$\overline{\text{RESET}}$
J	JTDI	ED[7]	ED[15]	CLKACQ	SIGN_MAG	SI	SK	SO	$\overline{\text{SS}}[0]$	$\overline{\text{SRESET}}$
K	JTRST	VDD_BB	AGCPWM	CLKACQ	SIGN_MAG	SPI_DO	SPI_CLK	SPI_DI	$\overline{\text{SPL_CEB}}$	RTC_OUT
L	JTMS	VDD_BB	VDD_BB	GND_RF	GND_RF	GND_RF	GND_RF	GND_RF	GND_RF	RTC_XO
M	JTDO	VCC_RF	VCC_RF	VCC_RF	VCC_RF	VCC_RF	VCC_RF	VCC_RF	VCC_RF	VCC_RF
N	JTCK	GND_RF	GND_RF	GND_RF	GND_RF	GND_RF	GND_RF	GND_RF	GND_RF	GND_RF
P	$\overline{\text{GRFRST}}$	XTAL_IN	XTAL_OUT	TP_IF	GND_RF	RFIN	GND_RF	VCC_IO_EXT	VCC_RTC	RTC_XI

Figure 5. GSC3-7871 140 pin BGA Ball Configuration Diagram (Top View)

Note: Refer to Table 2. for signals that have alternate functions.

Table 2. GSC3 Series Pin Identification

Name	7851 Ball	Name	7851 Ball	Name	7851 Ball	Name	7851 Ball
AGCPWM/GPIO[2]	K3	ED[6]	H4	GPIO[0]	A4	SS[0] / GPIO[3]	J9
CLKACQ (In)	J4	ED[7]	J2	GPIO[1] / ODO	A2	SS[1]/ GPIO[4]	H1
CLKACQ (Out)	K4	ED[8]	E3	GRFRST	P1	TIMEMARK / GPIO[9]	C6
Reserved	A3	ED[9]	E2	JTCK	N1	TMODE	D10
CS[0]	D3	ED[10]	C3	JTDI	J1	TP_IF	P4
CS[1]/ GPIO[13]/ CTS	F1	ED[11]	G3	JTDO	M1	TXA	A6
CS[2]/ GPIO[14]/ RTS	C1	ED[12]	G2	JTMS	L1	TXB	B7
CS[3]/GPIO[15]/YCLK	E1	ED[13]	H3	JTRST	K1	VCC_IO_EXT	P8
EA[0]	A9	ED[14]	G4	MOE	D1	VCC_RF	M2
EA[1]	B9	ED[15]	J3	MWE	B2		M3
EA[2]	D7	EIT[0]/ GPIO[10]	B5	ON_OFF	G10		M4
EA[3]	C9	GND_BB	A1	PLL_FILTER	H6		M5
EA[4]	B6		D5	Reserved	C8		M6
EA[5]	D8		D6		B8		M7
EA[6]	D9		E5	RESET	H10		M8
EA[7]	E8		E6	RFIN	P6		M9
EA[8]	E9		F5	RFPWRUP/ GPIO[8]	B1		M10
EA[9]	G9		F6	RIN	F10	VCC_RTC	P9
EA[10]	H9	GND_RF	L4	ROUT	E10	VDD_RTC	B4
EA[11]	G8		L5	RTC_OUT	K10	VDD_BB	D4
EA[12]	H8		L6	RTC_XI	P10		E4
EA[13]	G7		L7	RTC_XO	L10		F4
EA[14]	H7		L8	RXA	A5		K2
EA[15]	G6		L9	RXB	C7		L2
EA[16]	G5		N2	SCLK	A8		L3
EA[17]	H5		N3	SI / GPIO[5]	J6	VDD_FLASH	B3
EA[18]	F8		N4	SIGN_MAG (In)	J5	VDD_PLL	C5
EA[19]	F9		N5	SIGN_MAG (Out)	K5	VDD_REG	C4
ECLK	A7		N6	SK / GPIO[7]	J7		F7
ED[0]	G1		N7	SO/ GPIO[6]	J8	VDDK	C10
ED[1]	C2		N8	SPI_CEB	K9		B10
ED[2]	F3		N9	SPI_CLK	K7	VDDKPLL_O	A10
ED[3]	F2		N10	SPI_DI	K8	WAKEUP	E7
ED[4]	D2		P5	SPI_DO	K6	XTAL_IN	P2
ED[5]	H2		P7	SRESET	J10	XTAL_OUT	P3

Table 3. GSC3 Signal Description

Signals	Type	Description															
Address and Data Pins - CPU Interface																	
EA[19:0] ³	O	System address bus.															
ED[0] ⁴	I/O	External data bus bit 0. Read on power-up to determine boot: 1 = internal 0 = external															
ED[1] ⁴	I/O	External data bus bit 1															
ED[3:2] ⁴	I/O	External data bus bits 2 to 3. Read on power-up to determine boot clock: <table border="1"> <tr> <td>Boot Clock</td><td>ED[3]</td><td>ED[2]</td></tr> <tr> <td>Reserved</td><td>0</td><td>0</td></tr> <tr> <td>RTCCLK</td><td>0</td><td>1</td></tr> <tr> <td>ECLK</td><td>1</td><td>0</td></tr> <tr> <td>CLKACQ</td><td>1</td><td>1</td></tr> </table>	Boot Clock	ED[3]	ED[2]	Reserved	0	0	RTCCLK	0	1	ECLK	1	0	CLKACQ	1	1
Boot Clock	ED[3]	ED[2]															
Reserved	0	0															
RTCCLK	0	1															
ECLK	1	0															
CLKACQ	1	1															
ED[6:4] ⁴	I/O	External data bus bits 4 to 6.															
ED[7] ⁴	I/O	External data bus bit 7. Must be pulled down.															
ED[15:8] ^{1, 4}	I/O	Upper 8 bits of the bi-directional system data bus.															
$\overline{\text{CS}}[0]$ ¹	O	External memory chip select.															
$\overline{\text{CS}}[3:1]$ ^{1, 5}	I/O	External memory chip select.															
$\overline{\text{MWE}}, \overline{\text{MOE}}$ ³	O	External memory write enable and output enable.															
ECLK ²	In	External CMOS clock source.															
SCLK	O	System clock. All the control signals on the system bus synchronize with the system clock.															
$\overline{\text{SRESET}}$	In	The system reset that triggers an internally generated reset called RESET. The RTC counters are not affected by $\overline{\text{SRESET}}$.															
RTC Interface Pins																	
RIN	In	32 kHz clock input from RF section.															
ROUT	O	No connect. May be used as a test point.															
$\overline{\text{WAKEUP}}$	OD	Wake-up from RTC (Open Drain).															

Table 3. GSC3 Signal Description (Continued)

Signals	Type	Description
RF Interface Pins		
AGCPWM	I/O	Not used.
CLKACQ	In	Data acquisition clock.
SIGN_MAG ⁵	In	Satellite sign and magnitude bits.
$\overline{\text{RESET}}$	OD	An internally generated reset based on $\overline{\text{SRESET}}$. This reset acts on the digital core, RF section, and any external devices controlled by $\overline{\text{RESET}}$.
RFPWRUP ^{3, 5}	O	Power control of RF chip. Alternate function is GPIO line 8.
Peripheral Interface		
CTS ⁵	I/O	Clear to send/not, hardware flow control. Alternate functions are CS1 and GPIO 13.
$\overline{\text{EIT}}[0]$ ⁴	I/O	External interrupt[0]. Alternate function is GPIO line 10.
ON_OFF	In	Edge triggered soft on/off request. Should only be used to wake up chip.
PLL_FILTER	Ana	External filter for PLL (analog pin).
RXA, RXB ¹	In	Serial inputs for channel A and B.
$\overline{\text{RTS}}$ ⁵	I/O	Request to send/not, hardware flow control. Alternate functions are CS2 and GPIO 14.
$\overline{\text{SS}}[0]$ ^{1, 5}	I/O	SPI slave select 0. Alternate function GPIO[3]
$\overline{\text{SS}}[1]$ ^{1, 5}	I/O	SPI slave select 1. Alternate function GPIO[4].
SI, SO, SK ^{2, 4, 5}	I/O	Digital synchronous serial interface (in, out and clock). Reserved for RF interface.
TIMEMARK ^{2, 5}	I/O	1 PPS timemark output.
TMODE	In	Reserved.
TXA, TXB	O	Serial outputs for channel A and B.
YCLK ⁵	In	Y Clock is an auxiliary clock input that supports dual frequency oscillator calibration systems. Alternate functions are CS3 and GPIO 15.

Table 3. GSC3 Signal Description (Continued)

Signals	Type	Description															
Debug Interface Pins																	
JTDI, JTCK, JTRST, JTMS	In	JTAG Interface. During boot-strap these pins determine RF reference frequency as follows: <table> <tr> <td>Frequency</td><td>JTCK</td><td>JTDI</td></tr> <tr> <td>16.369 MHz</td><td>0</td><td>0</td></tr> <tr> <td>24.5535 MHz</td><td>0</td><td>1</td></tr> <tr> <td>26.0 MHz</td><td>1</td><td>0</td></tr> <tr> <td>Reserved*</td><td>1</td><td>1</td></tr> </table> Strapping options cannot be used when in debug mode, software must configure ref freq setting. *Can also be programmed for 13, 16.8, 19.2 or 33.6 MHz. See SiRF representative for details.	Frequency	JTCK	JTDI	16.369 MHz	0	0	24.5535 MHz	0	1	26.0 MHz	1	0	Reserved*	1	1
Frequency	JTCK	JTDI															
16.369 MHz	0	0															
24.5535 MHz	0	1															
26.0 MHz	1	0															
Reserved*	1	1															
JTDO	O	Part of JTAG interface.															
GPIO Lines⁶																	
GPIO [0] ^{2, 4}	I/O	GPIO Line															
GPIO [1] ^{2, 4}	I/O	GPIO Line. Alternate function is Odometer interface for SiRFDRIve.															
GPIO [2] ²	I/O	GPIO Line. Alternate function is AGCPWM.															
GPIO [3] ^{1, 4}	I/O	GPIO Line. Alternate function is SPI slave select 0.															
GPIO [4]	I/O	GPIO line. Alternate function is SPI slave select 1. Default state is input mode. Pad has no pull-up or pull-down resistor.															
GPIO [5-7] ^{2, 4}	I/O	GPIO Lines															
GPIO [8] ³	O	Reserved for RF power control. See RFPWUP.															
GPIO [9] ^{2,4}	I/O	GPIO Line															
GPIO [10] ⁴	I/O	GPIO Line. Alternate function is EIT[0]. Pad has no pull-up or pull-down resistor.															
GPIO [13] ^{1, 4}	I/O	GPIO Lines. Alternate function is CS1 or CTS.															
GPIO [14] ^{1, 4}	I/O	GPIO Lines. Alternate function is CS2 or RTS.															
GPIO [15] ^{1, 4}	I/O	GPIO Lines. Alternate function is CS3 or YCLK.															

Table 3. GSC3 Signal Description (Continued)

Signals	Type	Description
Supply		
VDD_BB	Supply	Digital section and I/O supply.
VDD_FLASH	Supply	Flash power at 3 V.
VDDK	Supply	Core power at 1.5 V (if using VDD_REG, VDDK requires output bypass capacitor).
VDDPLL_O	Supply	Regulator output supply to PLL.
VDD_PLL	Supply	Power for PLL.
VDD_REG	Supply	Power input at 3 V to core regulator.
VDD_RTC	Supply	RTC circuit supply.
GND_BB	Ground	GSC3 ground.
GSC3 RF Signals		
XTAL_OUT	Output	Crystal oscillator output: Use only when a crystal network is placed between this output and the XTAL_IN input in lieu of using an external oscillator.
VCC_RF	Supply	RF supply; must be properly bypassed.
RFIN	In	RFA input; GPS RF signal input. Must be AC coupled.
RTC_XI	In	RTC crystal oscillator input; a crystal network may be placed between this output and the RTC_XO input in lieu of using an external oscillator.
VCC_RTC	Supply	Backup battery supply; must be properly bypassed.
RTC_XO	O	RTC crystal oscillator output; a crystal network may be placed between this output and the RTC_XI input in lieu of using an external oscillator.
RTC_OUT	O	RTC crystal oscillator buffered output.
SPI_CEB, SPI_DI, SPI_CLK	In	RF synchronous serial interface (enable, data, and clock). Reserved for RF to digital interface.
SPI_DO	O	RF SPI interface output.
SIGN_MAG	O	SIGN and MAG combined output.
CLKACQ	O	CLKACQ output.
GRFRST	In	Reset input signal.



Table 3. GSC3 Signal Description (*Continued*)

Signals	Type	Description
GSC3 RF Signals (Continued)		
VCC_IO_EXT	Supply	Supply to external I/O section.
XTAL_IN	In	Reference oscillator input; a crystal network may be placed between this output and the XTAL_OUT input in lieu of using an external oscillator.
TP_IF	O	RF test point.
GND_RF	Ground	
Reserved		No connect reserved pins.

- Note 1:** Internal pull-up resistor (100k Ω nominal).
- Note 2:** Internal pull-down resistor (100k Ω nominal).
- Note 3:** Default output high at reset.
- Note 4:** Default input at reset.
- Note 5:** Share function with GPIO line.
- Note 6:** GPIO Lines are 3.3 V tolerant.
- Note 7:** All GND and VCC pins must be connected to ensure reliable operation. Good RF design practices must be adhered to in the PC board layout. A ground plane and a power plane must be used to obtain good performance.

ELECTRICAL SPECIFICATIONS

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Table 4. Absolute Maximum Ratings

Parameter	Symbol	Rating	Units
Digital Core and I/O (Volatile)			
Power Supply Voltage	VDD	4.8	V
Input Pin Voltage	VIN	5.25	V
Output Pin Voltage	VOUT	5.25	V
Latch-up Current	ILATCH	±200	mA
Storage Temperature	TSTG	-65 to 150	°C
Battery Block (Non-Volatile)			
Power Supply Voltage	VDD_RTC	2.0	V
Input Pin Voltage	VRIN	2.0	V
Output Voltage	VROUT	2.0	V
Latch-Up Current	ILATCHRTC	±200	mA
Open Drain Pull-Up Voltage	VOD	4.5	V
RF Section			
Maximum RF Supply Voltage		3.15	V
Maximum RF Input (RFA)		10	dBm
Minimum RF Voltage on Any Pin	GND	-0.5	V
Maximum RF Voltage on Any Pin		3.15	V
RTC Voltage	VCC_RTC	2.0	V

Warning – Stressing the device beyond the “Absolute Maximum Ratings” may cause permanent damage. These are stress ratings only. Operation beyond the “Operating Conditions” is not recommended and extended exposure beyond the “Operating Conditions” may affect device reliability.

Table 5. Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Units
Power Supply Voltage	VDD_(all)	2.7	2.85	3.0	V
Power Supply Voltage	VCC_(all)	2.7	2.85	3.0	V
RTC Supply Voltage	VCC_RTC	1.4	1.5	1.6	V
Battery Backed SRAM	VDD_RTC	1.4	1.5	1.6	V
Operating Temperature	TOPR	-40		85	°C
Peak Acquisition Current ¹	IDD			TBD	mA
Tracking Current ²	IDD		TBD		mA
Standby Current ³	IDD		1		mA
External Reference Amplitude (when driven externally, XTALIN must be ac-coupled)		200	-	1200	mVpp
External Reference Frequency Range		13	-	33.6	MHz

Note 1: Satellite acquisition is typically only the first few milliseconds of TTFF.

Note 2: Satellite tracking typically includes tracking and the post-acquisition portion of TTFF.

Note 3: During standby state the RTC block and core are powered on and the clock is off.

Table 6. Battery Conditions

Parameter	Symbol	Min.	Typ.	Max.	Units
RTC Supply	VDD_RTC	1.4 ¹	1.5	1.6	V
Supply Current ²	IDDRTC		10		µA
Power Supply ³	VDD	0	0	0	V

Note 1: Guaranteed by design.

Note 2: GSC3 includes a hibernate state where the chip can restart itself from the battery state.

Note 3: All external I/O lines must be driven low or disabled during battery back-up or hibernate state.

DC CHARACTERISTICS

Table 7. DC Electrical Characteristics for RTC Block (Non-Volatile Digital Section)

(Pins: RIN, ROUT, WAKEUP, ON_OFF, SRESET, RESET, and TMODE)

Parameter	Symbol	Min.	Typ.	Max.	Conditions	Units
High Level Input Voltage	V_{IH}	$0.8 \cdot V_{DDRTC}$		$V_{DDRTC} + 0.3$		V
Low Level Input Voltage	V_{IL}			$0.2 \cdot V_{DDRTC}$		V
Switching Threshold	V_T		$0.5 \cdot V_{DDRTC}$			V
High Level Input Current	I_{IH}	-10		10 60	$V_{IN} = V_{DD}$ with pull-down	μA
Low Level Input Current	I_{IL}	-10		10 -60	$V_{IN} = V_{SS}$ with pull-up	μA
High Level Output Voltage	V_{OH}	$0.75 \cdot V_{DDRTC}$			$I_{OH} = -2 \text{ mA}$	V
Low Level Output Voltage	V_{OL}			$0.25 \cdot V_{DDRTC}$	$I_{OL} = 2 \text{ mA}$ $I_{OL} = 1 \text{ mA}$ for $\overline{\text{WAKEUP}}$ and $\overline{\text{RESET}}$	V
Tri-State Output Leakage	I_{OZ}	-10		10	$V_{OUT} = V_{SS}$ or V_{DD}	μA
Input Capacitance	C_{IN}			5	Input or Bi-directional	pF
Output Capacitance	C_{OUT}			5	Output Buffer	pF

Table 8. DC Electrical Characteristics for Core (Volatile Digital Section)

Parameter	Symbol	Min.	Typ.	Max.	Conditions	Units
High Level Input Voltage	V_{IH}	$0.7 \cdot V_{DD}$		$V_{DD} + 0.3$		V
Low Level Input Voltage	V_{IL}	-0.3		$0.3 \cdot V_{DD}$		V
Switching Threshold	V_T		$0.5 \cdot V_{DD}$			V
High Level Input Current	I_{IH}	-10		10 60	$V_{IN} = V_{DD}$ with pull-down	μA
Low Level Input Current	I_{IL}	-10		10 -60	$V_{IN} = V_{SS}$ with pull-up	μA
High Level Output Voltage	V_{OH}	$0.75 \cdot V_{DD}$			$I_{OH} = -2 \text{ mA}$ for JTAG, GPIOs, TX and CS pins $I_{OH} = -4 \text{ mA}$ for all other pins	V
Low Level Output Voltage	V_{OL}			$0.25 \cdot V_{DD}$	$I_{OL} = 2 \text{ mA}$ for JTAG, GPIOs, TX, and CS pins $I_{OL} = 4 \text{ mA}$ for all other pins	V
Tri-State Output Leakage	I_{OZ}	-10		10	$V_{OUT} = V_{SS}$ or V_{DD}	μA
Input Capacitance	C_{IN}			4	Input or Bi-directional	pF
Output Capacitance	C_{OUT}			4	Output Buffer	pF



Table 9. GSC DC Electrical Characteristics (RF Section)

All specifications under conditions TOPR=25°C, VCC=2.85 V.

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Total Supply Current SPI Mode Sleep (SPI Off) Normal Power = (SPI On) Clock Only Mode (SPI On) Low Power Mode (SPI On)	I _{CC}	- - —	0.006 13 1 10.5	0.009 15	mA	Full Power Acq Clk and RTC only Full power functionality with noise figure increased to 9 dB.
SPI CMOS Input High Level	V _{Ih}	V _{CC_IO_EXT} * 0.8	-	-	V	
SPI CMOS Input Low Level	V _{Il}	-	-	V _{CC_IO_EXT} * 0.2	V	

AC CHARACTERISTICS

All measurements in Table 10. and Table 11. are characterized except as noted with (*) which are guaranteed by design.

Table 10. AC Characteristics for Write Access

Parameter List	Timing	Min.	Typ.	Max.	Unit
SCLK -> EA	T1		0		ns
SCLK -> $\overline{\text{CS}}$	T2		4.7		ns
SCLK -> $\overline{\text{MWE}}$	T3		0		ns
SCLK -> ED*	T5		0		ns
$\overline{\text{MWE}}$ Pulse Width*	T8	20			ns
SCLK -> $\overline{\text{MWE}}$	T10		0		ns
SCLK -> EA	T11		0		ns
SCLK -> $\overline{\text{CS}}$	T12		5.5		ns
SCLK -> ED*	T13		0		ns

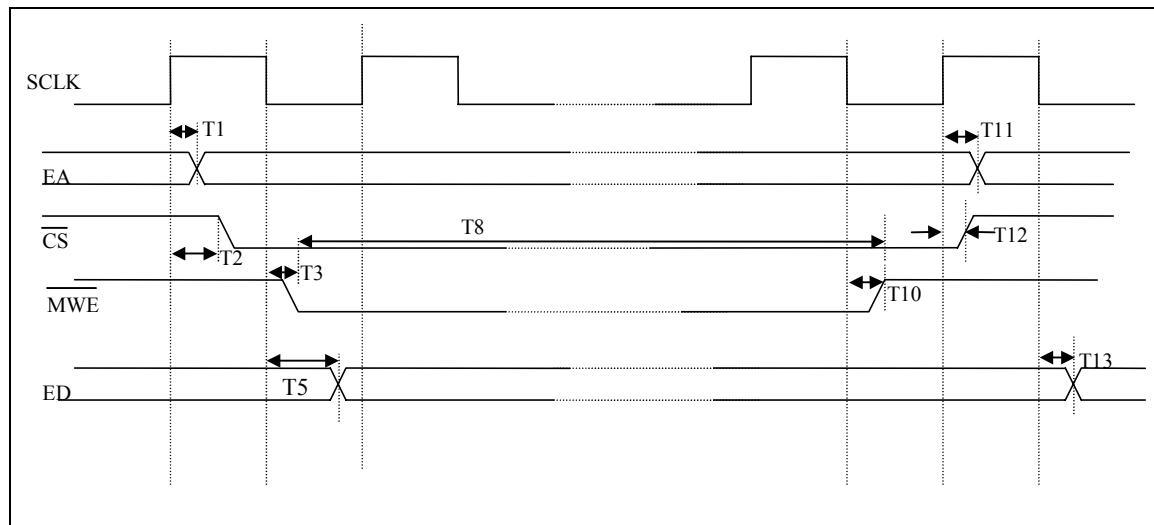


Figure 6. Write Access Timing Diagram

Table 11. AC Characteristics for Read Access

Parameter List	Timing	Min.	Typ.	Max.	Unit
SCLK -> EA	T1		0		ns
SCLK -> $\overline{\text{CS}}$	T2		4.2		ns
SCLK -> $\overline{\text{MOE}}$	T6		0		ns
SCLK -> $\overline{\text{MOE}}$	T7		0		ns
$\overline{\text{MOE}}$ Pulse Width*	T8	20			ns
SCLK -> EA	T11		0		ns
SCLK -> $\overline{\text{CS}}$	T12		5.0		ns
SCLK -> ED HOLD*	T13		10		ns
Cache Off for CSN[7:0] SCLK -> ED SET UP	T14	18.9			ns
Cache On for CSN[0] SCLK -> ED SET UP	T14	20 + $\frac{1}{2}$ CPU Clock Cycle			ns
Cache On for SCN[7:1] SCLK -> ED SET UP	T14		18.9		ns

Test Conditions: Vcc_core = 1.8 V; Vcc_IO = 3.0 V; Loading 60 pF (tester 36 pF, load board 24 pF); Temp. 25°C, 85°C, and -30°C.

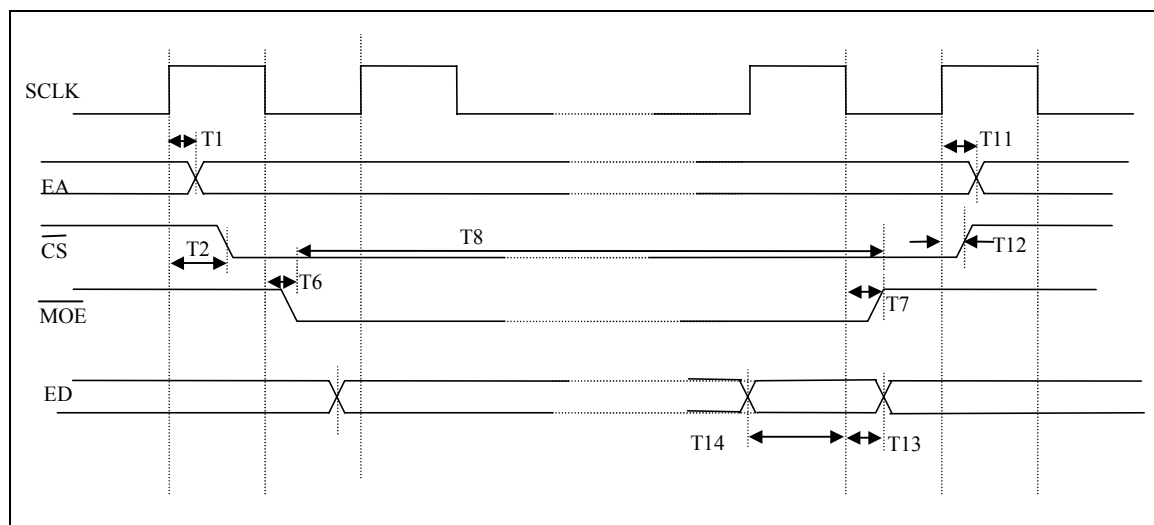


Figure 7. Read Access Timing Diagram

All measurements in Table 12. and Table 13. are guaranteed by design.

Table 12. SCLK Timing

Parameter	Symbol	Min.	Typ.	Max.	Units
Rise/Fall Time	T17		Rise 4.5 Fall 4.0		ns
Clock Pulse Width	T18		10		ns
Clock Period	T19		10		ns

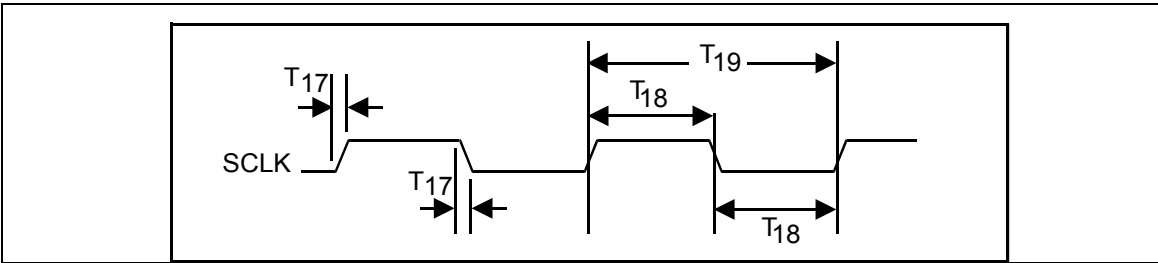


Figure 8. SCLK Timing Diagram

Table 13. Reset Timing

Parameter	Symbol	Min.	Typ.	Max.	Units
Reset Duration	T20		40		Clock Cycles

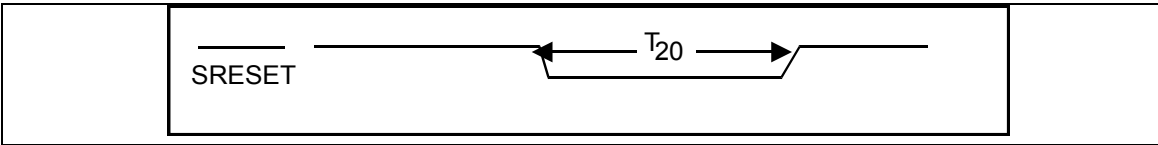


Figure 9. Reset Timing Diagram

Table 14. GSC3 Thermal Characteristics

Parameter	Symbol	Typical	Units	Conditions
Thermal Resistance Junction-to-Ambient	θ_{JA}	40	°C/W	
Power Supply Current Temperature Coefficient	$\frac{(\Delta I_{CC}/I_{CC})}{\Delta T}$	TBD	%/°C	

All specifications under conditions TOPR=25°C, VCC=2.85 V.

All RF measurements are made with appropriate matching to the input or output impedance.

Table 15. GSC RF Section AC Characteristics

AC Characteristic	Symbol	Min.	Typical	Max.	Units	Conditions
RFA/Mixer/AGC						
Noise Figure (AGC @ min. Gain)	NF	-	6.0	11	dB	
Input 1 dB Gain Compression (AGC @ min. Gain)	IP _{1db}	-	-65	-	dBm	
Input Return Loss w/ External Match	RL	-	11	-	dB	
Image Rejection Ratio (AGC @ min. Gain)		20	-	-	dB	
Synthesizer						
Spurious <100 kHz Δf >100 kHz Δf	Spur Near Spur Far	- -	- -	-20 -30	dBc	
LO SSB Phase Noise @ 1.0 kHz @ 10 kHz > 10 kHz		- - -	- - -	-80 -80 -70	dBc/Hz	
IF Filter/AGC-AMP						
Filter Attenuation at 12 MHz	F(12 MHz)	20	-	-	dB	
Filter Bandwidth	BW	-	7	-	MHz	3 dB bandwidth
Voltage Gain Resolution		-	1.7	-	dB	
Gain Adjust Range		45	51	-	dB	
Minimum Receiver Gain		-	50	-	dB	
Maximum Receiver Gain		-	100	-	dB	
Gain Linearity		-2.0	-	2.0	dB	
Frequency Synthesizer						
Operating Frequency			1571.424		MHz	
Type of Synthesizer		Integer-N				
Reference Frequency		13	-	33.6	MHz	7 discrete frequencies
Reference Input Level		200	-	1200	mVpp	

Table 15. GSC RF Section AC Characteristics (Continued)

AC Characteristic	Symbol	Min.	Typical	Max.	Units	Conditions
CMOS Driver						
Logic Level High	V_{oh}	$0.9 * V_{cc_IO_EX_T}$	-	-	V	
Logic Level Low	V_{ol}	-	-	$0.1 * V_{cc_IO_EX_T}$	V	
Rise Time @ 12 pF Load (10% to 90%)		-	4.0		ns	
Fall Time @ 12 pF Load (90% to 10%)		-	4.0		ns	
Static Sink Current and Source Current		$V_{CC} \div 5 \text{ k}\Omega$	-	-	mA	

Table 16. Operating Modes

Operating Modes	Comments
Normal Power	Entire chip enabled (normal operation).
Clock Only Mode	Acq Clock enabled and RTC only. PLL and receiver chain disabled.
Sleep	All circuits disabled.
Low Power Mode	Normal power functionality with noise figure increased to 9 dB.
Wake-Up Time (ms)	Wake-up from GPS Clock only of Sleep mode (<10 μ A current); wake-up with external reference clock <5 ms.

SAMPLE CIRCUIT FOR GSC3

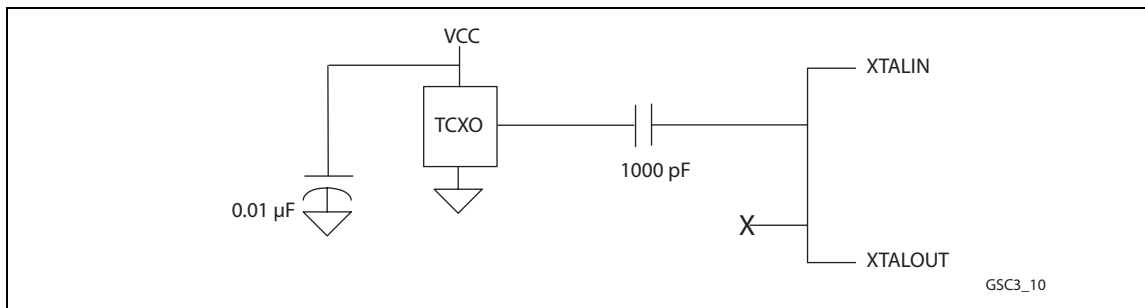


Figure 10. Typical Crystal Application Circuitry

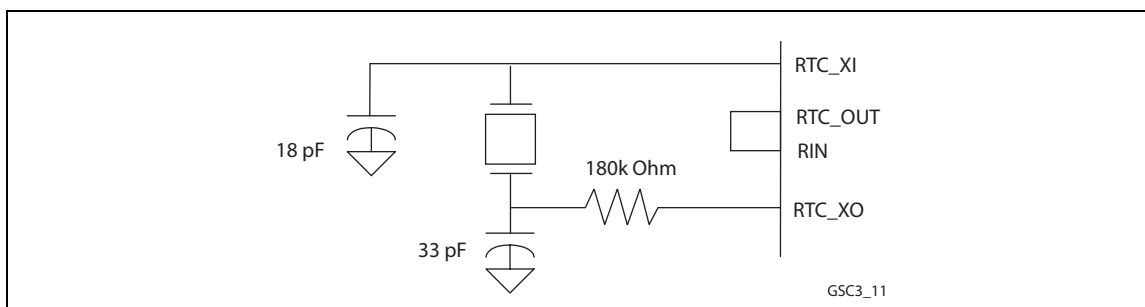


Figure 11. Typical RTC Circuitry

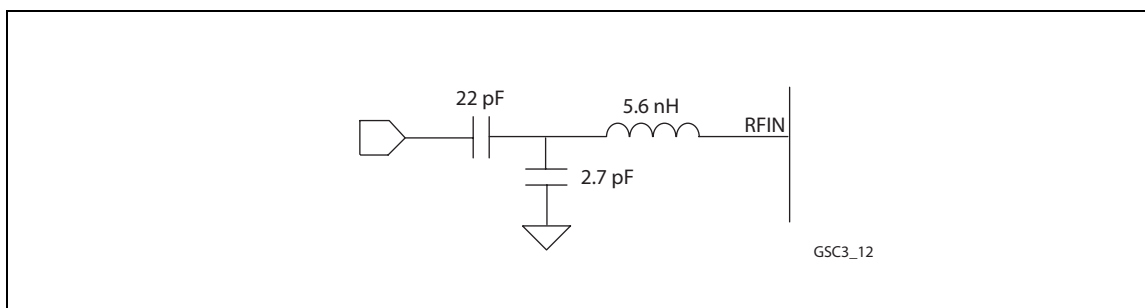


Figure 12. Typical RFIN Input Impedance Matching Circuitry (16.369 MHz)

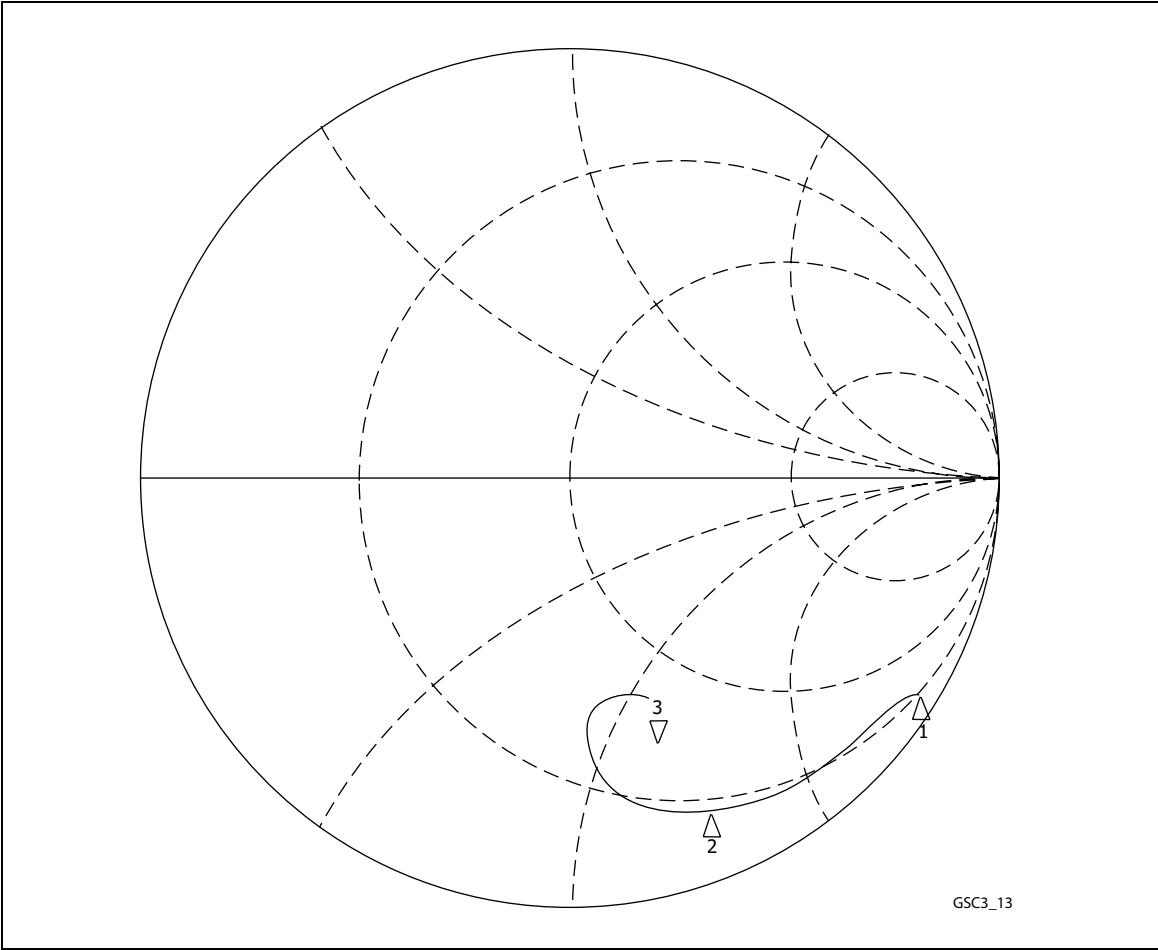


Figure 13. RFA Input Impedance Smith Chart for GSC3

Table 17. RFA Input Impedance Over Frequency (S11)

Test Conditions: RF Input = -60 dB, $Z_o = 50\Omega$, 2.85 V, 25°C, using matching circuitry of Figure 13.

Marker	1	2	3
Frequency	500 MHz	1,575 MHz	2,000 MHz
Impedance	$10.72 - j 171.81\Omega$	$12.25 + j 72.16\Omega$	$27.81 + j 59.24\Omega$

MECHANICAL SPECIFICATIONS

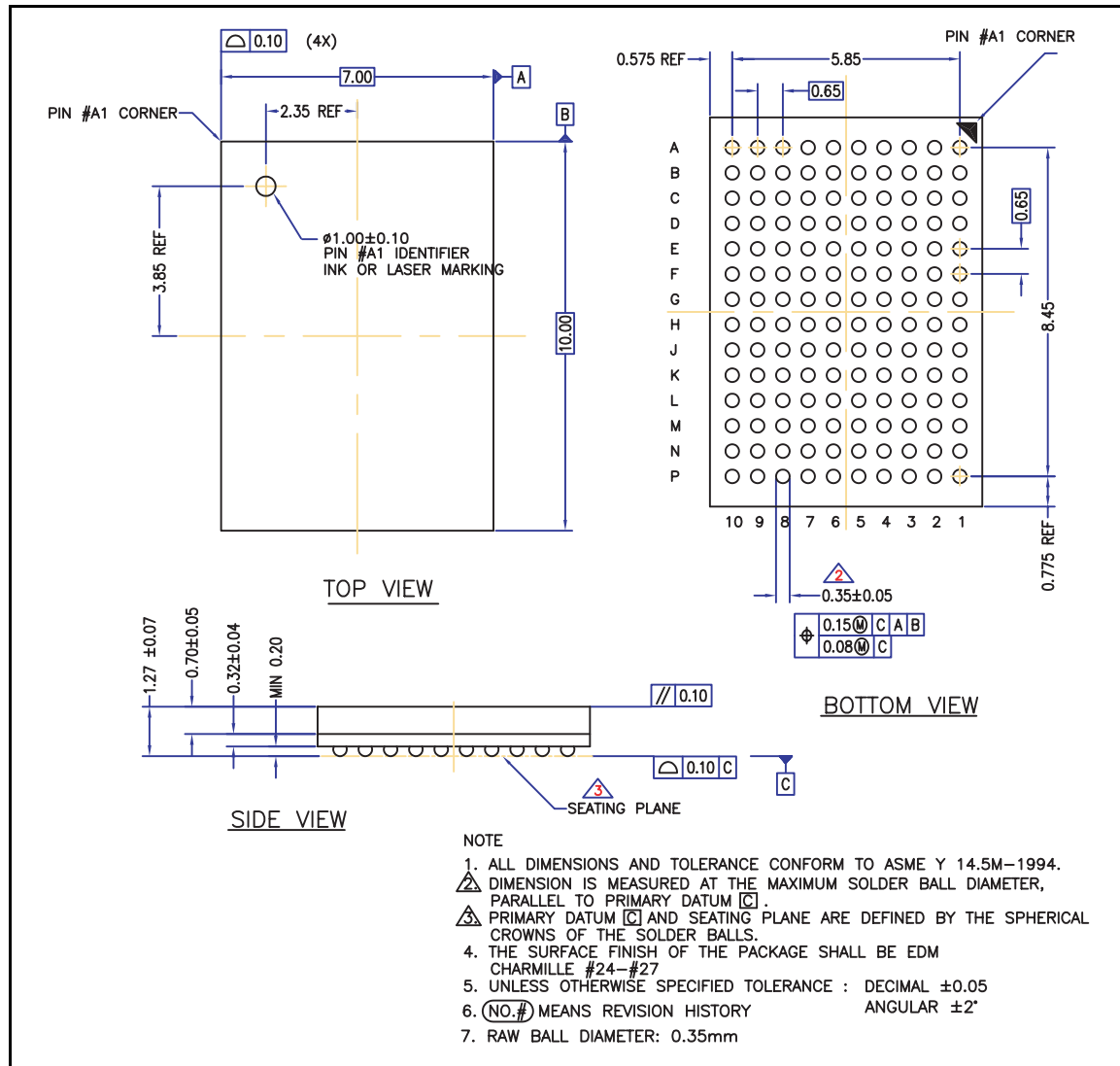


Figure 14. GSC3 140 PIN BGA Package

Note: The GSC3 is available in a lead-free package (-7875), which uses the same pinouts and maintains the same electrical specifications as the standard part (-7871).



ADDITIONAL INFORMATION

Item	Description
SiRF Application Notes	
APNT3001	SiRFstarIII System Design Guidelines and Considerations
APNT3002	PCB Design Guidelines for SiRFstarIII Implementations
APNT3003	Troubleshooting Notes for SiRFstarIII Board Development
APNT3004	Co-Location and Jamming Considerations for SiRFstarIII Integration
APNT3005	GPIO Pin Functionality for SiRFstarIII
APNT3006	I/O Message Definitions for SiRFstarIII
APNT3007	Implementing User Tasks in the SiRFstarIII Architecture
APNT3008	Advanced Power Management (APM) Considerations for SiRFstarIII
APNT3009	Production Testing of SiRFstarIII Modules

ORDERING INFORMATION

Part Number	Description
GSC3 Options	
GSC3-7871	GSC3, 16-bit, 140-pin, BGA
GSC3-7875	GSC3, 16-bit, 140-pin, BGA, Lead-Free
Development Tools	
9900-0224	SiRFstarIII Evaluation Kit
9900-0223	SiRFstarIII System Development Kit (SDK)



GSC3 Family
High Performance GPS Single Chip



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