Piccolo Competitive Analysis against STMicroelectronics STM32F101/2/3

C2000 Product Marketing

January 2009

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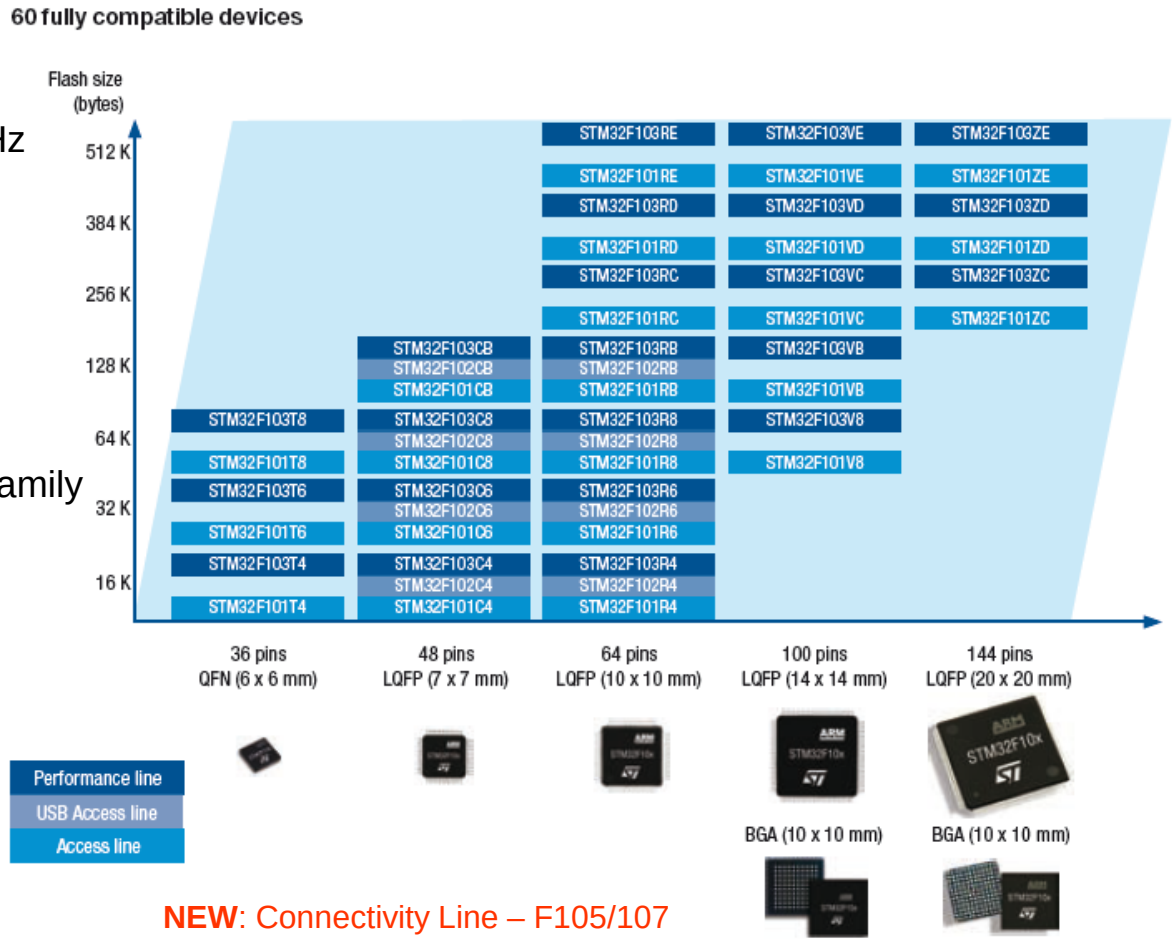
STM32 Product Overview

- Product Overview
  - ARM Cortex M3 Core:
    36-72MHz, 1.25 DMIPS/MHz
  - Real-time behavior
  - Low power
  - Innovative peripherals
  - Easy development,
    fast time to market
  - Maximum Integration
  - Compatibility across STM32 family
  - Multipurpose Module-based
    peripheral system
- Configurations
  - Access Line
  - USB Line
  - Performance Line
    - 2-3 onboard ADCs
    - Advanced Control Timers
    - USB
  - **Low**/Medium/High Density
    - Flash Size
    - Features/Communication



NEW: Connectivity Line – F105/107

-Performance Line with Ethernet

-More communication interfaces – up to 14

-Up to 256KB Flash, 64KB RAM

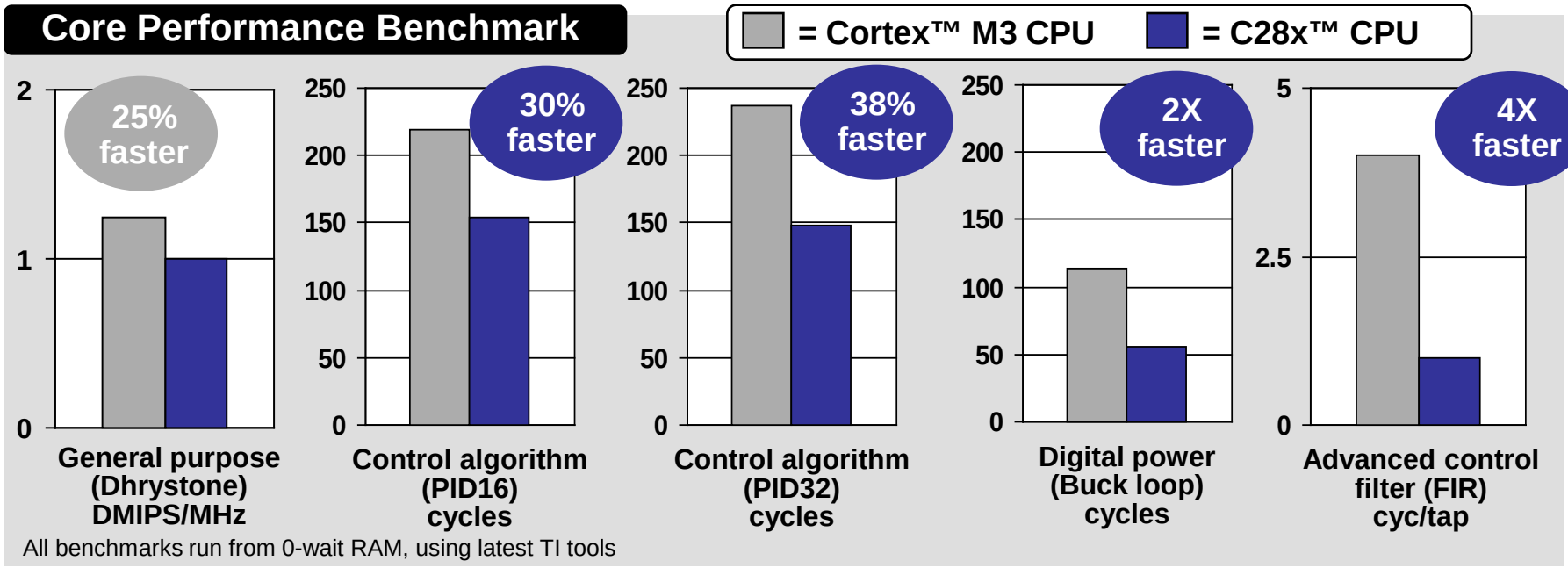
Competitive Overview

	Piccolo F2802x	Piccolo F2803x	STM F101/102x Low-Density Access	STM F103x Low-Density Performance
CPU Performance				
• CPU	40 – 60MHz*	60Mhz	36-48 MHz	72 MHz
• Features	None	CLA (Floating Point)	DMA	DMA
Memory & Peripherals				
• Flash / RAM	32-64kB / 6-12kB	64-128kB / 20kB	16-32kB / 4-6kB	16-32kB / 6-10kB
• PWMs	9 PWM / 4 HiRes	Up to 15 PWM / 7 HiRes	Up to 8	Up to 15
• QEP / Position Sensing	No	Yes	Yes – SW decode	Yes – SW decode
• ADC	12-bit, 7-13 ch (3 MSPS)	12-bit, 14-16 ch (4.6 MSPS)	12-bit, up to 16-ch (1 MSPS)	2x 12-bit, up to 16-ch (1 MSPS)
• Capture	1 (32-bit)	1 (32-bit)	Up to 8 (16-bit)	Up to 12 (16-bit)
• Timers	9 (four 32-bit)	Up to 12 (four 32-bit)	5 (No 32-bit)	6 (No 32-bit)
• Communication	SPI, I2C, UART	LIN, CAN, SPI, I2C, UART	USB, LIN, SPI, I2C, UART	USB, CAN, LIN, SPI, I2C, UART, SDIO
Integration				
• Supply Voltage	Single 3.3V	Single 3.3V	Single 3.3V	Single 3.3V
• I/O Pin Voltage Tolerance	3.3V	3.3V	5V	5V
• Comparator	Analog	Analog	Digital	Digital
• Oscillators	2x10MHz (+/- 3%)	2x10MHz (+/- 3%)	1x8MHz, 1x40kHz	1x8MHz, 1x40kHz
Other				
• Active Power Consumption	88mA – 105mA	?	17.3mA	29.2mA
• Minimum Power Consumption	100uA	?	3.4uA	3.4uA
• Packages	38 TSSOP, 48 LQFP	56 QFN, 64 TQFP, 80QFP, 80 LQFP	36 QFN, 48/64 LQFP	36 QFN, 48/64 LQFP
• Temp	-40^{0}C to 105/125^{0}C	-40C to 105/125C	-40^{0}C to 105^{0}C	-40^{0}C to 105^{0}C
• Pricing (per 10ku)	$1.79 - $2.85	$3.22 - $6.21	$1.68-$2.18	$2.20 - $2.90

Applications Comparison

Motor Control **Winner: Piccolo**	**F2802x** • 8 **dedicated enhanced PWM** channels. • C28 core **62% faster** than STM32 in 32-bit PID benchmarks, fast interrupts increases responsiveness. • Control Law Accelerator makes Piccolo B up to **5x faster** than Cortex-M3. • Dual Sample-and-hold allows **concurrent VI measurements** for accurate sensorless control. **STM32** • Up to 12 PWM outputs from 12 shared multipurpose channels. • Fast interrupts, sensorless loop control.
Digital Power Supplies **Winner: Piccolo**	**F2802x** • HiRes PWM allows much **higher resolution** (12.6-13.2 bits at 400kHz). • Powerful, optimized core, offers **stability and responsiveness.** • Hardware-based differential phase synchronization and feature-packed ADC allows **more customizability**. • HiRes frequency control very useful in increasingly popular **resonant power topologies.** **STM32** • Standard PWM (6.5-7.5 bits resolution at 400kHz) • Phase synchronization only at 0 degrees
Low Power Applications **Winner: STM32**	**F2802x** • 3 low power modes, minimum power consumption of ~100uA. **STM32** • Built in RTC, 3 low power modes, Minimum power consumption of ~3.4 uA.
Cost-sensitive Applications **Winner: ?**	**F2802x** • **On-chip integration:** voltage regulator, two 10MHz oscillators, Power-on reset / Brown-out reset, analog comparators. • **Fewer external components**: One VDD rail saves external caps, no external voltage supervisor needed. • With the integration, you can **save up to $1.75** more than STM32 in total system cost. **STM32** • On-chip regulator, one 8MHz oscillator, one 40kHz oscillator, digital comparators. • Lower pricing in some segments.
Reliability-dependent Applications **Winner: Piccolo**	**F2802x** • **3-tier** clock protection • Advanced trip-zone detection and handling and programmable deadband **prevent damage** to components. • Up to 125 degree temperature tolerance, sacrifices power consumption for **reliability.** • Built-in **digital filtering** on all input GPIOs **STM32** • 2-tier clock protection. • Deadband protection, emergency shutoff.

CPU Comparison



Dhrystone Benchmark:

- Generally Used To Measure GP Capability Of Processors
- Heavily Dominated By String Copy/Compare Operations
- Gives No Indication Of The "Math" Capability Of A Processor

PID16/PID32:

- Most Common Control Algorithm In Many Applications
- Benchmark Includes Some "if-then-else", Bit Operations, Multiply & Division Operations
- PID16 Exercises 16-bit "Math" Capabilities, PID32 Exercises 32-bit "Math" Capabilities
- A Good Indicator Of Processor Performance When Controlling Motors

Buck Loop:

- Most Common Control Algorithm In Digital Power (i.e DC-DC) Applications
- Includes Interrupt Response Of Processor And Uses 32-bit Math
- Every Cycle Counts, So Code Typically Written In Assembly

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Control Law Accelerator and System Performance

Operation	Cortex-M3 (72 MHz)	C28 (60MHz)	C28/CLA (60MHz)
Feedforward control cycles	786	482	482 / 0
Feedback control cycles	1762	1081	0 / 550
Total Control Law cycles	2548	1563	482 / 550
MHz used (20 kHz loop)	**~51MHz**	**~32MHz**	**~10/11MHz**

	20% faster, lower frequency,	5X faster, lower frequency
71% CPU utilization	53% CPU utilization	18% CPU utilization

- **Performance is not just the core. In applications like digital power, ADC & interrupt latencies need to be factored in.**

7

Benchmark	Optimization	Buck Loop (includes ADC & Interrupt latency)	
		Sample To Output Delay (affects stability)	Max Control Loop Frequency (x5 to x10 of sample to output delay)
Buck Loop	F2803x - MCLA	28 cycles	~214 to 428KHz @60MHz
	F2802x/3x - C28	41 cycles	~146 to 293KHz @60MHz
	STM32	120 cycles	~60 to 120KHz @72MHz

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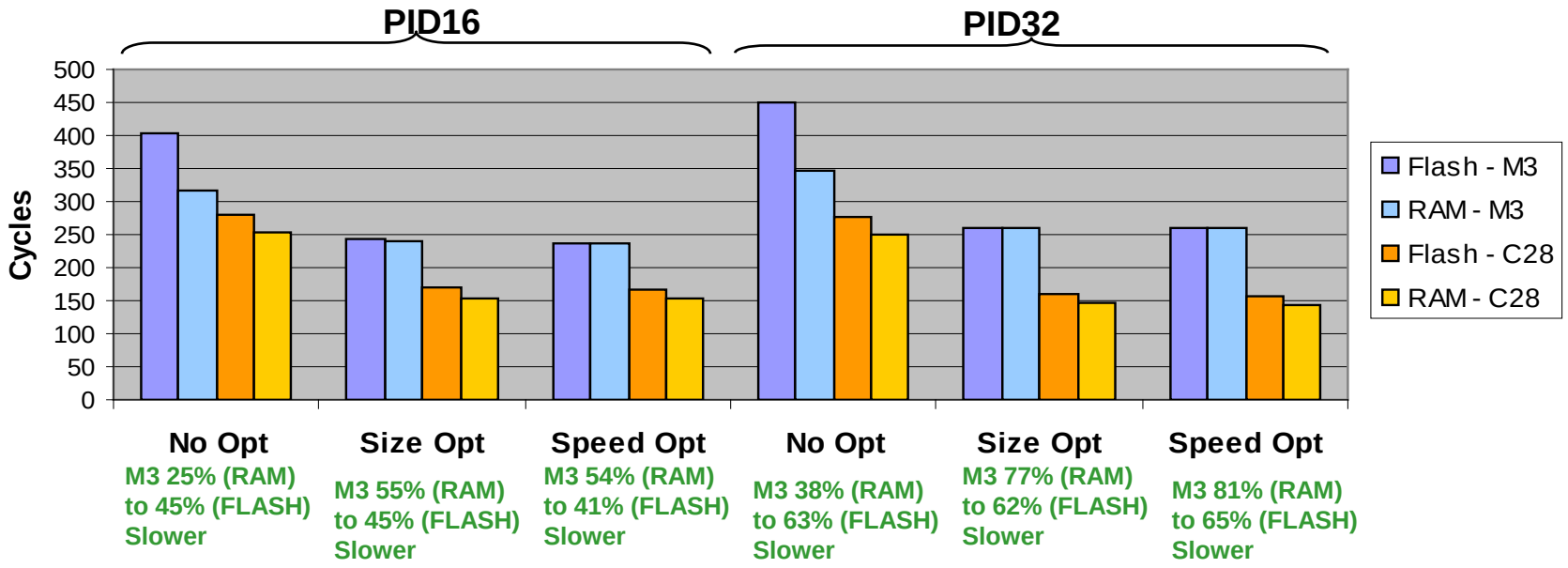
Flash and RAM Performance Comparison

Jeff Stafford Benchmarked PID16/32 Benchmarks On IAR Development System As Cross Check Also Wanted To Understand Impact Of FLASH Wait States On Performance Relative To RAM



- **On STM32 devices, running code from FLASH vs RAM produces varying results**
  (from ~10 to 25% variation @72MHz)
- **On F28x devices, FLASH vs RAM performance is consistent**
  (~9% difference @72MHz)

- **C28 core code efficiency similar to ARM-Thumb or Thumb2 mode**

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Active Mode Power Comparison

Parameter	F2802x @ 40 MHz	F2802x @ 60MHz	F101/102	F103*
Typical Run Mode Power Consumption - ***Peripherals On***	88mA	105mA	17.3mA	29.2mA
Typical Run Mode Power Consumption - ***Peripherals Off***	?	45mA	13.1mA	21.6mA

*F103 cannot run at speeds higher than 64MHz on internal high-speed oscillator. Amperage quoted is at 72MHz with external oscillator.

“Peripherals On” Footnotes

F2802x – Code running from Flash with 1 wait-state when running at 40MHZ and 2 wait-state at 60MHz, Vreg Enabled, internal clock, PWM pins toggled @40kHz, I/O pins unconnected, data transmitting out of SPI and SCI ports, COMP1/2 continuously switching, GPIO17 toggling, watchdog on, 25° C, 3.3V. The following peripheral clocks are enabled: ePWM1/2/3/4, eCAP1, SCI-A, SPI-A, ADC, I2C, COMP1/2, CPU-TIMER0/1/2

STM32 – Code running from Flash with 1 wait-state, internal regulator on, internal clock, “all peripherals enabled”, I/O pins unconnected with static value at V_{dd} or V_{ss}, 25° C, 3.3V.

“Peripherals Off” Footnotes

F2802x – Core is executing dummy code with no peripherals enabled

• STM also has a “Max Current Consumption @ 105C – 26mA for F101/101 and 46mA for F103

Peripheral Power Consumption

Piccolo A

Table 6-3. Typical Current Consumption by Various Peripherals (at 60 MHz)(1)

PERIPHERAL MODULE(2)	I_{DD} CURRENT REDUCTION (mA)
ADC	2(3)
I2C	3
ePWM	2
eCAP	2
SCI	2
SPI	2
COMP/DAC	1
HRPWM	3
CPU-TIMER	1
Internal zero-pin oscillator	0.5

(1) All peripheral clocks are disabled upon reset. Writing to/reading from peripheral registers is possible only after the peripheral clocks are turned on.
(2) For peripherals with multiple instances, the current quoted is per module. For example, the 2 mA value quoted for ePWM is for one ePWM module.
(3) This number represents the current drawn by the digital portion of the ADC module. Turning off the clock to the ADC module results in the elimination of the current drawn by the analog portion of the ADC (I_{DDA}) as well. ← **13 mA**

• Peripheral modules derived from automotive spec, contain many extra features

F101/2

Table 17. Peripheral current consumption

Peripheral		Typical consumption at 25 °C	Unit
APB1	TIM2	0.6	mA
	TIM3	0.6	
	USART2	0.21	
	I2C	0.18	
APB2	GPIO A	0.21	
	GPIO B	0.21	
	GPIO C	0.21	
	GPIO D	0.21	
	ADC(1)	1.4	
	SPI	0.24	
	USART1	0.35	

1. Specific conditions for ADC: f_{HCLK} = 28 MHz, $f_{APB1} = f_{HCLK}/2$, $f_{APB2} = f_{HCLK}$, $f_{ADCCLK} = f_{APB2}/2$, ADON bit in the ADC_CR2 register is set to 1.

On-chip peripheral current consumption

The current consumption of the on-chip peripherals is given in *Table 17*. The MCU is placed under the following conditions:

- all I/O pins are in input mode with a static value at V_{DD} or V_{SS} (no load)
- all peripherals are disabled unless otherwise mentioned
- the given value is calculated by measuring the current consumption
  - with all peripherals clocked off
  - with only one peripheral clocked on
- ambient operating temperature and V_{DD} supply voltage conditions summarized in *Table 5*.

• The same peripherals on the F103 consume about twice as much current.

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Low Power Modes

	Parameter	Condition	F2802x @ 40MHz	F2803x @ 60MHz	F101/102	F103
1	Idle	**F2802x – CPU on low-power mode. Flash off, XCLKOUT off, peripherals off, watchdog on.** STM32 - *does not have a comparable state*.	**14mA**	**20mA**	**-**	**-**
2	Standby (Sleep)	**F2802x – CPU off, peripherals off, oscillator on, PLL on, watchdog on** **STM32 - CPU off and peripherals on**	**4mA**	**5mA**	**2.5mA**	**4.2mA**
3	Halt (Stop)	**F2802x – CPU off, flash off, peripherals off, input clock disabled, oscillator off, WDCLK on.** **STM32 – CPU off, peripherals off, PLL off, oscillators off, watchdog off, regulator in run mode.**	**100uA**	**100uA**	**21.7uA**	**21.7uA**
4	Standby	F2802x – *does not have a comparable state* **STM32 - everything off except for watchdog and low-speed oscillator, register values lost except backup (need external battery)**	**-**	**-**	**3.4uA**	**3.4uA**
5	Wakeup from Idle (Sleep)	**F2802x - No solid experimental data** **STM32 – from High Speed Internal (HSI) RC clock**	**?**	**?**	**1.8 us**	**1.8 us**
6	Wakeup from Standby (Stop)	**F2802x - No solid experimental data** **STM32 - 3.6us when regulator in run mode, 5.4 when regulator is in low power mode**	**?**	**?**	**3.6 – 5.4us**	**3.6 – 5.4us**
7	Wakeup from Halt (Standby)	**F2802x - No solid experimental data**	**?**	**?**	**50us**	**50us**

- Do not be fooled by low standby mode power consumption - STM32 needs backup battery to achieve 3.4uA. See extra BoM.

Power

- **What Contributes To F28x Power:**
  - **TI 0.18u Flash Technology**
    - Designed For Reliability & Automotive Spec
    - Consumes ~100mW (one third of chip power)
    - We Can Use ROM or RAM In Cases Where This Is An Issue (turn Flash off)
  - **CPU Core**
    - Difficult To Compare Apples For Apples
    - Quality Of MIPS Is A Factor
    - M3 Measures Power Using Dhrystone Benchmark
    - F28x Measures Power Using PID Benchmark
    - MCLA On Piccolo-B Helps To Improve Power Efficiency By 3x to 4x
  - **Peripherals**
    - Biggest Contributor To Peripheral Power On F28x Devices Is ADC
    - ADC On F28x Is Designed For Performance (5 to 12 times faster then STM32)
    - Some Key Targeted Applications (Digital Power) Require High Performance

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PWM Comparison

	Parameter	Notes	F2802x @ 40 MHz	F2802x @ 60MHz	F101/102	F103
1	Step Size	F2802x - With HiRes PWM	150ps	150ps	14us	14us
2	Effective Bit Resolution	At 200kHz. Resolutions under ~12 bits is inadequate and can cause problems like “hunting”	13.7	14.9	7.5	8.5
		At 400kHz	12.6	13.2	6.5	7.5
3	High Resolution Waveform Control	Allows for precise control of the output	Duty cycle, frequency, and phase	Duty cycle, frequency, and phase	None	None
4	Control Loop	Control loop execution time based on Buck Loop benchmark. Includes ADC and interrupt latency.	10.3us	6.8us	33.3us	16.7us
5	Time Bases	Channels on same time base have same period	4	4	2	3
6	Channels	F103 - 3 additional complimentary outputs for inverters	8	8	8	12 (15)
7	QEP	Senses the position and direction of motor	No	No	Yes - SW	Yes - SW
8	Deadband protection	Prevents shorting when switching from high to low	Yes	Yes	No	Yes
9	Trip zone protection	F2802x has a much more flexible system, i.e. allows cycle-by-cycle or complete shut-off	Yes	Yes	Yes	Yes
10	Phase Synchronization	Differential phase sync saves CPU time and allows applications like full-bridge and zero voltage converters	Differential and same phase	Differential and same phase	Same phase only	Same phase
11	Power Inverter Support	Requires 6 total outputs, 3 of which need to be complimentary (synced)	Yes	Yes	Yes	Yes
12	High-Power Inverter Support	Piccolo has PWM chopping by high-frequency carrier signal, useful for high-end power inverters (pulse transformer gate drives)	Yes	Yes	No	No
13	Digital Power Supply	Higher resolution, faster control loops contribute to more stable output and smaller components	Yes	Yes	Yes	Yes

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Note: Control loop time calculated from benchmarks on slide 6

ADC Comparison

	Parameter	Notes	F2802x @ 40 MHz	F2802x @ 60MHz	F101/102	F103
1	Resolution		12 bits	12 bits	12 bits	12 bits
2	MSPS	MegaSamples per Second	3.07	4.6	1	1
3	Minimum Total Conversion Time	Conversion + Sample and Hold Piccolo @ clock spd, STM32 @ 14MHz	500ns	333ns	1.1us	1.1us
4	Gain Error (in LSB)	Ratio of the ideal conversion to actual conversion	10 *	10 *	3	2
5	Offset Error (in LSB)	Absolute deviation of actual conversion	10 *	10 *	2.5	2.5
6	DNL/INL Error (in LSB)	DNL - Variation in step size INL - Non-linearity of conversion line	1 / 2	1 / 2	2 / 3	2 / 3
9	Channels		7 / 13	13	10 / 16	16
	# of Sample-and-holds per ADC module	Dual sample-and-hold means we can measure VI without delay error.	2	2	1	1
10	Power-up time	Piccolo – due to internal reference	1ms *	1ms *	1us	1us
	Conversion Range		Fixed and ratio-metric	Fixed and ratio-metric	Ratio-metric	Ratio-metric
11	Interrupts	Early interrupt eliminates interrupt call latency	9 + Early Interrupt	9 + Early Interrupt	3	3
12	Channel Management	Piccolo: allows for more flexible channel linking	16 indep SOCs	16 indep SOCs	2 state sequencers	2 state sequencers
13	Out-of-range protection	Comparator	Comparator	Comparator	Dedicated watchdog	Dedicated watchdog

*** Parameters not fully characterized, this is just a hypothetical worst case number**

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Other Features

	F2802x	STM32
Captures **Winner: ?**	• 32-bit time base, registers up to 4 programmable events • Can be configured to generate an auxiliary PWM signal • Powerful for collecting Delta timing data from pulse train waveforms	•Each timer module has up to 4 captures
Timers **Winner: F2802x**	• 4 PWM timers (16-bit) • 1 eCAP timer (32-bit) • 3 CPU timers (32-bit) • 8-bit CPU-watchdog	• 2 General Purpose (16-bit) • 1 CPU clock (24-bit) • 2 watchdog timers (12-bit, 7-bit) • 1 Advanced Timer (16-bit, only on F103)
Oscillators **Winner: ?**	• 2 on-chip 10MHz oscillators with 3% error • External Clock Support • 3-tier clock protection	One 8MHz oscillator with 3% error • One 40KHz oscillator with 50% error • External Clock Support: HSE at 4-16 MHz, LSE 32.768 kHz • RTC support • 2-tier clock protection
General Reliability **Winner: F2802x**	• Built-in digital filtering on all input GPIOs and analog comparator • Numerous features to simplify IEC 60730 compliance • AEC-Q100 certified • Up to 125C tolerance • 3-tier clock protection + external oscillator support • Power-on / Brown-out protection	• Filtering on select pins • Up to 105C tolerance • IEC 60730 compliance possible • Power-on / Brown-out protection

"Winner: ?" means it depends on the application and what the customer views as important.

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Piccolo B vs STM32:

Feature	F28035PNT	STM32F103RB
Clock Speed	60 MHz	72 MHz
ROM	128KB Flash	128KB Flash
RAM	20KB RAM	20KB SRAM
ADC	12-bit, 16 ch, 4.6 MSPS	2x 12-bit, 16 ch, 1 MSPS
PWM	14 total, (7 HiRes)	Up to 16 total, 4(+3) Advanced
Captures	1	Up to 16
GPIOs	44	51
Communication	2x SPI, SCI, Lin, CAN, I2C	2x SPI, 3x USART, CAN, USB, 2x I2C
Timers	7 PWM, 3 CPU	3x General, 1x Advanced
Price (per 10ku)	$4.51 - $4.92	$3.49 per 10ku

- STM32F103RB
  - Closest match to our best Piccolo B
  - Part of Medium-Density Performance Line
  - All PWM/Capture/Compare share channels, each channel can only do one at a time.
- High-Density: STM32F103Zx
  - Up to 512KB Flash, 64KB SRAM
  - Timers: 4x GP, 2x Advanced, 2x CPU
  - Communication: 3x SPI, 5x USART, 2x I2C, USB, CAN, SDIO
  - GPIOs: 51-112
  - ADC: 3x 12-bit, 16-21 ch, 1 MSPS
  - External Memory Controller
  - Price: $6.51 per 10k

Debug

- Piccolo
  - 5-pin standard JTAG
  - In-silicon real-time debugging
  - Single-step non-time-critical code while time-critical interrupts continue to be serviced
  - Change variables while running
  - Watch registers, not only variables
  - Visit community.ti.com for help forums actively perused by engineers and tutorial videos
- STM32
  - 5-pin standard JTAG interface
  - 2-pin serial wire debug port
  - Standard ARM Cortex-M3 on-chip debug support
    - Embedded trace macrocell
  - MCU debug box
    - Support for low-power modes
    - Control over peripheral clocks

Tools and Development Overview

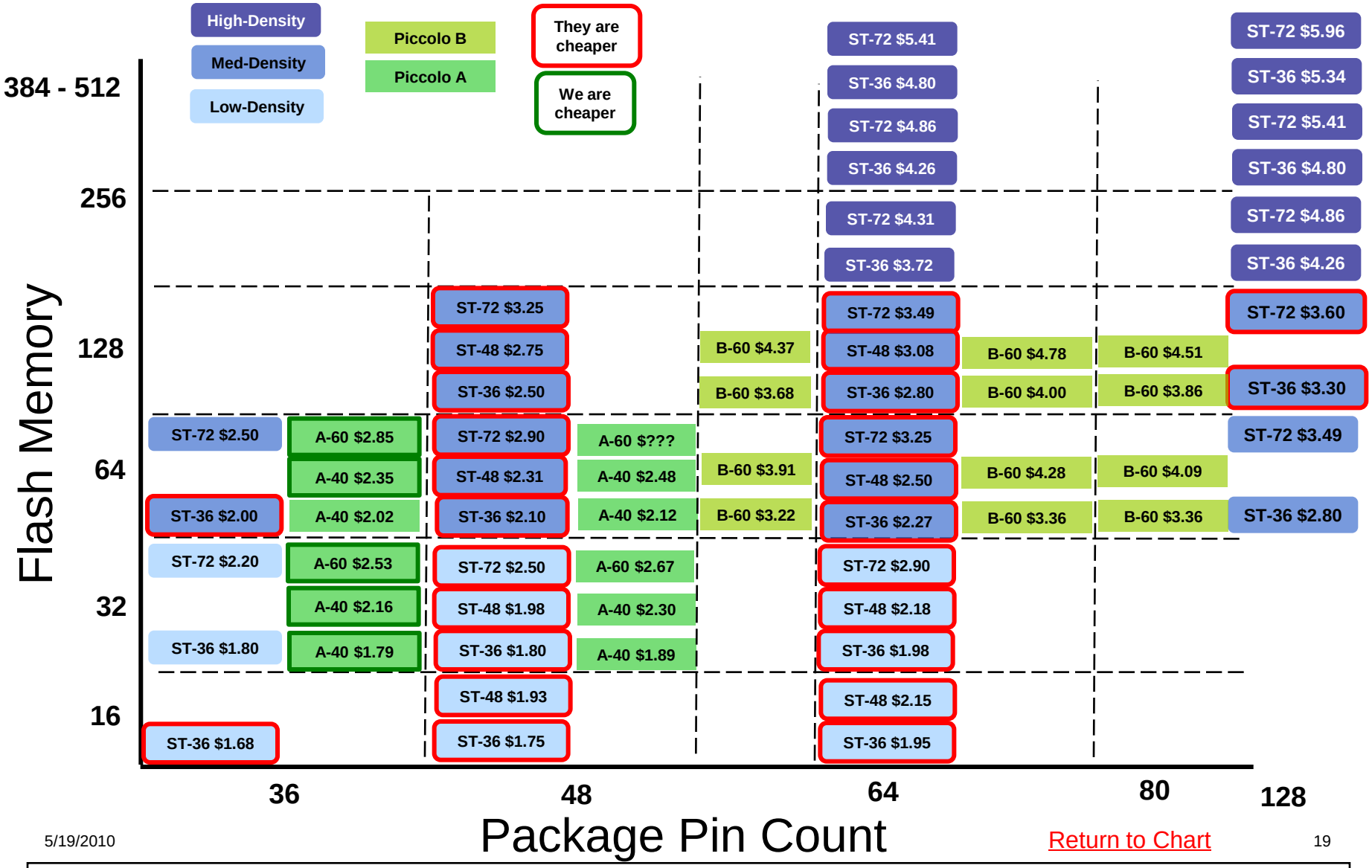
Piccolo Dev Tools and Boards

- USB controlSTICK - $39
  - Many useful example projects
- USB Experimenter's Kit - $129
  - Includes docking station and controlCARD
  - Docking station with onboard USB JTAG emulation is compatable with all C2000 controlCARDs.
- DMC board in development
- Future support for Digital Power Kits and AC/DC Developer's Kit
- Future compatibility with C2000 Software Libraries
  - Signal Processing
  - DSP/BIOS Real-Time IS
  - Digital Power
  - Motor Control
  - IQ Math: greatly simplifies code development

STM32 Dev Tools

- Many evaluation boards and starter kits
  - ST-made boards from $210
  - Third-party boards
- STM32 Primer - $36
- USB PerformanceStick - $63
- STM32 Motor Control Starter Kit
  - PMSM motor with sensorless vector control and debugger - $1080
  - LCD screen with GUI for real-time control
- Software Libraries
  - Standard Library
  - USB Developer Kit
  - DSP Software Library
  - Speech Codec Software Library
  - Code Examples
  - Motor Control Library

Pricing Comparison



Additional Bill of Materials for STM32

Does not include parts that both STM32 and Piccolo need like decoupling capacitors

Required

- Ten 100nF capacitors: ~$0.05
  - STM32 has up to 11 VDD rails vs one for Piccolo, each rail requires one 100nF cap

Optional

- One 4-16 MHz crystal, two 20 pF capacitors, one resistor (~390 ohms): ~$0.30
  - Required to use USB functionality
  - Required to achieve same level of clock protection Piccolo has
- External reference: >$0.20
  - To obtain a high-precision fixed scale ADC range, STM32 needs to purchase a precision external reference
- External analog comparator: >$0.20
  - Clock dependency or latency of digital comparator is not adequate for "protection" usage
  - User needs to add external comparators for current and temp protection
- Backup Battery : ~$1
  - To keep data when in Standby mode, the STM32 needs an external battery, includes battery mount (CR1220)

STM32 Strengths & Weaknesses

- Strengths
  - Very low power compared to Piccolo, many more power-saving features
  - Provides the necessary basics for almost all applications that Piccolo targets
  - High connectivity
  - Cortex M3 core widely used and supported
  - Wide range of options (50+ configurations)
  - Solid development tools portfolio and software libraries
  - Very competitive pricing with room to decrease
- Weaknesses
  - All PWM comes from multi-function timers, lacks functionality such as high resolution and chopping
  - Significantly less powerful ADC that requires external reference
  - Less powerful core, especially in digital power applications (2x-4x slower)
- USB function and full 72MHz speed can only be used with an external clock signal
- In many cases, superior core on Piccolo surpasses advantages given by DMA on the STM32
- One of their oscillators is a RTC, good for frequent sleep-mode applications, but can't be used as a system clock backup
- Because of limited applications in motor control and digital power, we have an advantage for clients who want to develop multiple products with similar MCU/code
- Touts many channels for peripherals, but they all share pins. Confusing mapping and remapping scheme

Possible attacks by STM32

- With the ARM core, you're using a widely used and extensively supported core. You're not locked into one manufacturer and you can easily port between hardware.
  - TI designed the C28 based on feedback from the field. You're getting a quality, optimized core that's better than Cortex M3 in many aspects. Also, check out https://community.ti.com/ for support from TI and our growing community.
  - The ARM message that a common core architecture makes development significantly easier is not entirely true. First of all, yes, every ARM-based chip shares a common core, but peripherals are JUST as important as the core and there can be a WIDE variety of configurations. Even with a common core, you still have to adjust your code/hardware to fit different manufacturers, even different configurations of the same line of processors.
- STM32 offers DMA for peripherals.
  - For real-time control, DMA is practically useless because you must process data immediately. For example, our ADC has a just-in-time interrupt system so that the CPU can start processing data the instant conversion data is read (no interrupt latency). To alleviate CPU load when necessary, Piccolo has a FIFO buffer on serial ports that provides a similar function to DMA but without the extra programming involved with DMA data management.
- STM32's ARM Cortex-M3 core is capable of more Dhrystone MIPS.
  - True, but Dhrystone gives no indication of math computing power. Even if our core is slower in some applications, its up to 5x faster in others like digital power supplies. You really have to look at specific applications.
- STM32 has up to 3 ADCs while Piccolo has only 1.
  - Piccolo has two sample-and-holds per ADC, allows for concurrent voltage and current measurement with a much lower variation error than 2 separate ADCs. Our ADCs are also 4x faster and much more flexible.
- STM32 devices have more channels for PWM/capture/compare.
  - These channels all stem from multi-purpose timers, 4 channels per time base means less flexibility. Cannot do, or even output, everything at once, confusing three-level remapping scheme.
- STM32 has much lower power consumption with RTC.
  - That's a true statement, and if low power is of the utmost importance, you should probably take a look at MSP430. But, **do not be fooled** by extremely low standby mode power consumption - STM32 needs backup battery to achieve 3.4uA and retain any data, meaning higher system cost. Our low power modes are also different - if you compare apples-to-apples low power modes, its not such an astronomical difference. Also, RTC is only good if your device spends the majority of time in sleep modes. MSP430 is also better than STM32 is this aspect.
- We can sell you STM32 for cheaper.
  - Piccolo offers a much better value proposition because of the feature-packed peripherals and optimized core. But even if you don't need any of those, Piccolo has a higher level of integration. Extra components needed to use STM32 take up more space and bring up their system cost.

Call to Action

- Got any compelling arguments by ST salespeople that I haven't covered?
  - Email me! I'll help you come up with a rebuttal.
- Have suggestions or additional information?
  - Let me know so we can make this presentation more useful
- Heard lowball price offerings from ST?
  - Please let us know so we know what to expect.

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References :

- STM32F101x Low-density Data Sheet
- STM32F103x Low-density Data Sheet
- STM32 Users Manual
- STM32 App Notes
- TMS320F28027 Data Sheet
- Piccolo Reference Guides
- Champs2008 C2000 Competition Presentation

Backup

Run Mode

Low-Density Performance Line

Table 16. Typical current consumption in Run mode, code with data processing running from Flash

Symbol	Parameter	Conditions	f_{HCLK}	Typ(1)		Unit
				All peripherals enabled(2)	All peripherals disabled	
I_{DD}	Supply current in Run mode	External clock(3)	72 MHz	31.3	24.5	mA
			48 MHz	21.9	17.4	
			36 MHz	17.2	13.8	
			24 MHz	11.2	8.9	
			16 MHz	8.1	6.6	
			8 MHz	5	4.2	
			4 MHz	3	2.6	
			2 MHz	2	1.8	
			1 MHz	1.5	1.4	
			500 kHz	1.2	1.2	
			125 kHz	1.05	1	
		Running on high speed internal RC (HSI), AHB prescaler used to reduce the frequency	64 MHz	27.6	21.6	mA
			48 MHz	21.2	16.7	
			36 MHz	16.5	13.1	
			24 MHz	10.5	8.2	
			16 MHz	7.4	5.9	
			8 MHz	4.3	3.6	
			4 MHz	2.4	2	
			2 MHz	1.5	1.3	
			1 MHz	1	0.9	
			500 kHz	0.7	0.65	
			125 kHz	0.5	0.45	

1. Typical values are measures at T_A = 25 °C, V_{DD} = 3.3 V.
2. Add an additional power consumption of 0.8 mA per ADC for the analog part. In applications, this consumption occurs only while the ADC is on (ADON bit is set in the ADC_CR2 register).
3. External clock is 8 MHz and PLL is on when f_{HCLK} > 8 MHz.

Low-Density Access Line

Table 15. Typical current consumption in Run mode, code with data processing running from Flash

Symbol	Parameter	Conditions	f_{HCLK}	Typ(1)	Typ(1)	Unit
				All peripherals enabled(2)	All peripherals disabled	
I_{DD}	Supply current in Run mode	External clock(3)	36 MHz	17.2	13.8	mA
			24 MHz	11.2	8.9	
			16 MHz	8.1	6.6	
			8 MHz	5	4.2	
			4 MHz	3	2.6	
			2 MHz	2	1.8	
			1 MHz	1.5	1.4	
			500 kHz	1.2	1.2	
			125 kHz	1.05	1	
		Running on high speed internal RC (HSI), AHB prescaler used to reduce the frequency	36 MHz	16.5	13.1	
			24 MHz	10.5	8.2	
			16 MHz	7.4	5.9	
			8 MHz	4.3	3.6	
			4 MHz	2.4	2	
			2 MHz	1.5	1.3	
			1 MHz	1	0.9	
			500 kHz	0.7	0.65	
			125 kHz	0.5	0.45	

1. Typical values are measures at T_A = 25 °C, V_{DD} = 3.3 V.
2. Add an additional power consumption of 0.8 mA per ADC for the analog part. In applications, this consumption occurs only while the ADC is on (ADON bit is set in the ADC_CR2 register).
3. External clock is 8 MHz and PLL is on when f_{HCLK} > 8 MHz.

Sleep Mode

Low-Density Performance Line

Table 17. Typical current consumption in Sleep mode, code with data processing code running from Flash or RAM

Symbol	Parameter	Conditions	f_{HCLK}	Typ(1)		Unit
				All peripherals enabled(2)	All peripherals disabled	
I_{DD}	Supply current in Sleep mode	External clock(3)	72 MHz	12.6	5.3	mA
			48 MHz	8.7	3.8	
			36 MHz	6.7	3.1	
			24 MHz	4.8	2.3	
			16 MHz	3.4	1.8	
			8 MHz	2	1.2	
			4 MHz	1.5	1.1	
			2 MHz	1.25	1	
			1 MHz	1.1	0.98	
			500 kHz	1.05	0.96	
			125 kHz	1	0.95	
		Running on high speed internal RC (HSI), AHB prescaler used to reduce the frequency	64 MHz	10.6	4.2	
			48 MHz	8.1	3.2	
			36 MHz	6.1	2.5	
			24 MHz	4.2	1.7	
			16 MHz	2.8	1.2	
			8 MHz	1.4	0.55	
			4 MHz	0.9	0.5	
			2 MHz	0.7	0.45	
			1 MHz	0.55	0.42	
			500 kHz	0.48	0.4	
			125 kHz	0.4	0.38	

1. Typical values are measures at $T_A = 25$ °C, $V_{DD} = 3.3$ V.
2. Add an additional power consumption of 0.8 mA per ADC for the analog part. In applications, this consumption occurs only while the ADC is on (ADON bit is set in the ADC_CR2 register).
3. External clock is 8 MHz and PLL is on when $f_{HCLK} > 8$ MHz.

Low-Density Access Line

Table 16. Typical current consumption in Sleep mode, code with data processing code running from Flash or RAM

Symbol	Parameter	Conditions	f_{HCLK}	Typ(1)	Typ(1)	Unit
				All peripherals enabled(2)	All peripherals disabled	
I_{DD}	Supply current in Sleep mode	External clock(3)	36 MHz	6.7	3.1	mA
			24 MHz	4.8	2.3	
			16 MHz	3.4	1.8	
			8 MHz	2	1.2	
			4 MHz	1.5	1.1	
			2 MHz	1.25	1	
			1 MHz	1.1	0.98	
			500 kHz	1.05	0.96	
			125 kHz	1	0.95	
		Running on High Speed Internal RC (HSI), AHB prescaler used to reduce the frequency	36 MHz	6.1	2.5	
			24 MHz	4.2	1.7	
			16 MHz	2.8	1.2	
			8 MHz	1.4	0.55	
			4 MHz	0.9	0.5	
			2 MHz	0.7	0.45	
			1 MHz	0.55	0.42	
			500 kHz	0.48	0.4	
			125 kHz	0.4	0.38	

1. Typical values are measures at $T_A = 25$ °C, $V_{DD} = 3.3$ V.
2. Add an additional power consumption of 0.8 mA per ADC for the analog part. In applications, this consumption occurs only while the ADC is on (ADON bit is set in the ADC_CR2 register).
3. External clock is 8 MHz and PLL is on when $f_{HCLK} > 8$ MHz.

Sleep Mode

Low-Density Access Line

Table 14. Typical and maximum current consumptions in Stop and Standby modes

Symbol	Parameter	Conditions	Typ(1)		Max	Unit
			V_{DD}/V_{BAT} = 2.4 V	V_{DD}/V_{BAT} = 3.3 V	T_A = 85 °C(2)	
I_{DD}	Supply current in Stop mode	Regulator in Run mode, Low-speed and high-speed internal RC oscillators and high-speed oscillator OFF (no independent watchdog)	21.3	21.7	160	µA
		Regulator in Low Power mode, Low-speed and high-speed internal RC oscillators and high-speed oscillator OFF (no independent watchdog)	11.3	11.7	145	
	Supply current in Standby mode	Low-speed internal RC oscillator and independent watchdog ON	2.6	3.4	-	
		Low-speed internal RC oscillator ON, independent watchdog OFF	2.4	3.2	-	
		Low-speed internal RC oscillator and independent watchdog OFF, low-speed oscillator and RTC OFF	1.7	2	3.2	
I_{DD_VBAT}	Backup domain supply current	Low-speed oscillator and RTC ON	1.1	1.4	1.9	

1. Typical values are measured at T_A = 25 °C.
2. Based on characterization, not rested in production.

Low-Density Performance Line

Table 15. Typical and maximum current consumptions in Stop and Standby modes

Symbol	Parameter	Conditions	Typ(1)		Max		Unit
			V_{DD}/V_{BAT} = 2.4 V	V_{DD}/V_{BAT} = 3.3 V	T_A = 85 °C	T_A = 105 °C	
I_{DD}	Supply current in Stop mode	Regulator in Run mode, low-speed and high-speed internal RC oscillators and high-speed oscillator OFF (no independent watchdog)	21.3	21.7	160	200	µA
		Regulator in Low-Power mode, low-speed and high-speed internal RC oscillators and high-speed oscillator OFF (no independent watchdog)	11.3	11.7	145	185	
	Supply current in Standby mode	Low-speed internal RC oscillator and independent watchdog ON	2.75	3.4	-	-	
		Low-speed internal RC oscillator ON, independent watchdog OFF	2.55	3.2	-	-	
		Low-speed internal RC oscillator and independent watchdog OFF, low-speed oscillator and RTC OFF	1.55	1.9	3.2	4.5	
I_{DD_VBAT}	Backup domain supply current	Low-speed oscillator and RTC ON	1.1	1.4	1.9(2)	2.2	

1. Typical values are measured at T_A = 25 °C.
2. Based on characterization, not tested in production.

Wakeup timings

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Table 24. Low-power mode wakeup timings

Symbol	Parameter	Conditions	Typ	Unit
$t_{WUSLEEP}$(1)	Wakeup from Sleep mode	Wakeup on HSI RC clock	1.8	µs
t_{WUSTOP}(1)	Wakeup from Stop mode (regulator in run mode)	HSI RC wakeup time = 2 µs	3.6	µs
	Wakeup from Stop mode (regulator in low-power mode)	HSI RC wakeup time = 2 µs, Regulator wakeup from LP mode time = 5 µs	5.4	
$t_{WUSTDBY}$(1)	Wakeup from Standby mode	HSI RC wakeup time = 2 µs, Regulator wakeup from power down time = 38 µs	50	µs

1. The wakeup times are measured from the wakeup event to the point at which the user application code reads the first instruction.

Table 6-15. IDLE Mode Switching Characteristics(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{d(WAKE-IDLE)}$	Delay time, external wake signal to program execution resume (2)					
	• Wake-up from Flash – Flash module in active state	Without input qualifier			$20t_{c(SCO)}$	cycles
		With input qualifier			$20t_{c(SCO)} + t_{w(IQSW)}$	
	• Wake-up from Flash – Flash module in sleep state	Without input qualifier			$1050t_{c(SCO)}$	cycles
		With input qualifier			$1050t_{c(SCO)} + t_{w(IQSW)}$	
	• Wake-up from SARAM	Without input qualifier			$20t_{c(SCO)}$	cycles
		With input qualifier			$20t_{c(SCO)} + t_{w(IQSW)}$	

(1) For an explanation of the input qualifier parameters, see Table 6-13.
(2) This is the time taken to begin execution of the instruction that immediately follows the IDLE instruction. execution of an ISR (triggered by the wake up) signal involves additional latency.

Where (25ns < $t_{c(SCO)}$ < 500ns)