GPS

locate, communicate, accelerate

LEA-5, NEO-5, TIM-5H

u-blox 5 GPS Modules

Hardware Integration Manual

Abstract

This document describes the hardware features and specifications of the cost effective and high-performance LEA-5, NEO-5 and TIM-5H GPS modules featuring the u-blox 5 positioning engine.

These compact, easy to integrate stand-alone GPS receiver modules combine exceptional GPS performance with highly flexible power, design, and connectivity options. Their compact form factors and SMT pads allow fully automated assembly with standard pick & place and reflow soldering equipment for cost-efficient, high-volume production enabling short time-to-market.

Document Information	
Title	LEA-5, NEO-5, TIM-5H
Subtitle	u-blox 5 GPS Modules
Document type	Hardware Integration Manual
Document number	GPS.G5-MS5-09027-A2
Document status	Released This document contains the final product specification.

This document applies to the following products:

Name	Type number	ROM/FLASH version	PCN reference
LEA-5H	LEA-5H-0-009	FW6.02	UBX-TN-09017
	LEA-5H-0-008	FW6.00	UBX-TN-09001-A
	LEA-5H-0-007	FW5.00	UBX-TN-08027
LEA-5S	LEA-5S-0-004	ROM5.00	UBX-TN-08023
LEA-5A	LEA-5A-0-003	ROM5.00	UBX-TN-08023
LEA-5Q	LEA-5Q-0-002	ROM5.00	UBX-TN-08023
LEA-5M	LEA-5M-0-002	ROM5.00	UBX-TN-08023
LEA-5T	LEA-5T-0-003	FW6.02	UBX-TN-09017
	LEA-5T-0-002	FW6.00	UBX-TN-09001-A
	LEA-5T-0-001	FW5.00	UBX-TN-08027
NEO-5Q	NEO-5Q-0-002	ROM5.00	N/A
NEO-5M	NEO-5M-0-001	ROM5.00	N/A
NEO-5G	NEO-5G-0-000	ROM5.00	N/A
NEO-5D	NEO-5D-0-001	ROM5.00	N/A
TIM-5H	TIM-5H-0-004	FW6.02	UBX-TN-09017
	TIM-5H-0-003	FW6.00	UBX-TN-09001-A

Preface

u-blox Technical Documentation

As part of our commitment to customer support, u-blox maintains an extensive volume of technical documentation for our products. In addition to our product-specific technical data sheets, the following manuals are available to assist u-blox customers in product design and development.

- **GPS Compendium:** This document, also known as the GPS book, provides a wealth of information regarding generic questions about GPS system functionalities and technology.
- **Receiver Description including Protocol Specification:** Messages, configuration and functionalities of the u-blox 5 software releases and receivers are explained in this document.
- **Hardware Integration Manual:** This Manual provides hardware design instructions and information on how to set up production and final product tests.
- **Application Note:** document provides general design instructions and information that applies to all u-blox GPS receivers. See Section Related documents for a list of Application Notes related to your GPS receiver.

How to use this Manual

The LEA-5, NEO-5, TIM-5H Hardware Integration Manual provides the necessary information to successfully design in and configure these u-blox 5-based GPS/GALILEO receiver modules. For navigating this document please note the following:

This manual has a modular structure. It is not necessary to read it from the beginning to the end. To help in finding needed information, a brief section overview is provided below:

1. **Hardware description**: This chapter introduces the basics of function and architecture of the u-blox 5 modules.
2. **Design-in**: This chapter provides the Design-In information necessary for a successful design.
3. **Handling and soldering**: This chapter defines packaging, handling, shipment, storage and soldering.
4. **Product testing**: This chapter provides information about testing of OEM receivers in production.
5. **Appendix**: The Appendix includes guidelines on how to successfully migrate to u-blox 5 designs, and useful information about the different antenna types available on the market and how to reduce interference in your GPS design.

This manual has a modular structure. It is not necessary to read it from the beginning to the end.

The following symbols are used to highlight important information within the manual:

☞ An index finger points out key information pertaining to module integration and performance.

⚠ **A warning symbol indicates actions that could negatively impact or damage the module.**

Questions

If you have any questions about u-blox 5 Hardware Integration, please:

- Read this manual carefully.
- Contact our information service on the homepage http://www.u-blox.com
- Read the questions and answers on our FAQ database on the homepage http://www.u-blox.com

Technical Support

Worldwide Web

Our website (www.u-blox.com) is a rich pool of information. Product information, technical documents and helpful FAQ can be accessed 24h a day.

By E-mail

If you have technical problems or cannot find the required information in the provided documents, contact the nearest of the Technical Support offices by email. Use our service pool email addresses rather than any personal email address of our staff. This makes sure that your request is processed as soon as possible. You will find the contact details at the end of the document.

Helpful Information when Contacting Technical Support

When contacting Technical Support please have the following information ready:

- Receiver type (e.g. LEA-5A) and firmware version (e.g. V6.00)
- Receiver configuration
- Clear description of your question or the problem together with a u-center logfile
- A short description of the application
- Your complete contact details

Contents

1 Hardware description

1.1 Overview

The LEA-5, NEO-5 and TIM-5H modules are a family of standalone GPS receivers featuring the high performance u-blox 5 positioning engine. These compact, easy to integrate modules combine exceptional GPS performance with highly flexible power, design, and connectivity options. Their compact form factors and SMT pads allow fully automated assembly with standard pick & place and reflow-soldering equipment for cost-efficient, high-volume production enabling short time-to-market.

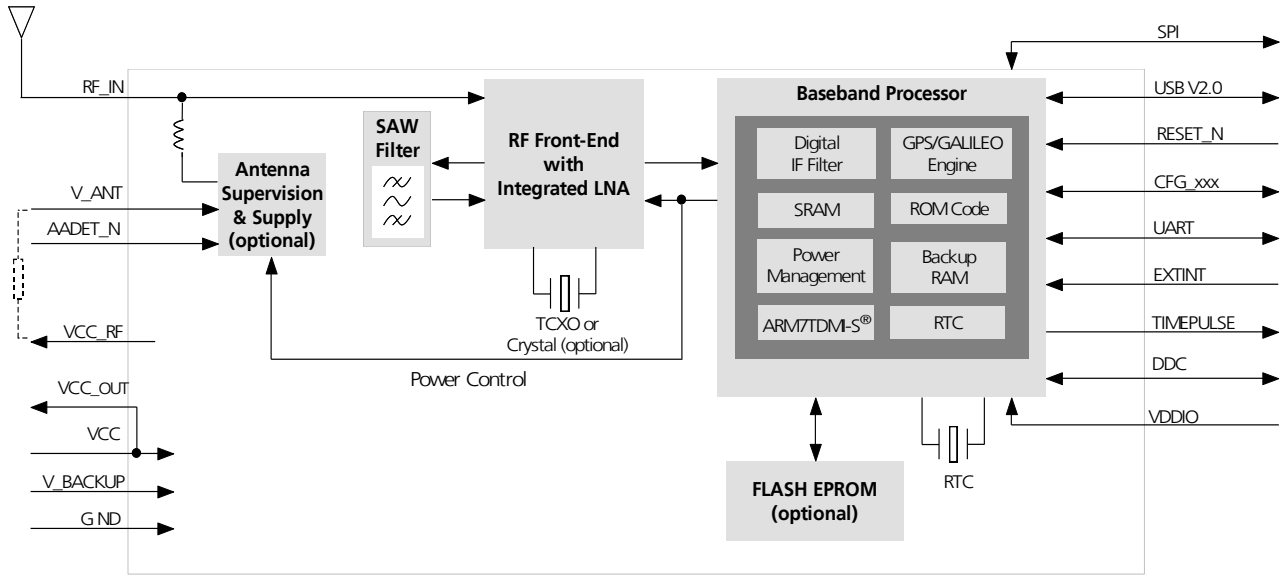
u-blox GPS modules are not designed for life saving or supporting devices or for aviation and should not be used in products that could in any way negatively impact the security or health of the user or third parties or that could cause damage to goods.

1.2 Architecture

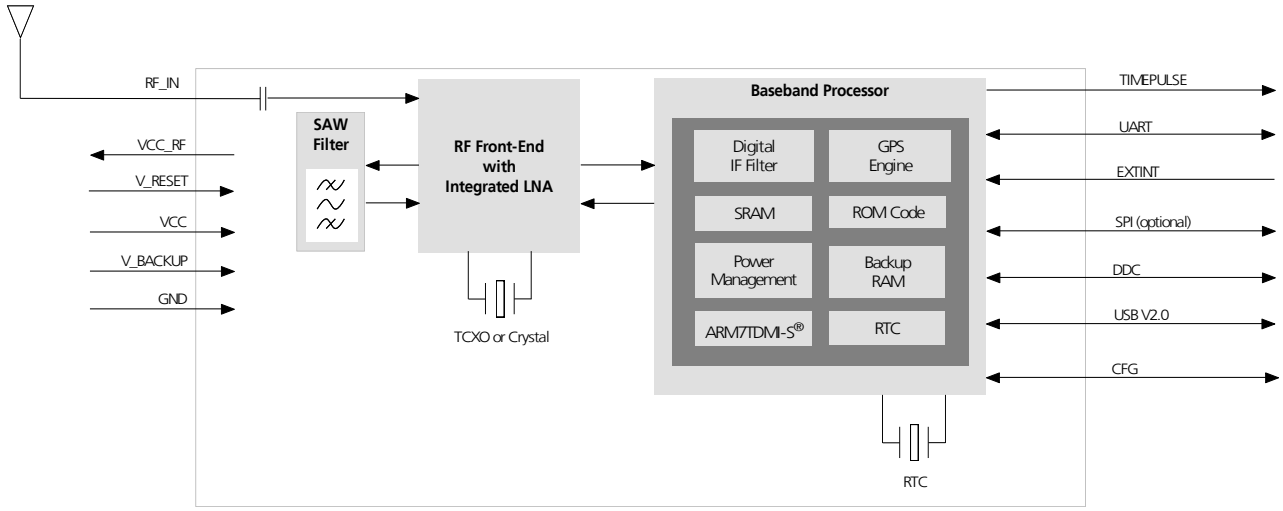
LEA-5, NEO-5 and TIM-5H modules consist of two functional parts - –he RF and the Baseband sections. See Figure 1 for a block diagram of the modules.

The RF Front-End includes the input matching elements, the integrated Low Noise Amplifier (LNA), the SAW bandpass filter, the u-blox 5 RF-IC and the Crystal.

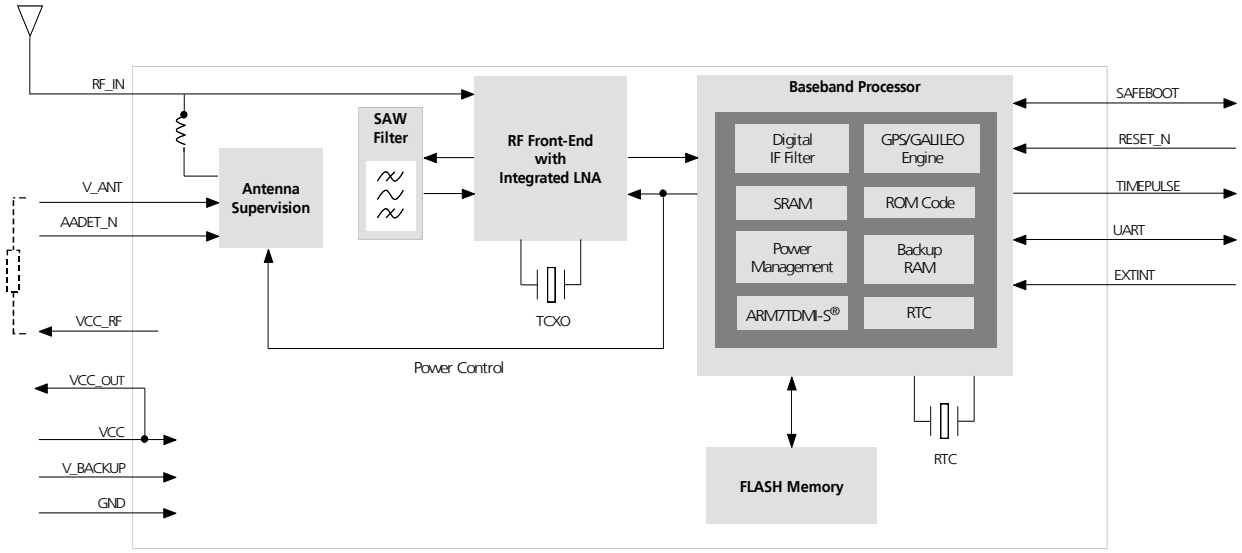
The Baseband section contains the u-blox 5 Baseband processor, the RTC crystal and additional elements such as the optional FLASH Memory for enhanced programmability and flexibility.



LEA-5 Block Diagram



NEO-5 Block Diagram



TIM-5H Block Diagram

Figure 1: Block diagrams of LEA-5, NEO-5 and TIM-5H modules

1.3 Power management

1.3.1 Connecting power

u-blox 5 receiver modules have up to three power supply pins: **VCC**, **V_BCKP** and **VDDUSB**[1].

1.3.1.1 VCC - –ain power

The main power supply is fed through the **VCC** pin. During operation, the current drawn by the u-blox 5 GPS module can vary by some orders of magnitude, especially, if low-power operation modes are enabled. It is important that the system power supply circuitry is able to support the peak power (see datasheet for

[1] Not available with TIM-5H

specification) for a short time. In order to define a battery capacity for specific applications the sustained power figure shall be used.

☞ When switching from backup mode to normal operation u-blox 5 modules must charge the internal capacitors in the core domain. This can result in certain situations result in a significant current draw. For low power applications using Power Save and backup modes it is important that the power supply or low ESR capacitors at the module input can deliver this current/charge.

1.3.1.2 V_BCKP - –ackup battery

In case of a power failure on pin **VCC**, the real-time clock and backup RAM are supplied through pin **V_BCKP**. This enables the u-blox 5 receiver to recover from a power failure with either a Hotstart or a Warmstart (depending on the duration of **VCC** outage) and to maintain the configuration settings. If no backup battery is connected, the receiver performs a Coldstart at power up.

☞ If no backup battery available connect the V_BCKP pin to GND (or VCC).

As long as **VCC** is supplied to the u-blox 5 receiver, the backup battery is disconnected from the RTC and the backup RAM in order to avoid unnecessary battery drain (see Figure 2). Power to RTC and BBR is supplied from **VCC** in this case.

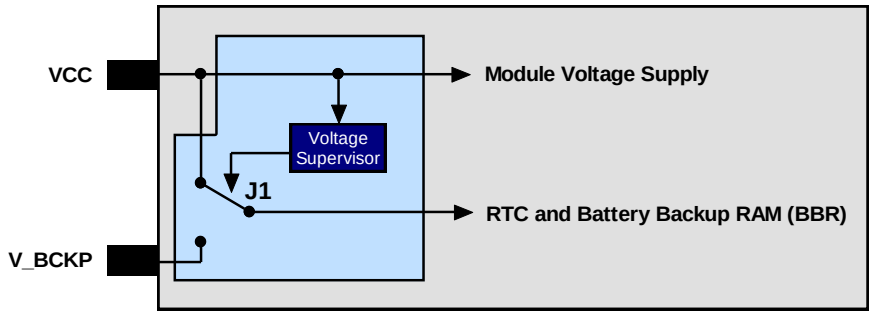


Figure 2: Backup Battery and Voltage

1.3.1.3 VDD_USB - –SB interface power supply (LEA-5, NEO-5)

VDD_USB supplies the I/Os of the USB interface. If the USB interface is not used, the **VDD_USB** pin must be connected to GND. For more information regarding the correct handling of **VDD_USB** see section 1.5.2.1

1.3.2 Operating modes

u-blox 5 modules with FW 6.00 have 2 continuous operating modes (Maximum Performance and Eco) and 1 intermittent operating mode (Power Save mode). Maximum Performance mode freely uses the acquisition engine, resulting in the best possible TTFF, while Eco mode optimizes the use of the acquisition engine to deliver lower current consumption. At medium to strong signals, there is almost no difference for acquisition and tracking performance in these modes.

1.3.2.1 Maximum Performance mode

In Maximum Performance mode, u-blox 5 receivers use the acquisition engine at full performance to search for all possible satellites until the Almanac is completely downloaded.

As a consequence, tracking current consumption level will be achieved when:

- A valid GPS position is fixed
- Almanac is entirely downloaded
- Ephemeris for all satellites in view are valid

1.3.2.2 Eco mode

In Eco mode, u-blox 5 receivers use the acquisition engine to search for new satellites ***only when needed*** for navigation:

- In cold starts, u-blox 5 searches for enough satellites to navigate and optimizes use of the acquisition engine to download their ephemeris.
- In non-cold starts, u-blox 5 focuses on searching for visible satellites whose orbits are known from the Almanac.

In Eco mode, the u-blox 5 acquisition engine limits use of its searching resources to minimize power consumption. As a consequence the time to find some satellites at weakest signal level might be slightly increased in comparison to the Maximum Performance mode.

u-blox 5 deactivates the acquisition engine as soon as a position is fixed and a sufficient number (at least 4) of satellites are being tracked. The tracking engine continues to search and track new satellites without orbit information.

1.3.2.3 Power Save mode (new with FW 6.00)

u-blox 5 modules include power saving options that allow reducing the average tracking current consumption by periodically switching off parts of or the complete GPS receiver and waking it up at configurable intervals from one second to one week. This can be done by using a hardware interrupt or by sending a serial command. The firmware also offers the option to reduce the peak and acquisition current independently of the power down option.

1.3.3 V_ANT (LEA-5H/5S/5A, TIM-5H)

TIM-5H and LEA-5 modules supporting active antenna supply and supervision use the pin **V_ANT** to supply the active antenna. Use a 10R resistor in front of **V_ANT**[2]. See chapter 2.6.

1.4 System functions

1.4.1 EXTINT - –xternal interrupt pin

EXTINT0 is an external interrupt pin used for the time mark function on LEA-5T. With FW 6.0, it can be used for wake-up functions in low-power modes.

1.4.2 System monitoring

The u-blox 5 receiver modules provide system monitoring functions that allow the operation of the embedded processor and associated peripherals to be supervised. These System Monitoring functions are output as part of the UBX protocol, class 'MON'.

Please refer to the u-blox 5 Receiver Description including Protocol Specification [2]. For more information on UBX messages, serial interfaces for design analysis and individual system monitoring functions.

1.5 Interfaces

1.5.1 UART

u-blox 5 modules include up to 2 Universal Asynchronous Receiver Transmitter (UART) serial interfaces. UART 1 (**RxD1/TxD1**) is the default. It supports data rates from 4.8 to 230.4 kBit/s. The signal output levels are 0 V to

[2] Only applies to modules supporting active antenna supply and supervision.

VCC (or VDDIO where available). An interface based on RS232 standard levels (+/- 12 V) can be realized using level shifters such as Maxim MAX3232.

☞ The **RxD1** has fixed input voltage thresholds, which do not depend on **VCC** (see module data sheet). Leave open if unused.

Hardware handshake signals and synchronous operation are not supported.

For the default settings see the module data sheet.

1.5.2 USB (LEA-5, NEO-5)

The u-blox 5 Universal Serial Bus (USB) interface supports the full-speed data rate of 12 Mbit/s.

1.5.2.1 USB external components

The USB interface requires some external components in order to implement the physical characteristics required by the USB 2.0 specification. These external components are shown in Figure 3 and listed in Table 1.

In order to comply with USB specifications, VBUS must be connected through a LDO (U1) to pin **VDD_USB** of the module.

If the USB device is **self-powered** it is possible that the power supply (VCC) is shut down and the Baseband-IC core is not powered. Since VBUS is still available, it still would be signaled to the USB host that the device is present and ready to communicate. This is not desired and thus the LDO (U1) should be disabled using the enable signal (EN) of the VCC-LDO or the output of a voltage supervisor. Depending on the characteristics of the LDO (U1) it is recommended to add a pull-down resistor (R11) at its output to ensure **VDD_USB** is not floating if LDO (U1) is disabled or the USB cable is not connected i.e. VBUS is not supplied.

If the device is **bus-powered**, LDO (U1) does not need an enable control.

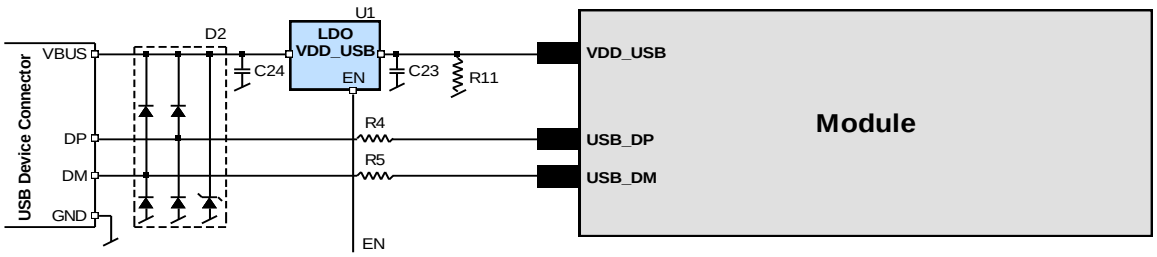


Figure 3: USB Interface

Name	Component	Function	Comments
U1	LDO	Regulates VBUS (4.4 …5.25 V) down to a voltage of 3.3 V).	Almost no current requirement (~1 mA) if the GPS receiver is operated as a USB self-powered device, but if bus-powered LDO (U1) must be able to deliver the maximum current of ~150 mA. A low-cost DC/DC converter such as LTC3410 from Linear Technology may be used as an alternative.
C23, C24	Capacitors		Required according to the specification of LDO U1
D2	Protection diodes	Protect circuit from overvoltage / ESD when connecting.	Use low capacitance ESD protection such as ST Microelectronics USBLC6-2.
R4, R5	Serial termination resistors	Establish a full-speed driver impedance of 28…44 Ohms	A value of 27 Ohms is recommended.
R11	Resistor		10k R is recommended for USB self-powered setup. For bus-powered setup R11 can be ignored.

Table 1: Summary of USB external components

1.5.3 DDC (LEA-5, NEO-5)

An I²C compatible Display Data Channel (DDC) interface is available with LEA-5 and NEO-5 modules for serial communication. For more information about DDC implementation refer to the u-blox 5 Receiver Description including Protocol Specification [2].

☞ u-blox 5 GPS receivers normally run in the slave mode. Master Mode is only supported when external EEPROM is used to store configuration. No other nodes are connected to the bus. In this case, the receiver attempts to establish presence of such a non-volatile memory component by writing and reading from a specific location.

Two wires, serial data (SDA) and serial clock (SCL), carry information between the devices connected to the bus. These lines are connected to all devices on the DDC. SCL is used to synchronize data transfers and SDA is the data line. Both SCL and SDA lines are "o"en drain" "rivers. This means that DDC devices can only drive them low or leave them open. The pull-up resistor (Rp) pulls the line up to V_{DD} if no DDC device is pulling it down to GND. If the pull-up resistors are missing, the SCL and SDA lines –are undefined and the DDC bus will not work. For most DDC systems the low and high input voltage level thresholds of SDA and SCL depend on V_{DD}. See receiver datasheet for the applicable voltage levels.

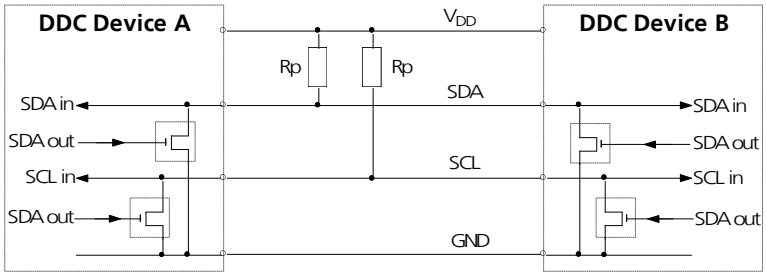


Figure 4: A simple DDC connection

The signal shape and the maximum rate in which data can be transferred over SDA and SCL is limited by the values of Rp and the wire and I/O capacitance (Cp). Long wires and a large number of devices on the bus increase Cp, therefore DDC connections should always be as short as possible. The resistance of the pull-up resistors and the capacitance of the wires should be carefully chosen.

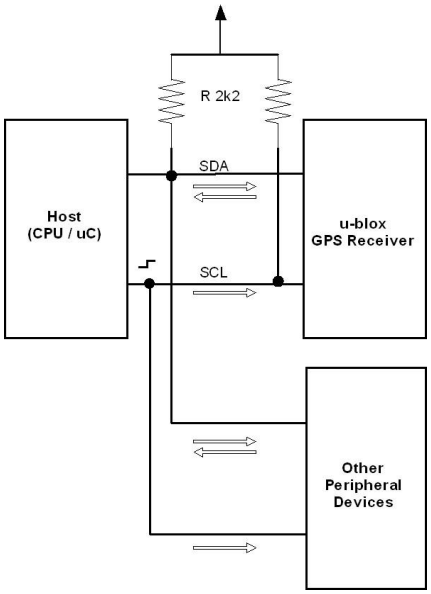


Figure 5: DDC block diagram

1.5.3.1 Addresses, roles and modes

Each device connected to a DDC is identified by a unique 7-bit address (e.g. whether it's a microcontroller, EEPROM or D/A Converter, etc) and can operate as either a transmitter or receiver, depending on the function of the device. The default DDC address for u-blox GPS receivers is set to 0x42. Setting the mode field in the CFG-PRT message for DDC accordingly can change this address.

☞ The first byte sent is comprised of the address field and R/W bit. Hence the byte seen on the bus 0x42 is shifted by 1 to the left plus R/W bit thus being 0x84 or 0x85 if analyzed by scope or protocol analyzer.

In addition to transmitters and receivers, devices can also be considered as masters or slaves when performing data transfers. A master is the device which initiates a data transfer on the bus and generates the clock signals to permit that transfer. At that time, any device addressed is considered a slave. The DDC-bus is a multi-master bus, i.e. multiple devices are capable of controlling the bus. Such architecture is not permanent and depends on the direction of data transfer at any given point in time. A master device not only allocates the time slots when slaves can respond but also enables and synchronizes designated slaves to physically access the bus by driving the clock. Although multiple nodes can assume the role of a master, only one at any time is permitted to do so. Thus, when one node acts as master, all other nodes act as slaves. Table 2 shows the possible roles and modes for devices connected to a DDC bus.

	Transmit	Receive
Master: sends the clock and addresses slaves	Sends data to slave	Receives data from slave
Slave: receives the clock and address	Sends data to master	Receives data from master

Table 2: Possible roles and modes of devices connected to DDC bus

u-blox 5 GPS receivers normally run in the slave mode. There is an exception when an external EEPROM is attached. In that case, the receiver attempts to establish presence of such a non-volatile memory component by writing and reading from a specific location. If EEPROM is present (assumed to be located at a fixed address 0xA0), the receiver assumes the role of a master on the bus and never changes role to slave until the following start-up (subject to EEPROM presence). This process takes place only once at the start-up, i.e. the receiver's role cannot be changed during the normal operation afterward. This model is an exception and should not be implemented if there are other participants on the bus contending for the bus control (μC / CPU, etc.).

Since the physical layer lacks a handshake mechanism to indicate the data availability, a layer has been inserted between the physical layer and the UBX and NMEA layer. The DDC implements a simple streaming interface that allows for constant data polling, discarding the segments of the data stream that do not belong to a valid UBX or NMEA message. Thus the u-blox GPS receiver returns 0xFf If no data is available. If the polling process is suspended for an extended period of time of 1.5 sec, the receiver temporarily stops writing data to the output buffer to prevent overflowing.

As a slave on the bus, the u-blox 5 GPS receiver cannot initiate the data transfers. The master node has the exclusive right and responsibility to generate the data clock, therefore the slave nodes need not be configured to use the same baud rate. For the purpose of simplification, if not specified differently, SLAVE denotes the u-blox 5 GPS receiver while MASTER denotes the external device (CPU, µC) controlling the DDC bus by driving the SCL line.

☞ u-blox GPS receivers support standard mode I^2C-bus specification with 7-bit addressing and a data transfer rate up to 100 kbit/s.

1.5.3.2 Communicating to a slave with the GPS receiver as master

Pins SDA2 and SCL2 have internal pull-ups. If capacitive bus load is large, additional external pull-ups may be needed in order to reduce the pull-up resistance.

Table 3 lists the maximum total pull-up resistor values for the DDC interface. The pull-up resistors integrated in the pads of the baseband-IC can simply be ignored for high capacitive loads. However, for small loads, e.g. if just connecting to an external EEPROM, these built-in pull-ups are sufficient.

Load Capacitance	Pull-Up Resistor Value R20, R21
50 pF	18 kΩ
100 pF	9 kΩ
250 pF	4 kΩ

Table 3: Pull-up resistor values for DDC interface

Serial I^2C memory can be connected to the DDC interface. It will automatically be recognized by firmware. The memory address must be set to 0b1010000 and the size fixed to 4 kB.

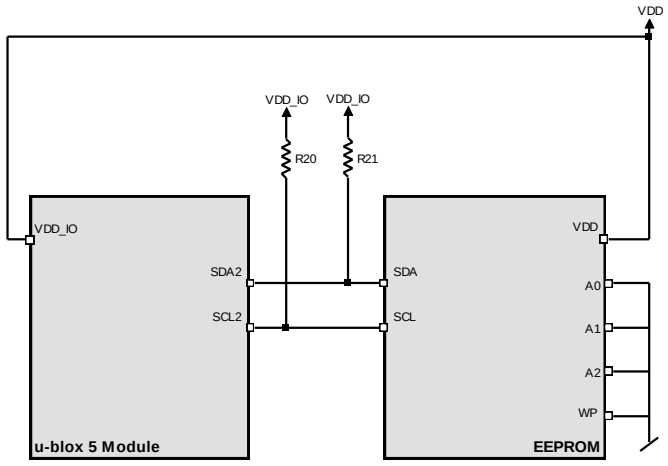


Figure 6: Connecting external serial I2C memory used by the GPS receiver (see data sheet for exact pin orientation)

Note that the case shown on Figure 6 is different than the case when EEPROM is present but used by external host / CPU as indicated on Figure 7. This is allowed but precaution is required to ensure that the GPS receiver does not detect the EEPROM device, which would effectively configure the GPS receiver to be MASTER on the bus causing collision with the external host.

To ensure that the EEPROM device (connected to the bus and used by the host) is not detected by the GPS receiver it is important to set the EEPROM's address to a value different than 0xA0. This way EEPROM remains free to be used for other purposes and the GPS receiver will assume the SLAVE mode.

☞ Ensure that at the start up the host allows enough time for the receiver to communicate over the bus to establish presence of the EEPROM. It is only when this interrogation is complete that the host can exercise full control over the bus (MASTER mode).

☞ Also note that the FLASH based modules do not attempt to store any information in the external EEPROM and as such do not attempt to communicate to the external EEPROM. The ROM based receivers always interrogate external EEPROM at the start-up. The interrogation process is guaranteed to complete within 250ms upon start up. This is the time the external host has to give to the ROM based GPS receiver to complete the EEPROM interrogation.

☞ Although the FLASH based modules do not attempt to detect the EEPROM at the start up, an attempt to communicate to the GPS receiver via DDC before 250msec expires is not advised because the GPS receiver is unable to respond due to other start up activities.

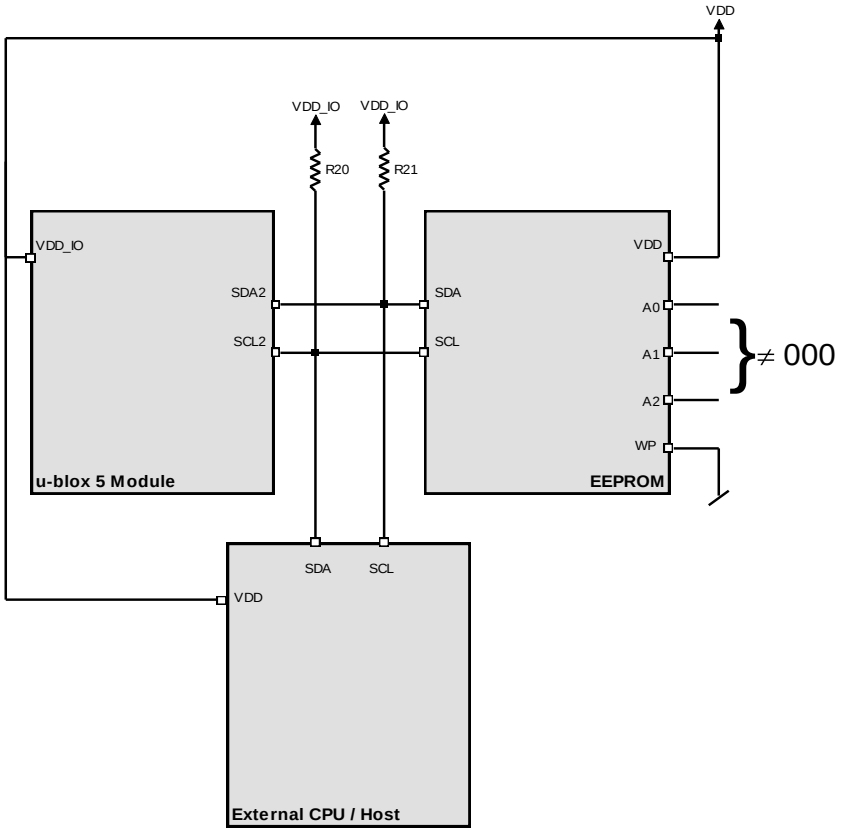


Figure 7: Connecting external serial I²C memory used by external host (see data sheet for exact pin orientation)

1.5.3.3 DDC troubleshooting

Consider the following questions when implementing DDC in designs:

- Is there a stable supply voltage Vcc? Often, external I²C devices (like I²C masters or monitors) must be provided with Vcc.
- Are appropriate termination resistances attached between SDA, SCL and Vcc? The voltage level on SDA and SCL must be Vcc as long as the bus is idle and drop near GND if shorted to GND. [Note: Very few I²C masters exist which drive SCL high and low, i.e. the SCL line is not open-drain. In this case, a termination resistor is not needed and SCL cannot be pulled low. These masters will not work together with other masters (as they have no multi-master support) and may not be used with devices which stretch SCL during transfers.]
- Are SDA and SCL mixed up? This may accidentally happen e.g. when connecting I²C buses with cables or connectors.
- Do all I²C devices support the I²C supply voltage used on the bus?
- Do all I²C devices support the maximum SCL clock rate used on the bus?
- If more than one I2C master is connected to the bus: do all masters provide multi-master support?
- Are the high and low level voltages on SDA and SCL correct during I2C transfers? The I²C standard defines the low level threshold with 0.3 Vcc, the high level threshold with 0.7 Vcc. Modifying the termination resistance Rp, the serial resistors Rs or lowering the SCL clock rate could help here.
- Are there spikes or noise on SDA, SCL or even Vcc? They may result from interferences from other components or because the capacitances Cp and/or Cc are too high. The effects can often be reduced by using shorter interconnections.

☞ For more information about DDC implementation refer to the u-blox 5 Receiver Description including Protocol Specification [2].

1.5.4 SPI (planned with LEA-5Q and NEO-5Q/5G)

A Serial Peripheral Interface (SPI) will be available with selected u-blox 5 modules for serial communication. This is a synchronous serial data link standard that operates in full duplex mode. SPI is primarily used to enable a microcontroller unit (µC) to communicate with peripheral devices. Peripheral devices can be as simple as an ordinary transistor-transistor logic (TTL) shift register or as complex as a complete subsystem.

1.5.4.1 SPI basics

Devices communicate in master/slave mode where the master device provides the clock signal (SCK) and determines the state of the chip select (SCS/SS_N) lines, i.e. it activates the slave it wants to communicate with. The slave device receives the clock and chip select from the master. Multiple slave devices are allowed with individual slave select (chip select) lines. This means that there is one master, while the number of slaves is only limited by the number of chip selects. In addition to reliability and relatively high speed (with respect to the conventional UART), the SPI interface is easy to use and requires no special handling or complex communication stack implementation in the software.

The standard configuration for a slave device (see Figure 8) uses two control and two data lines. These are identified as follows:

- SCS — Slave Chip Select (control: output from master, usually active low)
- SCK — Serial Clock (control: output from master)
- MOSI — Master Output, Slave Input (data: output from master)
- MISO — Master Input, Slave Output (data: output from slave)

☞ Alternative naming conventions are also widely used. Confirm the pin/signal naming with specific components used.

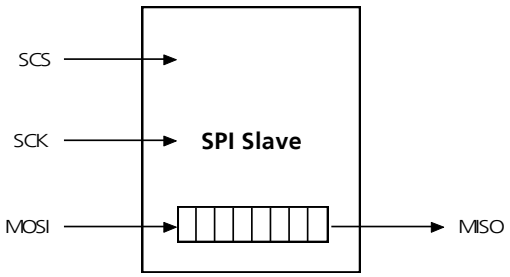


Figure 8: SPI slave

SPI always follows the basic principle of a shift register. During an SPI transfer, command codes and data values are simultaneously transmitted (shifted out serially) and received (shifted in serially). The data is entered into a shift register and then internally available for parallel processing. The length of the shift registers is not fixed, but can vary from device to device. Normally the shift registers are 8Bit or integral multiples thereof. However, they can also have an odd number of bits. For example two cascaded 9Bit EEPROMs can store 18Bit data.

When an SPI transfer occurs, an 8-bit character is shifted out one data pin while a different 8-bit character is simultaneously shifted in a second data pin. Another way to view this transfer is that an 8-bit shift register in the master and another 8-bit shift register in the slave are connected as a circular 16-bit shift register. When a transfer occurs, this distributed shift register is shifted eight bit positions; thus, the characters in the master and slave are effectively exchanged.

The serial clock (SCK) line synchronizes shifting and sampling of the information on the two serial data lines (MOSI and MISO). The chip select (SCS/SS_N) line allows individual selection of a slave SPI device. If an SPI slave

device is not selected (i.e. its chip select is not activated), its data output enters a high-impedance state (hi-Z) and does not interfere with SPI bus activities.

The data output MISO functions as the data return signal from the slave to the master.

Figure 9 shows a typical block diagram for an SPI master with several slaves. Here, the SCK and MOSI data lines are shared by all of the slaves. Also the MISO data lines are linked together and led back to the master. Only the chip selects are separately brought to each SPI device.

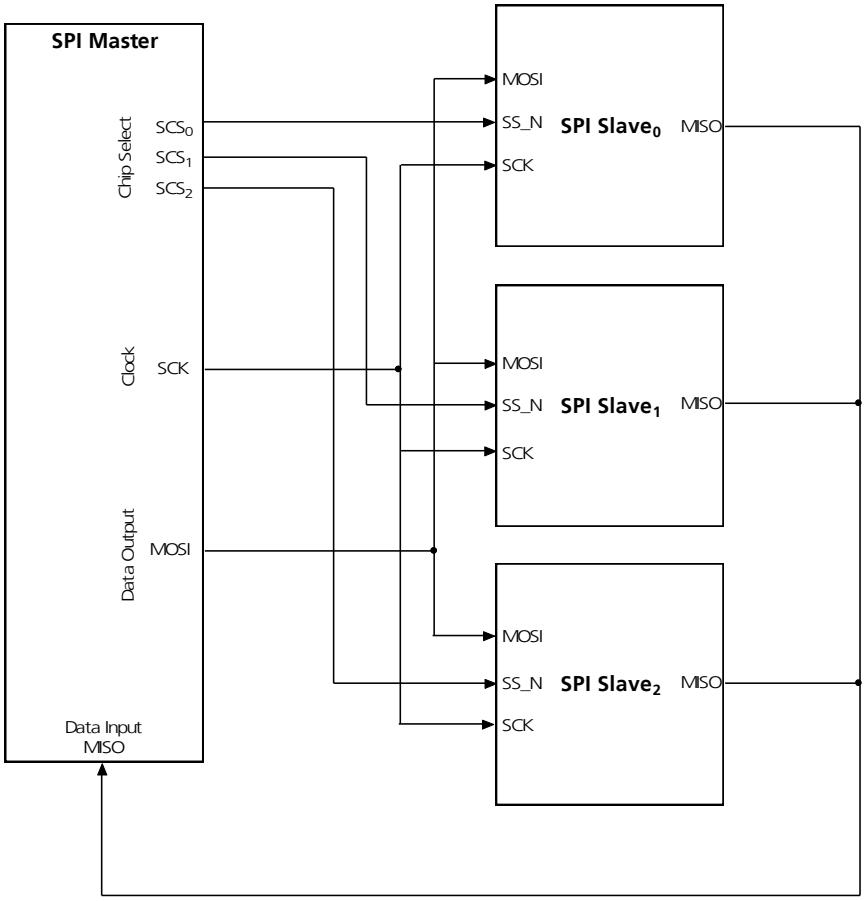


Figure 9: Master with independent slaves

SPI allows multiple microcontrollers to be linked together. These can be configured according to single or multiple master protocols. In the first variant the microcontroller(s) designated as slave(s) behave like a normal peripheral device. The second variant allows for several masters and allows each microprocessor the possibility to take the role of master and to address another microprocessor. In this case one microcontroller must permanently provide the clock signal.

There are two SPI system errors. The first occurs if several SPI devices want to become master at the same time. The other is a collision error that occurs for example when SPI devices work with different polarities.

☞ Systems involving multiple microcontrollers are beyond the scope of this document.

☞ Cascading slave peripherals is not supported.

Four I/O pin signals are associated with SPI transfers: the SCK, the MISO data line, the MOSI data line, and the active low SCS/SS_N pin. In the unselected state the MISO lines are hi-Z and therefore inactive. The master

decides with which peripheral device it wants to communicate. The clock line SCK provides synchronization for data communication and is brought to the device whether or not it is selected.

The majority of SPI devices provide all four of these lines. Sometimes MOSI and MISO are multiplexed, or else one is missing. A peripheral device, which must not or cannot be configured, requires no input line but only a data output. As soon as it gets selected it starts sending data. In some ADCs therefore the MOSI line is missing. Some devices have no data output (e.g. LCD controllers which can be configured, but cannot send data or status messages).

The following rules should answer the most common questions concerning these signals:

- **SCK:** The SCK pin is an output when the SPI is configured as a master and an input when the SPI is configured as a slave. When the SPI is configured as a master, the SCK signal is derived from the internal bus clock. When the master initiates a transfer, eight clock cycles are automatically generated on the SCK pin. When the SPI is configured as a slave, the SCK pin is an input, and the clock signal from the master synchronizes the data transfer between the master and slave devices. Slave devices ignore the SCK signal unless the slave select pin is active low. In both the master and slave SPI devices, data is shifted on one edge of the SCK signal and is sampled on the opposite edge where data is stable. Edge polarity is determined by the SPI transfer protocol.
- **MISO/MOSI:** The MISO and MOSI data pins are used for transmitting and receiving serial data. When the SPI is configured as a master, MISO is the master data input line, and MOSI is the master data output line. When the SPI is configured as a slave, these pins reverse roles.
- **SCS/SS_N:** In master mode, the SCS output(s) select external slaves (e.g. SCS1_N, SCS2_N). In slave mode, SS_N is the slave select input. The chip select pin behaves differently on master and slave devices. On a slave device, this pin is used to enable the SPI slave for a transfer. If the SS_N pin of a slave is inactive (high), the device ignores SCK clocks and keeps the MISO output pin in the high-impedance state. On a master device, the SCS pin can serve as a general-purpose output not affecting the SPI.

1.5.4.2 Connecting serial memory to u-blox 5 modules

Serial SPI memory can be connected to the SPI interface. It will automatically be recognized by firmware when connected to SCS1_N.

Figure 10 shows how external memory can be connected. Note that an external voltage is required to power the EEPROM (VDD_IO on the receiver is an input).

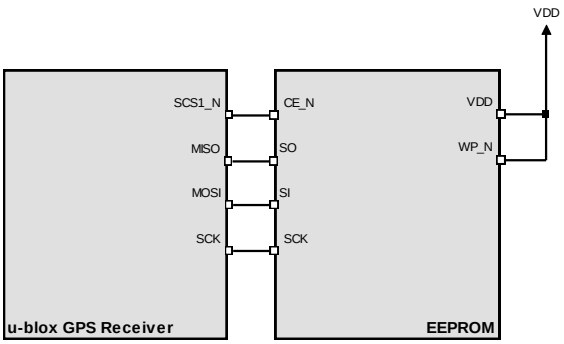


Figure 10: Connecting external Serial SPI Memory to u-blox GPS receivers

☞ External memory on the SPI interface is only supported by FW 6.00 and above. Only 128 kByte memory size is supported.

1.5.4.3 Connecting u-blox 5 modules to an SPI master

Figure 11 shows how to connect a u-blox GPS receiver to a host/master. The signal on the pins must meet the conditions specified in the Data Sheet.

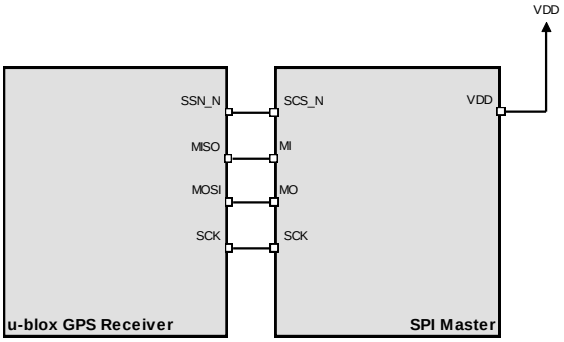


Figure 11: Connecting to SPI Master

1.5.4.4 SPI and u-blox 5 configuration pins

With some u-blox 5 modules the SPI MOSI, MISO and SCK pins have a shared configuration function at start up. To secure correct receiver operation make sure that the SS_N pin is high at start up. Afterwards the SPI function will not affect the configuration pins.

1.5.4.5 Pin configuration with u-blox 5 module as one of several slaves

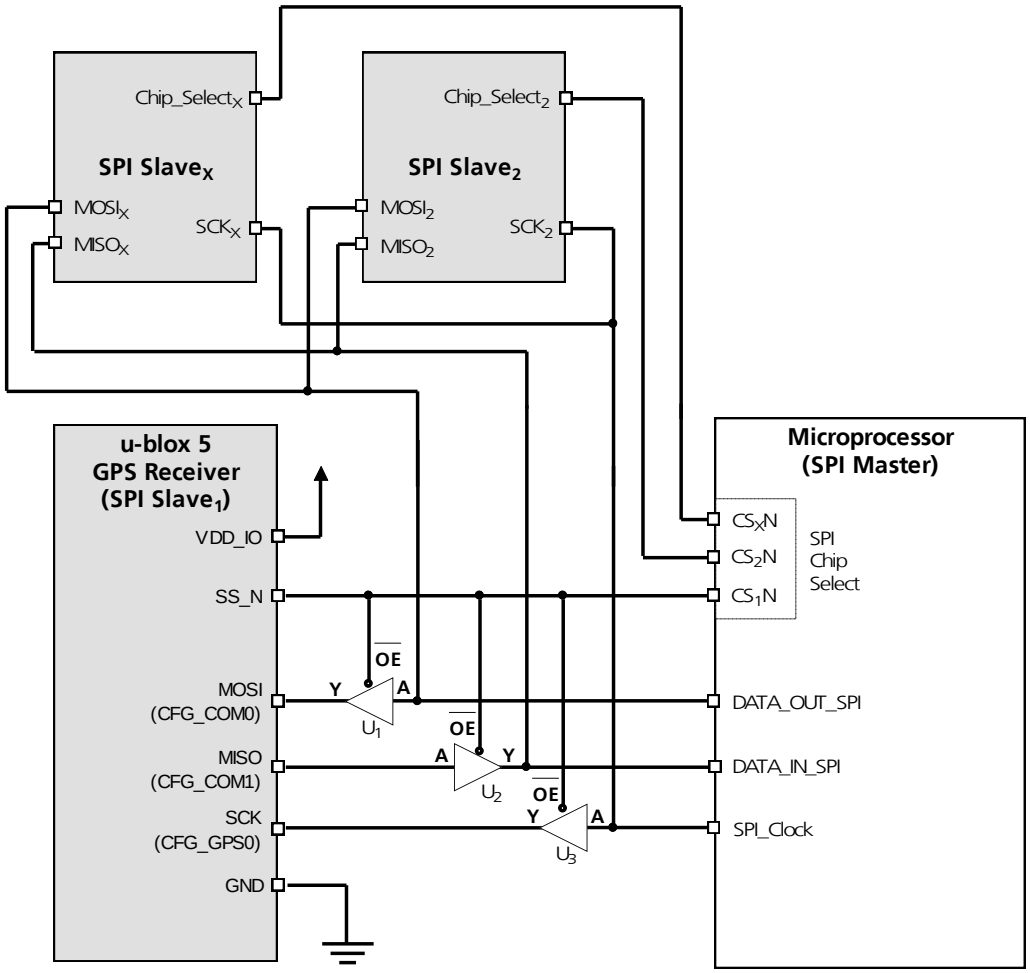


Figure 12: Diagram of SPI Pin Configuration

Component	Description	Model	Supplier
$U_1 – U_3$	Buffer	NC7SZ125	Fairchild

Figure 13: Recommended components for SPI pin configuration

Use same power voltage to supply $U_1 – U_3$ and VDD_IO.

1.6 I/O pins

1.6.1 RESET_N (LEA-5, TIM-5H)

As with ANTARIS 4 versions, LEA-5 and TIM-5H modules come equipped with a **RESET_N** pin. Driving **RESET_N** low activates a hardware reset of the system. Unlike ANTARIS 4 modules, **RESET_N** is not an I/O with u-blox 5. It is only an input and will not reset external circuitry.

Use components with open drain output (i.e. with buffer or voltage supervisor).

There is an internal pull up resistor of 3k3 to VCC inside the module that requires that the reset circuitry can deliver enough current (e.g. 1mA).

Do not drive **RESET_N** high.

1.6.2 EXTINT0

EXTINT0 is an external interrupt pin with fixed input voltage thresholds independent of VCC (see the data sheet for more information). Leave open if unused.

1.6.3 AADET_N (LEA-5, TIM-5H)

AADET_N is an input pin and is used to report whether an external circuit has detected a external antenna or not. Low means antenna has been detected. High means no external antenna has been detected.

See chapter 2.6.5 for an implementation example.

1.6.4 Configuration pins (LEA-5S/5A/5Q/5M, NEO-5)

ROM-based modules provide up to 3 pins (**CFG_COM0, CFG_COM1**, **CFG_GPS0**) for boot-time configuration. These become effective immediately after start-up. Once the module has started, the configuration settings can be modified with UBX configuration messages. The modified settings remain effective until power-down or reset. If these settings have been stored in battery-backup RAM, then the modified configuration will be retained, as long as the backup battery supply is not interrupted.

Some configuration pins are shared with other functions, e.g. SPI. During start-up, the module reads the state of the configuration pins. Afterwards the other functions can be used.

☞ For more information about settings and messages see the module data sheet.

2 Design-in

☞ For migrating existing ANTARIS®4 product designs to u-blox 5 please refer to Appendix **A**.

In order to obtain good performance with a GPS receiver module, there are a number of points that require careful attention during the design-in. These include:

- Power Supply
  Good performance requires a clean and stable power supply.
- Interfaces
  Ensure correct wiring, rate and message setup on the module and your host system.
- Antenna interface
  For optimal performance seek short routing, matched impedance and no stubs.

2.1 Design-in checklist

Good performance requires a clean and stable power supply with minimal ripple. Care needs to be exercised in selecting a strategy to achieve this. Series resistance in the Vcc supply line can negatively impact performance. For better performance, use an LDO to provide a clean supply at Vcc and consider the following:

- Wide power lines or even power planes are preferred.
- Place LDO near the module.
- Avoid resistive components in the power line (e.g. narrow power lines, coils, resistors, etc.).
- Placing a filter or other source of resistance at Vcc can create significantly longer acquisition times.

2.1.1 Layout design-in checklist

Designing-in a u-blox 5 module is easy, especially when based on a u-blox reference design. Nonetheless, it pays to do a quick sanity check of the design. This section lists the most important items for a simple design check. The Layout Design-In Checklist also helps to avoid an unnecessary respin of the PCB and helps to achieve the best possible performance.

☞ Follow the design-in checklist when developing any u-blox 5 GPS applications. This can significantly reduce development time and costs.

Have you chosen the optimal module?

u-blox 5 modules have been intentionally designed to allow GPS receivers to be optimally tailored to specific applications. Changing between the different variants is easy.

- ❑ Do you need Kick-start performance – Then choose an **H**[3]**, S**[4], **Q**[5], or **G**[6] variant.
- ❑ Do you want to be able to upgrade the firmware or to permanently save configuration settings? Then you will have to use a Programmable receiver module: choose an **H**[3] variant.
- ❑ Do you need USB? All LEA-5 and NEO-5 modules based on FW/ROM 5.00 and above support USB.
- ❑ Do you need Precision Timing – Then choose a LEA-5**T**.

Check Power Supply Requirements and Schematic:

- ❑ Is the power supply within the specified range (see data sheet)?

[3] LEA-5H, TIM-5H.
[4] LEA-5S
[5] LEA-5Q, NEO-5Q
[6] NEO-5G

- ❑ Is the voltage **VDDUSB** within the specified range?
- ❑ Compare the peak current consumption of your u-blox 5 module with the specification of the power supply.
- ❑ GPS receivers require a stable power supply, avoid ripple on **VCC** (<50mVpp)
- ❑ For low power applications using Power Save and backup modes, ensure that the power supply or low ESR capacitors at the module input can deliver the required current/charge for switching from backup mode to normal operation. In certain situations charging the internal capacitors in the core domain can result in a significant instantaneous current draw.

Backup Battery

- ❑ For achieving a minimal Time To First Fix (TTFF), connect a backup battery to **V_BCKP** after power down.

Antenna

- ❑ The total noise figure should be well below 3dB.
- ❑ If a patch antenna is the preferred antenna, choose a patch of at least 15x15mm. For smaller antennas an LNA with a noise figure <2dB Is recommended, this can increase sensitivity up to 2dB. To optimize TTFF make use of u-blox' free A-GPS services AssistNow Online and AssistNow Offline.
- ❑ Make sure the antenna is not placed close to noisy parts of the circuitry. (e.g. micro-controller, display, etc.)
- ❑ For active antennas add a 10R resistor in front of **V_ANT**[7] input for short circuit protection or use the antenna supervisor circuitry.
- ❑ To optimize performance in environments with out-band jamming sources, use an additional SAW filter.

☞ For more information dealing with interference issues see the GPS Antenna Application Note [6].

Schematic

- ❑ If required, does your schematic allow using different module variants?
- ❑ Don't drive **RESET_N** high!
- ❑ Plan use of 2nd Interface (Testpoints on serial port, DDC or USB) for firmware updates or as a service connector.

Layout optimizations (*Section 2.5*)

- ❑ Is the GPS module placed according to the recommendation in Section 2.5.2?
- ❑ Has the Grounding concept been followed (see Section 2.5.3)?
- ❑ Has the micro strip been kept as short as possible?
- ❑ Add a ground plane underneath the GPS module to reduce interference.
- ❑ For improved shielding, add as many vias as possible around the micro strip, around the serial communication lines, underneath the GPS module etc.
- ❑ Have ESD protection measures been included (see Section 2.7)?

Calculation of the micro strip (Section 2.5.4**)**

- ❑ The micro strip must be 50 Ohms and be routed in a section of the PCB where minimal interference from noise sources can be expected.
- ❑ In case of a multi-layer PCB, use the thickness of the dielectric between the signal and the 1st GND layer (typically the 2nd layer) for the micro strip calculation.
- ❑ If the distance between the micro strip and the adjacent GND area (on the same layer) does not exceed 5 times the track width of the micro strip, use the "Coplanar Waveguide" model in AppCad to calculate the micro strip and not the "micro strip" model.

[7] Only available with LEA-5-H, LEA-5S, LEA-5A, LEA-5T and TIM-5H

2.1.2 Design considerations

For a minimal design with a u-blox 5 GPS module the following functions and pins need to be considered:

- Connect the Power supply to **VCC.**
- **VDDUSB**[8]**:** Connect the USB power supply to a LDO before feeding it to **VDDUSB** and **VCC**. Or connect to GND if USB is not used.
- Assure a optimal ground connection to all ground pins of the module
- Connect the antenna to **RF_IN** over a matching 50 Ohm micro strip and define the antenna supply (**V_ANT**)[9] for active antennas (internal or external power supply)
- Choose the required serial communication interface (UART, USB[8] or DDC[8]) and connect the appropriate pins to your application
- If you need Hot- or Warmstart in your application, connect a backup battery to **V_BCKP**
- Decide whether **TIMEPULSE** or **RESET_N**[10] options are required in your application and connect the appropriate pins on your module

[8] LEA-5 and NEO-5 modules only
[9] Only available with LEA-5-H, LEA-5S, LEA-5A, LEA-5T, TIM-5H
[10] LEA-5 and TIM-5H modules only

2.2 LEA-5 design

2.2.1 LEA-5 passive antenna design

This is a minimal setup for a PVT GPS receiver with a LEA-5 module.

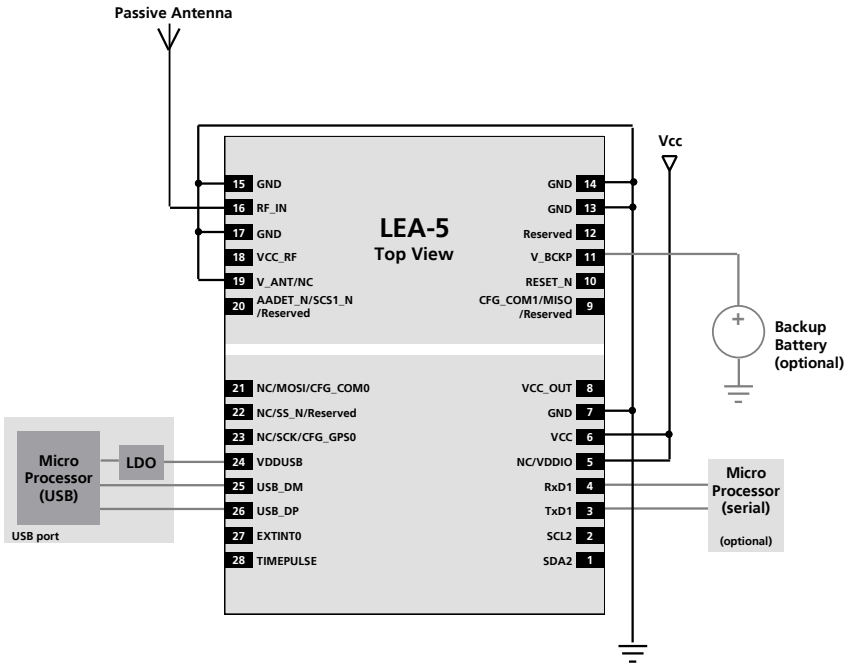


Figure 14: Passive antenna design for LEA-5 receivers using USB port

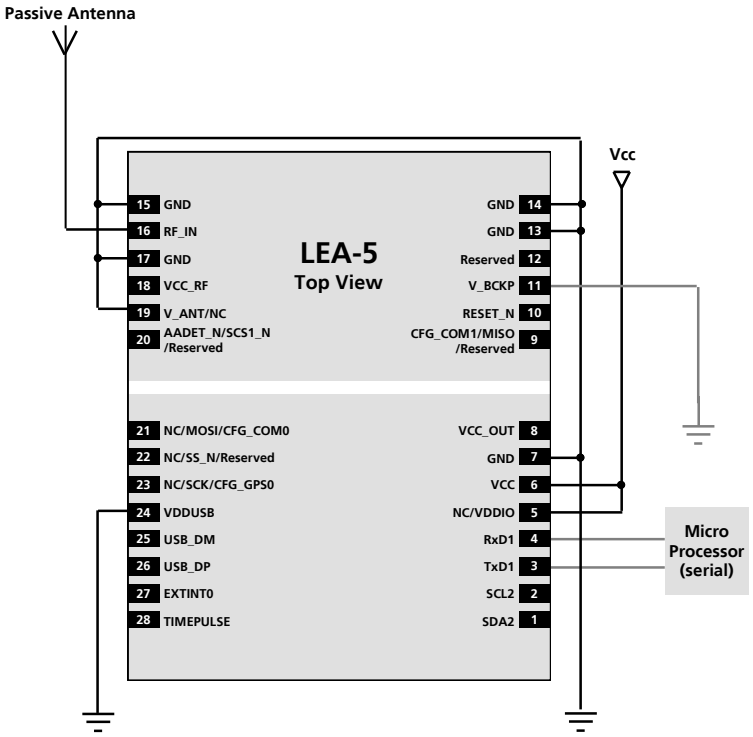


Figure 15: Passive antenna design for LEA-5 receivers not using USB port and not using backup battery

☞ For passive antenna designs use an LNA to increase sensitivity up to 2dB.

2.2.2 Pin description for antenna designs (LEA-5H/5S/5A/5T)

Function	PIN	No	I/O	Description	Remarks
Power	**VCC**	6	I	Supply Voltage	Provide clean and stable supply.
	GND	7, 13-15, 17	I	Ground	Assure a good **GND** connection to all **GND** pins of the module, preferably with a large ground.
	VCC_OUT	8	O		Connected to VCC. Leave open if not used.
	V_BCKP	11	I	Backup voltage supply	It's recommended to connect a backup battery to **V_BCKP** in order to enable Warm and Hot Start features on the receivers. Otherwise connect to **GND** (or **VCC**).
	VDDUSB	24	I	USB Power Supply	To use the USB interface connect this pin to 3.0 – 3.6V derived from VBUS. If no USB serial port used connect to GND.
Antenna	**RF_IN**	16	I	GPS/GALILEO signal input from antenna	Use a controlled impedance transmission line of 50 Ohm to connect to RF_IN. Don't supply DC through this pin. Use **V_ANT** pin to supply power.
	VCC_RF	18	O	Output Voltage RF section	Can be used to power an external active antenna (**VCC_RF** connected to **V_ANT with 10R**). The max power consumption of the Antenna must not exceed the datasheet specification of the module. Leave open if not used.
	V_ANT	19	I	Antenna Bias voltage	Connect to **GND** (or leave open) if Passive Antenna is used. If an active Antenna is used, add a 10R resistor in front of **V_ANT** input to the Antenna Bias Voltage or **VCC_RF** for short circuit protection use the antenna supervisor circuitry.
	AADET_N	20	I	Active Antenna Detect	Input pin for optional antenna supervisor circuitry. Leave open if not used.

Function	PIN	No	I/O	Description	Remarks
UART	**TxD1**	3	O	Serial Port 1	Serial port output. Leave open if not used.
	RxD1	4	I	Serial Port 1	Serial port input with internal pull-up resistor to VCC. Leave open if not used. Don't use external pull up resistor.
USB	**USB_DM**	25	I/O	USB I/O line	USB2.0 bidirectional communication pin. Leave open if unused. Implementation see Section 1.5.2.
	USB_DP	26	I/O	USB I/O line	
System	**RESET_N**	10	I	Hardware Reset (Active Low)	Leave open if not used. Do not drive high.
	TIMEPULSE	28	O	Timepulse Signal	Configurable Timepulse signal (one pulse per second by default). Leave open if not used.
	EXTINT0	27	I	External Interrupt	External Interrupt Pin. Internal pull-up resistor to **VCC**. Leave open if not used.
	CFG_COM1 /Reserved	9	I	Config. Pin /Reserved	LEA-5S, LEA-5A: Leave open for default configuration. LEA-5H, LEA-5T: Reserved
	SDA2	1	I/O	DDC Pins	DDC Data. Leave open if not used.
	SCL2	2	I/O	DDC Pins	DDC Clock. Leave open if not used.
	Reserved	12	I		Leave open, do not drive low.
	NC	5			Can be left open, but **connection to VCC is recommended** for compatibility reasons. I/O voltage is always VCC.
	NC	21-22		Not Connect	Leave open
	NC	23		Not Connect	Leave open

Table 4: Pin description LEA-5H/5S/5A/5T

2.2.3 Pin description for antenna designs (LEA-5Q/5M)

Function	PIN	No	I/O	Description	Remarks
Power	**VCC**	6	I	Supply Voltage	Provide clean and stable supply.
	GND	7, 13-15, 17	I	Ground	Assure a good **GND** connection to all **GND** pins of the module, preferably with a large ground plane.
	VCC_OUT	8	O		Connected to VCC. Leave open if not used.
	V_BCKP	11	I	Backup voltage supply	It's recommended to connect a backup battery to **V_BCKP** in order to enable Warm and Hot Start features on the receivers. Otherwise connect to **GND** (or VCC).
	VDDUSB	24	I	USB Power Supply	To use the USB interface connect this pin to 3.0-3.6V derived from VBUS. If no USB serial port used connect to GND.
	VDDIO	5	I	I/O Voltage	Defines the I/O voltage. Do not leave open.
Antenna	**RF_IN**	16	I	GPS/GALILEO signal input from antenna	Use a controlled impedance transmission line of 50 Ohm to connect to RF_IN. Antenna bias voltage for active antennas is not provided on the **RF_IN** pin. If an active Antenna is used an external voltage is required (see Section 2.6.3).
	VCC_RF	18	O	Output Voltage RF section	Leave open
UART	**TxD1**	3	O	Serial Port 1	Serial port output. Leave open if not used.
	RxD1	4	I	Serial Port 1	Serial port input with internal pull-up resistor to VCC. Leave open if not used. Don't use external pull up resistor.
USB	**USB_DM**	25	I/O	USB I/O line	USB2.0 bidirectional communication pin. Leave open if unused. Implementation see Section 1.5.2.
	USB_DP	26	I/O	USB I/O line	

Function	PIN	No	I/O	Description	Remarks
System	**RESET_N**	10	I	Hardware Reset (Active Low)	Leave open if not used. Do not drive high.
	TIMEPULSE	28	O	Timepulse Signal	Configurable Timepulse signal (one pulse per second by default). Leave open if not used.
	EXTINT0	27	I	External Interrupt	External Interrupt Pin. Internal pull-up resistor to **VCC**. Leave open if not used.
	SDA2	1	I/O	DDC Pins	DDC Data. Leave open, if not used.
	SCL2	2	I/O	DDC Pins	DDC Clock. Leave open, if not used.
	Reserved	12	I		Leave open, do not drive low.
	NC	19		Not Connected	Leave open.
	SCS1_N/ Reserved	20	O	SPI	LEA-5Q: SPI Chip Select. Leave open if not used. (Planned) LEA-5M: Leave open.
	MISO/ CFG_COM1	9	I/O	SPI Configuration Pin	LEA-5Q: SPI MISO. Leave open, if not used. (Planned) LEA-5Q/LEA-5M: Leave open for default configuration.
	MOSI/ CFG_COM0	21	I/O	SPI Configuration Pin	LEA-5Q: SPI MOSI. Leave open, if not used. (Planned) LEA-5Q/LEA-5M: Leave open for default configuration.
	SS_N/ Reserved	22	I	SPI Reserved	LEA-5Q: SPI Slave Select. Leave open, if not used. (Planned) LEA-5M: Leave open.
	SCK/CFG_GPS/ Reserved	23	I/O	SPI/Power Mode	LEA-5Q: SPI Clock / Power Mode Configuration Pin. Leave open, if not used. (Planned) LEA-5M: Leave open.

Table 5: Pin description LEA-5Q/5M

☞ The above design is for the USB in BUS-powered mode. For Self-powered mode pin 21 (CFG_COM0) must be connected to GND. NMEA baud rate is 38400 when in self-powered mode. For more information see the LEA-5 Data Sheet [1].

2.3 NEO-5 design

2.3.1 Passive antenna design (NEO-5)

This is a minimal setup for a PVT GPS receiver with a NEO-5 module.

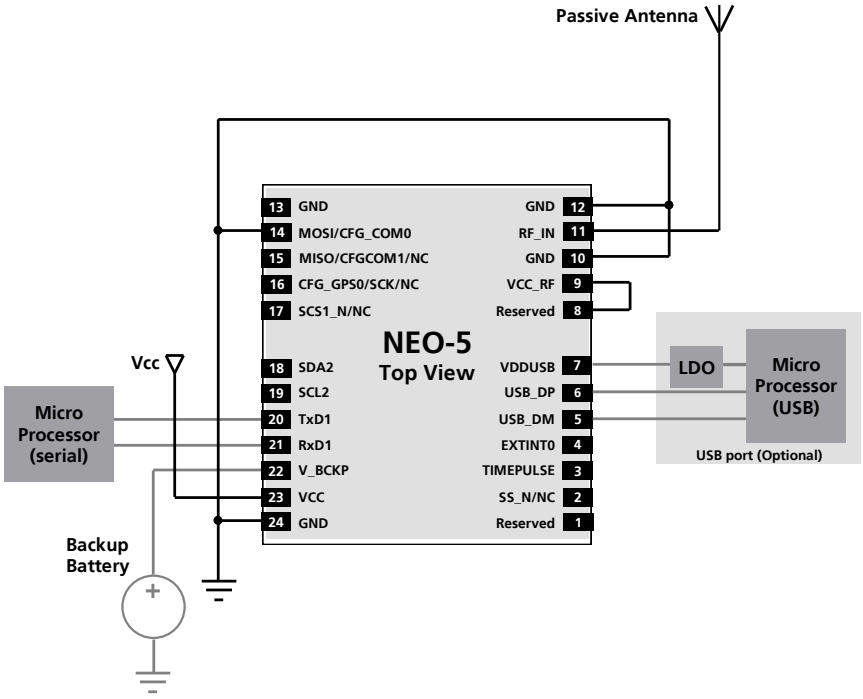


Figure 16: Passive antenna design for NEO-5 receivers

The above design is for the USB in self-powered mode. For bus-powered mode pin 14 (**CFG_COM0**) must be left open and **Vcc** must be connected to **VDDUSB**. NMEA baud rate is 38400 when in self-powered mode.

For passive antenna designs use an LNA to increase sensitivity up to 2dB.

Function	PIN	No	I/O	Description	Remarks
Power	**VCC**	23	I	Supply Voltage	Max allowed ripple on VCC=50mVpp
	GND	10,12,13,24	I	Ground	Assure a good **GND** connection to all **GND** pins of the module, preferably with a large ground plane.
	V_BCKP	22	I	Backup voltage supply	It's recommended to connect a backup battery to **V_BCKP** in order to enable Warm and Hot Start features on the receivers. Otherwise connect to **GND** (or VCC).
	VDDUSB	7	I	USB Power Supply	To use the USB interface connect this pin to 3.0 – 3.6V. If no USB serial port used connect to GND.
Antenna	**RF_IN**	11	I	GPS signal input from antenna	The connection to the antenna has to be routed on the PCB. Use a controlled impedance of 50 Ohm to connect RF_IN to the antenna or the antenna connector.
	VCC_RF	9	O	Output Voltage RF section	Pins 8 and 9 **must** be connected together. VCC_RF can also be used to power an external active antenna.
UART	**TxD1**	20	O	Serial Port 1	
	RxD1	21	I	Serial Port 1	3.6V tolerant serial input. Internal pull-up resistor to VCC. Leave open if not used.
USB	**USB_DM**	5	I/O	USB I/O line	USB2.0 bidirectional communication pin. Leave open if unused. Implementation see Section 1.5.2
	USB_DP	6	I/O	USB I/O line	

Function	PIN	No	I/O	Description	Remarks
System	**TIMEPULSE**	3	O	Timepulse Signal	Configurable Timepulse signal (one pulse per second by default). Leave open if not used.
	EXTINT0	4	I	External Interrupt	External Interrupt Pin. Internal pull-up resistor to **VCC**. Leave open if not used.
	SDA2	18	I/O	DDC Pins	DDC Data. Leave open, if not used.
	SCL2	19	I/O	DDC Pins	DDC Clock. Leave open, if not used.
	SCS1_N/NC	17	O	SPI MISO /CFG_COM1 /Not Connected	NEO-5Q/5G: Leave open if not used. NEO-5M/5D: not connected, leave open.
	MISO/ CFG_COM1 /NC	15	I/O	SPI Configuration Pin	NEO-5Q/5G[11]: CFG_COM1 is shared with SPI MISO pin. When using CFG & SPI port, apply configuration settings needed during setup. NEO-5M/5D[11]: Leave open.
	MOSI/ CFG_COM0	14	I	SPI MOSI/CFG_COM0	NEO-5Q/5G[11]: Leave open if not used. CFG_COM1 is shared with SPI MOSI pin. When using CFG & SPI port, apply configuration settings needed during setup. **Note** Connect to GND to use USB in Self Powered mode. See Section 1.6.4 and the NEO-5 Data Sheet [2] NEO-5M/5D[11]: Leave open if not used.
	NC/SS_N	2	I	Not Connected/ SPI Slave Select	NEO-5Q/5G: Slave select input for SPI. Leave open if not used.
	SCK/CFG_GPS0/ NC	16	I/O	SPI Clock/ Power Mode Configuration/ Not Connected	NEO-5Q/5G[11]: CFG_GPS0 pin shared with the SPI Clock pin. When using Eco Mode and SPI, pull CFG_GPS0 low during startup and then release it. NEO-5M/5D[11]: Leave open.

Table 6: Pinout NEO-5

2.4 TIM-5H design

This is a minimal setup for a PVT GNSS receiver with a TIM-5H module.

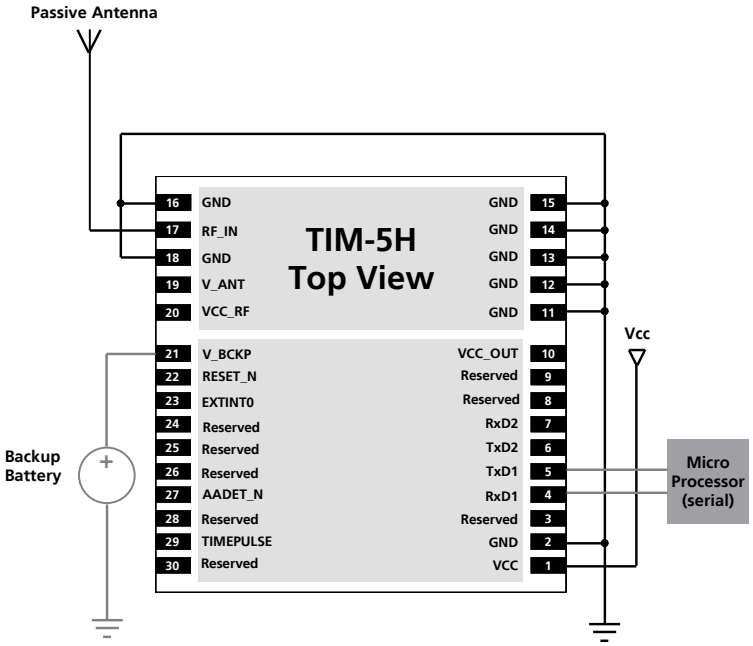


Figure 17: Passive antenna design for TIM-5H receivers

[11] Internal pull-up to define default CFG_xxx configuration during startup. Leave open if default setting is ok and pin not otherwise used. For other configurations apply the required pin settings during startup.

Function	PIN	No	I/O	Description	Remarks
Power	**VCC**	1	I	Supply Voltage	Provide clean and stable supply. Maximum allowed Ripple Vcc=50mV.
	GND	2,11-16,18	I	Ground	Assure a good **GND** connection to all **GND** pins of the module, preferably with a large ground plane.
	VCC_OUT	10	O		Connected to **VCC**. Leave open if not used.
	V_BCKP	21	I	Backup voltage supply	Connect a backup battery to **V_BCKP** in order to enable Warm and Hot Start features on the receivers. Otherwise connect to **GND** (or **VCC**).
Antenna	**RF_IN**	17	I	GNSS signal input from antenna	Use a controlled impedance transmission line of 50 Ohm to connect to **RF_IN**. Don't supply DC through this pin. Use **V_ANT** pin to supply power.
	VCC_RF	20	O	Output Voltage RF section	Can be used to power an external active antenna (**VCC_RF** connected to **V_ANT**). The max power consumption of the Antenna must not exceed the datasheet specification of the module. Leave open if not used.
	V_ANT	19	I	Antenna Bias voltage	Connect to **GND** (or leave open) if passive antenna is used. If an active Antenna is used, add a 10R resistor in front of **V_ANT** input for short circuit protection or use the antenna supervisor circuitry.
	AADET_N	27	I	Active Antenna Detect	Input pin for optional antenna supervisor circuitry. Leave open if not used.
UART	**TxD1**	5	O	Serial Port 1	Serial port output. Leave open if not used.
	TxD2	6	O	Serial Port 2	3.6V tolerant serial input. Internal pull-up resistor to VCC. Leave open if not used.
	RxD1	4	I	Serial Port 1	Serial port input with internal pull-up resistor to VCC. Leave open if not used. Note Don't use an external pull up resistor.
	RxD2	7	I	Serial Port 2	
System	**RESET_N**	22	I	Hardware Reset (Active Low)	Leave open if not used. Do not drive high.
	TIMEPULSE	29	O	Timepulse Signal	Configurable Timepulse signal (one pulse per second by default). Leave open if not used.
	EXTINT0	23	I	External Interrupt	External Interrupt Pin. Internal pull-up resistor to **VCC**. Leave open if not used.

Table 7: Pinout TIM-5H

2.5 Layout

This section provides important information for designing a reliable and sensitive GPS system.

GPS signals at the surface of the Earth are about 15dB Below the thermal noise floor. Signal loss at the antenna and the RF connection must be minimized as much as possible. When defining a GPS receiver layout, the placement of the antenna with respect to the receiver, as well as grounding, shielding and jamming from other digital devices are crucial issues and need to be considered very carefully.

2.5.1 Footprint and paste mask

Figure 18 through Figure 23 describe the footprint and provide recommendations for the paste mask for LEA-5, NEO-5 and TIM-5H modules. These are recommendations only and not specifications. Note that the Copper and Solder masks have the same size and position.

To improve the wetting of the half vias, reduce the amount of solder paste under the module and increase the volume outside of the module by defining the dimensions of the paste mask to form a T-shape (or equivalent) extending beyond the Copper mask. The solder paste should have a total thickness of 170 to 200 µm.

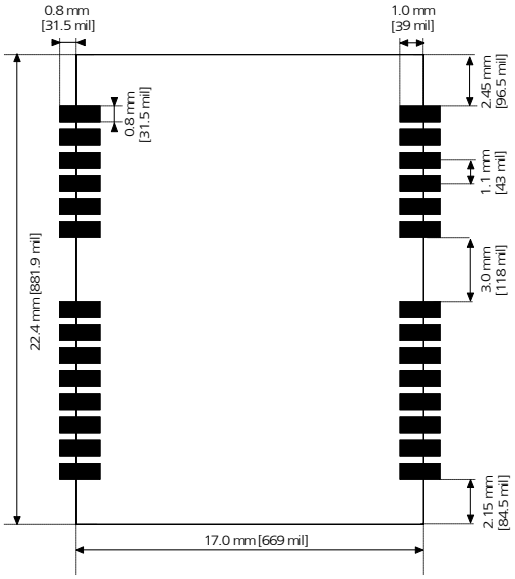


Figure 18: LEA-5 footprint

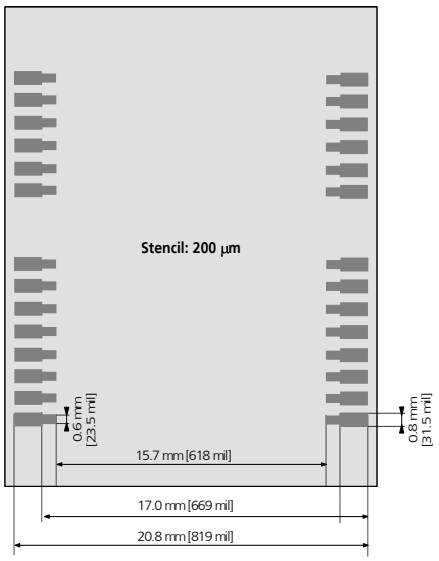


Figure 19: LEA-5 paste mask

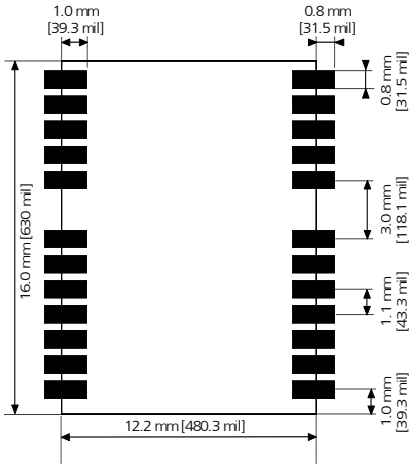


Figure 20: NEO-5 footprint

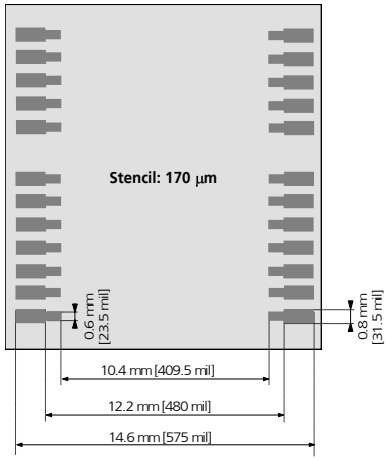


Figure 21: NEO-5 paste mask

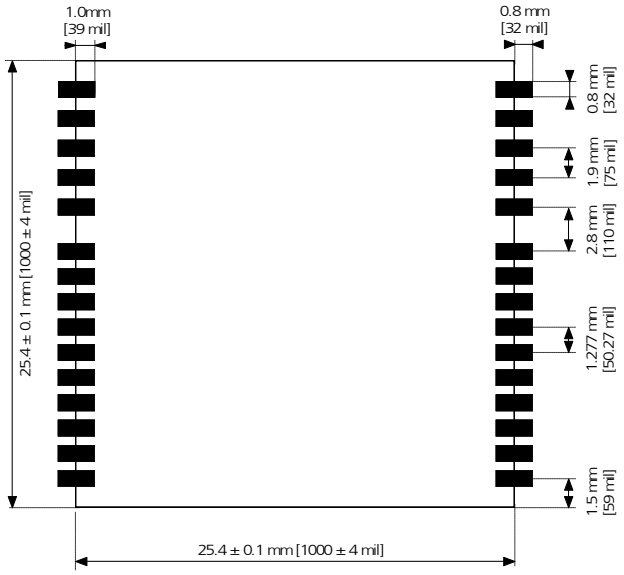


Figure 22: TIM-5H footprint

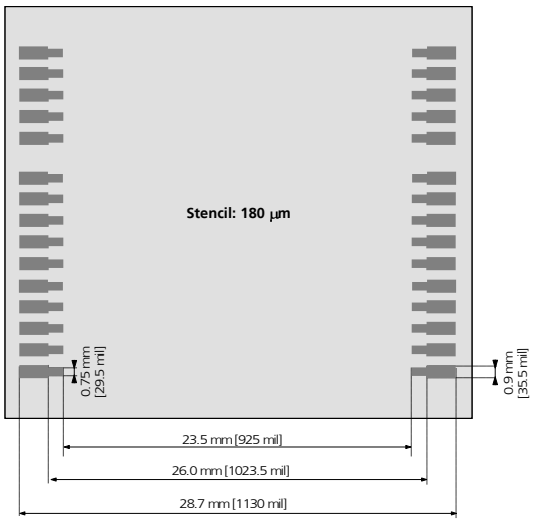


Figure 23: TIM-5H paste mask

The paste mask outline needs to be considered when defining the minimal distance to the next component.

The exact geometry, distances, stencil thicknesses and solder paste volumes must be adapted to the specific production processes (e.g. soldering etc.) of the customer.

2.5.2 Placement

A very important factor in achieving maximum performance is the placement of the receiver on the PCB. The connection to the antenna must be as short as possible to avoid jamming into the very sensitive RF section.

Make sure that RF critical circuits are clearly separated from any other digital circuits on the system board. To achieve this, position the receiver digital part towards your digital section of the system PCB. Care must also be exercised with placing the receiver in proximity to circuitry that can emit heat. The RF part of the receiver is very sensitive to temperature and sudden changes can have an adverse impact on performance.

The RF part of the receiver is a temperature sensitive component. Avoid high temperature drift and air vents near the receiver.

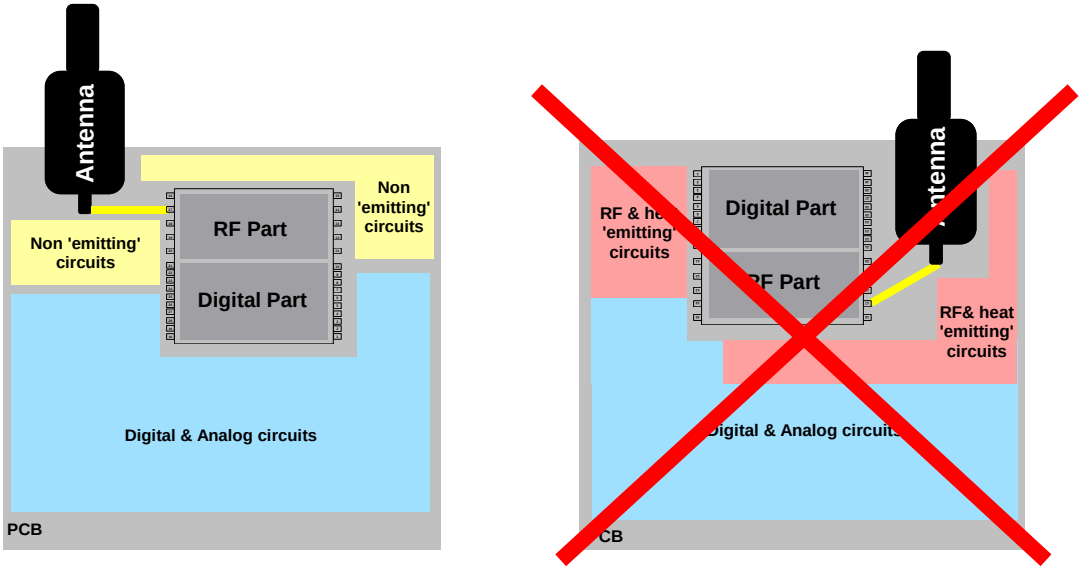


Figure 24: Placement (for exact pin orientation see data sheet)

2.5.3 Antenna connection and grounding plane design

u-blox 5 modules can be connected to passive patch or active antennas. The RF connection is on the PCB and connects the **RF_IN** pin with the antenna feed point or the signal pin of the connector, respectively. Figure 25 illustrates connection to a typical five-pin RF connector. One can see the improved shielding for digital lines as discussed in the GPS Antenna Application Note [6]. Depending on the actual size of the ground area, additional vias should be placed in the outer region. In particular, the edges of the ground area should be terminated with a dense line of vias.

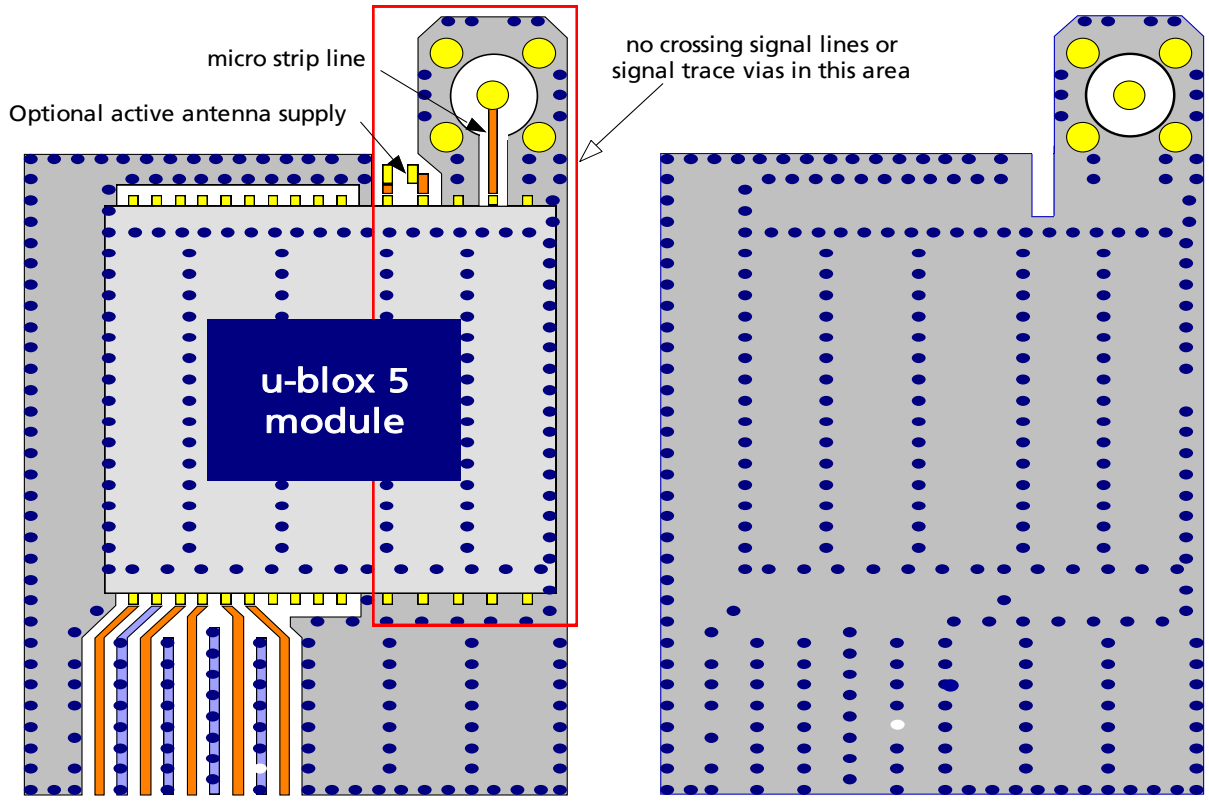


Figure 25: Recommended layout (for exact pin orientation see data sheet)

As seen in Figure 25, an isolated ground area is created around and below the RF connection. This part of the circuit MUST be kept as far from potential noise sources as possible. Make certain that no signal lines cross, and that no signal trace vias appear at the PCB surface within the area of the red rectangle. The ground plane should also be free of digital supply return currents in this area. On a multi layer board, the whole layer stack below the RF connection should be kept free of digital lines. This is because even solid ground planes provide only limited isolation.

The impedance of the antenna connection has to match the 50 Ohm impedance of the receiver. To achieve an impedance of 50 Ohms, the width W of the micro strip has to be chosen depending on the dielectric thickness H, the dielectric constant ε_r of the dielectric material of the PCB and on the build-up of the PCB (see Section 2.5.4). Figure 26 shows two different builds: A 2 Layer PCB and a 4 Layer PCB. The reference ground plane is in both designs on layer 2 (red). Therefore the effective thickness of the dielectric is different.

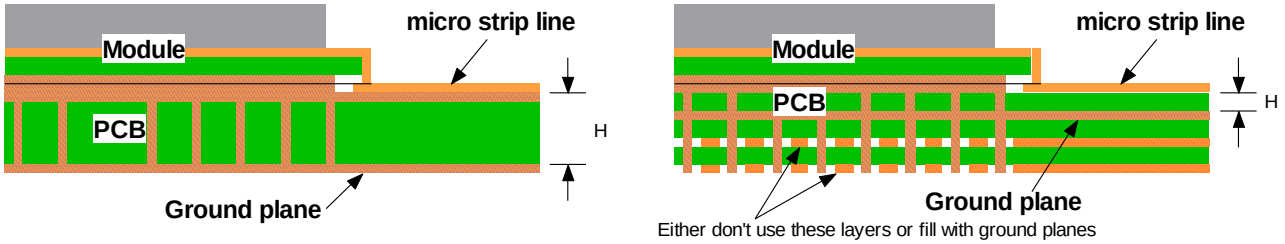


Figure 26: PCB build-up for micro strip line. Left: 2-layer PCB, right: 4-layer PCB

General design recommendations:

- The length of the micro strip line should be kept as short as possible. Lengths over 2.5 cm (1 inch) should be avoided on standard PCB material and without additional shielding.
- For multi layer boards the distance between micro strip line and ground area on the top layer should at least be as large as the dielectric thickness.
- Routing the RF connection close to digital sections of the design should be avoided.
- To reduce signal reflections, sharp angles in the routing of the micro strip line should be avoided. Chamfers or fillets are preferred for rectangular routing; 45-degree routing is preferred over Manhattan style 90-degree routing.

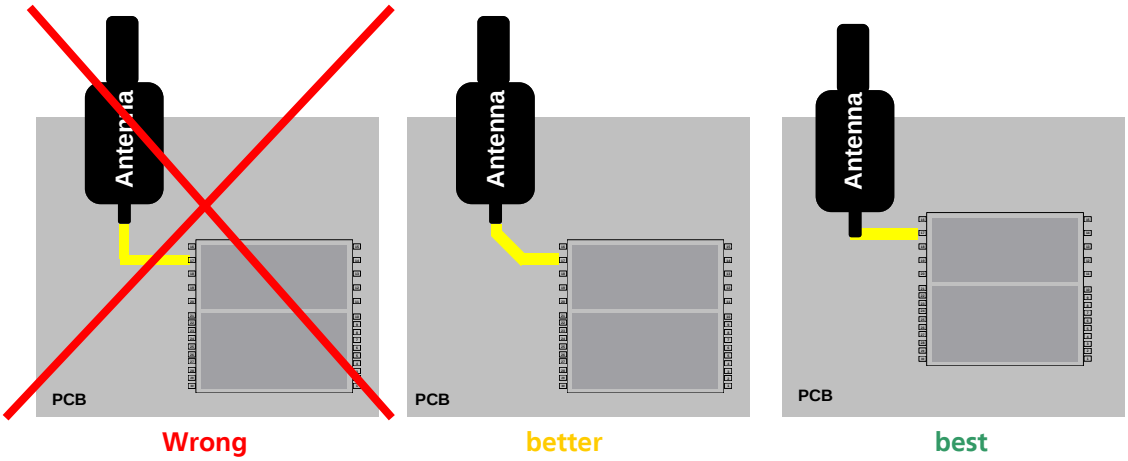


Figure 27: Recommended micro strip routing to RF pin (for exact pin orientation see data sheet)

- Do not route the RF-connection underneath the receiver. The distance of the micro strip line to the ground plane on the bottom side of the receiver is very small (some 100 µm) and has huge tolerances (up to 100%). Therefore, the impedance of this part of the trace cannot be controlled.
- Use as many vias as possible to connect the ground planes.
- In order to avoid reliability hazards, the area on the PCB under the receiver should be entirely covered with solder mask. Vias should not be open. Do not route under the receiver.

2.5.4 Antenna micro strip

There are many ways to design wave-guides on printed circuit boards. Common to all is that calculation of the electrical parameters is not straightforward. Freeware tools like AppCAD from Agilent or TXLine from Applied Wave Research, Inc. are of great help. They can be downloaded from www.agilent.com and www.mwoffice.com.

The micro strip is the most common configuration for printed circuit boards. The basic configuration is shown in Figure 28 and Figure 29. As a rule of thumb, for a FR-4 material the width of the conductor is roughly double the thickness of the dielectric to achieve 50 Ohms line impedance.

For the correct calculation of the micro strip impedance, one does not only need to consider the distance between the top and the first inner layer but also the distance between the micro strip and the adjacent GND plane on the same layer

☞ Use the Coplanar Waveguide model for the calculation of the micro strip.

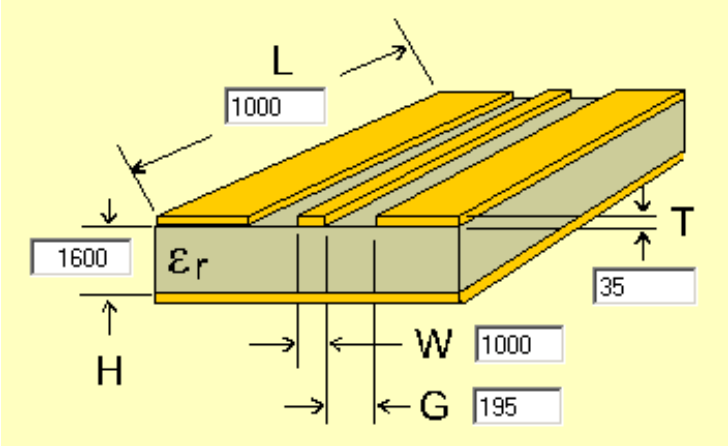


Figure 28: Micro strip on a 2-layer board (Agilent AppCAD Coplanar Waveguide)

Figure 28 shows an example of a 2-layer FR4 board with 1.6 mm thickness and a 35µm (1 ounce) copper cladding. The thickness of the micro strip is comprised of the cladding (35µm) plus the plated copper (typically 25µm). Figure 29 is an example of a multi layer FR4 board with 18µm (½ ounce) cladding and 180µ dielectric between layer 1 and 2.

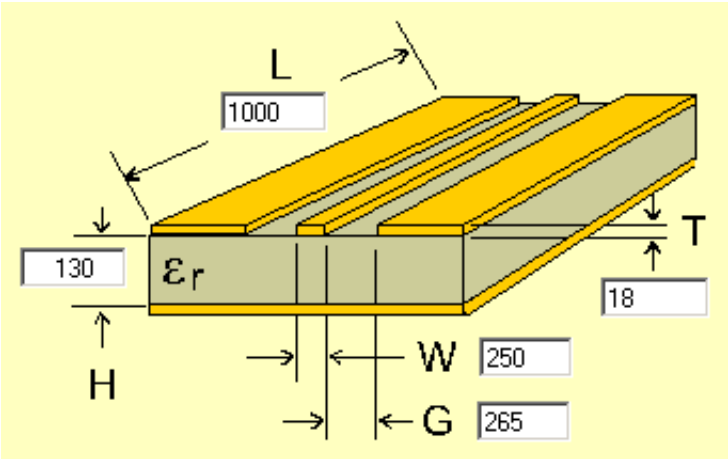


Figure 29: Micro strip on a multi layer board (Agilent AppCAD Coplanar Waveguide)

2.6 Antenna and antenna supervisor

u-blox 5 modules receive L1 band signals from GPS and GALILEO satellites at a nominal frequency of 1575.42 MHz. The RF signal is connected to the **RF_IN** pin.

u-blox 5 modules can be connected to passive or active antennas.

☞ For u-blox 5 receivers, the total preamplifier gain (minus cable and interconnect losses) must not exceed 50 dB. Total noise figure should be below 3 dB.

u-blox 5 Technology supports either a short circuit protection of the active antenna or an active antenna supervisor circuit (open and short circuit detection). For further information refer to Section 2.6.2).

2.6.1 Passive antenna

A design using a passive antenna requires more attention regarding the layout of the RF section. Typically a passive antenna is located near electronic components; therefore care should be taken to reduce electrical 'noise' that may interfere with the antenna performance. Passive antennas do not require a DC bias voltage and can be directly connected to the RF input pin **RF_IN**. Sometimes, they may also need a passive matching network to match the impedance to 50 Ohms.

Some passive antenna designs present a DC short to the RF input, when connected. If a system is designed with antenna bias supply AND there is a chance of a passive antenna being connected to the design, consider a short circuit protection.

All u-blox 5 receivers have a built-in LNA required for passive antennas.

Cosider optional ESD protection (see Section 2.7).

2.6.2 Active antenna (LEA-5H/5S/5A/5T, TIM-5H)

Active antennas have an integrated low-noise amplifier. They can be directly connected to **RF_IN**. If an active antenna is connected to **RF_IN**, the integrated low-noise amplifier of the antenna needs to be supplied with the correct voltage through pin **V_ANT**. Usually, the supply voltage is fed to the antenna through the coaxial RF cable. Active antennas require a power supply that will contribute to the total GPS system power consumption budget with additional 5 to 20 mA Typically. Inside the antenna, the DC component on the inner conductor will be separated from the RF signal and routed to the supply pin of the LNA (see Figure 30).

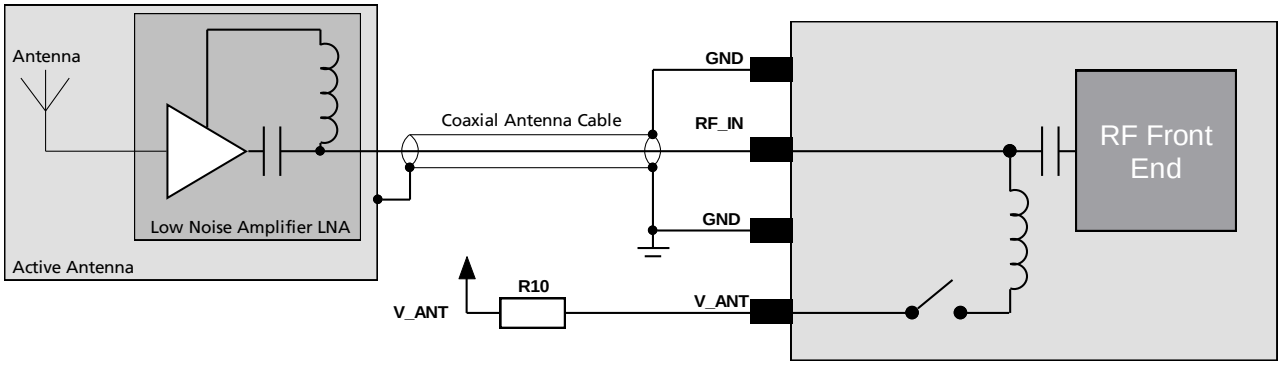


Figure 30: Active antenna biasing (for exact pin orientation see data sheet)

Generally an active antenna is easier to integrate into a system design, as it is less sensitive to jamming compared to a passive antenna. But an active antenna must also be placed far from any noise sources to have good performance.

Antennas should only be connected to the receiver when the receiver is not powered. Do not connect or disconnect the Antenna when the u-blox 5 receiver is running as the receiver calibrates the noise floor on power-up. Connecting the antenna after power-up can result in prolonged acquisition time.

Never feed supply voltage into RF_IN. Always feed via V_ANT.

☞ To test GPS signal reacquisition, it is recommended to physically block the signal to the antenna, rather than disconnecting and reconnecting the receiver.

2.6.3 Active antenna (LEA-5Q/5M, NEO-5)

LEA-5Q/5M and NEO-5 modules do not provide the antenna bias voltage for active antennas on the **RF_IN** pin. It is therefore necessary to provide this voltage outside the module via an inductor as indicated in Figure 31. u-Blox recommends using an inductor from Murata (LQG15HS27NJ02). Alternative parts can be used if the inductor's resonant frequency matches the GPS frequency of 1575.4MHz.

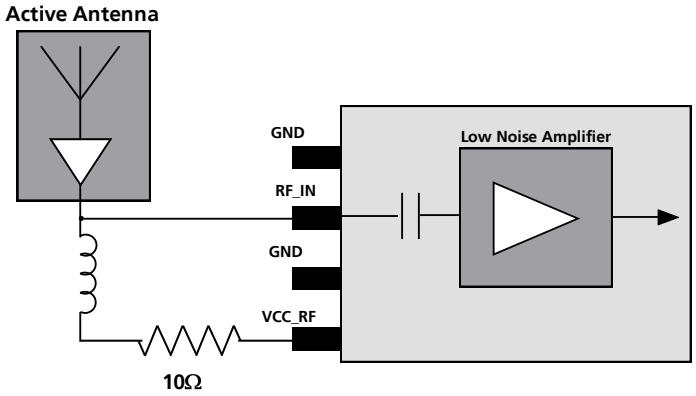


Figure 31: Recommended wiring for active antennas (for exact pin orientation see data sheet)

For optimal performance, it is important to place the inductor as close to the microstrip as possible. Figure 30 illustrates the recommended layout and how it should not be done.

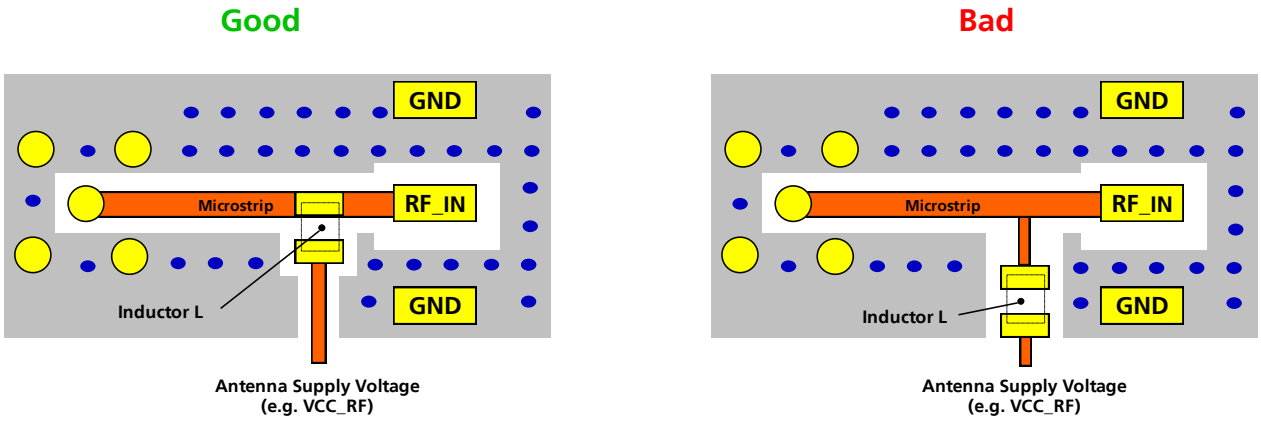


Figure 32: Recommended layout for connecting the antenna bias voltage for LEA-/5M and NEO-5

2.6.4 Active antenna bias power (LEA-5H/5S/5A/5T, TIM-5H)

There are two ways to supply the bias voltage to pin **V_ANT**. It can be supplied externally (please consider the datasheet specification) or internally. For Internal supply, the **VCC_RF** output must be connected to **V_ANT** to supply the antenna with a filtered supply voltage. However, the voltage specification of the antenna has to match the actual supply voltage of the u-blox 5 Receiver (e.g. 3.0 V).

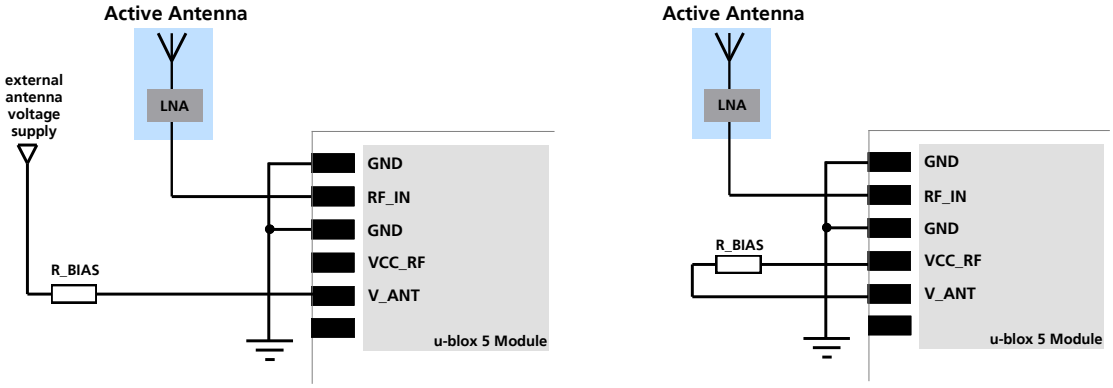


Figure 33: Supplying Antenna bias voltage (for exact pin orientation see data sheet)

Since the bias voltage is fed into the most sensitive part of the receiver, i.e. the RF input, this supply should be virtually free of noise. Usually, low frequency noise is less critical than digital noise with spurious frequencies with harmonics up to the GPS/GALILEO band of 1.575 GHz. Therefore, it is not recommended to use digital supply nets to feed pin **V_ANT**.

An internal switch (under control of the u-blox 5 software) can shut down the supply to the external antenna whenever it is not needed. This feature helps to reduce power consumption.

2.6.4.1 Short circuit protection

If a reasonably dimensioned series resistor **R_BIAS** is placed in front of pin **V_ANT**, a short circuit situation can be detected by the baseband processor. If such a situation is detected, the baseband processor will shut down supply to the antenna. The receiver is by default configured to attempt to reestablish antenna power supply periodically.

☞ To configure the antenna supervisor use the UBX-CFG-ANT message. For further information refer to the u-blox 5 Receiver Description including Protocol Specification [2].

References	Value	Tolerance	Description	Manufacturer
R_BIAS	10 Ω	± 10%	Resistor, min 0.250 W	

Table 8: Short circuit protection, bill of material

⚠ **Short circuits on the antenna input without limitation of the current can result in permanent damage to the receiver! Therefore, it's recommended to implement an R_BIAS in all risk applications, such as situations where the antenna can be disconnected by the end-user or that have long antenna cables.**

☞ An additional R_BIAS is not required when using a short and open active antenna supervisor circuitry as defined in Section 2.6.5.1, as the R_BIAS is equal to R2.

2.6.5 Active antenna supervisor (LEA-5H/5S/5A/5T, TIM-5H)

u-blox 5 Technology provides the means to implement an active antenna supervisor with a minimal number of parts. The antenna supervisor is highly configurable to suit various different applications.

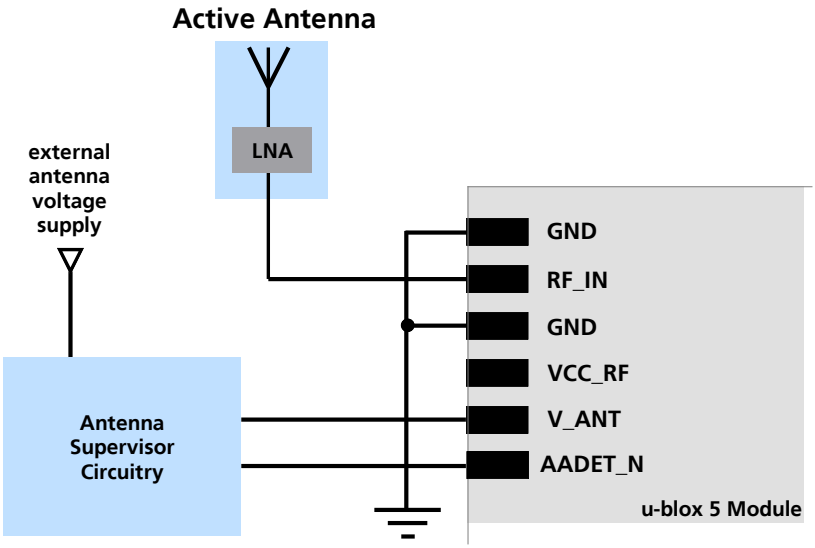


Figure 34: External antenna power supply with full antenna supervisor (for exact pin orientation see data sheet)

2.6.5.1 Short and open circuit active antenna supervisor

The Antenna Supervisor can be configured by a serial port message (using only UBX binary message). When enabled the active antenna supervisor produces serial port messages (status reporting in NMEA and/or UBX binary protocol) which indicates all changes of the antenna circuitry (**disabled** antenna supervisor, antenna circuitry **ok**, **short** circuit, **open** circuit) and shuts the antenna supply down if required.

The active antenna supervisor provides the means to check the active antenna for open and short circuits and to shut the antenna supply off, if a short circuit is detected. The state diagram in Figure 35 applies. If an antenna is connected, the initial state after power-up is "Active Antenna OK".

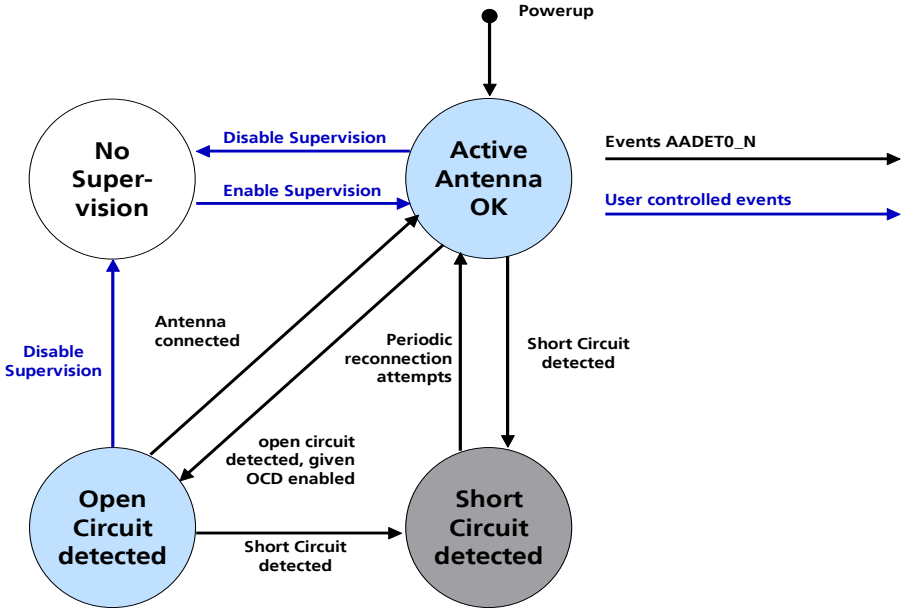


Figure 35: State diagram of active antenna supervisor

Firmware supports an active antenna supervisor circuit, which is connected to the pin **AADET_N**. An example of an open circuit detection circuit is shown in Figure 36 and Figure 37. High on **AADET_N** means that an external antenna is not connected.

Short Circuit Detection (SCD)

A short circuit in the active antenna pulls **V_ANT** to ground. This is detected inside the u-blox 5 module and the antenna supply voltage will be immediately shut down.

☞ Antenna short detection (SCD) and control is enabled by default.

Open Circuit Detection (OCD)

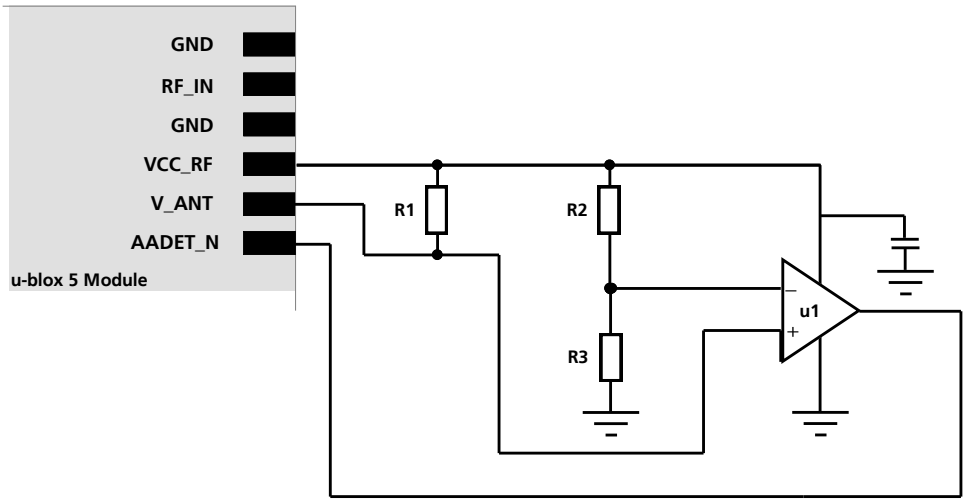


Figure 36: Schematic of open circuit detection variant A (for exact pin orientation see data sheet)

References	Value	Tolerance	Description	Remarks
R1	10 Ω	± 5%	Resistor, min 0.063 W	
R2	560 Ω	± 5%	Resistor	
R3	100 kΩ	± 5%	Resistor	
u1	LT6000		Rail to Rail Op Amp	

Table 9: Active antenna supervisor, bill of material

$$I = \frac{\left(\frac{R2}{R2+R3}\right)}{R1} \bullet Vcc\_RF$$

Equation 1: Calculation of threshold current for open circuit detection

☞ If the antenna supply voltage is not derived from Vcc_RF, do not exceed the maximum voltage rating of AADET_N.

The open circuit detection circuit uses the current flow to detect an open circuit in the antenna. The threshold current can be calculated using Equation 1.

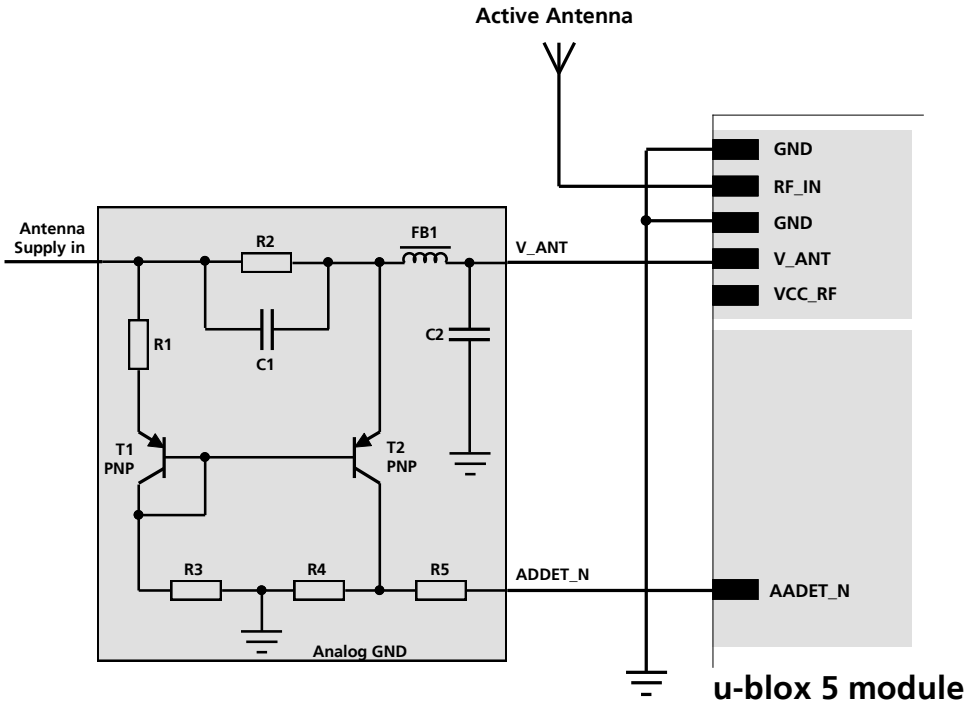


Figure 37: Schematic of open circuit detection variant B (for exact pin orientation see data sheet)

References	Value	Tolerance	Description	Remarks
C1	2.2 µF	± 10%	Capacitor, X7R, min 10 V	
C2	100 nF	± 10%	Capacitor, X7R, min 10 V	
FB1	600 Ω		Ferrite Bead	e.g. Murata BLM18HD601SN1
R1	15 Ω	± 10%	Resistor, min 0.063 W	
R2	10 Ω	± 10%	Resistor, min 0.250 W	
R3, R4	10 kΩ	± 10%	Resistor, min 0.063 W	
R5	33 kΩ	± 10%	Resistor, min 0.063 W	
T1, T2			PNP Transistor BC856B	e.g. Philips Semiconductors[12]

Table 10: Active antenna supervisor, bill of material

Status reporting

At startup and on every change of the antenna supervisor configuration the u-blox 5 GPS/GALILEO module will output a NMEA **($GPTXT**) or UBX (**INF-NOTICE**) message with the internal status of the antenna supervisor (disabled, short detection only, enabled).

None, one or several of the strings below are part of this message to inform about the status of the active antenna supervisor circuitry (e.g. "**ANTSUPERV= AC SD OD PdoS**").

[12] Transistors from other suppliers with comparable electrical characteristics may be used.

Abbreviation	Description
AC	Antenna Control (e.g. the antenna will be switched on/ off controlled by the GPS receiver)
SD	Short Circuit Detection Enabled
OD	Open Circuit Detection Enabled
PdoS	Power Down on short

Table 11: Active Antenna Supervisor Message on startup (UBX binary protocol)

☞ To activate the antenna supervisor use the **UBX-CFG-ANT** message. For further information refer to the u-blox 5 Receiver Description including Protocol Specification [2].

Similar to the antenna supervisor configuration, the status of the antenna supervisor will be reported in a NMEA (**$GPTXT**) or UBX (**INF-NOTICE**) message at start-up and on every change.

Message	Description
ANTSTATUS=DONTKNOW	Active antenna supervisor is not configured and deactivated.
ANTSTATUS=OK	Active antenna connected and powered
ANTSTATUS=SHORT	Antenna short
ANTSTATUS=OPEN	Antenna not connected or antenna defective

Table 12: Active antenna supervisor message on startup (NMEA protocol)

☞ The open circuit supervisor circuitry shown in Figure 37 has a quiescent current of approximately 2mA. This current can be reduced with an advanced circuitry such as shown in Figure 36.

2.7 EOS/ESD/EMI Precautions

When integrating GPS receivers into wireless systems, careful consideration must be given to electromagnetic and voltage susceptibility issues. Wireless systems include components which can produce Electrostatic Discharge (ESD), Electrical Overstress (EOS) and Electro-Magnetic Interference (EMI). CMOS devices are more sensitive to such influences because their failure mechanism is defined by the applied voltage, whereas bipolar semiconductors are more susceptible to thermal overstress. The following design guidelines are provided to help in designing robust yet cost effective solutions.

To avoid overstress damage during production or in the field it is essential to observe strict EOS/ESD/EMI handling and protection measures.

To prevent overstress damage at the RF_IN of your receiver, never exceed the maximum input power of –5dBm.

2.7.1 Abbreviations

Abbreviation	Definition
ANSI	American National Standards Institute
CDMA	Code Division Multiple Access
EMC	Electromagnetic compatibility
EMI	Electromagnetic interference
EOS	Electrical Overstress
EPA	Electrostatic Protective Area
ESD	Electrostatic discharge
GND	Ground
GPS	Global Positioning System
GSM	Global System for Mobile Communications
IEC	International Electrotechnical Commission
PCB	Printed circuit board

Table 13: Explanation of abbreviations used in this section

2.7.2 Electrostatic discharge (ESD)

Electrostatic discharge (ESD) is the sudden and momentary electric current that flows between two objects at different electrical potentials caused by direct contact or induced by an electrostatic field. The term is usually used in the electronics and other industries to describe momentary unwanted currents that may cause damage to electronic equipment.

2.7.3 ESD protection measures

GPS receivers are sensitive to Electrostatic Discharge (ESD). Special precautions are required when handling.

Most defects caused by ESD can be prevented by following strict ESD protection rules for production and handling. When implementing passive antenna patches or external antenna connection points, then additional ESD measures as shown in Figure 38 can also avoid failures in the field.

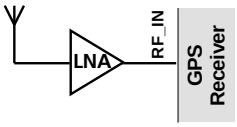
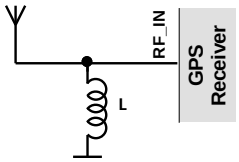
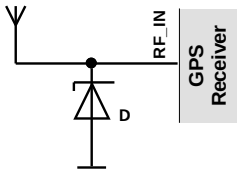
Small passive antennas (<2 dBic and performance critical)	**Passive antennas** (>2 dBic or performance sufficient)	**Active Antennas**
A  LNA with appropriate ESD rating	B 	C 

Figure 38: ESD Precautions

☞ Protection measure A is preferred due to performance and protection level considerations.

2.7.4 Electrical Overstress (EOS)

Electrical Overstress (EOS) usually describes situations when the maximum input power exceeds the maximum specified ratings. EOS failure can happen if RF emitters are close to a GPS receiver or its antenna. EOS causes damage to the chip structures.

If the RF_IN is damaged by EOS, it's hard to determine whether the chip structures have been damaged by ESD or EOS.

2.7.5 EOS protection measures

EOS protection measures as shown in Figure 39 are recommended for any designs combining wireless communication transceivers (e.g. GSM, GPRS) and GPS in the same design or in close proximity.

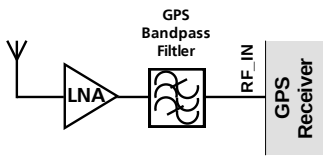
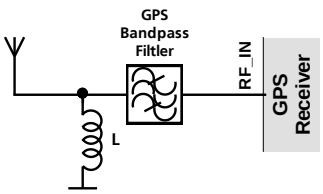
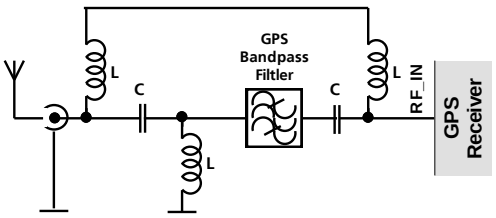
Small passive antennas (<2 dBic and performance critical)	**Passive antennas** (>2 dBic or performance sufficient)	**Active Antennas** (without internal filter which need the module antenna supervisor circuits)
D  LNA with appropriate ESD rating and maximum input power	E  GPS Bandpass Filter: SAW or Ceramic with low insertion loss and appropriate ESD rating	F 

Figure 39: EOS and ESD Precautions

2.7.6 Electromagnetic interference (EMI)

Electromagnetic interference (EMI) is the addition or coupling of energy released from any RF emitting device. This can cause a spontaneous reset of the GPS receiver or result in unstable performance. Any unshielded line or

segment (>3mm) connected to the GPS receiver can effectively act as antenna and lead to EMI disturbances or damage.

The following elements are critical regarding EMI:

- Unshielded connectors (e.g. pin rows etc.)
- Weakly shielded lines on PCB (e.g. on top or bottom layer and especially at the border of a PCB)
- Weak GND concept (e.g. small and/or long ground line connections)

EMI protection measures are recommended when RF emitting devices are near the GPS receiver. To minimize the effect of EMI a robust grounding concept is essential. To achieve electromagnetic robustness follow the standard EMI suppression techniques.

http://www.murata.com/products/emc/knowhow/index.html

http://www.murata.com/products/emc/knowhow/pdf/4to5e.pdf

Improved EMI protection can be achieved by inserting a resistor or better yet a ferrite bead (BLM15HD102SN1) into any unshielded PCB lines connected to the GPS receiver. Place the resistor as close as possible to the GPS receiver pin.

Example of EMI protection measures on the RX/TX line using a ferrite bead:

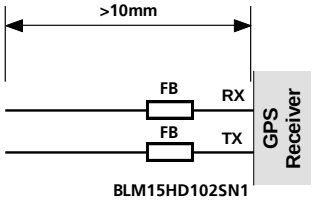


Figure 40: EMI Precautions

VCC can be protected using a feed thru capacitor. For electromagnetic compatibility (EMC) of the RF_IN pin refer to section 2.7.5

2.7.7 GSM applications

GSM uses power levels up to 2W (+33dBm). The absolute maximum power input at the GPS receiver is **-5dBm** for Antaris-4 and u-blox 5 GPS receivers.

2.7.7.1 Isolation between GPS and GSM antenna

For GSM applications plan a minimum isolation of 40dB. In a handheld type design an isolation of approximately 20dB Can be reached with careful placement of the antennas, but this isn't sufficient. In such applications an additional input filter is needed on the GPS side to block the high energy emitted by the GSM transmitter. Examples of these kinds of filters would be the SAW Filters from Epcos (B9444 or B7839) or Murata.

2.7.7.2 Increasing jamming immunity

Jamming signals come from in-band and out-band frequency sources.

2.7.7.3 In-band jamming

With in-band jamming the signal frequency is very close to the GPS frequency of 1575 MHz (see Figure 41). Such jamming signals are typically caused by harmonics from displays, micro-controller, bus systems, etc.

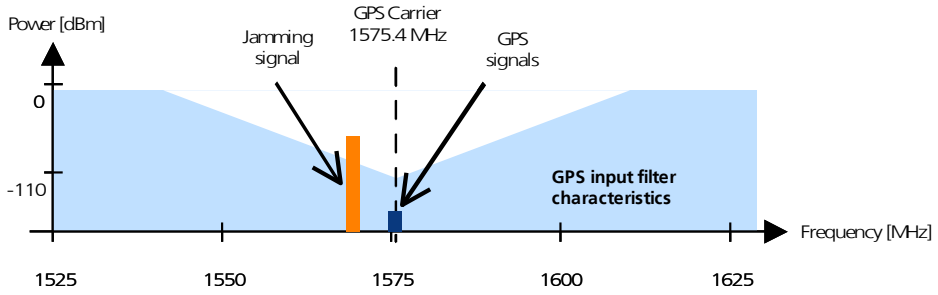


Figure 41: In-band jamming signals

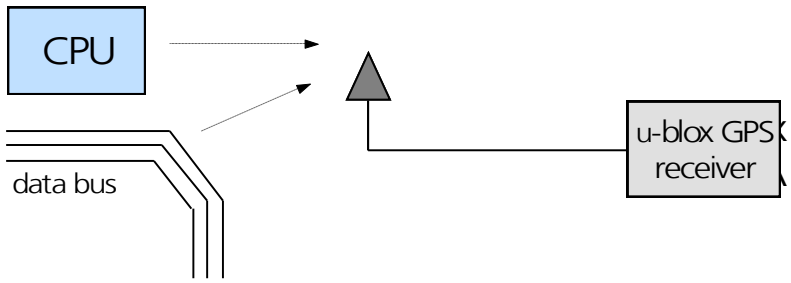


Figure 42: In-band jamming sources

Measures against in-band jamming include:

- Maintaining a good grounding concept in the design
- Shielding
- Layout op emperature iltering
- Placement of the GPS antenna
- Adding a CDMA, GSM, WCDMA bandbass filter before handset antenna

2.7.7.4 Out-band jamming

Out-band jamming is caused by signal frequencies that are different from the GPS carrier (see Figure 43). The main sources are wireless communication systems such as GSM, CDMA, WCDMA, WiFi, BT, etc..

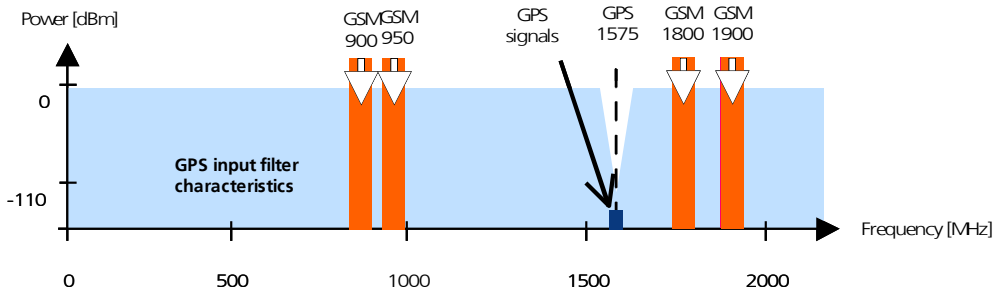


Figure 43: Out-band jamming signals

Measures against out-band jamming include maintaining a good grounding concept in the design and adding a SAW or bandpass ceramic filter (as recommend in Section 2.7.5) into the antenna input line to the GPS receiver (see Figure 44).

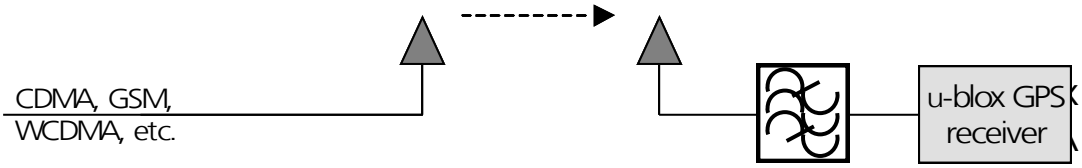


Figure 44: Measures against out-band jamming

2.7.8 Recommended parts

	Manufacturer	Part ID	Remarks	Parameters to consider
Diode	ON Semiconductor	ESD9R3.3ST5G ESD9L3.3ST5G ESD9L5.0ST5G	(2.7.3 C) Standoff Voltage>3.3V (2.7.3 C) Standoff Voltage>3.3V (2.7.3 C) Standoff Voltage>5V	• Low Capacitance < 0.5pF • Standoff Voltage > Voltage for active antenna • Low Inductance
SAW	Epcos	**B9444**: B39162-B9444-M410 **B7839**: B39162-B7839-K410	(2.7.5) 15dBm Max Power Input (2.7.5) 25dBm Max Power Input	
	Murata	SAFEA1G57KD0F00 SAFSE1G57KA0T90	(2.7.5) 1.35x1.05x0.5 mm (2.7.5) 2.5x2.0x1.0 mm	• Low-loss RF filter for GPS • Unbalanced to unbalanced operation • Insertion Loss • Bandwith and BW over te emperature• Electrostatic Sensitive Device (ESD MM)
	CTS	CER0032A	(2.7.5) 4.2x4.0x2.0 mm > 8kV eSD HBM	
LNA	Avago	ALM-1106 ALM-1412 ALM-1712 ALM-2412	(2.7.3 A) LNA (2.7.5 D) LNA + FBAR Filter (2.7.5 D) Filter + LNA + FBAR Filter (2.7.3 A) LNA + FBAR Filter	pHemt (GaAS)
	MAXIM	MAX2659ELT+	(2.7.3 A) LNA	SiGe
Inductor	Murata	LQG15HS27NJ02		Impedance @ freq GPS > 500 Ohm
Capacitor	Murata	GRM1555C1E470JZ01	(2.7.5 F) C, 47p	
Ferrite Bead	Murata	BLM15HD102SN1	(2.7.5 F) FB	High IZI @ fGsm
Feed thru Capacitor for Signal	Murata	NFL18SP157X1A3 NFA18SL307V1A45	Monolithic Type Array Type	Load Capacitance appropriate to Baude rate CL < xxx pF
Feed thru Capacitor for VCC	Murata	NFM18PC …. NFM21P….	0603 2A 0805 4A	Rs < 0.5 Ohm

Table 14: Recommended parts for ESD/EOS protection

3 Handling and soldering

3.1 Packaging, shipping, storage and moisture preconditioning

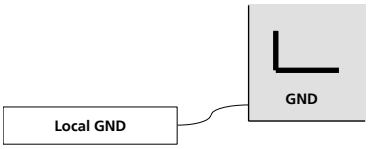
For information pertaining to reels and tapes, Moisture Sensitivity levels (MSD), shipment and storage information, as well as drying for preconditioning see the data sheet of the specific u-blox 5 GPS module.

3.2 ESD handling precautions

ESD prevention is based on establishing an Electrostatic Protective Area (EPA). The EPA can be a small working station or a large manufacturing area. The main principle of an EPA is that there are no highly charging materials in the vicinity of ESD sensitive electronics, all conductive materials are grounded, workers are grounded, and charge build-up on ESD sensitive electronics is prevented. International standards are used to define typical EPA and can be obtained for example from International Electrotechnical Commission (IEC) or American National Standards Institute (ANSI).

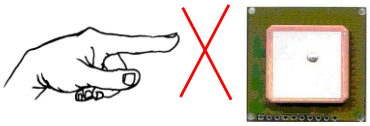
GPS receivers are sensitive to ESD and require special precautions when handling. Particular care must be exercised when handling patch antennas, due to the risk of electrostatic charges. In addition to standard ESD safety practices, the following measures should be taken into account whenever handling the receiver.

- Unless there is a galvanic coupling between the local GND (i.e. the work table) and the PCB GND, then the first point of contact when handling the PCB shall always be between the local GND and PCB GND.
- Before mounting an antenna patch, connect ground of the device.

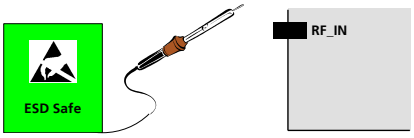


- When handling the RF pin, do not come into contact with any charged capacitors and be careful when contacting materials that can develop charges (e.g. patch antenna ~10pF, coax cable ~50-80pF/M, soldering iron, …)

- To prevent electrostatic discharge through the RF input, do not touch the mounted patch antenna.



- When soldering RF connectors and patch antennas to the receiver's RF pin, make sure to use an ESD safe soldering iron (tip).



Failure to observe these precautions can result in severe damage to the GPS receiver!

3.3 Soldering

3.3.1 Soldering paste

Use of "N" Clean" "oldering paste is strongly recommended, as it does not require cleaning after the soldering process has taken place. The paste listed in the example below meets these criteria.

Soldering Paste:	LFSOLDER TLF-206-93F (Tamura Kaken (UK) Ltd.)
Alloy specification:	Sn 95.5/ Ag 3.9/ Cu 0.6 (95.5% Tin/ 0.6 % Silver/ 0.6% Copper)
Melting Temperature:	216 - –21°C
Stencil Thickness:	150 µm for base boards

The final choice of the soldering paste depends on the approved manufacturing procedures.

The paste-mask geometry for applying soldering paste should meet the recommendations in section 2.5.1.

☞ The quality of the solder joints on the connectors ('half vias') should meet the appropriate IPC specification.

3.3.2 Reflow soldering

A convection type-soldering oven is strongly recommended over the infrared type radiation oven. Convection heated ovens allow precise control of the temperature and all parts will be heated up evenly, regardless of material properties, thickness of components and surface color.

Consider the "I"C-7530 Guidelines for temperature profiling for mass soldering (reflow and wave) processes, published 2001"."Preheat phase

Initial heating of component leads and balls. Residual humidity will be dried out. Please note that this preheat phase will not replace prior baking procedures.

- Temperature rise rate: 1 - –°C/s — If the temperature rise is too rapid in the preheat phase it may cause excessive slumping.
- Time: 60 – 120 seconds — If the preheat is insufficient, rather large solder balls tend to be generated. Conversely, if performed excessively, fine balls and large balls will be generated in clusters.
- End Temperature: 150 - –00°C — If the temperature is too low, non-melting tends to be caused in areas containing large heat capacity.

Heating/ Reflow phase

The temperature rises above the liquidus temperature of 216 - –21°C. Avoid a sudden rise in temperature as the slump of the paste could become worse.

- Limit time above 220°C liquidus temperature: 20 - –0s
- Peak reflow temperature: 230 - –50°C

Cooling phase

A controlled cooling avoids negative metallurgical effects (solder becomes more brittle) of the solder and possible mechanical tensions in the products. Controlled cooling helps to achieve bright solder fillets with a good shape and low contact angle.

- Temperature fall rate: max 3°C / s

☞ To avoid falling off, the u-blox 5 GPS module should be placed on the topside of the motherboard during soldering.

The final soldering temperature chosen at the factory depends on additional external factors like choice of soldering paste, size, thickness and properties of the base board, etc. Exceeding the maximum soldering temperature in the recommended soldering profile may permanently damage the module.

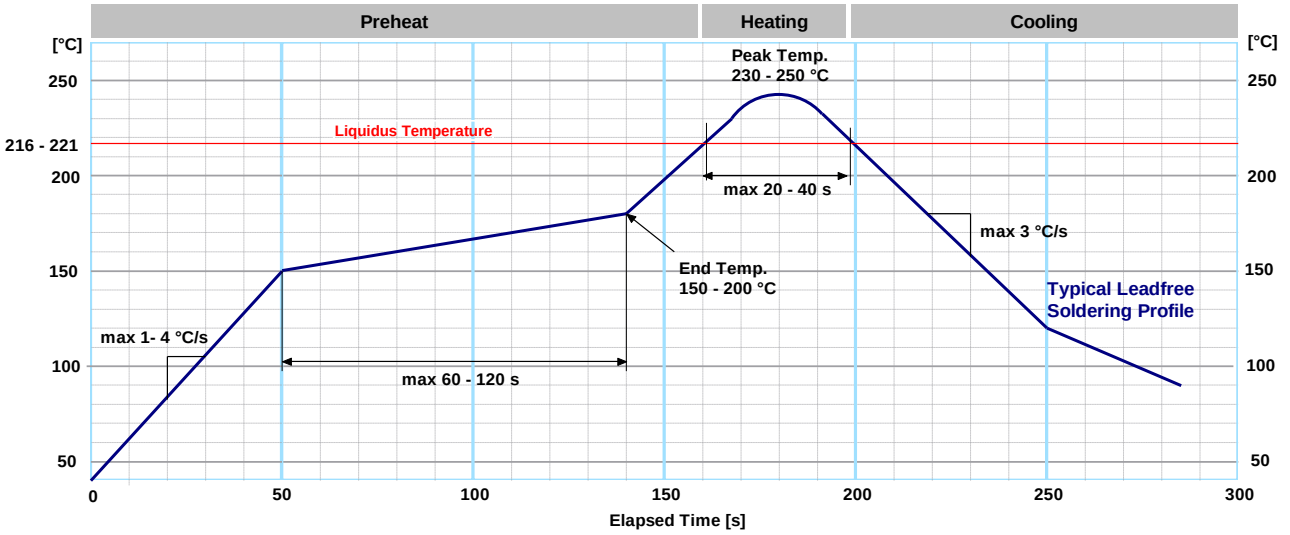


Figure 45: Recommended soldering profile

When soldering u-blox 5 modules in a leaded process, check the following temperatures:

- PB- Technology Soaktime: 40-80sec
- Time above Liquidus: 40-90 sec
- Peak temperature: 225-235 °C

u-blox 5 modules **must not** be soldered with a damp heat process.

3.3.3 Optical inspection

After soldering the u-blox 5 module, consider an optical inspection step to check whether:

- The module is properly aligned and centered over the pads
- All pads are properly soldered
- No excess solder has created contacts to neighboring pads, or possibly to pad stacks and vias nearby.

3.3.4 Cleaning

In general, cleaning the populated modules is strongly discouraged. Residues underneath the modules cannot be easily removed with a washing process.

- Cleaning with water will lead to capillary effects where water is absorbed in the gap between the baseboard and the module. The combination of residues of soldering flux and encapsulated water leads to short circuits or resistor-like interconnections between neighboring pads.
- Cleaning with alcohol or other organic solvents can result in soldering flux residues flooding into the two housings, areas that are not accessible for post-wash inspections. The solvent will also damage the sticker and the ink-jet printed text.
- Ultrasonic cleaning will permanently damage the module, in particular the quartz oscillators.

The best approach is to use a "n" clean" "oldering paste and eliminate the cleaning step after the soldering.

3.3.5 Repeated reflow soldering

Only single reflow soldering processes are recommended for boards populated with u-blox 5 modules. The reason for this is the risk of the module falling off due to high weight in relation to the adhesive properties of the solder. This also applies to soldering processes with the module upside down.

☞ Repeated reflow soldering processes and soldering the module upside down are not recommended.

3.3.6 Wave soldering

Base boards with combined through-hole technology (THT) components and surface-mount technology (SMT) devices require wave soldering to solder the THT components. Only a single wave soldering process is encouraged for boards populated with u-blox 5 modules.

3.3.7 Hand soldering

Hand soldering is allowed. Use a soldering iron temperature setting of "7" "hich is equivalent to 350°C and carry out the hand soldering according to the IPC recommendations / reference documents IPC7711. Place the module precisely on the pads. Start with a cross-diagonal fixture soldering (e.g. pins 1 and 15), and then continue from left to right.

3.3.8 Rework

The u-blox 5 module can be unsoldered from the baseboard using a hot air gun.

⚠ **Attention: use of a hot air gun can lead to overheating and severely damage the module. Always avoid overheating the module.**

After the module is removed, clean the pads before placing and hand-soldering a new module.

⚠ **Never attempt a rework on the module itself, e.g. replacing individual components. Such actions immediately terminate the warranty.**

3.3.9 Conformal coating

Certain applications employ a conformal coating of the PCB using HumiSeal® or other related coating products.

These materials affect the HF properties of the GPS module and it is important to prevent them from flowing into the module.

The RF shields do not provide 100% protection for the module from coating liquids with low viscosity, therefore care is required in applying the coating.

☞ Conformal Coating of the module will void the warranty.

3.3.10 Casting

If casting is required, use viscose or another type of silicon pottant. The OEM is strongly advised to qualify such processes in combination with the u-blox 5 module before implementing this in the production.

☞ Casting will void the warranty.

3.3.11 Grounding metal covers

Attempts to improve grounding by soldering ground cables, wick or other forms of metal strips directly onto the EMI covers is done at the customer's'own risk. The numerous ground pins should be sufficient to provide optimum immunity to interferences and noise.

☞ u-blox makes no warranty for damages to the u-blox 5 module caused by soldering metal cables or any other forms of metal strips directly onto the EMI covers.

3.3.12 Use of ultrasonic processes

Some components on the u-blox 5 module are sensitive to Ultrasonic Waves. Use of any Ultrasonic Processes (cleaning, welding etc.) may cause damage to the GPS Receiver.

☞ u-blox offers no warranty against damages to the u-blox 5 module caused by any Ultrasonic Processes.

4 Product testing

4.1 u-blox in-series production test

u-blox focuses on high quality for its products. To achieve a high standard it's our philosophy to supply fully tested units. Therefore at the end of the production process, every unit is tested. Defective units are analyzed in detail to improve the production quality.

This is achieved with automatic test equipment, which delivers a detailed test report for each unit. The following measurements are done:

- Digital self-test (Software Download, verification of FLASH firmware, etc.)
- Measurement of voltages and currents
- Measurement of RF characteristics (e.g. C/No)

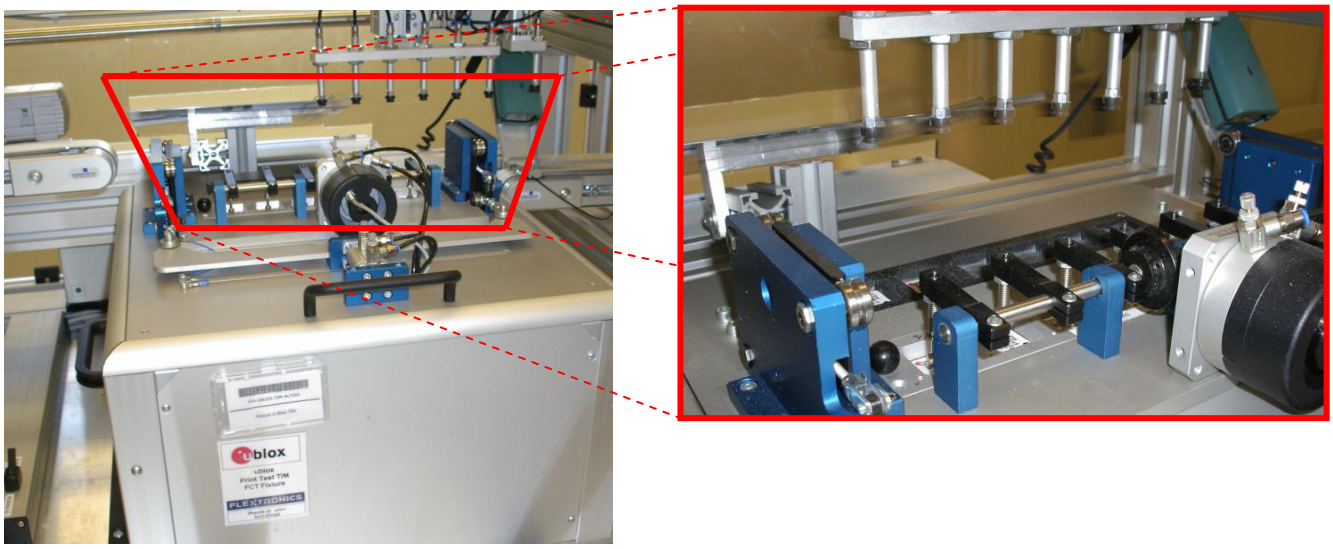


Figure 46: Automatic Test Equipment for Module Tests

4.2 Test parameters for OEM manufacturer

Because of the testing done by u-blox (with 100% coverage), it is obvious that an OEM manufacturer doesn't need to repeat firmware tests or measurements of the GPS parameters/characteristics (e.g. TTFF) in their production test.

An OEM manufacturer should focus on:

- Overall sensitivity of the device (including antenna, if applicable)
- Communication to a host controller

4.3 System sensitivity test

The best way to test the sensitivity of a GPS device is with the use of a 1-channel GPS simulator. It assures reliable and constant signals at every measurement.

Figure 47: 1-channel GPS simulator

u-blox recommends the following Single-Channel GPS Simulator:

- Spirent GSS6100
  Spirent Communications Positioning Technology
  (previously GSS Global Simulation Systems) www.positioningtechnology.co.uk

4.3.1 Guidelines for sensitivity tests

1. Connect a 1-channel GPS simulator to the OEM product
2. Choose the power level in a way that the "Golden Device" would report a C/No ratio of 38-40 dBHz
3. Power up the DUT (Device Under Test) and allow enough time for the acquisition
4. Read the C/No value from the NMEA GSV or the UBX-NAV-SVINFO message (e.g. with u-center)
5. Compare the results to a "Golden Device" or a u-blox 5 Evaluation Kit.

4.3.2 'Go/No go' tests for integrated devices

The best test is to bring the device to an outdoor position **with excellent sky view** (HDOP < 3.0). Let the receiver acquire satellites and compare the signal strength with a "Golden Device".

☞ As the electro-magnetic field of a redistribution antenna is not homogenous, indoor tests are in most cases not reliable. These kind of tests may be useful as a 'go/no go' test but not for sensitivity measurements.

Appendix

A Migration to u-blox 5 receivers

Migrating ANTARIS®4 to a u-blox 5 receiver module is a fairly straightforward procedure. Nevertheless there are some points to be considered during the migration.

☞ Not all of the functionalities available with ANTARIS®4 are supported by u-blox 5. These include:

- RTCM
- UTM

A.1 Checklist for migration

Have you chosen the optimal module?

- ❑ Although all u-blox 5 receivers outperform ANTARIS 4 acquisition (i.e. better sensitivity level and acquisition time) select a TIM-5H, LEA-5H, LEA-5S, LEA-5Q, NEO-5Q or NEO-5G for the advantage of KickStart performance.
- ❑ If KickStart performance is not required, choose a LEA-5A or LEA-5M, NEO-5M or NEO-5D.
- ❑ Further information on KickStart can be found under: http://www.u-blox.ch/en/kickstart.html.
- ❑ For active antenna applications, choose a TIM-5H, LEA-5H, LEA-5S or LEA-5A, since an antenna supply circuit is already built in.
- ❑ For the ability to upgrade the firmware or to permanently save configuration, choose a TIM-5H or LEA-5H.
- ❑ For USB select a LEA-5 or NEO-5.
- ❑ For precision timing choose a LEA-5T

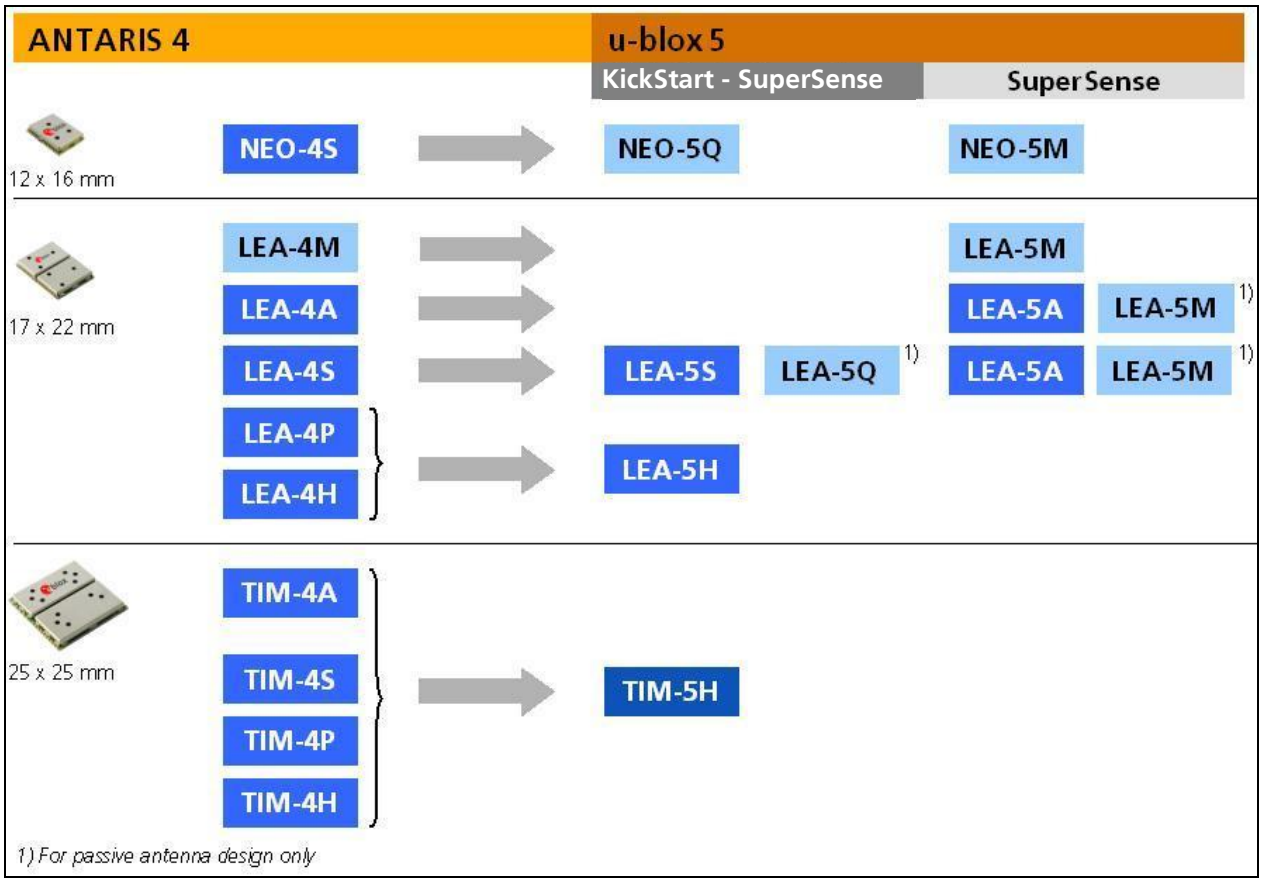


Figure 48: u-blox5 module migration made easy

Check u-blox 5 Hardware Requirements:

- ❑ Check the battery power to supply the battery backup pin, since u-blox5 draws higher current in comparison to ANTARIS 4 receivers.
- ❑ Compare the u-blox 5 module peak current consumption (150 mA) with the specification of the power supply.
- ❑ u-blox 5 modules can be operated in two different power modes: Max. Performance or Eco mode. Select Eco mode for reduced current consumption. For FW 6.00 and additional Power Save mode is available.
- ❑ u-blox5 modules with KickStart (LEA-5**S**, LEA-5**H**, LEA-5**T**, LEA-5**Q,** NEO-5**G,** NEO-5**Q** and TIM-5**H**) operate in Max. Performance mode by default. Standard u-blox5 modules (NEO-5**D,** NEO-5**M,** LEA-5**A** and LEA-5**M**) are set to Eco mode by default.
- ❑ NEO-5**G**, NEO-5**Q** and LEA-5**Q** also feature a Configuration Pin to switch between the power modes.
- ❑ For more information on u-blox5 Power supply specifications and power modes, check our latest LEA-5 Data Sheet [1], NEO-5 Data Sheet [2] and TIM-5 Data Sheet [3].
- ❑ If you use an active antenna supervisor circuitry to detect open conditions, you need to verify resistor reference recommendations in our integration manuals.
- ❑ See chapter 2.7 EOS/ESD/EMI Precautions.
- ❑ No need to power Vbat before power-up.

Check u-blox 5 Software Requirements:

- ❑ Not all of the functionalities available with ANTARIS 4 are supported by u-blox 5 Firmware version 4.00, 4.01 or 5.00. These include:

- FixNow Mode: Low power modes are supported with FW 6.00 or ROM 6.00. For migration of FXN functionalities consult the u-blox 5 Firmware Version 6.00 Release Note [5].
- No UTM (Universal Transverse Mercator Projection).
- No RTCM protocol for DGPS support.
- Raw Data support with LEA-5**T** only supported with FW 6.00 and above.

❑ For more information on u-blox5 firmware version 4.00 or later, refer to: http://www.u-blox.com/customersupport/ublox5_fw.html

❑ Check A.2 Software migration

A.2 Software migration

Software migration from ANTARIS 4 to a u-blox5 GPS receiver is a straightforward procedure. Nevertheless there are some differences to be considered with u-blox5 firmware version 5.00. Like its ANTARIS 4 predecessor, u-blox 5 technology supports UBX and NMEA protocol messages. Backward compatibility has been maintained as far as possible. New messages have been introduced for new functions. Only minor differences have to be expected in the UBX-NAV and UBX-AID classes of the UBX protocol and for the standard NMEA messages such as **GGA, GLL, GSA, GSV, RMC, VTG** and **ZDA**.

ANTARIS 4	u-blox5	Remarks
UBX-CFG-NAV2	UBX-CFG-NAV5	UBX-CFG-NAV2 has been replaced by UBX-CFG-NAV5. The new message has additional features. The default dynamic platform is "Portable". This platform is rather generic and allows the receiver to be operated in a wide dynamic range covering pedestrians, cars as well as commercial aircrafts. Automotive applications such as first-mount navigation systems may better utilize the "Automotive" platform, which is better geared to the dynamics of land vehicles but is only of limited use in airborne and high-dynamics environments. UBX-CFG-NAV5 does not support following features: Almanac Navigation Navigation Input filters UBX-CFG-NAV5 has a message length of 36 Bytes (40 Bytes for UBX-CFG-NAV2) UBX-CFG-NAV5 FixMode is set by default to "Auto 3D/2D" as for ANTARIS4. Check the u-blox 5 Receiver Description including Protocol Specification [4] if this mode needs to be changed.
UBX-CFG-MSG	UBX-CFG-MSG	No support for multiple configurations in one UBX-CFG-MSG command
UBX-CFG-RXM	N/A	Contrary to ANTARIS 4, u-blox5 does not need selecting GPS acquisition sensitivity mode (Fast, Normal, High Sens and Auto mode) since the acquisition engine is powerful enough to search all satellite in one go. FixNow mode is not available anymore. Low power modes are planned for Q1/09. Contact your local u-blox support team should you need further information.
PUBX,01	N/A	Other UBX or NMEA messages can be used to replace this message
UBX-NAV-POSUTM	N/A	
UBX-CFG-TP	UBX-CFG-TP	u-blox 5 offers the possibility to activate Timepulse signal without GPS fix.
UBX-CFG-ANT	UBX-CFG-ANT	Antenna Open Circuit Detection: The default setting for LEA-4S and LEA-4A was "enabled". With all LEA-5 modules the default setting is "disabled". Automatic Short Circuit Recovery: With ANTARIS 4 this was "disabled" by default. With u-blox 5 the default setting is "enabled".
UBX-CFG-RATE	UBX-CFG- RATE	Set to 1 with u-blox 5
UBX-CFG-TMODE	UBX-CFG-TMODE	With u-blox 5 FW 6.00 and above it is no longer necessary to configure the number of satellites in UBX-CFG-NAV to 1 to enable the timing mode. This is performed automatically.
UBX-MON-HW	UBX-MON-HW	Message length has changed as the number of pins is different with u-blox5.

ANTARIS 4	u-blox5	Remarks
0s Leap second by default	FW 5.00: 14 s Leap second by default FW 6.00: 15 s Leap second by default	
UBX-CFG-RATE	UBX-CFG-RATE	Disable SBAS services to achieve 4Hz navigation
UBX-CFG-PRT	UBX-CFG-PRT	With firmware V5.00, no acknowledge (ACK) is returned for the UBX-CFG-PRT message if the port that is being reconfigured is the same as the port being communicated over. This is true even in the event of a successful reception of this message.

Table 15: Main differences between ANTARIS 4 and u-blox 5 software for migration

The default NMEA message set for u-blox 5 is **GGA, GLL, GSA, GSV, RMC** and **VTG**. Contrary to ANTARIS 4, **ZDA** is disabled by default.

Firmware update is supported by all of these interfaces. The firmware update mechanism of u-blox 5 is more sophisticated than with ANTARIS 4. It is now based on UBX protocol messages. Customers, who implemented firmware download in their application processor, will need to replace the software. A template is available from your u-blox support team.

Please refer to the u-blox 5 Receiver Description including Protocol Specification [4] for more information. This document is available on the ublox website.

A.3 Hardware Migration

u-blox 5 modules have been designed with backward compatibility in mind but some minor differences were unavoidable. These minor differences will however not be relevant for the majority of the LEA-4 and TIM-4 designs.

Good performance requires a clean and stable power supply with minimal ripple. Care needs to be exercised in selecting a strategy to achieve this. Avoid placing any resistance on the Vcc line. For better performance, use an LDO to provide a clean supply at Vcc and consider the following:

- Wide power lines or even power planes are preferred.
- Place LDO near the module.
- Avoid resistive components in the power line (e.g. narrow power lines, coils, resistors, etc.).

Placing a filter or other source of resistance at Vcc can create significantly longer acquisition times.

A.4 Migration from LEA-4 to LEA-5

The pin-outs of LEA-4 and LEA-5H/T differ slightly. Table 16 and Table 17 compare the modules and highlight the differences to be considered.

Pin	LEA-4H/LEA-4P/LEA-4T		LEA-5H/LEA-5T		Remarks for Migration
	Pin Name	Typical Assignment	Pin Name	Typical Assignment	
1	**Reserved**	VDDIO level I/O; not connected	**SDA2**	NC	
2	**Reserved**	VDDIO level I/O; not connected	**SCL2**	NC	
3	**TXD1**	VDDIO level I/O	**TxD1**	Output	
4	**RXD1**	VDDIO level I/O	**RxD1**	Input	Leave open if not used.
5	**VDDIO**	1.65 – 3.60V	**NC**	Connect to VCC	Can be left open, but connection to VCC is recommended for compatibility reason (e.g LEA-5Q). With LEA-5H the I/O voltage is always VCC.

Pin	LEA-4H/LEA-4P/LEA-4T		LEA-5H/LEA-5T		Remarks for Migration
	Pin Name	Typical Assignment	Pin Name	Typical Assignment	
6	**VCC**	2.70 – 3.30V	**VCC**	2.70 – 3.60V	Extended power supply range, higher peak supply current.
7	**GND**	GND	**GND**	GND	No difference
8	**VDD18OUT**	NC	**VCC_OUT**	NC	Internally connected to VCC, if you have circuitry connected to this pin, check if it withstands the VCC voltage.
9	**Reserved**	NC	**Reserved**	NC	
10	**RESET_N**	1.8V	**RESET_N**	NC	Input only, do not drive high. Internal pull up to VCC.
11	**V_BAT**	1.50 – 3.6V	**V_BCKP**	1.4 – 3.6V	Wider voltage range but needs more current. Check your backup supply, regarding the higher consumption.
12	**BOOT_INT**	NC	**Reserved**	NC	do not drive low.
13	**GND**	GND	**GND**	GND	No difference
14	**GND**	GND	**GND**	GND	No difference
15	**GND**	GND	**GND**	GND	No difference
16	**RF_IN**	RF_IN	**RF_IN**	RF_IN	No difference
17	**GND**	GND	**GND**	GND	No difference
18	**VCC_RF**	VCC - –.1V	**VCC_RF**	VCC - –.1V	No difference
19	**V_ANT**	3.0V –5.0V	**V_ANT**	2.7V -5.5V	No difference
20	**AADET_N**	NC	**AADET_N**	NC	
21	**EXTINT1**	NC	**NC**	NC	
22	**Reserved**	NC	**NC**	NC	
23	**Reserved**	NC	**NC**	NC	
24	**VDDUSB**	Connected to GND or VDD_USB	**VDDUSB**	Connected to GND or VDD_USB	Do not leave open. (VDD_USB is 3.3V regulated power supply from VBUS.)
25	**USB_DM**	NC	**USB_DM**	NC	No difference
26	**USB_DP**	NC	**USB_DP**	NC	No difference
27	**EXTINT0**	NC	**EXTINT0**	NC	
28	**TIMEPULSE**	VDDIO level I/O	**TIMEPULSE**	Output	

: Pins to be checked carefully; NC: Not connected

Table 16: Pin-out comparison LEA-4H/LEA-4P/LEA-4T vs. LEA-5H/LEA-5T

Pin	LEA-4A/LEA-4S		LEA-5A/LEA-5S		Remarks for Migration
	Pin Name	Typical Assignment	Pin Name	Typical Assignment	
1	**TxD2**	3.0V out	**SDA2**	NC	
2	**RxD2**	1.8 - –.0V	**SCL2**	NC	
3	**TxD1**	3.0V out	**TxD1**	Output	
4	**RxD1**	1.8 - –.0V in	**RxD1**	Input	Leave open if not used.
5	**VDDIO**	VCC	**NC**	Connect to VCC	Can be left open, but connection to VCC is recommended for compatibility reason (e.g LEA-5Q).
6	**VCC**	2.70 – 3.30V	**VCC**	2.70 – 3.60V	Extended power supply range, higher peak supply current.
7	**GND**	GND	**GND**	GND	No difference
8	**VDD18OUT**	1.8V out	**VCC_OUT**	NC	Internally connected to VCC, if you have circuitry connected to this pin, check if it withstands the VCC voltage.
9	**GPSMODE6**	NC (GND or VDD18OUT)	**CFG_COM1**	NC	
10	**RESET_N**	ACTIVE LOW	**RESET_N**	NC	Input only, do not drive high. Internal pull up to VCC.
11	**V_BAT**	1.50 – 3.6V	**V_BCKP**	1.4 – 3.6V	Wider voltage range but needs more current. Check your backup supply, regarding the higher consumption.

Pin	LEA-4A/LEA-4S		LEA-5A/LEA-5S		Remarks for Migration
	Pin Name	Typical Assignment	Pin Name	Typical Assignment	
12	**BOOT_INT**	NC	**Reserved**	NC	do not drive low.
13	**GND**	GND	**GND**	GND	No difference
14	**GND**	GND	**GND**	GND	No difference
15	**GND**	GND	**GND**	GND	No difference
16	**RF_IN**	RF_IN	**RF_IN**	RF_IN	No difference
17	**GND**	GND	**GND**	GND	No difference
18	**VCC_RF**	VCC - –.1V	**VCC_RF**	VCC - –.1V	No difference
19	**V_ANT**	3.0V - –.0V	**V_ANT**	2.7V -5.5V	No difference
20	**AADET_N**	NC (1.8 to 5.0V)	**AADET_N**	NC	
21	**GPSMODE5**	NC (GND or VDD18OUT)	**NC**	NC	
22	**GPSMODE2 GPSMODE2 3**	NC (GND or VDD18OUT)	**NC**	NC	
23	**GPSMODE7**	NC (1.8 to 5.0V)	**NC**	NC	
24	**VDDUSB**	3.0 –3.6V/ GND	**VDDUSB**	Connected to GND or VDD_USB	Do not leave open. (VDD_USB is 3.3V regulated power supply from VBUS.)
25	**USB_DM**	VDDUSB I/O	**USB_DM**	NC	No difference
26	**USB_DP**	VDDUSB I/O	**USB_DP**	NC	No difference
27	**EXTINT0**	NC (1.8 to 5.0V)	**EXTINT0**	NC	
28	**TIMEPULSE**	VDDIO out	**TIMEPULSE**	Output	

: Pins to be checked carefully; NC: Not connected

Table 17: Pin-out comparison LEA-4A/LEA-4S vs. LEA-5A/LEA-5S

A.5 Migration from NEO-4S to NEO-5Q/NEO-5M

The pin-outs of NEO-4S and NEO-5M/NEO-5Q differ slightly. Table 18 compares the modules and highlights the differences to be considered.

Pin	NEO-4S		NEO-5Q/NEO-5M		Remarks for Migration
	Pin Name	Typ. Assignment	Pin Name	Typ. Assignment	
1	**BOOT_INT**	NC	**Reserved**	NC	do not drive low.
2	**SELECT**	VDDIO level I/O; not connected	**NC/ SS_N**	NC	NEO-5M: NC NEO-5Q: SS_N
3	**TIMEPULSE**	VDDIO level I/O	**TIMEPULSE**	Output	
4	**EXTINT0**	NC	**EXTINT0**	NC	
5	**USB_DM**	NC	**USB_DM**	NC	
6	**USB_DP**	NC	**USB_DP**	NC	
7	**VDDUSB**	Connected to GND or VDD_USB	**VDDUSB**	Connected to GND or VDD_USB	Do not leave open. (VDD_USB is 3.3V regulated power supply from VBUS.)
8	**Reserved**	NC	**Reserved**	NC	Pins 8 and 9 must be connected.
9	**VCC_RF**	VCC-0.1V	**VCC_RF**	VCC-0.1V	No difference
10	**GND**	GND	**GND**	GND	No difference
11	**RF_IN**	RF_IN	**RF_IN**	RF_IN	No difference
12	**GND**	GND	**GND**	GND	No difference
13	**GND**	GND	**GND**	GND	No difference
14	**MOSI**	NC	**MOSI/CFG_COM0**	NC	The function of the CFG pin has changed. See Section 2.3 for more details.
15	**MISO**	NC	**MISO//CFG_COM1/ NC**	NC	
16	**SCK/ CFG_USB**	RF_IN	**SCK/CFG_GPS0/ NC**	NC	Leave open if not used. The function of the CFG pin has changed. See Section 2.3 for more details.
17	**NCS**	NC	**SCS1_N/ NC**	NC	No difference
18	**Reserved**	NC	**SDA2**	NC	
19	**Reserved**	NC	**SCL2**	NC	
20	**TXD1**	VDDIO level I/O	**TxD1**	Output	
21	**RXD1**	VDDIO level I/O	**RxD1**	Input	Leave open if not used.
22	**V_BAT**	1.5-3.6V	**V_BCKP**	1.4-3.6V	Wider voltage range but needs more current. Check your backup supply, regarding the higher consumption.
23	**VCC**	2.7-3.3V	**VCC**	2.7-3.6V	Higher peak supply current
24	**GND**	GND	**GND**	GND	No difference

: Pins to be checked carefully; NC: Not connected

Table 18: Pin-out comparison NEO-4S vs. NEO-5

A.6 Migration from TIM-4H / TIM-4P to TIM-5H

The pin-outs of TIM-4H/4P and TIM-5H differ slightly. Table 19 compares the modules and highlights the differences to be considered.

Pin	TIM-4x		TIM-5H		Remarks for Migration
	Pin Name	Typical Assignment	Pin Name	Typical Assignment	
1	**VCC**	2.70 – 3.30V	**VCC**	2.70 – 3.60 V	Increased Voltage range and peak supply current.
2	**GND**	GND	**GND**	GND	No difference
3	**BOOT_INT**	NC	**NC**	Reserved	Do not drive low
4	**RXD1**	1.8 to 5.0V in	**RXD1**	Input	No difference
5	**TXD1**	3.0V out	**TXD1**	Output	No difference
6	**TXD2**	3.0V out	**TXD2**	Output	No difference
7	**RXD2**	1.8 to 5.0V in	**RXD2**	Input	No difference
8	**SCK1/ P17/ GPSMODE5**	NC	**Reserved**	NC	No difference
9	**EXTINT1/ GPSMODE3**	NC	**Reserved**	NC	No difference
10	**VDD18OUT**	NC	**VCC_OUT**	NC	Internally connected to VCC, if you have circuitry connected to this pin, check if it withstands the VCC voltage.
11 to 16	**GND**	GND	**GND**	GND	No difference
17	**RF_IN**	RF_IN	**RF_IN**	RF_IN	No difference
18	**GND**	GND	**GND**	GND	No difference
19	**V_ANT**	3.0V - –.0V	**V_ANT**	2.7 – 5.5V	
20	**VCC_RF**	VCC - –.1V	**VCC_RF**	VCC - –.1V	No difference
21	**V_BAT**	1.50 – 3.6V	**V_BCKP**	1.40 – 3.6V	Wider voltage range but needs more current. Check your backup supply, regarding the higher consumption.
22	**RESET_N**	1.8V	**RESET_N**	NC	Input only, do not drive high. Internal pull up to VCC.
23	**EXTINT0**	NC	**EXTINT0**	NC	No difference
24	**PCS1_N / GPSMODE2**	NC	**Reserved**	NC	Check GPSMODE pin
25	**PCS0_N/ GPSMODE6**	NC	**Reserved**	NC	Check GPSMODE pin
26	**SCK/ NC**	NC	**Reserved**	NC	No difference
27	**AADET_N**	NC	**AADET_N**	NC	No difference
28	**MOSI/ NC**	NC	**Reserved**	NC	No difference
29	**TIMEPULSE**	3.0V out	**TIMEPULSE**	Output	No difference
30	**PCS3_N/ GPSMODE 12**	NC	**Reserved**	NC	No difference

: Pins to be checked carefully; NC: Not connected

Table 19: Pin-out comparison TIM-4H / TIM-4P vs. TIM-5H

A.7 Typical Pin Assignment TIM modules

Pin	ANTARIS®4				u-blox-5		Pin
	TIM-4A/S		TIM-4P/H		TIM-5H		
	Pin Name	Typical Assignment	Pin Name	Typical Assignment	Pin Name	Typical Assignment	
1	**VCC**	2.70 – 3.30V	**VCC**	2.70 – 3.30V	**VCC**	2.70 – 3.60 V	1
2	**GND**	GND	**GND**	GND	**GND**	GND	2
3	**BOOT_INT**	NC	**BOOT_INT**	NC	**Reserved**	NC	3
4	**RXD1**	1.8 to 5.0V in	**RXD1**	1.8 to 5.0V in	**RXD1**	Input	4
5	**TXD1**	3.0V out	**TXD1**	3.0V out	**TXD1**	Output	5
6	**TXD2**	3.0V out	**TXD2**	3.0V out	**TXD2**	Output	6
7	**RXD2**	1.8 to 5.0V in	**RXD2**	1.8 to 5.0V in	**RXD2**	Input	7
8	**SCK1/ P17/ GPSMODE5**	NC	**SCK1/ P17**	NC	**Reserved**	NC	8
9	**EXTINT1/ GPSMODE3**	NC	**EXTINT1**	NC	**Reserved**	NC	9
10	**VDD18OUT**	NC	**VDD18OUT**	NC	**VCC_OUT**	NC	10
11 to 16	**GND**	GND	**GND**	GND	**GND**	GND	11 to 16
17	**RF_IN**	RF_IN	**RF_IN**	RF_IN	**RF_IN**	RF_IN	17
18	**GND**	GND	**GND**	GND	**GND**	GND	18
19	**V_ANT**	3.0V -5.0V	**V_ANT**	3.0V -5.0V	**V_ANT**	2.7 – 5.5V	19
20	**VCC_RF**	VCC - –.1V	**VCC_RF**	VCC - –.1V	**VCC_RF**	VCC - –.1V	20
21	**V_BAT**	1.50 – 3.6V	**V_BAT**	1.50 – 3.6V	**V_BCKP**	1.4-3.6V	21
22	**RESET_N**	1.8V	**RESET_N**	1.8V	**RESET_N**	NC	22
23	**EXTINT0**	NC	**EXTINT0**	NC	**EXTINT0**	NC	23
24	**GPSMODE2**	NC	**GPSMODE2**	NC	**Reserved**	NC	24
25	**GPSMODE6**	NC	**GPSMODE6**	NC	**Reserved**	NC	25
26	**NC**	NC	**SCK**	NC	**Reserved**	NC	26
27	**AADET_N**	NC	**AADET_N**	NC	**AADET_N**	NC	27
28	**NC**	NC	**MOSI**	NC	**Reserved**	NC	28
29	**TIMEPULSE**	3.0V out	**TIMEPULSE**	3.0V out	**TIMEPULSE**	Output	29
30	**GPSMODE 12**	NC	**PCS3_N**	NC	**Reserved**	NC	30

: Pins to be checked carefully; NC: Not connected

Table 20: Typical Pin Assignment TIM modules

Related documents

[1] LEA-5 Data Sheet, Docu. No GPS.G5-MS5-07026

[2] NEO-5 Data Sheet, Docu. No GPS.G5-MS5-07025

[3] TIM-5H Data Sheet, Docu. No GPS.G5-MS5-07014

[4] u-blox 5 Receiver Description including Protocol Specification, Docu. No GPS.G5-X-07036

[5] u-blox 5 Firmware Version 6.00 Release Note, Docu. No GPS.G5-SW-09022

[6] GPS Antenna Application Note, Docu. No GPS-X-08014

All these documents are available on our homepage (http://www.u-blox.com).

☞ For regular updates to u-blox documentation and to receive product change notifications please register on our homepage.

Revision history

Revision	Date	Name	Status / Comments
-	6/15/2009	tgri	Initial release
A	22/07/2009	tgri	Revision of structure, sections 3.7 and 4.
A1	30/07/2009	tgri	Minor corrections
A2	20/11/2009	tgri	Update to FW 6.02

The current document replaces the following:	
Document number	**Document Name**
GPS.G5-MS5-07005	LEA-5 Hardware Integration Manual
GPS.G5-MS5-08003	NEO-5 Hardware Integration Manual
GPS.G5-MS5-07015	TIM-5H Hardware Integration Manual

Contact

For complete contact information visit us at www.u-blox.com

Offices

North, Central and South America

u-blox America, Inc.
Phone: +1 (703) 483 3180
E-mail: info_us@u-blox.com

Regional Office West Coast:
Phone: +1 (703) 483 3184
E-mail: info_us@u-blox.com

Technical Support:
Phone: +1 (703) 483 3185
E-mail: support_us@u-blox.com

Headquarters
Europe, Middle East, Africa

u-blox AG
Phone: +41 44 722 74 44
E-mail: info@u-blox.com

Technical Support:
Phone: +41 44 722 74 44
E-mail: support@u-blox.com

Asia, Australia, Pacific

u-blox Singapore Pte. Ltd.
Phone: +65 6734 3811
E-mail: info_ap@u-blox.com
Support: support_ap@u-blox.com

Regional Office China:
Phone: +86 10 68 133 545
E-mail: info_cn@u-blox.com
Support: support_cn@u-blox.com

Regional Office Japan:
Phone: +81 03 5775 3850
E-mail: info_jp@u-blox.com
Support: support_jp@u-blox.com

Regional Office Korea:
Phone: +82 2 542 0861
E-mail: info_kr@u-blox.com
Support: support_kr@u-blox.com

Regional Office Taiwan:
Phone: +886 2 2657 1090
E-mail: info_tw@u-blox.com
Support: support_tw@u-blox.com