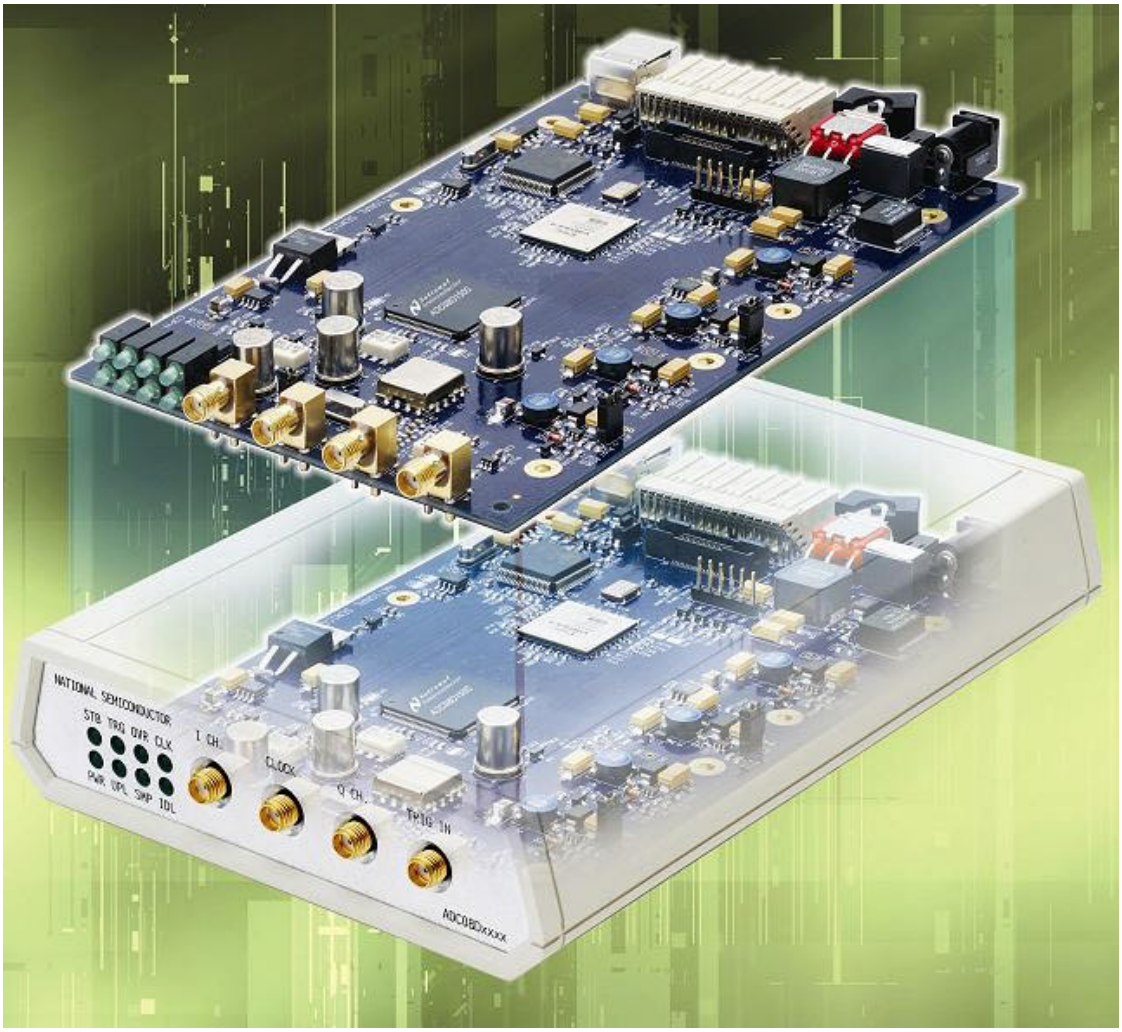
National Semiconductor

November, 2007
Revision 2.3

ADC08(D)500/10X0/15X0DEV

Development Board Users' Guide

Ultra High Speed A/D Converter with Xilinx Virtex 4 (XC4VLX15) FPGA



ADC08(D)XXXX-DEV BOARD USERS' GUIDE – TABLE OF CONTENTS

1.0 Introduction

The ADC08(D)XXXXDEV Board is designed to allow quick evaluation and design development of National Semiconductor's ADC08(D)XXXX ultra high speed 8-bit Analog-to-Digital Converters. Reference to ADC08(D)XXXX through out this document applies to the following devices: ADC08500, ADC08D500, ADC081000, ADC08D1000, ADC08D1020, ADC081500, ADC08D1500, and ADC08D1520.

The ADC08500, ADC081000 and ADC081500 have a single channel input with a sampling rate of 500 MSPS, 1.0 GSPS and 1.5 GSPS, respectively. The ADC08D500, ADC08D10X0 and ADC08D15X0 are specified for 500 MSPS, 1.0 GSPS, and 1.5 GSPS operation in 2-input channel mode, respectively. The ADC08D10X0, and ADC08D15X0 may be configured to sample at 2 GSPS or 3 GSPS, respectively, in Dual Edge Sampling (DES) mode.

This development board is designed to function with National Semiconductor's WaveVision Software, for fast evaluation. It requires only three connections to get started: a power supply, a USB Interface to a PC, and a signal source. An on-board clock generator is provided, and the system also allows for an external clock to be used if alternate sample rates are required.

The ADC connects to a Xilinx Virtex4 FPGA which stores up to 4K of data from each channel before transferring it through the USB interface to the PC.

2.0 Board Assembly

The ADC08(D)XXXXDEV Development Board comes in a low profile plastic enclosure and does not require assisted cooling due to its low power consumption. The ADC08(D)XXXX device is configured entirely through software and also allows changes to easily be made to the FPGA configuration to enable system development.

3.0 Board Specifications

The following shows the board specifications for the ADC08(D)XXXX, Table 1.

Board Size:	168 mm x 100 mm
Power Requirements:	+12V, 800 mA
Clock Frequency Range (25° C) :	ADC08(D)500DEV: 150 MHz - 700 MHz ADC08(D)10X0DEV: 500 MHz - 1.0 GHz ADC08(D)15X0DEV: 800 MHz - 1.5 GHz
Analog Input Range (AC Coupled):	30 MHz to 1800 MHz
Nominal Analog Input Voltage:	560 mV_{P-P} to 870 mV_{P-P}
Analog Input Impedance:	50 Ohms

Table 1. Board Specifications

3.1 FPGA Specification

The board supports a Xilinx LX15 Virtex 4 363-pin FPGA. This device is responsible for collecting and storing the data from ADC, measuring the clock frequency, and uploading the data through the microcontroller to the PC.

Three separate FPGA images are used to support clock speeds at 500 MHz, 1 GHz, and 1.5 GHz. The 500 MHz image typically supports a clock range of 150 MHz to 700 MHz. The 1 GHz image typically supports a clock range of 500 MHz to 1.0 GHz, while the 1.5 GHz image typically supports a clock range of 800 MHz to 1.5 GHz.

Normally, the FPGA is configured automatically by the WaveVision software. It is possible, through modification of the board, to configure the FPGA using a FLASH ROM, so that the system may be run without the USB microcontroller.

NOTE: Though the development board provides a powerful capability for the user to develop his own FPGA code, National does not support such custom FPGA code development.

3.2 Microcontroller

A Cypress CY7C68013A microcontroller manages the USB interface and general control of the board hardware (for Evaluation boards REV 2.0 and above). It uses a 24 MHz crystal oscillator.

3.3 Memory Components

One 2K EEPROM (24C02 or similar) is connected to the I^2C Bus for Microcontroller and USB configuration data. This EEPROM also identifies the ADC and clock source.

3.4 Power Supplies

Power to the board is supplied through a single-pin power jack to allow the use of an external brick power supply with a voltage range of 8V to 12V.

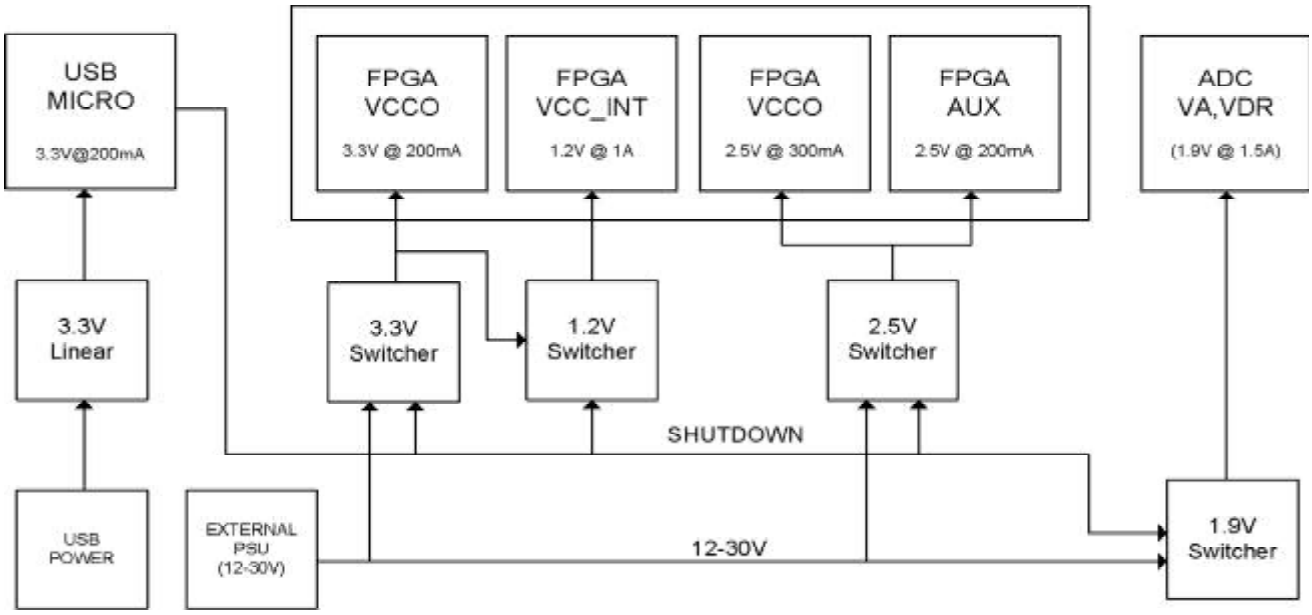


Figure 1. Power supply architecture

The following supplies are provided by on board regulators (Switching and Linear):

- 3.3V - USB Microcontroller
- 3.3V – FPGA (LVCMOS I/O)
- 2.5V - FPGA (AUX Supply and LVDS25 I/O)
- 1.9V - ADC (V_A and V_{DR})
- 1.2V – FPGA (CORE)

A power LED indicator is provided on the front edge of the board along with the status LEDs.

A Rocker Switch is provided on the rear edge of the board to allow easy cold start/re-start.

Figure 1 shows the power supplies required for the design in more detail.

The USB Microcontroller controls the shutdown pins of all the switching regulators to minimize power in standby mode.

3.5 Clocking

The USB Microcontroller is clocked by its own 24 MHz crystal oscillator.

The ADC is clocked by either a National Semiconductor PLL and a VCO device, or an external clock source. Switching between clock sources is done through a relay controlled by the WaveVision software.

The PLL and VCO devices are selected to provide a 500 MHz, 1000 MHz or 1500 MHz very low jitter on-board clock depending on which ADC is used.

The on-board PLL is programmed over a serial interface through the FPGA.

The FPGA may be clocked by one of two sources:

1. When capturing data from the ADC, the FPGA is clocked from the source synchronous ADC clock, which will operate at a rate of either Fs/2 (Single Data Rate) or Fs/4 (Dual Data Rate).
2. When calculating the input clock frequency and uploading the captured data to the USB Microcontroller, an on-board crystal oscillator running at 100 MHz is used.

3.6 Resets

The USB Microcontroller utilizes a simple RC power-on-reset circuit along with local push-button reset. The FPGA has a RESET input signal which is controlled by the USB Microcontroller.

3.7 Thermal Management

The ADC and the Virtex 4 FPGA temperature diodes are connected to a National Semiconductor LM95221 Dual Temperature Sensor device. This temp sensor interfaces to the USB Microcontroller over a 2 wire serial bus. The ADC's temperature is monitored to determine when calibration cycles are required. The user may also initiate a calibration cycle using the WaveVision software.

3.8 ADC Analog Inputs

The analog inputs (I- and Q-channel) are provided through SMA connectors on the front edge of the board and are single-ended. The ADC I-channel input is capable of accepting an AC- or DC-coupled input signal. The Q-channel may be AC-coupled only.
Single-ended to differential input signal conversion is performed by a Mini-Circuits Balun (ADTL2-18) for the AC-coupled path. A LMH6555 Differential Op-Amp is used to DC couple the input signal. Software-controlled Teledyne RF relays are used to switch the signal path from AC- to DC-coupled.

3.9 Trigger Input

A trigger input is provided on the front panel through a SMA connector. This signal is connected to the FPGA via a Schmitt trigger and is TTL compatible with 5V tolerance. This input has no functionality, and is provided so the user may develop his own FPGA functionality if desired.

3.10 Status Indicators

The Following Status Indicators (LEDs) are provided on the front edge of the board, Figure2:

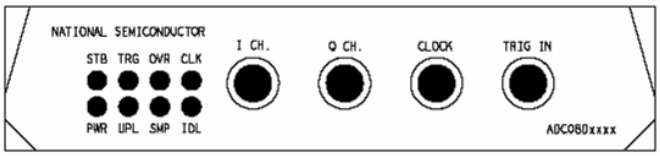


Figure 2. Component placement and front panel

This is a brief summary of the name, abbreviation and description of the status LEDs:

Name	Abbr.	Description
Standby	STB	All switching regulators powered down
Trigger	TRG	Trigger input indicator
Over-range	OVR	Over-range indicator
Clock	CLK	Clock active indicator (blinks)
Power-on	PWR	12V-30V power
Upload	UPL	Data is being uploaded to PC
Sample	SMP	Data is being captured by FPGA
FPGA RDY/IDLE	IDL	FPGA is programmed and IDLE

Table 2. Status Indicators

3.11 Debug

A Mictor Logic Analyzer Header is provided along with test-point headers both of which are connected to the FPGA. This allows monitoring of captured data and critical signals during board debug. A JTAG header is also provided to allow further FPGA development.

4.0 Quick Start

Refer to Figure 3 for the location of the power connection, signal input and USB port.

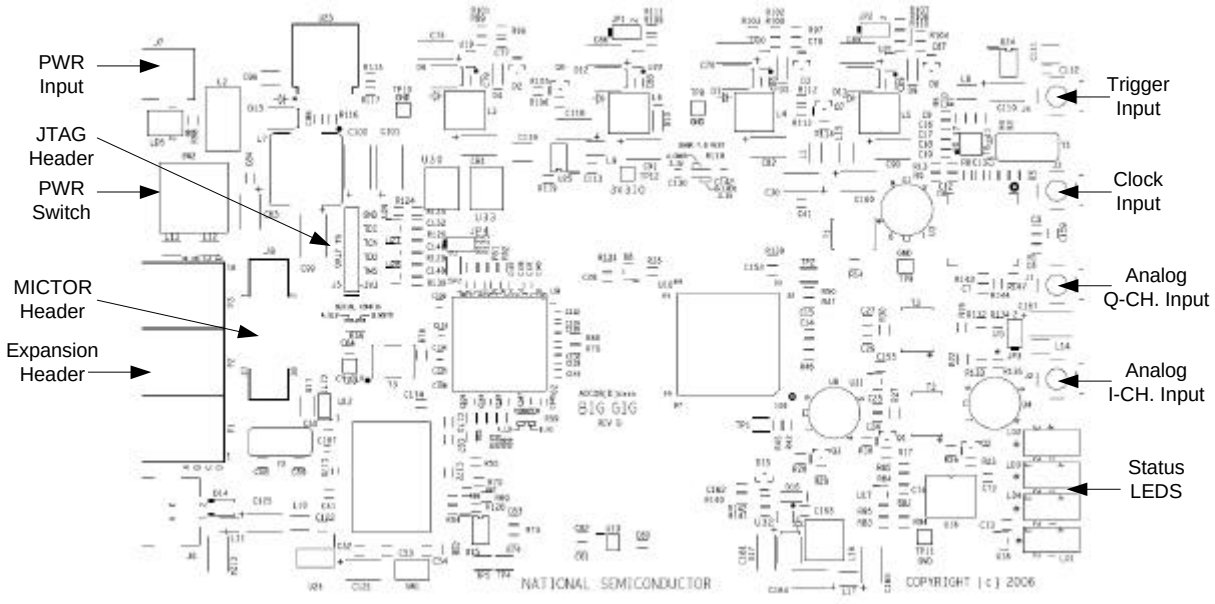


Figure 3. Development board overview

NOTE: Install the WaveVision4 software before connecting this product to the PC.

For quick start operation:

1. Install the WaveVision4 software. See Appendix B – Installing WaveVision.
2. Connect the 12V DC power source (included with the development board) to the rear Power Connector labeled (8V-12V DC).
3. Connect a stable sine wave source capable of supplying the desired input frequencies at up to 8 dBm. Connect this signal to the front panel SMA connector labeled "I CH." through a band-pass filter. The exact level required from the generator will depend upon the insertion loss of the filter used.
4. Connect the USB cable (included) from the USB port to the PC. If this is the first time the board has been connected, Windows may install the drivers for this product at this time.
5. Push the Power Switch to the ON position on the rear panel and check that the Green LED between the switch and the power connector illuminates.
6. Start the WaveVision4 Software.
7. Once loaded, the "Firmware Download" Progress bar should be displayed. See Appendix B for more information.
8. Upon Firmware Download completion, the control panel for the board should automatically be displayed on the PC and the CLK LED on the front panel should be flashing.
9. Set the signal source for the analog input to 8 dBm at the desired frequency. Observe the Out-of-Range LED labeled OVR on the front panel. If this LED is not illuminated, increase the input signal source until it is.
10. Reduce the input level until the OVR LED just turns off. Now, the input signal level should be maximized, without over-ranging.
11. From the WaveVision4 pull-down menu select **Acquire** and then **Samples**. The system will then capture the input signal waveform and display the results in the time domain.
12. For the FFT analysis of this sample, click the **FFT** Tab.

5.0 Functional Description

The ADC08(D)XXXXDEV Development Board schematic is included as an additional document.

5.1 Input circuitry

The input signal(s) to be digitized should be applied to the front panel SMA connectors labeled "I CH." and "Q CH." For single input devices such as the ADC08500, ADC081000 and ADC0815000, apply the signal only to the "I CH." These 50 Ohm inputs are intended to accept low-noise sine wave signals. To accurately evaluate the dynamic performance of this converter, the analog input signal(s) must be filtered by a high-quality bandpass filter with at least 10-bit equivalent noise and distortion characteristics.

This evaluation board is designed for operation with two single-ended analog inputs, which are converted to differential signals on-board.

Signal transformers T2 and T3 are connected as baluns, and provide the single-ended to differential conversion. The differential PCB traces to the ADC analog input pins have a characteristic differential impedance of 100 Ohms.

No other test equipment, such as an oscilloscope, should be connected anywhere in the signal path while gathering data because it will add noise to the signal.

The TRIG_IN input is buffered and passed to the FPGA. The intent of this input is to allow users to expand the existing capabilities of the current system by providing for external triggering of a data capture. The TRIG_IN input has no functionality in the provided FPGA firmware.

5.2 ADC reference

The ADC08(D)XXXX has an internal reference which can not be adjusted. However, the Full-Scale (differential) Range may be adjusted with the Software Control Panel. Refer to Section 6.0 for more information

5.3 ADC clock

The ADC clock, which is generated on-board, is a fixed frequency. An external clock signal may alternatively be supplied to the ADC through the SMA Connector labeled "CLOCK" on the front panel. The balun-transformer (T1) converts the single-ended clock source to a differential signal to drive the ADC clock pins.

If using an external clock source, it is very important that it is as low jitter as possible. Otherwise, the SNR of the ADC08(D)XXXX will be compromised.

When alternating between an externally applied clock to the on-board clock, the clock input should never be left floating. The user is advised

to switch to the on-board clock before disconnecting the external clock. If a problem does occur, simply reset the board. This may be found on the pull-down menu: **Settings**, **Capture Settings**. Click on the **Reset** button. Then, check that the **Evaluation Board** is reporting the correct clock frequency. When using the on-board clock, it is recommended to remove or turn off any external clock source.

5.4 Digital Data Output

The two channel digital output data from the ADC08(D)XXXX is connected to a Xilinx Virtex 4 FPGA. Up to 4K bytes of data per channel may be stored and then uploaded over the USB interface to the WaveVision software. The FPGA logic requires a small amount of space, allowing for further code to be written and tested for product development.

5.5 Power Requirements

The power supply requirement for the ADC08(D)XXXXDEV Evaluation Board is typically 12V at 800 mA. The board typically draws around 500 mA.

Most of the on-board regulators are switching regulators for increased power efficiency.

A Universal 100-240V AC input to 12V DC Brick Power Supply is included with the development board.

5.6 Power Supply Connections

Power to this board is supplied through the power connector on the rear panel. It is advised that only the supplied PSU is used with this board.

The ADC08(D)XXXX supply voltage has been set to 1.9V, ±50 mV using on-board regulators.

6.0 Obtaining Best Results

Obtaining the best results with any ADC requires both good circuit techniques and a good PC board layout. For layout information for this product, please contact your National Semiconductor representative.

6.1 Clock Jitter

When any circuitry is added after a signal source, jitter is almost always added to that signal. Jitter in a clock signal, depending upon the severity of that jitter, will degrade dynamic performance. The effects of jitter in the frequency domain (FFT) may be observed as "leakage" or "spectral spreading" around the input frequency, as seen in Figure 4a. Compare this with the more desirable plot of Figure 4b. Note that all dynamic performance parameters (shown to the right of the FFT) are improved by eliminating clock jitter.

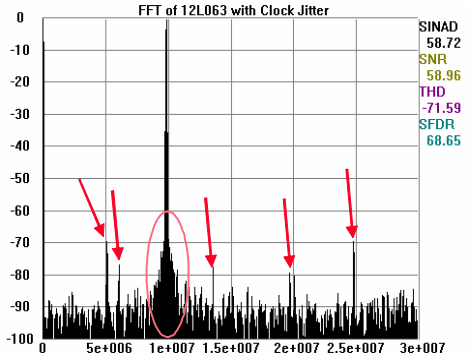


Figure 4a. Jitter causes spectral spreading and spurs

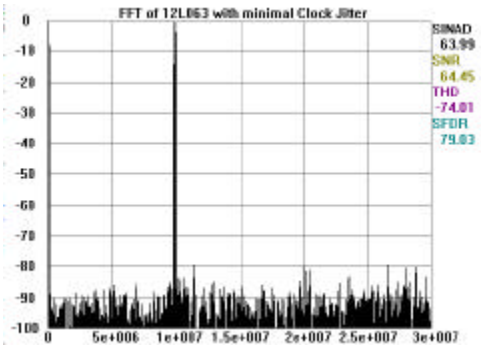


Figure 4b. Minimal clock jitter results in cleaner FFT, better dynamic performance

7.0 Using the WaveVision4 software with the ADC08(D)XXXXDEV

NOTE: Before connecting this board to the PC, install the Wavevision4 software from the CDROM included with the development kit. (See Appendix B.)

Connecting the Development Board before installation may result in the board being registered as an unknown USB device. If this occurs, the device must first be uninstalled using the Windows Device Manager before installing the WaveVision4 Software.

7.1 Getting Started

This development board is designed to connect to a PC running the WaveVision Software via a USB interface.

Ensure the board is connected to the 12V power supply (included with the package) and that the switch on the rear panel is pushed to the “ON” position. The Green LED on the rear panel should be illuminated.

Connect the USB cable between the PC which has WaveVision software installed and the ADC08(D)XXXXDEV board. The USB port may be found on the rear panel (Figure 5).

If this is the first time the board has been connected to the PC, drivers may be required to be installed (automatic) by the Operating System. Follow the on-screen instructions and use the recommended settings.

Figure 5. ADC08(D)XXXXDEV rear panel showing location of USB connector

Start the WaveVision software. (**Start** -> **All Programs** -> **WaveVision** -> **WaveVision4**)

The software may take several seconds to initialize, but should display a welcome screen similar to the Figure 6.

Figure 6. WaveVision welcome screen

If the board is connected correctly, the following popup box should appear (Figure 7) to indicate that the board has been recognized and the firmware for the FPGA is being downloaded over the USB interface.

Figure 7. Firmware downloading popup box

If the “Downloading firmware” box does not appear automatically, click on the “Settings” pull-down menu and then click Capture Settings (Figure 8).

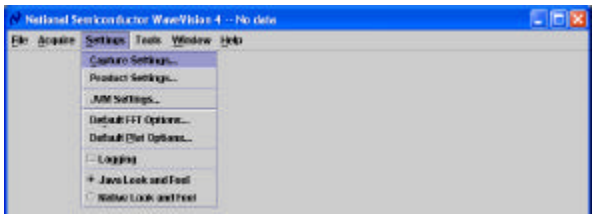


Figure 8. *Capture Settings* location

This will display the **System Settings** (Figure 9).

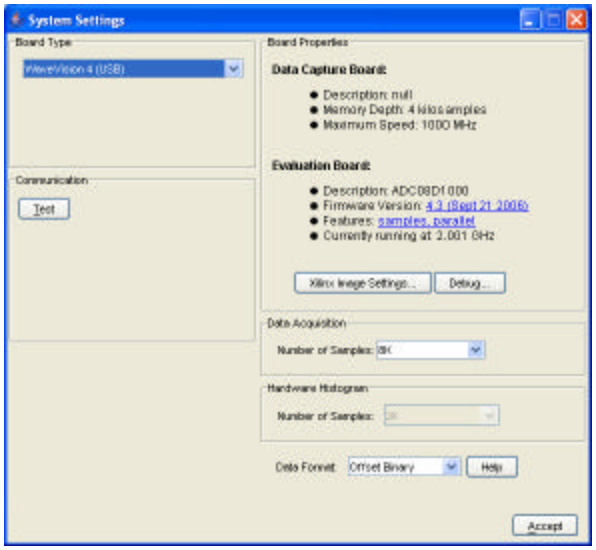


Figure 9. System Settings window

If the board has not been detected, click the **Test** button under the Communication heading. This forces the software to download the software to the FPGA. If the communications fail, check that the USB drivers are installed correctly. Then, disconnect and re-connect the USB cable. Finally, restart the WaveVision software. See Appendix B for more information.

7.2 Control Panel

Once the FPGA Firmware download is complete, the development board Control Panel will automatically be displayed (Figure 10).

Figure 10. Control Panel window

The following section describes the function of the pull-down selection tabs in the left-hand side of the ADC08(D)XXXXDEV product Control Panel. Note that some functions are device dependent. Refer to the device datasheet for available features.

- **Channel Selection**
  - **I** – Displays the data captured from the I-channel only after acquiring samples.
  - **Q**- Displays the data captured from the Q-channel only after acquiring samples.
  - **I and Q** – Displays the data captured from I- and Q-channels in two windows after acquiring samples.
  - **I/Q Interleaved** – Displays the data captured from the I- and Q-channels interleaved in a single window, after acquiring samples. Use when DES mode is enabled.

- **Temp Sensor**
  - This displays the die temperature of both the FPGA and the ADC.

- **Hardware/Serial Control**
  - **Hardware Pin Control** – The ADC is controlled by the logic states on the dedicated control pins. The logic on these pins is determined by the setting of **OUTV, OUTEDGE, DDR, DES and FSR,** as described below.
  - **Serial Register Program** – The ADC's registers are accessed through the Extended Control Mode. In this mode, the hardware pin control is disabled and the programmable registers are available for fine tuning.

Note: The Following Pull-down Tabs are available only when **Hardware Pin Control** is selected.

- **Out V**
  - **Low Amplitude** – LVDS output voltage amplitude is set to 510 mVpk-pk.
  - **High Amplitude** – LVDS output voltage amplitude is set to 710 mVpk-pk.

- **OutEdge**
  - **Falling Edge** – Data outputs are changed on the falling edge of DCLK+ (SDR mode only).
  - **Rising Edge** – Data outputs are changed on the rising edge of DCLK+ (SDR mode only).

- **DDR**
  - **Disable Dual Data Rate** – DDR Mode is disabled (data output follow OutEdge Setting).
  - **Enable Dual Data Rate** – Data is concurrent with rising and falling edge of DCLK+. (This is the default mode for 1.5 GHz clock).

- **DES**
  - **Disable Dual Edge Sample** – DES Mode is disabled, i.e. the I- and Q-channels are independent.
  - **Enable Dual Edge Sample** – The I-channel is sampled on the rising and falling edge of the clock.

- **FSR**
  - **650mV Full Scale** – Sets the full-scale range to 650 mVpk-pk.
  - **870mV Full Scale** – Sets the full-scale range to 870 mVpk-pk.

Note: The Following Pull-down Tabs are available regardless of Hardware/Serial Control setting.

- **Standby**
  - **Disable Standby** – Enable all on-board power regulators.
  - **Enable Standby** – Board is put into standby mode – All power is shutdown except USB power.

- **PDQ**
  - **Disable Q Shutdown** – The ADC's Q-channel is powered up and active.
  - **Enable Q Shutdown** – The ADC's Q-channel is shutdown.

- **PD**
  - **Disable Shutdown** – The ADC is powered up and active.
  - **Enable Shutdown** – The ADC is put into low power mode. Register Settings are retained.

- **DC_Coup**
  - **AC Coupling** – The I-channel is AC-coupled to the ADC's input.
  - **DC Coupling** – The I-channel is DC-coupled to the ADC's input (not available in AC only mode.)

- **Ext_Clock**
  - **Internal Clock** – The ADC is clocked using the on-board clock.
  - **External Clock** – The ADC is clocked from an external clock source which is connected to the "CLOCK" input.

- **Reset FPGA**
  - This button resets the FPGA, and also returns all the pull-down tabs to their default values.

- **Calibrate ADC**
  - This button issues an on-command calibration to the ADC by toggling the ADC's calibrate pin.

7.3 Serial Control Mode

When the Hardware/Serial Control tab is selected as **Serial Register Program**, the control panel display will enable the other bits (Figure 11).

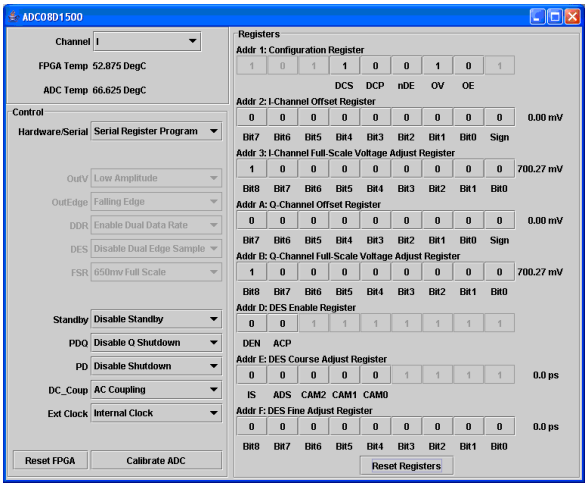


Figure 11. Serial Register Program window

In this mode, the register settings may be changed simply by clicking on the bits. Doing so will toggle each bit value. Any linear values such as **Full Scale Range** or **Offset** will automatically be updated.

The **Reset Registers** button at the bottom of the Control Panel will reset and write all the values to the power-on default settings.

Note: Please refer to the ADC08(D)XXXX datasheet for a full description of the ADC's internal registers.

7.4 Manually downloading the FPGA firmware

Although the WaveVision software is designed to automatically recognize the development board and download the appropriate FPGA code into it, it is possible for the user to download a different FPGA code (the .bit file) into the board. To download another FPGA code into the board, follow the subsequent instructions:

1. Place the desired .bit file (Xilinx object code that is known to operate correctly for the development board you are using) in a known directory of your choice on the C: drive.
2. Start WaveVision with the board connected via the USB.
3. The default FPGA will load automatically – this will be overwritten.
4. From the main WaveVision panel, under the **Settings** drop down menu, select **Capture Settings**. This will bring up another panel called **System Settings**.
5. Click the **Xilinx Image Settings** button within the **System Settings** panel. This will bring up another panel labeled **Select Xilinx Firmware**.
6. Deselect the **Select Images automatically** button.
7. Then click the **Browse** button and select the location of the bit file.
8. Click the **Accept** button. The **Select Xilinx Firmware** panel will disappear.
9. Load the FPGA image by clicking on the **Reset** (or **Test** in some versions) button. It may be found in the **Communication** sub-panel of the **System Settings** panel.
10. FPGA bit file download may be confirmed by observing the progress bar pop-up. If the progress bar goes half-way and suddenly terminates, the FPGA has not loaded. The second half should progress at a similar rate.

Please note that the development board's operation is only assured for the FPGA code provided by National. Though the board makes it possible for the user to develop and test his own FPGA code, such operation is not supported by National.

7.5 Capturing Waveforms

When the ADC has been properly configured, the selected input(s) may be sampled by clicking the **Acquire** pull-down menu and selecting **Samples**. Alternately, press **F1** then the **Escape** key. See Figure 12 for a sample waveform.

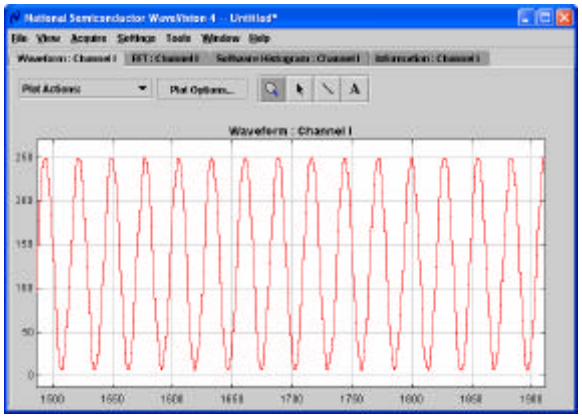


Figure 12. Waveform capture example

8.0 Appendix A - Hardware Information

8.1 Xilinx Virtex 4 FPGA

The ADC08(D)XXXXDEV development board implements the Xilinx Virtex 4 XC4VLX15-10SF363C FPGA for ADC control and data capture. The FPGA firmware is loaded over the USB port when the WaveVision software is started. The FPGA Verilog code and supplemental documentation is available to users upon request. Please contact your local National Semiconductor Sales or Field Applications Representative.

8.2 LED functions

The function of the LEDs on the front panel of the board (Figure 13) is as follows:

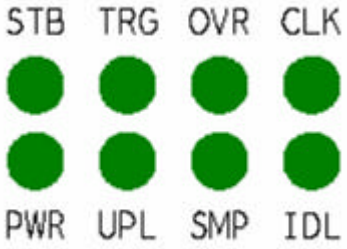


Figure 13. LED front panel

- **STB (STANDBY) -** illuminates when the board is in standby mode.
- **TRG (TRIGGER EVENT) -** illuminates when the Trigger Input makes low to high transition.
- **OVR (ADC OVER-RANGE) -** illuminates when the I- or Q-channel exceeds the full-scale range of the ADC.
- **CLK (CLOCK INPUT) -** flashes with 50% duty cycle if the ADC is receiving a clock input.
- **PWR (POWER) -** illuminates when the external 12V power supply is connected and the system is not in Standby.
- **UPL (UPLOAD) -** illuminates when the FPGA is uploading sample data to the PC.
- **SMP (SAMPLE) -** illuminates when the FPGA is sampling data and storing to the FIFO buffers.
- **IDL (IDLE) -** illuminates when the system is IDLE.

8.3 Expansion Header

A 72-pin Future Bus Expansion Header (Table 3) is provided on the rear panel to allow easy connection to a third-party microprocessor board to allow for the reading and analysis of the data captured by the FPGA.

The Data busses on this header may be configured as follows:

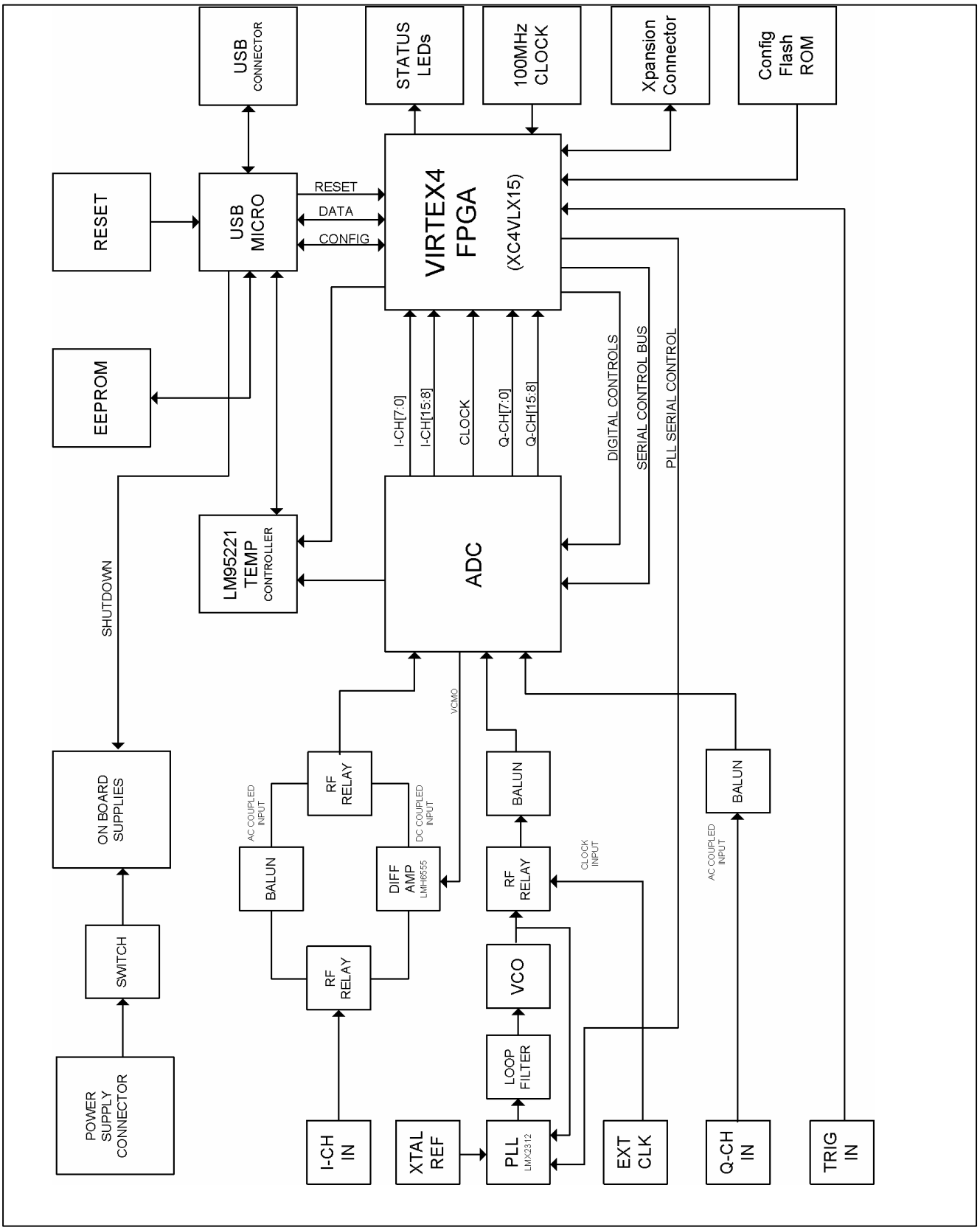
- Two 8-bit busses with LVDS differential signaling, plus two LVDS strobes.
- Four 8-bit busses with LVCMOS (3.3V I/O) signaling plus four CMOS strobes.

All control signals on pins A1 to A15 will be at LVCMOS 3.3V levels.

PIN	DESCRIPTION	PIN	DESCRIPTION
P1_A1	I2C – SDA	P1_B1	GROUND
P1_A2	I2C – SCL	P1_B2	GROUND
P1_A3	SSP – SERIAL DATA	P1_B3	GROUND
P1_A4	SSP – SERIAL CLOCK	P1_B4	GROUND
P1_A5	FPGA RESET	P1_B5	GROUND
P1_A6	READ FIFO	P1_B6	GROUND
P2_A1	WRITE FIFO	P2_B1	GROUND
P2_A2	FIFO FULL	P2_B2	GROUND
P2_A3	FIFO EMPTY	P2_B3	GROUND
P2_A4	ADC DCLK RESET	P2_B4	GROUND
P2_A5	FPGA CONF DONE	P2_B5	GROUND
P2_A6	FPGA JTAG – TMS	P2_B6	GROUND
P3_A1	FPGA JTAG – TCK	P3_B1	GROUND
P3_A2	FPGA JTAG – TDI	P3_B2	GROUND
P3_A3	FPGA JTAG – TDO	P3_B3	GROUND
P3_A4	Not SHUTDOWN	P3_B4	GROUND
P3_A5	3.3V SUPPLY	P3_B5	GROUND
P3_A6	12V SUPPLY	P3_B6	GROUND
P1_C1	DATA BUS A P0 (LVDS or CMOS)	P1_D1	DATA BUS A N0 (LVDS or CMOS)
P1_C2	DATA BUS A P1 (LVDS or CMOS)	P1_D2	DATA BUS A N1 (LVDS or CMOS)
P1_C3	DATA BUS A P2 (LVDS or CMOS)	P1_D3	DATA BUS A N2 (LVDS or CMOS)
P1_C4	DATA BUS A P3 (LVDS or CMOS)	P1_D4	DATA BUS A N3 (LVDS or CMOS)
P1_C5	DATA BUS A P4 (LVDS or CMOS)	P1_D5	DATA BUS A N4 (LVDS or CMOS)
P1_C6	DATA BUS A P5 (LVDS or CMOS)	P1_D6	DATA BUS A N5 (LVDS or CMOS)
P2_C1	DATA BUS A P6 (LVDS or CMOS)	P2_D1	DATA BUS A N6 (LVDS or CMOS)
P2_C2	DATA BUS A P7 (LVDS or CMOS)	P2_D2	DATA BUS A N7 (LVDS or CMOS)
P2_C3	INPUT STROBE P	P2_D3	INPUT STROBE N
P2_C4	DATA BUS B P0 (LVDS or CMOS)	P2_D4	DATA BUS B N0 (LVDS or CMOS)
P2_C5	DATA BUS B P1 (LVDS or CMOS)	P2_D5	DATA BUS B N1 (LVDS or CMOS)
P2_C6	DATA BUS B P2 (LVDS or CMOS)	P2_D6	DATA BUS B N2 (LVDS or CMOS)
P3_C1	DATA BUS B P3 (LVDS or CMOS)	P3_D1	DATA BUS B N3 (LVDS or CMOS)
P3_C2	DATA BUS B P4 (LVDS or CMOS)	P3_D2	DATA BUS B N4 (LVDS or CMOS)
P3_C3	DATA BUS B P5 (LVDS or CMOS)	P3_D3	DATA BUS B N5 (LVDS or CMOS)
P3_C4	DATA BUS B P6 (LVDS or CMOS)	P3_D4	DATA BUS B N6 (LVDS or CMOS)
P3_C5	DATA BUS B P7 (LVDS or CMOS)	P3_D5	DATA BUS B N7 (LVDS or CMOS)
P3_C6	OUTPUT STROBE P	P3_D6	OUTPUT STROBE N

Table 3. Future bus expansion header pins

8.4 System Block Diagram



9.0 Appendix B - Installing and running the WaveVision4 software

9.1 Installing the WaveVision Software

1. Insert the WaveVision CD-ROM into the computer's CD-ROM drive.
2. The WaveVision software requires a Java™ Runtime Environment or Java™ Development Kit, Version 1.4 or higher, from Sun Microsystems, Inc. For detailed information on WaveVision's use of Java technology, see Section 10.2. If the computer does not have this software, the WaveVision installer will instruct you on how to install it.
3. Locate and run the **WaveVision4 Setup.exe** program on the CD-ROM.
4. Follow the on-screen instructions to finish the install.

9.2 Java™ Technology

The WaveVision software uses Sun Microsystems® Java technology. The underlying Java software must be installed on the computer in order for the WaveVision software to run. The software can run on top of either the Java Runtime Environment (JRE) or the Java Development Kit (JDK), Version 1.4 or higher. A suitable copy of the JRE is included on the WaveVision CD-ROM.

The WaveVision installer will first search for an existing copy of the JRE or JDK on the computer. If neither is found, the installer will prompt you to first install a JRE. To do this, run the **`J2RE*.exe`** installer program which may be found on the CD-ROM. Follow the on-screen instructions to finish the install.

After a suitable JRE or JDK is installed, run the WaveVision installer again. The installer will detect the Java software and configure the WaveVision software to use it.

Java technology can allow software to run on different platforms. However, the WaveVision software contains Windows-specific hardware interface code and is therefore only supported under Windows.

9.3 Automatic Device Detection and Configuration

The WaveVision system provides automatic hardware detection and configuration for the device under test. The FPGA is re-programmed automatically by the host PC when the Development board is turned on.

Normally, the configuration process is completely transparent to the user and requires no intervention. However, this process can be overridden, if required, by specifying a new Xilinx configuration image. To do this, select the **Xilinx Image Settings** button (Figure 14) within the Capture Setting window (**Settings** ? **Capture Settings**).

Figure 14. Selecting Xilinx image settings

9.4 Windows Driver

The WaveVision software communicates with the WaveVision hardware through the Windows device driver software. If you are unable to connect to the WaveVision board after installing the software, do the following to uninstall and reinstall the driver:

1. Find the Windows **Control Panel** and select **System**. If you are using Windows 2000/XP, select the **Hardware** tab.
2. Click on **Device Manager** and scroll down to the **Universal Serial Bus controllers**.
3. With the WaveVision board connected, an unknown device will be listed.
4. Right click on the unknown device and uninstall the driver.
5. Unplug the USB cable from the board.
6. Plug in USB cable to the board again to reinstall the driver.

10.0 Appendix C - Using WaveVision Plots

The WaveVision software provides several tools to manipulate the plot view. A toolbar appears above each plot, similar to Figure 15.

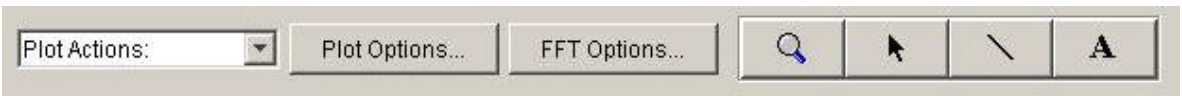


Figure 15. WaveVision plot tools

Seen from left to right, the following tools are available:

- **Plot Actions menu:** This menu contains commands that pertain to this particular plot. You may export the plot data to a file, print it, save it as a graphic, or change the plot's colors.

- **Plot Options**: This button opens a dialog box with options that pertain to this particular plot. You may turn off labels, annotations, or other elements in this dialog. The WaveVision software maintains default options for new plots. You may edit the default options by choosing **Default Plot Options** from the **Settings** menu.

- **FFT Options:** The toolbar shown in Figure 15 is from an FFT plot, and thus contains a button to edit the options for the FFT calculation. Depending upon the type of plot, various options will be present on the toolbar. Please consult the appropriate section below for more information about these options.

- **Magnifying glass tool:** This tool allows you to zoom in and out to see fine details in the plot. Click and drag a box from upper-left to lower-right to zoom in on the region of interest. Click and drag a box from lower-right to upper-left to zoom out. **With the magnifying glass tool selected, click the right mouse button to return to a full view.**

- **Arrow Tool:** The arrow tool is used to select, move, and edit annotations. To edit an annotation, double click it with the arrow tool. To delete an annotation, select it with the arrow tool and press the **Delete** key on your keyboard.

- **Line Annotation Tool:** To draw lines on the plot, select this tool. Drag to draw new lines. To add arrowheads or fix the endpoints of the line, double-click the appropriate end with the arrow tool.

- **Text Annotation Tool:** To draw labels on the plot, select this tool and click at the desired location in the plot. To edit the justification, location, or text of an annotation, double-click it with the arrow tool.

10.1 The Waveform Plot

The Waveform plot displays the raw samples collected from the hardware. This plot is primarily used to verify the integrity of collected data. The waveform is the best view in which to diagnose a distorted signal, an irregular clock, a low-amplitude signal, and many other common ADC system problems.

The Waveform plot also quickly shows how much of the ADC's dynamic range the analog input signal occupies.

10.2 The FFT Plot

The WaveVision software automatically computes a Fast Fourier Transform (FFT) of the sample set, and displays the results in an FFT plot. The resulting FFT plot is, in many respects, the heart of the software because it shows the frequency content of the analog input signal. It marks the fundamental frequency, and a selectable number of harmonics. It also labels their order and frequencies. It shows the power in the fundamental and harmonics. Hover the mouse cursor over a harmonic to display information about it.

The FFT may be used to diagnose common ADC problems such as input spectral impurity, clock phase noise, and clock jitter. The FFT plot also shows several statistics on the quality and purity of the collected samples including SNR, SINAD, THD, SFDR, and ENOB. These statistics are to be interpreted with the following definitions (which are repeated in every National Semiconductor ADC datasheet):

- **Signal to Noise Ratio (SNR)** is the ratio, expressed in dB, of the RMS value of the input signal to the RMS value of the sum of all other spectral components below one-half the sampling frequency, not including harmonics or DC.

- **Signal to Noise Plus Distortion (S/N+D or SINAD)** Is the ratio, expressed in dB, of the RMS value of the input signal to the RMS value of all of the other spectral components below half the clock frequency, including harmonics but excluding DC.

- **Total Harmonic Distortion (THD)** is the ratio, expressed in dBc, of the RMS total of the first five harmonic levels at the output to the level of the fundamental at the output. THD is calculated as

$$\mathrm{THD} = 20\log\sqrt{\frac{f_2^{\,2} + \cdots + f_N^{\,2}}{f_1^{\,2}}}$$

  where f_1 is the RMS power of the fundamental (output) frequency and f_2 through f_N are the RMS power in the first N harmonic frequencies.

- **Spurious-Free Dynamic Range (SFDR)** is the difference, expressed in dB, between the RMS values of the input signal and the peak spurious signal, where a spurious signal is any signal present in the output spectrum that is not present at the input.

- **Effective Number of Bits (ENOB, or Effective Bits)** is another method of specifying Signal-to-Noise and Distortion or SINAD. ENOB is defined as

$$ENOB = \frac{SINAD - 1.76}{6.02}$$

  and says that the converter is equivalent to a perfect ADC of this (ENOB) number of bits.

10.3 FFT Options

FFT plots can be configured in many different ways. Clicking the **FFT Options** button at the top of the plot will display a dialog showing the options for that particular plot. The software also maintains default options for new FFT plots, which are editable. The default FFT options may be edited by choosing **Default FFT Options** from the **Settings** menu. The options are:

- **Windowing:** You may choose from one of five different window functions. The window function is applied to the samples before computing the FFT to compensate for the fact that the sample set may not be an integral number of wavelengths of the input signal. In general, Flat-Top will give the best results, but it may be easier to compare data with other systems when the windowing functions are the same.

- **dB Scale:** You may select to represent power on the FFT in dBc (decibels relative to carrier), in which 0 dB is taken to be the fundamental (carrier) power, or dBFS (decibels relative to full-scale), in which 0 dB is taken to the be power contained in a signal which uses the entire dynamic range of the ADC.

- **Harmonics:** You may select the number of harmonics recognized (and labeled) by the software. You may also select the number of FFT bins excluded around harmonics in, for example, SNR calculations. The exclusion region around each harmonic will be shown in a different color than the rest of the data points.

- **IMD Calculations:** The WaveVision software is capable of performing Intermodulation Distortion calculations. When two fundamental frequencies within 3 dBFS are present in the waveform, the software will normally perform IMD calculations. You may inhibit this behavior by deselecting the **Allow IMD calculation** checkbox. When the IMD calculation is enabled, you may also select whether the software will include only 2nd order or both 2nd and 3rd order terms.

10.4 Histogram Plots

Histogram plots are created by counting the number of times each ADC output code appears in a dataset. Histograms may be computed by software, or by hardware. A software histogram is computed from a dataset which is normally 128k samples or smaller. A hardware histogram is collected directly by the hardware, and may include millions of counts per code. The resulting histogram will show discontinuities between comparators, gain or offset errors, and other common ADC system problems.

The Histogram plot also displays the number of codes that were never counted (missing codes), followed by the first ten such missing codes.

10.5 Information Viewer

The information viewer is not a plot, but it displays a variety of useful information about the dataset, such as the sampling rate, and any warnings generated by the software. You may also store comments about the dataset here, to be saved in a WaveVision file.

10.6 Data Import and Export

The WaveVision software provides a variety of means to share data with others, in both textual and graphical formats.

The most flexible way to import data into the software is from a tab-delimited ASCII text file. The contents can be either a sample set or a histogram, provided with or without time information. The simplest example of this would be a file with a single column of samples. You may open tab-delimited text files by choosing **Open** from the **File** menu; you can interleave data from multiple columns and/or files. You can choose **Reopen** to reopen the same file later with the same settings (for example, if you update the file with new data),

There are a variety of ways to export data from the software:

- Save the file as a normal WV4 (*.wv4) file. WV4 files are ASCII, tab-delimited text files. Samples are stored one per line in a single column. You can open a WV4 file directly into a spreadsheet program.
- Save the file as a TXT (*.txt) file. You will produce a one- or two-column tab-delimited ASCII text file of samples or histogram information, without the header information that is contained in a WV4 file.
- You can export the contents of an individual plot by choosing **Export Data** from the plot's **Plot Actions** menu. The format of the data is always tab-delimited ASCII text.
- You can export a plot as either a GIF (*.gif) or Encapsulated Postscript (*.eps) graphic by choosing **Export Plot as Graphic** from the plot's **Plot Actions** menu. GIF files are suitable for the web or for emails. Encapsulated Postscript files are high-resolution scalable files suitable for direct publication.