太欣半導體股份有限公司
SYNTEK SEMICONDUCTOR CO., LTD.

STK6037

80C51-based microcontroller

- **16K flash memory**
- **In-system programming**
- **IAP programming**
- **Main Data Memory: 256 bytes**
- **AUX Memory: 320 bytes**
- **Timers 0, 1, 2, 3**
- **Watchdog timer**
- **UART0 and UART1**
- **10-bit ADC**
- **21-channel, 10-bit PWM**
- **Ports：1, 2, 3 (different options)**
- **Low voltage detection and reset**
- **Operating voltage: 4.2 ~ 5.6 volts**
- **Operating temp. : -40 ~ +85°C**
- **ESD: > 4 KV (HBM)**

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1 FEATURES

- 80C51 Central Processing Unit (CPU).
  - Option for multiple CPU clock (XTAL1, XTAL1 x 2, XTAL 1 / 3, or XTAL 1 / 48).
  - Industrial standard 80C51 instruction set.
  - Normal mode, idle mode, and stop mode.
- Program Memory : 16 kbytes on-chip flash memory.
  - with hardware ISP (In-System Programming).
  - In-Application Progamming
  - Program code protection.
- Main Data RAM: 256 bytes (upper 128 + lower 128 bytes) of on-chip SRAM.
- Aux Memory (AUX RAM): 320 bytes of SRAM.
- Stretched memory cycle for the MOVX instruction.
- SFRs (Special Function Register): 98 SFRs.
- Timers: Timer 0, Timer 1, Timer 2, and Timer 3.
- On-chip Watchdog Timer.
- Full-duplex UART: UART0 and UART1
- Three I/O ports: Port 1, Port 2, and Port 3.
- On-chip power-on-reset with low-voltage detection and reset.
- Interrupts: 8 sources, 2 priority level, 8 vectored addresses.
- Software enable/disable of ALE output pulse to reduce EMI.
- 4-channel, 10-bit ADC.
- 21-channel, 10-bit PWM.
- CPU operating frequency range: 2 to 30 MHz
- Operating temperature range: -40 to +85°C
- Operating voltage range: 4.2 to 5.6 V.
- ESD: ≥4 KV (HBM).
- EFT: ≥4 KV .
- Latch-up: 150 mA.
- Relibility of 16K flash memory:
  - Data retention: 10 years at room temperature.
  - Number of read/write cycle: > 20K.
- Available in 5 types of green package: DIP28, SOP28, SSOP28, DIP20, and SOP20.

2 ORDERING INFORMATION

Table 1 Ordering information

TYPE NUMBER	PACKAGE	OUTLINE DRAWING
STK6037ASO20G	SOP 20 pin (Green package)	please refer to Figure 40 on page 112.
STK6037ADI20G	DIP 20 pin (Green package)	please refer to Figure 41 on page 113.
STK6037ASO28G	SOP 28 pin (Green package)	please refer to Figure 42 on page 114.
STK6037AKDI28G	SKINNY 28 pin (Green package)	please refer to Figure 44 on page 116.
STK6037A1S28G	SSOP 28 pin (Green package)	Please refer to Figure 43 on page 115.

3 FUNCTIONAL BLOCK DIAGRAM

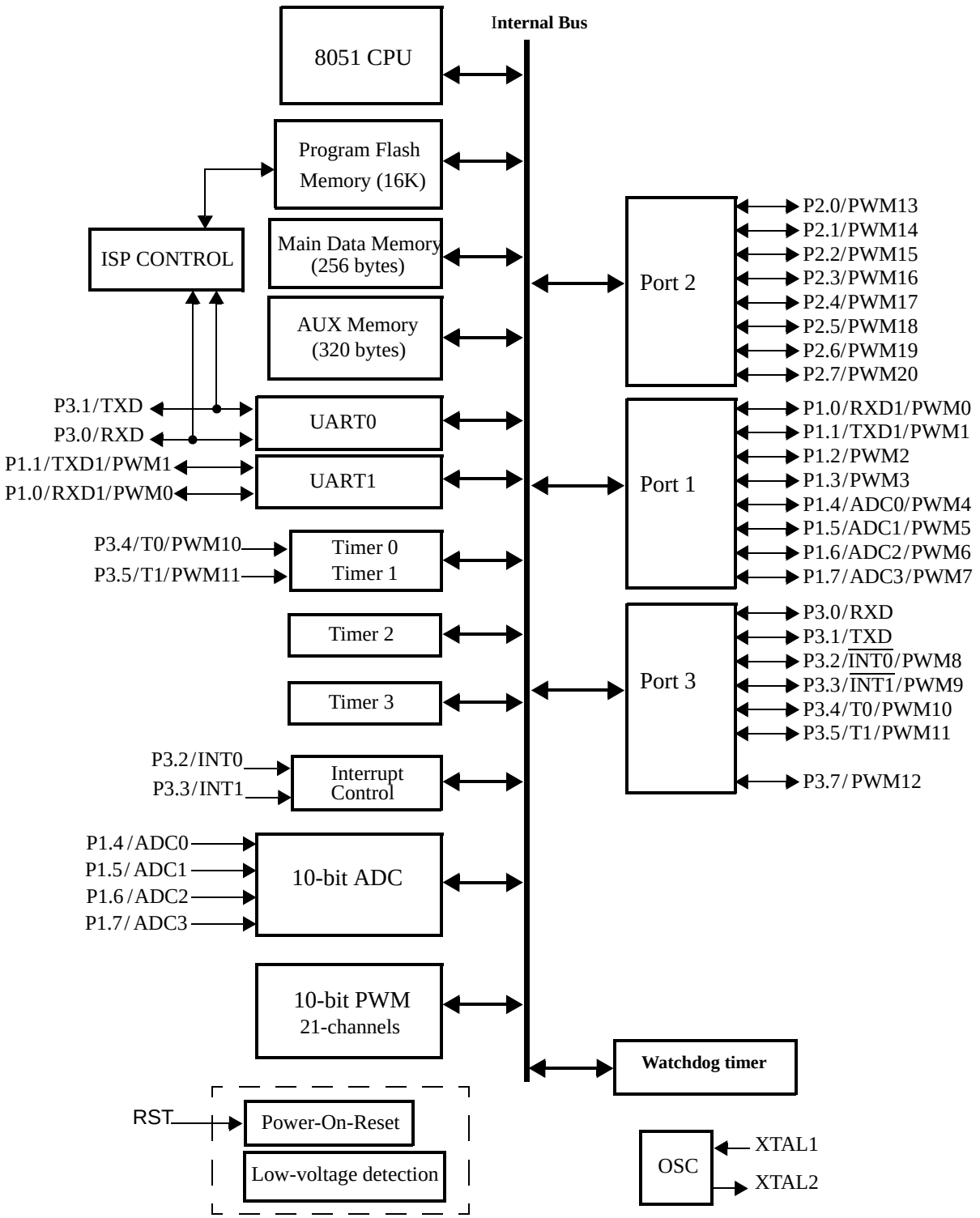


Fig.1 Functional block diagram

4 PINNING INFORMATION

4.1 Pinning diagram (DIP20 and SOP20)

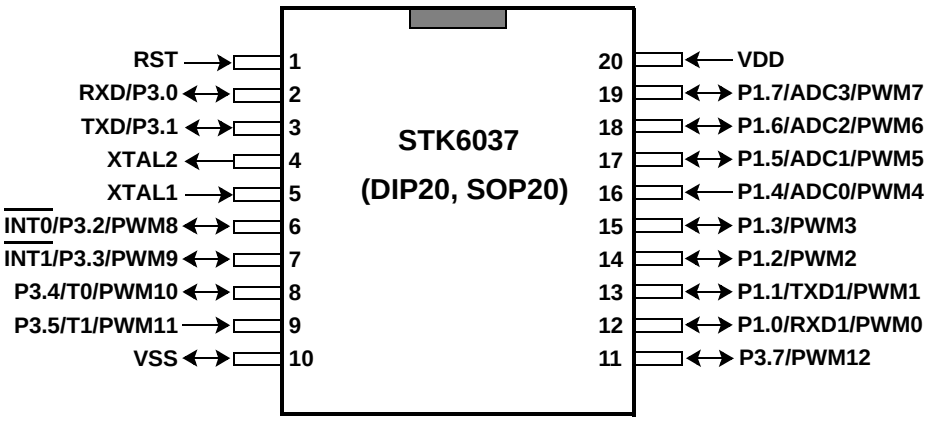


Fig.2 Pin configuration of DIP20 and SOP20 package.

4.2 Pinning diagram (package of SOP28, DIP28, and SSOP28)

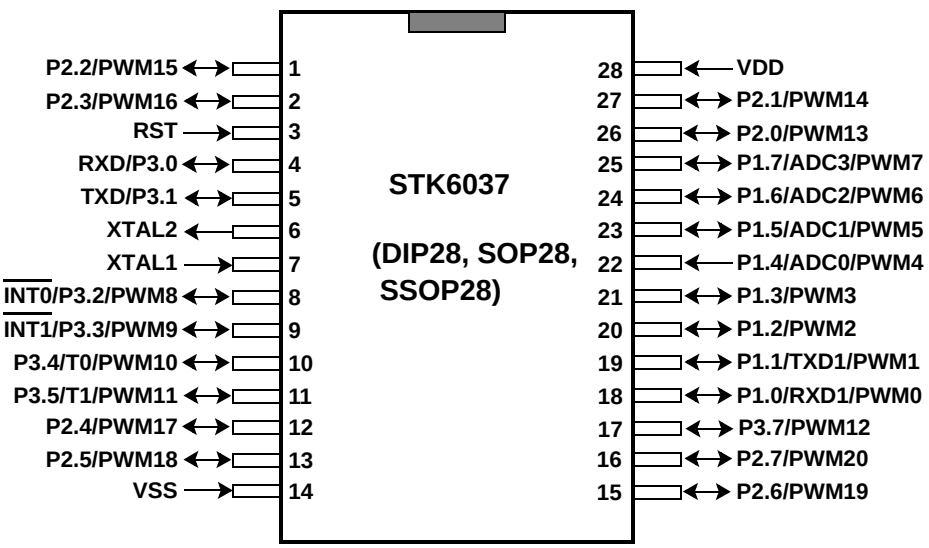


Fig.3 Pin configuration of SOP28, DIP28, and SSOP28

4.3 Pin description

Table 2 Pin description for 28-pin packages

To avoid a latch-up effect at power-on: V_{SS} – 0.5 V < voltage at any pin at any time < V_{DD} + 0.5 V .

SYMBOL	PIN	TYPE	DESCRIPTION
P2.0/PWM13, P2.1/PWM14, P2.2/PWM15, P2.3/PWM16, P2.4/PWM17, P2.5/PWM18, P2.6/PWM19, P2.7/PWM20,	26, 27,1, 2, 12, 13, 15, 16	I/O	Port 2 pins or PWM output pins.
RST	3	I	External reset input pin, active HIGH. A HIGH level on this pin for at least 8 XTAL1 clocks, while the oscillator is running, resets the STK6037.
P3.0/RXD	4	I/O	Bit 0 of Port 3 or data receiver pin of the UART0.
P3.1/TXD	5	I/O	Bit 1 of Port 3 or data transmitter pin of the UART0.
P3.2/$\overline{\text{INT0}}$/PWM8	8	I/O	Bit 2 of Port 3 or input of External Interrupt 0, or PWM8 output.
P3.3/$\overline{\text{INT1}}$/PWM9	9	I/O	Bit 3 of Port 3 or input of External interrupt 1, or PWM9 output.
P3.4/T0/PWM10	10	I/O	Bit 4 of Port 3 or Timer 0 input, or PWM10 output.
P3.5/T1/PWM11	11	I/O	Bit 5 of Port 3 or Timer 1 input or PWM11 output.
P3.7/PWM12	5	I/O	Bit 7 of Port 3 or PWM12 output.
XTAL2	6	O	**Crystal pin 2:** output of the inverting amplifier that forms the oscillator. This pin should be left open-circuit when an external oscillator clock is used.
XTAL1	7	I	**Crystal pin 1:** input to the inverting amplifier that forms the oscillator. Receives the external oscillator clock signal when an external oscillator is used.
VSS	14	I	Ground pin.
VDD	28		Power supply.
P1.0/RXD1/PWM0	18	I/O	This pin has three functions: • Bit 0 of Port 1, or • PWM0 output, or • Receiver pin of UART1.
P1.1/TXD1/PWM1	19	I/O	Bit 1 of Port 1, or Transmitter pin of UART1, or PWM1 output.
P1.2/PWM2, P1.3/PWM3,	21, 20,	I/O	Bit 2, 3 of Port 1 or outputs of PWM 2, 3.
P1.4/ADC0/PWM4 P1.5/ADC1/PWM5 P1.6/ADC2/PWM6 P1.7/ADC3/PWM7	22, 23, 24, 25	I/O	These pins have three functions: • Bit 4 ~ 7 of Port 1, or • Outputs of PWM 4 ~ 7, or • Input pins of ADC 0~ 3.

5 CENTRAL PROCESSING UNIT (CPU)

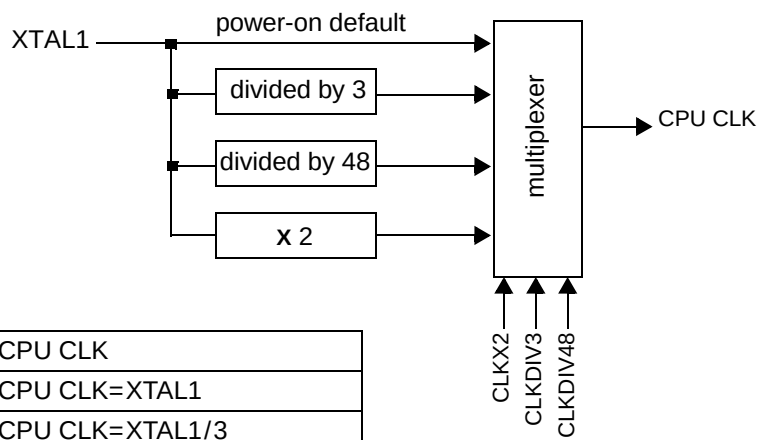
5.1 Instruction Set and addressing modes

The STK6037's instruction set and addressing modes are completely compatible with that of industrial standard 80C51. User codes written in traditional 80C51 instruction set can be ported directly to the STK6037. Howerver, due to difference in CPU instruction clocks and timing, applications in which timer loops are used may need modification in the number of loops.

For a description of instruction set, please refer to Chapter 24, *Instruction set*.

5.2 CPU clock and Chip Configuration Register (SFR CHIPCON)

The CPU clock of the STK6037 can be selected by use of bit 5, bit 2, and bit 1 of the Chip Configuration Register (SFR CHIPCON), as illustrated in Fig.4.



CPU clock selection

CLKDIV48	CLKX2	CLKDIV3	CPU CLK
0	0	0	CPU CLK=XTAL1
0	0	1	CPU CLK=XTAL1/3
1	0	0	CPU CLK=XTAL1/48
0	1	0	CPU CLK=XTAL1 X 2

Note: The default after power-on-reset is: CPU CLK = XTAL1.

Fig.4 CPU clock selection

The Chip Configuration Register (SFR CHIPCON, at SFR map address BF hex) controls the following:

- Enable or disable the on-chip AUX memory access,
- Enable or disable of the ALE output,
- Selection of CPU clock, and
- Enable or disable of low-power reset.
- Enable or disable Timer 3

Table 3 Chip Configuration Register

Chip Configuraton Register (SFR CHIPCON), located at BF hex of the SFR map, Read/Write								
Bit Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Mnemonics	x	T3EN	CLKDIV48	XRAMEN	X	CLKX2	CLKDIV3	LVR
Reset value	x	0	0	1	x	0	0	0

Table 4 Description of Chip Configuration Register (CHIPCON)

MNEMONIC	BIT POSITION	FUNCTION
	CHIPCON.7	Not implemented.
T3EN	CHIPCON.6	Enable or disable Timer 3. If T3EN=1, the selected CPU clock is added to Timer 3. If T3EN=0, the selected CPU clock is not added to Timer 3.
CLKDIV48	CHIPCON.5	Enable or disable the option of dividing XTAL1 clock by 48.
XRAMEN	CHIPCON.4	Enable or disable of the on-chip AUX memory access. • XRAMEN= 1 enables the read/write access to the on-chip AUX memory. • XRAMEN= 0 disable the read/write access to the address AUX memory.
	CHIPCON.3	Not implemented.
CLKx2	CHIPCON.2	Bits CLKDIV48, CLKx2, and CLKDIV3 are used to select CPU clock frequecny. The CPU clock can be selected to be XTAL1, XTAL1÷3, XTAL1÷48, or XTAL1**x**2, by programming bits CLKDIV48, CLKx2, and CLKDIV3. The default after power-on-reset is: CPU CLK = XTAL1. Please refer to Fig.4. for selected CPU frequency versus programmed value.
CLKDIV3	CHIPCON.1	
LVR	CHIPCON.0	Enable the low-voltage reset function. • LVR=0 enables the low-voltage reset function. • LVR=1 disables the low-voltage reset funcion.

5.3 Instruciton Cycle

The STK6037's CPU has a **pipe-line architecture**, and therefore execution of instructions are overlapped. While the CPU is executing the current instruction, the next instruction is also being fetched. The nominal instruction cycle is 4 CPU clocks. In each instruction cycle, the ALE signal rise to HIGH at the begining of the cycle and stays high for 1.5 CPU clocks.

The following diagram illustrates the relation among system clock (CPU CLK), instruciton cycle, CPU cycle, and ALE. Simple instructions can be executed in just one instruction cycle, which consists of 4 CPU clocks.

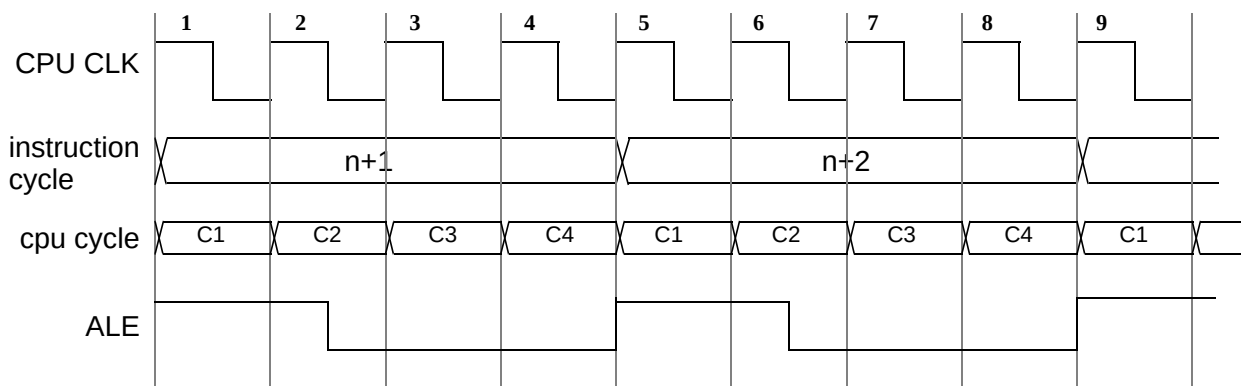


Fig.5 CPU instruction cycle.

5.4 Program Status Word

The current state of the CPU is reflected in the Program Status Word (PSW) register, which is located at SFR address D0(hex).

Table 5 Program Status Word

PROGRAM STATUS WORD (SFR PSW), LOCATED AT D0H OF THE SFR MAP								
Bit Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Mnemonics	CY	AC	F0	RS1	RS0	OV	F1	P

Table 6 Description of Program Status Word (PSW)

MNEMONIC	BIT POSITION	FUNCTION
CY	PSW.7	Carry flag. The Carry flag receives Carry-out from bit 7 of ALU. It is set to HIGH, when last arithmetic operation resulted in a carry (during addition) or borrow (during subtraction); otherwise, it is cleared to LOW by all arithmetic operations.
AC	PSW.6	Auxiliary Carry Flag. Auxiliary Carry Flag receives Carry-out from bit 3 of addition operands. It is set to HIGH, when last arithmetic operation resulted in a carry into (during addition) or borrow from (during subtraction) the high-order nibble; otherwise, it is cleared to LOW by all arithmetic operations
F0	PSW.5	General purpose flag. This bit is uncommitted and may be used as general purpose status flag.
RS1, RS0	PSW.4, PSW.3	Register Bank select control bits. • RS1, RS0 = 00 selects register bank 0, address 00h ~ 07h. • RS1, RS0 = 01 selects register bank 1, address 08h ~ 0Fh. • RS1, RS0 = 10 selects register bank 2, address 10h ~ 17h. • RS1, RS0 = 11 selects register bank 3, address 18h ~ 1Fh.
OV	PSW.2	Overflow flag. This bit is set to HIGH, when last arithmetic operation resulted in a carry (addition), borrow (subtraction), or overflow (multiply or divide); otherwise, it is cleared to LOW by all arithmetic operation.
F1	PSW.1	General purpose flag. This bit is uncommitted and may be used as general purpose status flag.
P	PSW.0	Parity flag. Set/Clear by hardware each instruction cycle to indicate an odd/even number of 1s in the accumulator, i.e., even parity.

6 MEMORY ORGANIZATION

The STK6037 has 4 blocks of memory phyically implemented on-chip. These are:

- 16384 bytes of flash program memory,
- 256 bytes of Main Data Memory,
- 320 bytes of AUX memory, and
- 98 bytes of Special Function Register.

The following diagram shows the overall memory spaces available in the microcontroller.

(1) The area drawn for each memory block is not proportional to its physical size.

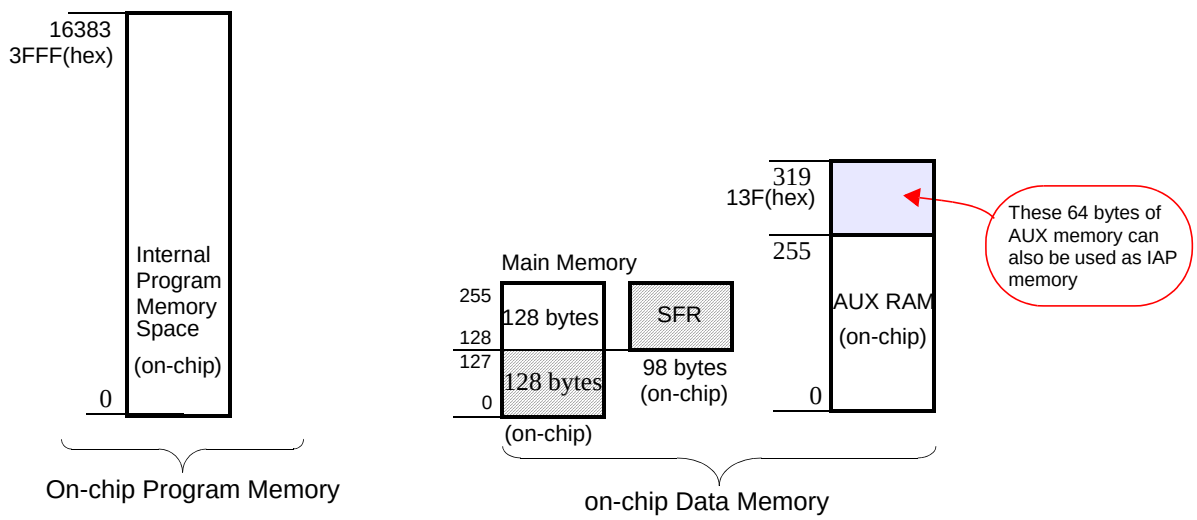


Fig.6 The phyical memories implemented on-chp

6.1 Program Memory

6.1.1 PRORAM ROM SPACE

The STK6037 CPU can fetches instructions only from the 16K on-chip program memory. The memory adddress range is from 0000(hex) to 3FFF(hex). As Port 0 is not implemented, it is impossible to expand memory space by adding external memory.

6.1.2 ISP PRGRAMMING FOR THE 16K FLASH MEMORY

The on-chip program memory is implemented using flash memory, with ISP (In-System Programming) capability. Detailed description of ISP programming is given in another document.

6.1.3 ROM CODE PROTECTION

ROM code protection is implemented in the 16K flash memory.

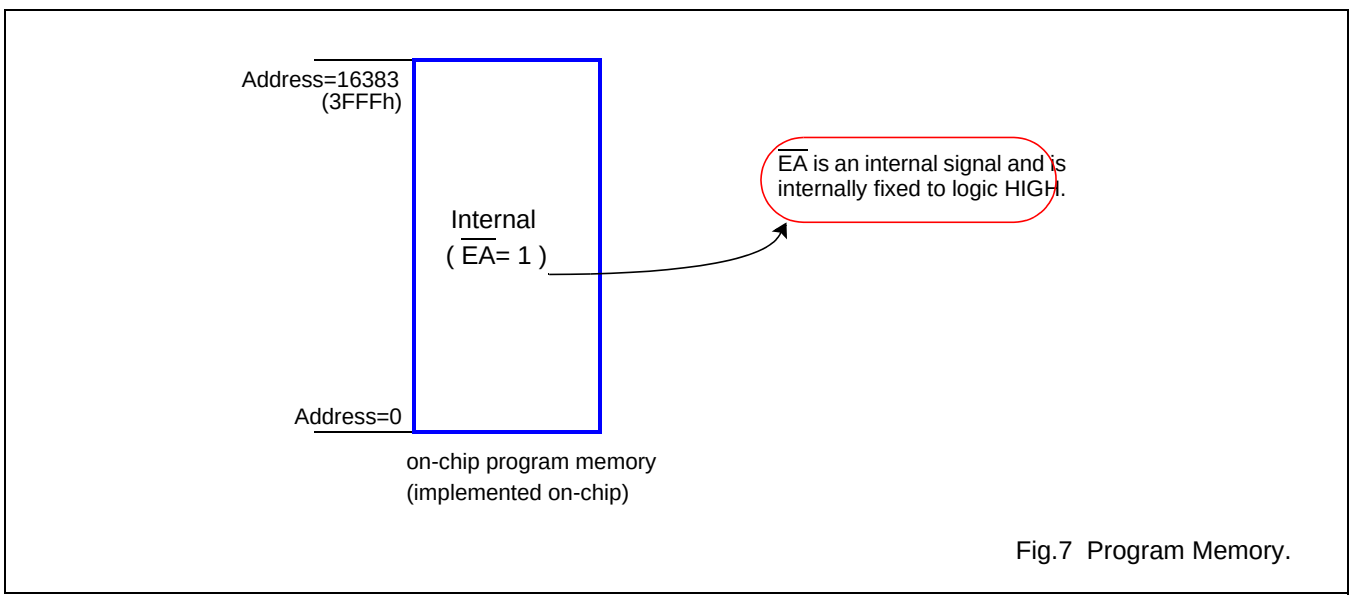
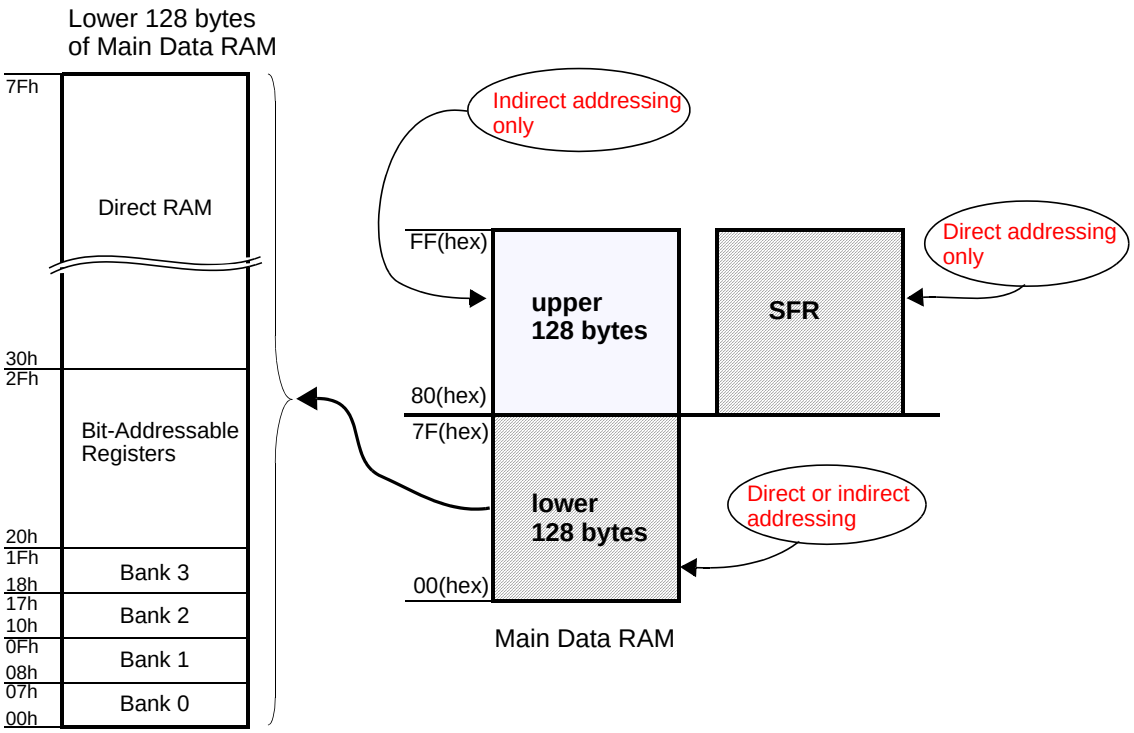


Fig.7 Program Memory.

6.2 Main Data RAM and Special Function Register (SFR)

The STK6037 has 256 bytes of on-chip Main Data RAM and 98 bytes of SFR. Although the Main Data RAM and the SFRs shares overlapped memory space, they are two physically separate blocks. The upper 128 bytes of the Main Data RAM, from address 80H to FFH can be accessed only by **Indirect Addressing**. The lower 128 bytes of the Main RAM, from address 00H to 7FH, can be accessed by **Direct Addressing** or **Indirect Addressing**.

The SFRs occupy the address range from 80H to FFH and are only accessible using **Direct Addressing**.



PSW SFR		
Bit 4	Bit 3	selected bank
1	1	3
1	0	2
0	1	1
0	0	0

Fig.8 Main Data Memory and SFRs

6.2.1 THE LOWER 128 BYTES OF THE MAIN DATA RAM

The lower 128 bytes are organized as shown in Fig.8. The lower 32 bytes form 4 banks of eight registers (R0 - R7). Two bits on the Program Status Word (PSW) select which bank is active (in use). The next 16 bytes, from 20 (hex) to 2F (hex) , form a block of bit-addressable memory space, at bit address 00(hex) ~ 07(hex).

6.3 AUX Memory

6.3.1 AUX Memory space

The STK6037 has 320 bytes of auxiliary memory (AUX RAM) implemented on-chip. This memory can be accessed by use of MOVX instruction. It is not possible to expand the AUX memory space by adding off-chip memory, because Port 0 is not implemented.

The MOVX @Ri instruction, where i=0 or 1, can access only the lower 256-bytes of the on-chip AUX RAM. The MOVX @DTPR instruction can access all 320 bytes of AUX memory.

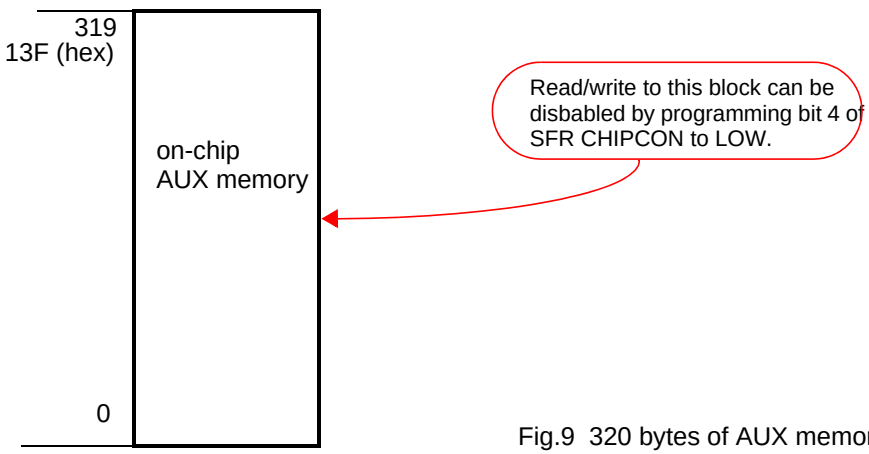


Fig.9 320 bytes of AUX memory

6.3.2 On-chip AUX Memory

The on-chip AUX RAM from address 0 to address 319 can be accessed by the CPU as normal data memory, by performing a MOVX instructon. Read/Write access to this memory can be disabled by setting bit 4 of the SFR CHIPCON to LOW. Please refer to Table 3 and Table 4 for detailed description of the SFR CHIPCON.

When executing MOVX instruction from the 16K program memory, an access (read or write) to the 320-bytes AUX RAM do not affect the status of pin P3.7.

6.3.3 Dual Data Pointer (Data Pointer 0 and Data Pointer 1) and DPTR Select Register (SFR DPS)

The STK6037 has two data pointers, Data Pointer 0 and Data Pointer 1. Data Pointer 0 is the traditional 8051 data pointer for MOVX instrucitons. Data Pointer 1 is an extra data pointer for fast moving a block of data. Before executing a MOVX instruction, an active data pointer must be selected by programming the Data Pointer Select Register (SFR DPS). Please refer to Table 7 for detailed description of SFR DPS.

Table 7 Data Pointer 0, Data Pointer 1, and DPTR Select Register

Address (Hex)	**R/W**	**SYMBOLS**	**DESCRIPTION**	Reset Value
82	R/W	DPL0	Data Pointer 0 Low (traditional 80C51 data pointer)	0000 0000
83	R/W	DPH0	Data Pointer 0 High (traditional 80C51 data pointer)	0000 0000
84	R/W	DPL1	Data Pointer 1 Low (extra data pointer), specific to the STK6037.	0000 0000
85	R/W	DPH1	Data Pointer 1 High (extra data pointer), specific to the STK6037.	0000 0000
86	R/W	DPS	DPTR Select Register (DPS), specific to the STK6037. The DPS register has only one bit. Only its bit 0, called SEL bit, is implemented on-chip. When SEL=0, instructions that use the DPTR will use SFR DPL0 and SFR DPH0. When SEL=1, instructions that use the DPTR will use SFR DPL1 and SFR DPH1. Bits 7~1 of SFR DPS can not be written to, and, when read, always return a 0 for any of these 7 bits.	0000 0000

All DPTR-related instrucitons use the currently selected data pointer. To switch the active pointer, toggle the SEL bit, by use of the instruciton INC DPS. The 6 instructions that use the DPTR are given in the following table. An active DPTR must be selected before executing these intructions.

Table 8 Instructions that use the DPTR

INSTRUCITON	**DESCRIPTION**
INC DPTR	Increment the data pointer by1.
MOV DPTR, #data16	Load the DPTR with a 16-bit constant.
MOVC A, @ A+DPTR	Move code byte relative to DPTR to Accumulator (ACC).
MOVX A, @DPTR	Move AUX Memory byte (16-bit address) to Accumulator (ACC)
MOVX @DPTR, A	Move ACC to AUX memory byte.
JMP @ A+DPTR	Jump indirect relative to DPTR.

Table 9 Clock Control Register, SFR CKCON

Clock Control Register (SFR CKCON), located at 8E(hex) of the SFR map								
Bit Address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Mnemonics	Reserved		T2M	T1M	T0M	Reserved	Reserved	Reserved
Reset value	0	0	0	0	0	0	0	1

Table 10 Description of the CKCON Register

MNEMONIC	BIT POSITION	FUNCTION
T2M	CKCON.5	Select Timer 2 clock frequecny. When T2M=0, Timer 2 uses (CPU CLK / 12) as clock frequency. When T2M=1, Timer 2 uses (CPU CLK / 4) as clock frequency.
T1M	CKCON.4	Select Timer 1 clock frequecny. When T1M=0, Timer 1 uses (CPU CLK / 12) as clock frequency. When T1M=1, Timer 1 uses (CPU CLK / 4) as clock frequency.
T0M	CKCON.3	Select Timer 0 clock frequecny. When T0M=0, Timer 0 uses (CPU CLK / 12) as clock frequency. When T0M=1, Timer 0 uses (CPU CLK / 4) as clock frequency.

7 SPECIAL FUNCTION REGISTERS

The STK6037 has 98 Special Function Registers (SFR).

7.1 SFR allocation table

Table 11 SFR allocation table

F8	EIP	PWM0H	PWM0L	PWM1H	PWM1L	PWM2H	PWM2L	
F0	B	PWM3H	PWM3L	PWM4H	PWM4L	PWM5H	PWM5L	
E8	EIE	PWM6H	PWM6L	PWM7H	PWM7L	PWM8H	PWM8L	
E0	ACC	WDT	ISPSLV	ISPEN	IAPEN	IAP_ADRL	IAP_ADRH	
D8	EICON		ADCSEL	ADCVALH	ADCVALL			
D0	PSW	P1_OPT	PWM_EA0	PWM_EA1	PWM_EA2			
C8	T2CON	T2MOD	RCAP2L	RCAP2H	TL2	TH2		
C0	SCON1	SBUF1						
B8	IP	PWM9H	PWM9L	PWM10H	PWM10L	PWM11H	PWM11L	CHIPCON
B0	P3	PWM12H	PWM12L	PWM13H	PWM13L	PWM13H	PWM14L	PCLKSEL
A8	IE	PWM15H	PWM15L	PWM16H	PWM16L	PWM17H	PWM17H	
A0	P2	PWM18H	PWM18L	PWM19H	PWM19L	PWM20H	PWM20L	
98	SCON0	SBUF0	TL3	TH3				
90	P1	EXIF						
88	TCON	TMOD	TL0	TL1	TH0	TH1	CKCON	
80	P0	SP	DPL0	DPH0	DPL1	DPH1	DPS	PCON

7.2 SFR Map Overview (98 SFRs)

Table 12 The SFR Map

Address (Hex)	R/W	SYMBOLS	DESCRIPTION	Reset Value
80	R/W	P0	Port 0 output latch (bit-addressable). *(not implemented, but reserved))*	1111 1111
81	R/W	SP	Stack Pointer	0000 0111
82	R/W	DPL0	Data Pointer 0 Low (traditional 80C51 data pointer)	0000 0000
83	R/W	DPH0	Data Pointer 0 High (traditional 80C51 data pointer)	0000 0000
84	R/W	DPL1	Data Pointer 1 Low (extra data pointer), specific to the STK6037.	0000 0000
85	R/W	DPH1	Data Pointer 1 High (extra data pointer), specific to the STK6037.	0000 0000
86	R/W	DPS	DPTR Select Register (DPS), specific to the STK6037.	0000 0000
87	R/W	PCON	Power Control Register.	0011 0000
88	R/W	TCON	Timer0/1 Control Register (bit-addressable)	0000 0000
89	R/W	TMOD	Timer0/1 Mode Register	0000 0000
8A	R/W	TL0	Timer0, Low byte	0000 0000
8B	R/W	TL1	Timer1, Low byte	0000 0000
8C	R/W	TH0	Timer0, High byte	0000 0000
8D	R/W	TH1	Timer1, High byte	0000 0000
8E	R/W	CKCON	Clock Control register, specific to the STK6037. The register is for controlling the frequency of the clock added to Timer 0, Timer 1, and Timer 2, and memory stretch cycle for the MOVX instruction.	0000 0001
8F	not used			
90	R/W	P1	Port 1 output latch (bit-addressable).	1111 1111
91	R/W	EXIF	Extended Interrupt Flag register	00001000
92	not used			
93, 94, 95, 96, 97, not implemented.				
98	R/W	SCON0	UART0 (Serial Port 0) Control/Status Register (bit-addressable)	0000 0000
99	R/W	SBUF0	UART0 (Serial Port 0) Buffer Register	0000 0000
9A	R/W	TL3	Timer 3 low byte.	0000 0000
9B	R/W	TH3	Timer 3 high byte.	0000 0000
9C, 9D, 9E, 9F not used				
A0	R/W	P2	Port 2 output latch (bit-addressable)	1111 1111
A1	R/W	PWM18H	PWM18 high byte.	1000 0000
A2	R/W	PWM18L	PWM18 low byte.	00xx xxxx
A3	R/W	PWM19H	PWM19 high byte.	1000 0000
A4	R/W	PWM19L	PWM19 low byte.	00xx xxxx
A5	R/W	PWM20H	PWM20 high byte.	1000 0000
A6	R/W	PWM20L	PWM20 low byte.	00xx xxxx
A7 not used.				
A8	R/W	IE	Interrupt Enable Register (bit-addressable)	0000 0000

Address (Hex)	R/W	SYMBOLS	DESCRIPTION	Reset Value
A9	R/W	PWM15H	PWM15 high byte.	1000 0000
AA	R/W	PWM15L	PWM15 low byte.	00xx xxxx
AB	R/W	PWM16H	PWM16 high byte.	1000 0000
AC	R/W	PWM16L	PWM16 low byte.	00xx xxxx
AD	R/W	PWM17H	PWM17 high byte.	1000 0000
AE	R/W	PWM17L	PWM17 low byte.	00xx xxxx
AF not used.				
B0	R/W	P3	Port 3 output latch (bit-addressable)	1111 1111
B1	R/W	PWM12H	PWM12 high byte.	1000 0000
B2	R/W	PWM12L	PWM12 low byte.	00xx xxxx
B3	R/W	PWM13H	PWM13 high byte.	1000 0000
B4	R/W	PWM13L	PWM13 low byte.	00xx xxxx
B5	R/W	PWM14H	PWM14 high byte.	1000 0000
B6	R/W	PWM14L	PWM14 low byte.	00xx xxxx
B7	R/W	PCLKSEL	PWM clock frequency setting	0000 0000
B8	R/W	IP	Interrupt Priority Register (bit-addressable)	1000 0000
B9	R/W	PWM9H	PWM9 high byte.	1000 0000
BA	R/W	PWM9L	PWM9 low byte.	00xx xxxx
BB	R/W	PWM10H	PWM10 high byte.	1000 0000
BC	R/W	PWM10L	PWM10 low byte.	00xx xxxx
BD	R/W	PWM11H	PWM11 high byte.	1000 0000
BE	R/W	PWM11L	PWM11 low byte.	00xx xxxx
BF	R/W	CHIPCON	Chip Configuration Register	x001 x000
C0	R/W	SCON1	UART1 (ie., Serial Port 1) Control/Status Register	0000 0000
C1	R/W	SBUF1	UART1 (ie., Serial Port 1) Buffer Register	0000 0000
C2, C3, C4, C5, C6, C7, not used.				
C8	R/W	T2CON	Timer 2 Control Register (bit-addressable)	0000 0000
C9	R/W	T2MOD	Timer 2 Mode Control Register	0000 xxx1
CA	R/W	RCAP2L	Timer 2 Reload Capture Register, Low byte	0000 0000
CB	R/W	RCAP2H	Timer 2 Reload Capture Register, High byte	0000 0000
CC	R/W	TL2	Timer 2, Low byte	0000 0000
CD	R/W	TH2	Timer 2, High byte	0000 0000
CE, CF not used.				
D0	R/W	PSW	Program Status Word Register (bit-addressable)	0000 0000
D1	R/W	P1_OPT	Selecting Port 1 pin function, as Port or ADC input pin.	xxxx 0000
D2	R/W	PWM_EA0	Enable PWM 0~7 outputs.	0000 0000
D3	R/W	PWM_EA1	Enable PWM 8~15 outputs.	0000 0000
D4	R/W	PWM_EA2	Enable PWM 16~20 outputs.	xxx0 0000
D5, D6, D7not used.				
D8	R/W	EICON	Extended Interrupt Control register.	0000 0000
D9 not used				
DA	R/W	ADCSEL	Select a channel as ADC input and enable ADC	0xx0 0000

Address (Hex)	**R/W**	**SYMBOLS**	**DESCRIPTION**	Reset Value
DB	R	ADCVALH	Buffer for storing the upper 8 bits (Bits 9 ~ 2)of the 10-bit ADC.	0000 0000
DC	R	ADCVALL	Buffer for storing the lower 2 bits (Bits 1 ~ 0) of the 10-bit ADC	xxxx xx00
DD, DE, DF not used.				
E0	R/W	ACC	Accumulator (bit-addressable)	0000 0000
E1	R/W	WDT	Watchdog Timer Control.	00xx x000
E2	R/W	ISPSLV	ISP Control Slave address	0000 0000
E3	R/W	ISPEN	ISP Enable register (write 93hex to enable the ISP mode)	0000 0000
E4	R/W	IAPEN	IAP ENable register.	0000 xxxx
E5	R/W	IAP_ADRL	Low-byte address of the flash memory location for IAP.	0000 0000
E6	R/W	IAP_ADRH	High-byte address of the flash memory location for IAP.	0000 0000
E7 not used.				
E8	R/W	EIE	Extended Interrupt Enable register.	1110 0000
E9	R/W	PWM6H	PWM6 high byte.	1000 0000
EA	R/W	PWM6L	PWM6 low byte.	00xx xxxx
EB	R/W	PWM7H	PWM7 high byte.	1000 0000
EC	R/W	PWM7L	PWM7 low byte.	00xx xxxx
ED	R/W	PWM8H	PWM8 high byte.	1000 0000
EE	R/W	PWM8L	PWM8 low byte.	00xx xxxx
EF not used.				
F0	R/W	B	B Register (bit-addressable)	0000 0000
F1	R/W	PWM3H	PWM3 high byte.	1000 0000
F2	R/W	PWM3L	PWM3 low byte.	00xx xxxx
F3	R/W	PWM4H	PWM4 high byte.	1000 0000
F4	R/W	PWM4L	PWM4 low byte.	00xx xxxx
F5	R/W	PWM5H	PWM5 high byte.	1000 0000
F6	R/W	PWM5L	PWM5 low byte.	00xx xxxx
F7 not used.				
F8	R/W	EIP	Extended Interrupt Priority register.	1110 0000
F9	R/W	PWM0H	PWM0 high byte.	1000 0000
FA	R/W	PWM0L	PWM0 low byte.	00xx xxxx
FB	R/W	PWM1H	PWM1 high byte.	1000 0000
FC	R/W	PWM1L	PWM1 low byte.	00xx xxxx
FD	R/W	PWM2H	PWM2 high byte.	1000 0000
FE	R/W	PWM2L	PWM2 low byte.	00xx xxxx
FF not used.				

7.3 SFR of Each Functional Block

Table 13 SFR related to each functional block

BLOCK	SYMBOL	NAME	Address (Hex format)	RESET VALUE
CPU	ACC	Accumulator.	E0	0000 0000
	B	B register	F0	0000 0000
	SP	Stack Pointer	81	0000 0111
	DPL0	Data Pointer 0, Low byte	82	0000 0000
	DPH0	Data Pointer 0, High byte	83	0000 0000
	DPL1	Data Pointer 1, Low byte	84	0000 0000
	DPH1	Data Pointer 1, High byte	85	0000 0000
	DPS	Selection for active Data Pointer	86	0000 0000
	PCON	Power Control Register	87	0011 0000
	PSW	Program Status Word	D0	0000 0000
	CHIPCON	Chip Configuration Register	BF	x001 x000
	CKCON	Clock Control Register	8E	0000 0001
Interrupt System	IE	Interrupt Enable register	A8	0000 0000
	IP	Interrupt Priority register	B8	x000 0000
	EXIF	Extended Interrupt Flag register	91	0000 1000
	EICON	Extended Interrupt Control register	D8	0000 0000
	EIE	Extended Interrupt Enable register	E8	110 0000
	EIP	Extended Interrupt Priority register	F8	1110 0000
Ports	P1	Port 1 latch	90	1111 1111
	P1_OPT	Port 1 pin option for Port or ADC input.	D1	xxxx 0000
	P2	Port 2 latch	A0	1111 1111
	P3	Port 3 latch	B0	1111 1111
UART0	SBUF0	Serial Port 0 Buffer Register	99	0000 0000
	SCON0	Serial Port 0 Control/Status Register	98	0000 0000
UART1	SBUF1	Serial Port 1 Buffer Register	C1	0000 0000
	SCON1	Serial Port 1 Control/Status Register	C0	0000 0000
Timer 0 / Time 1	TCON	Timer 0/1 Control Register	88	0000 0000
	TMOD	Timer 0/1 Mode Register	89	0000 0000
	TL0	Timer 0, Low byte	8A	0000 0000
	TL1	Timer 1, Low byte	8B	0000 0000
	TH0	Timer 0, High byte	8C	0000 0000
	TH1	Timer 1, High byte	8D	0000 0000
	CKCON	Clock Control Register	8E	0000 0001

BLOCK	SYMBOL	NAME	Address (Hex format)	RESET VALUE
Timer 2	T2CON	Timer 2 Control Register	C8	0000 0000
	T2MOD	Timer 2 Mode Control Register	C9	0000 xxx1x
	RCAP2L	Timer 2 Reload Capture Register, Low byte	CA	0000 0000
	RCAP2H	Timer 2 Reload Capture Register, High byte	CB	0000 0000
	TL2	Timer 2, Low byte	CC	0000 0000
	TH2	Timer 2, High byte	CD	0000 0000
	CKCON	Clock Control Register	8E	0000 0001
Timer 3	TL3	Timer 3, Low byte.	9A	0000 0000
	TH3	Timer 3, High byte.	9B	0000 0000
Watchdog Timer	WDT	Watchdog Timer Control Register	E1	00xx x000
PWM	PWM_EA0	PWM Enable Register 0	D2	0000 0000
	PWM_EA1	PWM Enable Register 1	D3	0000 0000
	PWM_EA2	PWM Enable Register 2	D4	0000 0000
	PCLKSEL	PWM clock setting register	B7	0000 0000
	PWM0H	PWM0 high byte	F9	1000 0000
	PWM0L	PWM0 low byte	FA	00xx xxxx
	PWM1H	PWM1 high byte	FB	1000 0000
	PWM1L	PWM1 low byte	FC	00xx xxxx
	PWM2H	PWM2 high byte	FD	1000 0000
	PWM2L	PWM2 low byte	FE	00xx xxxx
	PWM3H	PWM3 high byte	F1	1000 0000
	PWM3L	PWM3 low byte	F2	00xx xxxx
	PWM4H	PWM4 high byte	F3	1000 0000
	PWM4L	PWM4 low byte	F4	00xx xxxx
	PWM5H	PWM5 high byte	F5	1000 0000
	PWM5L	PWM5 low byte	F6	00xx xxxx
	PWM6H	PWM6 high byte	E9	1000 0000
	PWM6L	PWM6 low byte	EA	00xx xxxx
	PWM7H	PWM7 high byte	EB	1000 0000
	PWM7L	PWM7 low byte	EC	00xx xxxx
	PWM8H	PWM8 high byte	ED	1000 0000
	PWM8L	PWM8 low byte	EE	00xx xxxx
	PWM9H	PWM9 high byte	B9	1000 0000
	PWM9L	PWM9 low byte	BA	00xx xxxx
	PWM10H	PWM10 high byte	BB	1000 0000
	PWM10L	PWM10 low byte	BC	00xx xxxx
	PWM11H	PWM11 high byte	BD	1000 0000
	PWM11L	PWM11 low byte	BE	00xx xxxx
	PWM12H	PWM12 high byte	B1	1000 0000

BLOCK	SYMBOL	NAME	Address (Hex format)	RESET VALUE
PWM	PWM12L	PWM12 low byte	B2	00xx xxxx
	PWM13H	PWM13 high byte	B3	1000 0000
	PWM13L	PWM13 low byte	B4	00xx xxxx
	PWM14H	PWM14 high byte	B5	1000 0000
	PWM14L	PWM14 low byte	B6	00xx xxxx
	PWM15H	PWM15 high byte	A9	1000 0000
	PWM15L	PWM15 low byte	AA	00xx xxxx
	PWM16H	PWM16 high byte	AB	1000 0000
	PWM16L	PWM16 low byte	AC	00xx xxxx
	PWM17H	PWM17 high byte	AD	1000 0000
	PWM17L	PWM17 low byte	AE	00xx xxxx
	PWM18H	PWM18 high byte	A1	1000 0000
	PWM18L	PWM18 low byte	A2	00xx xxxx
	PWM19H	PWM19 high byte	A3	1000 0000
	PWM19L	PWM19 low byte	A4	00xx xxxx
	PWM20H	PWM20 high byte	A5	1000 0000
	PWM20L	PWM20 low byte	A6	00xx xxxx
ADC	P1_OPT	Select Port 1 function as Port or ADC input	D1	xxxx 0000
	ADCSEL	Select ADC input channel for conversion	DA	0xx0 0000
	ADCVALH	Buffer for the uppper 8 bits of the converted ADC value.	DB	0000 0000
	ADCVALL	Buffer for the lower 2 bits of the converted ADC value.	DC	xxxx xx00
ISP	ISPSLV	ISP Control slave address	E2	0000 0000
	ISPEN	Write 93 (hex) to enable the ISP mode	E3	0000 0000
IAP	IAPEN	IAP ENable register	E4	0000 xxxx
	IAP_ADRL	Low-byte address of the flash memory location for IAP.	E5	0000 0000
	IAP_ADRH	High-byte address of the flash memory location for IAP.	E6	0000 0000

8 INTERRUPTS

8.1 General Description

Table 14 gives an overview of the interrupt system, as implemented in the STK6037.

Table 14 Overview of the interrupt system

Source number	Interrupt sources	Flags generated by the interrupt	Interrupt enable bit	Interrupt priority bit	Priority within level	Vector Address (hex)
1	External Interrupt 0	IE0 (TCON.1)	EX0 (IE.0)	PX0 (IP.0)	1 (the highest)	03
2	Timer 0 Overflow	TF0 (TCON.5)	ET0 (IE.1)	PT0 (IP.1)	2	0B
3	External Interrupt 1	IE1 (TCON.3)	EX1 (IE.2)	PX1 (IP.2)	3	13
4	Timer 1 Overflow	TF1 (TCON.7)	ET1 (IE.3)	PT1 (IP.3)	4	1B
5	UART0 Interrupt (UART0 receive or transmit)	TI_0 (SCON0.1) / RI_0 (SCON0.0)	ES0 (IE.4)	PS0 (IP.4)	5	23
6	Timer 2 overflow / T2EX pin	TF2 (T2CON.7) / EXF2 (T2CON.6)	EX2 (IE.5)	PT2 (IP.5)	6	2B
7	UART1 Interrupt (UART1 receive or transmit)	TI_1 (SCON1.1) / RI_1 (SCON1.0)	ES1 (IE.6)	PS1 (IP.6)	7	3B
8	External Interrupt 2 (Timer 3 overflow)	EXIF.4	EX2 (EIE.0)	PX2 (EIP.0)	8	43
9	External Interrupt 4 (ADC data ready)	EXIF.6	EX4 (EIE.2)	PX4 (EIP.2)	10	53

Note:

1. Because Timer2 overflow and T2EX share the same interrupt vector address 002BH, it is the responsibility of software programmer to check individual interrupt flag to see which one caused the interrupt.
2. Timer 3 overflow interrupt shares with External Interrupt 2. But, External Interrupt 2 is not connected to an external pin.
3. ADC Data Ready shares with External Interrupt 4. But, External Interrupt 4 is not connected to an external pin.

8.2 Interrupt Enable Registers: SFR IE and SFR EIE

Each of the interrupt sources can be individually enabled or disabled by setting its enable/disable bit in the Interrupt Enable Registers SFR IE and SFR EIE.

All interrupts can be globally enabled or disabled by clearing the EA bit of SFR IE. Enabling an interrupt is a two-steps procedure. First the interrupt must be globally enabled. Second, the desired interrupt must be enabled.

The Interrupt Enable Registers are described in Table 15, Table 16, Table 17, and Table 18.

Table 15 Interrupt Enable Register SFR IE

INTERRUPT ENABLE REGISTER (SFR IE), LOCATED AT A8H OF THE SFR MAP								
Bit Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Mnemonics	EA	ES1	ET2	ES0	ET1	EX1	ET0	EX0
Reset value	0	0	0	0	0	0	0	0

Table 16 Description of Interrupt Enable Register SFR IE

MNEMONIC	BIT POSITION	FUNCTION
EA	IE.7	Global enable or disable of all interrupts. When IE.7 = 0, all interrupts are globally disabled. When IE.7 = 1, all interrupt sources are ***globaly*** enabled.
ES1	IE.6	Enable or disable serial port 1 (UART1) ES1=0 disables serial port 1 interrupt (TI_1 and RI_1). ES1=1 enables serial port 1 interrupt (TI_1 and RI_1).
EX2	IE.5	Enable or disable interrupt due to Timer 2 overflow, or T2EX pin (shared with P1.1) interrupt. When IE.5 = 1, external interrupt 2 is enabled. When IE.5 = 0, external interrupt 2 is disabled.
ES0	IE.4	Enable or disable UART0 interrupt. When IE.4 = 1, UART0 interrupt is enabled. When IE.4 = 0, UART0 interrupt is disabled.
ET1	IE.3	Enable Timer 1 overflow interrupt. When IE.3 = 1, Timer 1 overflow interrupt is enabled. When IE.3 = 0, Timer 1 overflow interrupt is disabled.
EX1	IE.2	Enable External Interrupt 1. When IE.2 = 1, External Interrupt 1 is enabled. When IE.2 = 0, External Interrupt 1 is disabled.
ET0	IE.1	Enable Timer 0 overflow interrupt. When IE.1 = 1, Timer 0 overflow interrupt is enabled. When IE.1 = 0, Timer 0 overflow interrupt is disabled.
EX0	IE.0	Enable External Interrupt 0. When IE.0 = 1, External Interrupt 0 is enabled. When IE.0 = 0, External Interrupt 0 is disabled.

Table 17 Extended Interrupt Enable Register SFR EIE

EXTENDED INTERRUPT ENABLE REGISTER (SFR EIE), LOCATED AT E8H OF THE SFR MAP								
Bit Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Mnemonics	reserved.			Reserved	Reserved	EX4	Reserved	EX2
Reset value	read as 1.			0	0	0	0	0

Table 18 Description of Extended Interrupt Enable Register SFR EIE

MNEMONIC	BIT POSITION	FUNCTION
bits 5, 6, 7 not implemented.		
EX4	EIE.2	Enable ADC Data Ready interrupt. When EIE.2 = 1, interrupt generated by ADC Data Ready flag is enabled. When EIE.2 = 0, interrupt generated by ADC Data Ready is disabled. ADC Data Ready interrupt is actually external interrupt 4.
EX2	EIE.0	Enable Timer 3 overflow interrupt. When EIE.0 = 1, Timer 3 overflow interrupt is enabled. When EIE.0 = 0, Timer3 overflow interrupt is disabled. Timer 3 overflow interrupt is actually external interrupt 2.

8.3 Interrupt Priority Registers: SFR IP and SFR EIP

Each interrupt source can be assigned one of two priority levels: high and low. Interrupt priority is defined by the Interrupt Priority Registers: SFR IP, at B8 hex , and SFR EIP. Table 19 , Table 20, Table 21, Table 22 give detail description for these two SFRs.

An interrupt's priority depends on it bit value, as shown below:

- logic 0 = low priority
- logic 1 = high priority.

A low priority interrupt may be interrupted by a high priority interrupt. A high priority interrupt cannot be interrupted by any other interrupt source. If two requests of different priority occur simultaneously, the high priority level request is serviced. If requests of the same priority are received simultaneously, an internal polling sequence determines which request is serviced. Thus, within each priority level, there is a second priority structure determined by the polling sequence. This second priority structure is shown in Table 14.

Table 19 Interrupt Priority Register SFR IP

SFR Interrupt Priority Register (SFR IP), located at B8 hex of the SFR map								
Bit Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Mnemonics			PT2	PS0	PT1	PX1	PT0	PX0
Reset value	1	0	0	0	0	0	0	0

Table 20 Description of Interrupt Priority Register SFR IP

MNEMONIC	BIT POSITION	FUNCTION
	IP.7	not implemented, return a 1 when read.
	IP.6	not implemented.
PT2	IP.5	Define the priority of Timer2 overflow interrupt, or T2EX-pin (shared with P1.1) interrupt. When IP.5 = 1, Timer 2 overflow is a high priority interrupt. When IP.5 = 0, Timer 2 overflow is a low priority interrupt.
PS0	IP.4	Define the priority level of UART interrupt. When IP.4 = 1, UART interrupt is a high priority interrupt. When IP.4 = 0, UART interrupt is low priority interrupt.
PT1	IP.3	Define the interrupt level of Timer 1 overflow interrupt. When IP.3 = 1, Timer 1 overflow interrupt is a high priority interrupt. When IP.3 = 0, Timer 1 overflow interrupt is a low priority interrupt.
PX1	IP.2	Define the interrupt level of External Interrupt 1. When IP.2 = 1, External Interrupt 1 is a high priority interrupt. When IP.2 = 0, External Interrupt 1 is a low priority interrupt.
PT0	IP.1	Define the interrupt level of Timer 0 overflow interrupt. When IP.1 = 1, Timer 0 overflow is a high priority interrupt. When IP.1 = 0, Timer 0 overflow is a low priority interrupt.
PX0	IP.0	Define the interrupt level of External Interrupt 0. When IP.0 = 1, External Interrupt 0 is a high priority interrupt. When IP.1 = 0, External Interrupt 0 is a low priority level.

Table 21 Interrupt Priority Register SFR EIP

SFR Interrupt Priority Register (SFR EIP), located at F8 hex of the SFR map								
Bit Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Mnemonics				Reserved	Reserved	PX4	Reserved	PX2
Reset value	Reserved, and read as 1.			0	0	0	0	0

Table 22 Description of Interrupt Priority Register SFR EIP

MNEMONIC	BIT POSITION	FUNCTION
Bits 7, 5, and 6 not implemented.		
PX4	EIP.2	Define the interrupt priority level of ADC Data Ready interrupt. When EIP.2 = 1, ADC Data Ready is a high priority interrupt. When EIP.2 = 0, ADC Data Ready is a low priority interrupt.
PX2	EIP.0	Define the interrupt priority level of Timer 3 overflow. When EIP.0 = 1, Timer 3 overflow is a high priority interrupt. When IP.1 = 0, External Interrupt 0 is a low priority level.

8.4 Interrupt Vectors

The vector indicates the Program Memory location where the appropriate interrupt service routine starts. Please refer to Table 14 for interrupt vector addresses.

8.5 Flag Register of Extended Interrupts: SFR EXIF at address 91 hex

External interrupts 2 and 4 are called extended interrupts and their flags are recorded in SFR EXIF.

Table 23 Flag Register SFR EXIF of Extended Interrupts 2~5

BIT	FUNCTION
EXIF.7	Reserved.
EXIF.6	Flag of External Interrupt 4.
EXIF.5	Reserved.
EXIF.4	Flag of External Interrupt 2.
EXIF 3	Reserved.
EXIF 2~0	Reserved.

9 TIMER/COUNTER 0, TIMER/COUNTER 1

9.1 General Description

There are seven SFRs associtated with Timer/Counter 0 and Timer/Counter 1, as given in Table 24. Both Timer/Counter 0 and Timer/Counter 1 can be configured to operate either as timers or event counters.

Table 24 SFRs associated with Timer/Counter 0 and Timer/Counter 1.

SFR name	Address (hex) in SFR space	**Description**	Reset value (hex)
TL0	8A	These two SFRs are the lower 8 bits and higher 8 bits of Timer/Counter 0.	00
TH0	8C		00
TL1	8B	These two SFRs are the lowr 8 bits and higher 8 bits of Timer/Counter 1.	00
TH1	8D		00
TCON	88	Control register for Timer/Counter 0 and Timer/Counter 1.	00
TMOD	89	Mode selection register for Timer/Counter 0 and Timer/Counter 1.	00
CKCON	8E	Clock frequency selection for Timer/Counter 0 and Timer/Counter 1.	01

Timer/Counter 0 and Timer/Couter 1 can be programmed to work in 4 operating modes:

- Mode 0: 13-bit timer/counter
- Mode 1: 16-bit timer/counter
- Mode 2: 8-bit counter with auto-reload
- Mode 3: Two 8-bit counters (only available from Timer 0)

9.2 Mode Selection Regiser, SFR TMOD (at 89H of SFR space)

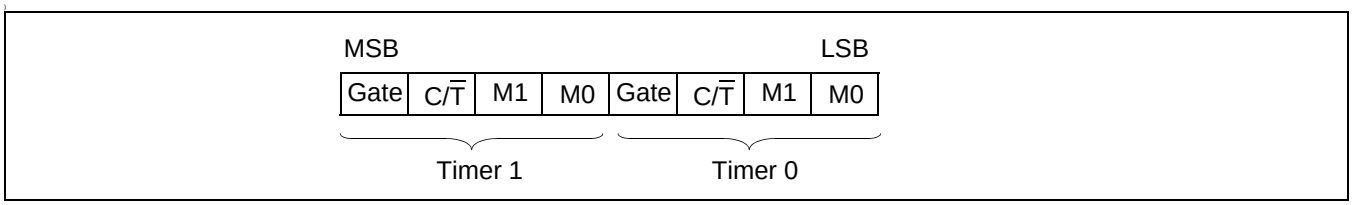


Table 25 Timer 0/1 Mode Selection Register

TIMER 0/1 MODE REGISTER (TMOD), LOCATED AT 89H OF THE SFR SPACE								
Bit Address	TMOD.7	TMOD.6	TMOD.5	TMOD.4	TMOD.3	TMOD.2	TMOD.1	TMOD.0
Mnemonics	Gate (Timer1)	C/T (Timer1)	M1 (Timer1)	M0 (Timer1)	Gate (Timer0)	C/T (Timer0)	M1 (Timer0)	M0 (Timer 0)

Table 26 Description of Timer 0/1 Mode Selection Register

MNEMONIC	BIT POSITION	FUNCTION
GATE	TMOD.7	Gating control for Timer 1. When set, Timer 1 is enabled only while INT1 pin is high and TR1 control bit is set. When cleared, Timer 1 is enabled whenever TR1 control bit is set.
C/$\overline{T}$	TMOD.6	Timer or Counter selection of Timer 1. When set, counter operation is selected. When cleared, timer operation is selected.
M1, M0	TMOD.5 TMOD.4	Mode selection of Timer 1 • (M1, M0) = 00 selects Mode 0 operation. • (M1, M0) = 01 selects Mode 1 operation. • (M1, M0) = 10 selects Mode 2 operation. • (M1, M0) = 11 selects Mode 3 operation.(In mode 3, Timer/Counter 1 is stopped.)
GATE	TMOD.3	Gating control for Timer 0. When set, Timer 0 is enabled only while INT0 pin is high and TR0 control bit is set. When cleared, Timer 0 is enabled whenever TR0 control bit is set.
C/T	TMOD.2	Timer or Counter selection of Timer 0. When set, counter operation is selected. When cleared, timer operation is selected.
M1, M0	TMOD.1, TMOD.0	Mode selection of Timer 0 • (M1, M0) = 00 selects Mode 0 operation. • (M1, M0) = 01 selects Mode 1 operation. • (M1, M0) = 10 selects Mode 2 operation. • (M1, M0) = 11 selects Mode 3 operation. (In mode 3, Timer/Counter 1 is stopped.)

9.3 Timer 0/1 Control Register (SFR TCON at 88 H of the SFR space)

Table 27 Timer 0/1 Control Register

TIMER 0/1 CONTROL REGISTER (TCON), LOCATED AT 88H OF THE SFR SPACE								
Bit Address	TCON.7	TCON.6	TCON.5	TCON.4	TCON.3	TCON.2	TCON.1	TCON.0
Mnemonics	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0

Table 28 Description of Timer 0/1 Control Register

MNEMONIC	BIT POSITION	FUNCTION
TF1	TCON.7	Timer 1 overflow flag. Set by hardware on Timer/Counter 1 overflow. Cleared by hardware when processor vectors to interrupt routine, or clearing the bit in software.
TR1	TCON.6	Timer 1 Run control bit. Set/cleared by software to turn Timer/Counter on/off.
TF0	TCON.5	Timer 0 overflow flag. Set by hardware on Timer/Counter 0 overflow. Cleared by hardware when processor vectors to interrupt routine, or clearing the bit in software.
TR0	TCON.4	Timer 0 Run control bit. Set/cleared by software to turn Timer/Counter on/off.
IE1	TCON.3	External Interrupt 1 Flag. Set by hardware when external interrupt 1 is detected. This bit is cleared after the interrupt is processed. That is, when the Return from Interrupt instruction is executed.
IT1	TCON.2	Interrupt 1 Type Control bit. Set/cleared by software to specify falling edge/low level triggered external interrupt.
IE0	TCON.1	External Interrupt 0 Flag. Set by hardware when external interrupt 0 is detected. This bit is cleared after the interrupt is processed. That is, when the Return from Interrupt instruction is executed.
IT0	TCON.0	Interrupt 0 Type Control bit. Set/cleared by software to specify falling edge/low level triggered external interrupt.

9.4 Clock Control Register, SFR CKCON, at address 8E hex of the SFR map

For a description of the Clock Control Regsiter, please refer to Table 3 and Table 4.

9.5 Operating Modes

9.5.1 MODE 0 (13-BIT TIMER/COUNTER)

When in mode 0, either of Timer 0 and Timer1 acts as a 13-bit counter. Fig.10 shows the operation of both Timer 0 and Timer 1 in mode 0 operation.

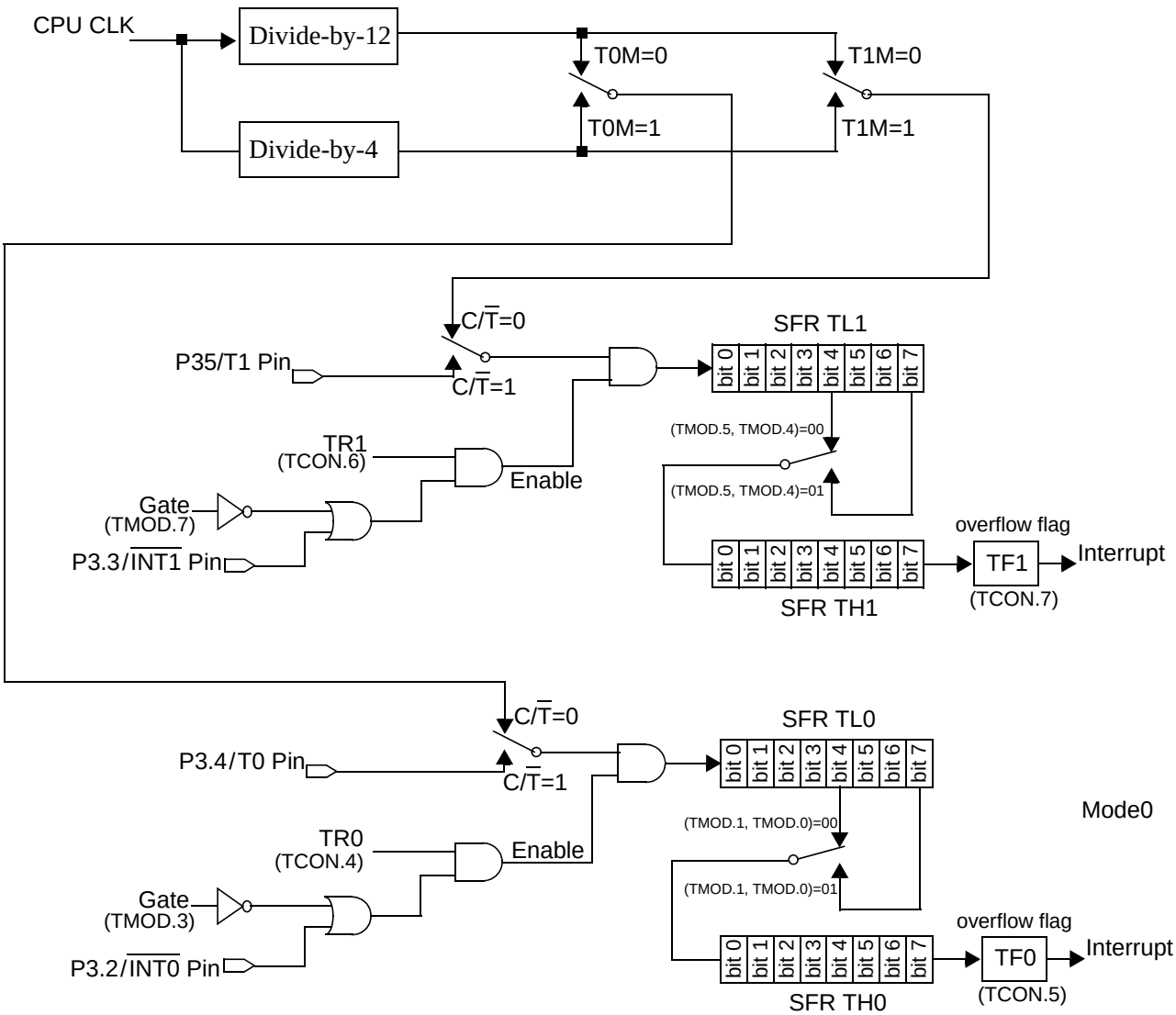


Fig.10 Mode 0 (13-bit timer/counter) and Mode 1 (16-bit timer/counter)

In this mode, the **Timer 0/Timer 1** registers are configured as a 13-bit register, which is composed of all the 8 bits of the TH1 (TH0) and the lower 5 bits of TL1 (TL0). The upper 3 bits of the TL1 (TL0) are indeterminate. The Timer Interrupt flag TF1 (TF0) is set to HIGH when the 13-bit register, acting as a counter, rolls over from all 1s to all 0s.

The 13-bit register(counter) is enabled only under the following conditions:

1. TR0 (TR1)=1, and
2. Either Gate=0 or $\overline{\text{INT1}}$ ($\overline{\text{INT0}}$)=1.

9.5.2 MODE 1 (16-BIT TIMER/COUNTER)

The configuration and operation of Mode 1 is the same as that of Mode 0, except that the registers are now 16 bits, instead of 13 bits when in Mode 0. Please refer to Fig.10.

9.5.3 MODE 2 (8-BIT COUNTER WITH AUTO-RELOAD)

Mode 2 configures the SFR TL0 and SFR TL1 as an 8-bit counter, respectively, with automatic reloading from SFR TH0 and SFR TH1, respectively. When the contents of TL1(TL0) changes from all 1s to all 0, the corresponding flags TF1 (TF0) is set to HIGH and the content of TH1(TH0) is reloaded into TL1 (TL0).The action of this reloading does not change the content TH1(TH0). The content of TH1 (TH0) can only be changed via programming these two SFRs.

As illustrated in Fig.10 and Fig.11, the control (enable) signal for mode 0, mode 1 and mode 2 are all the same.

Fig.11 shows the operation of Timer 0 and Timer 1 in mode 2.

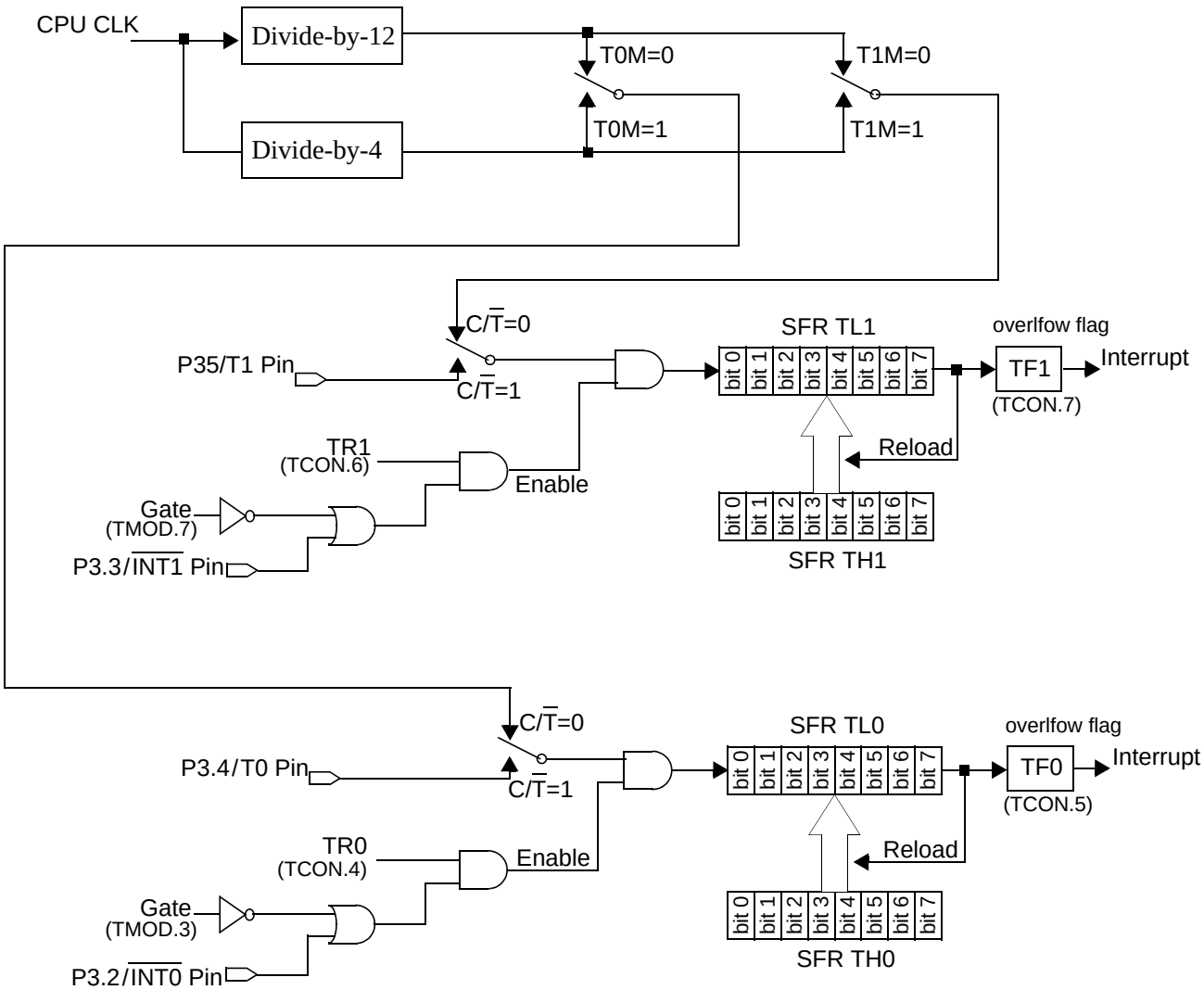


Fig.11 Mode 2 operation of Timer 0, Timer 1.

9.5.4 MODE 3 (TWO 8-BIT COUNTERS FROM TIMER 0)

When in Mode 3, Timer 1 stops counting and holds it value, and Timer 0 is configured into two separate counters: **TL0** and **TH0**. The logic of Timer 0 in Mode 3 is shown below.

TL0 uses the Timer 0 control bits: C/T, GATE, TR0, INT0, and TF0. TH0 is configured into a timer function(counting machines cycles) and takes over the use of TR1 and TF1 from Timer 1. Hence, TH0 now controls the Timer 1 interrupt.

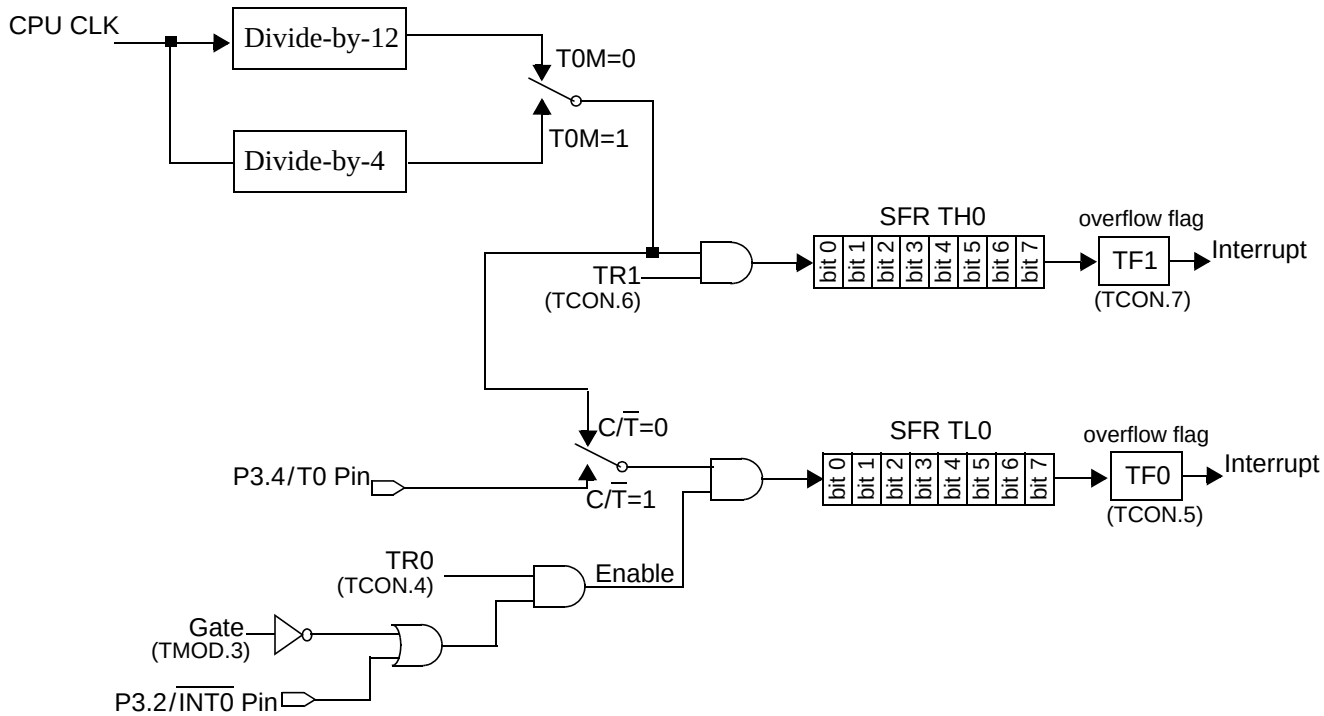


Fig.12 Mode 3 operation of Timer 0, Timer 1

10 TIMER/COUNTER 2

10.1 General Description and operation modes

Timer 2 is mainly composed of four SFRs, TH2, TL2, RCAP2L, RCAP2H, and their contorl logic.

SFR TH2 and SFR TL2 are cascaded into a 16-bit timer or counter, called Timer 2, which can be driven by either CPU clock or off-chip clock pulse.

SFR RCAP2L and SFR RCAP2H are cascaded into a 16-bit register. This register is used as a capture register or reload register. When used as a capture register, it can capture the content of Timer 2. When used as a reload register, it can reload its content into Timer 2.

Timer 2's clock source can be from on-chip CPU clock or off-chip clock pulse, depending on the state of the C/$\overline{T2}$ bit, bit 1 of SFR T2CON.

Timer 2 can operate in four different modes, listed below:

- 16-bit timer/counter,
- 16-bit timer/counter with capture,
- 16-bit timer/counter with auto-reload, or
- Baud-rate generator for UART.

Table 29 describes how to configigure Timer 2 to operate in different operating modes.

Table 29 Configuring Timer 2 into various operating modes

RCLK (T2CON.5)	**TCLK (T2CON.4)**	**CP/$\overline{RL2}$ (T2CON.0)**	**TR2 (T2CON.2)**	**OPERATING MODE**
0	0	1	1	• 16-bit timer/counter, or • 16-bit timer/counter with capture capability.
0	0	0	1	16-bit timer/counter with auto-reload.
1	X	X	1	Baud rate generator for UART.
X	1	X	1	• Either RCLK=1 or TCLK=1 will configure Timer 2 into Baud Rate Generator mode. • When Timer 2 is in Baud Rate Generator Mode, bit CP/$\overline{RL2}$ is ignored.
X	X	X	0	When TR=1, clock pulses is blocked from entering into Timer 2. That is, Timer 2 is disabled.
X=don't care				

10.2 Special Function Registers associated with Timer 2

Timer 2 is associated with the 7 SFRs, listed in Table 30. Three SFRs, CKCON, T2CON, and T2MOD, must be properly programmed to have timer 2 work properly.

Table 30 Timer 2 SFRs

ADDRESS	R/W	MNEMONICS	DESCRIPTION	VALUE AFTER RESET
8E	R/W	CKCON	Select clock frequency for Timer 0, Timer 1, and Timer 2, and memory stretch cycle for the MOVX instruciton.	0000 0000
C8	R/W	T2CON	Timer 2 Control Register (bit-addressable)	0000 0000
C9	R/W	T2MOD	Timer 2 Mode Control register	xxxx xx0x
CA	R/W	RCAP2L	Timer 2 Reload/Capture Register, Low byte	0000 0000
CB	R/W	RCAP2H	Timer 2 Reload/Capture Register, High byte	0000 0000
CC	R/W	TL2	Timer 2, Low byte	0000 0000
CD	R/W	TH2	Timer 2, High byte	0000 0000

10.2.1 THE T2M BIT OF CLOCK CONTROL REGISTER (SFR CKCON)

The T2M bit (bit 5) of the Clock Control Register (CKCON SFR), located at 8E(hex) of the SFR memory space, selects the frequency of the clock used to drive Timer 2.

When the T2M bit is programmed to LOW (T2M=0), (CPU CLK÷12) clock is selected to drive Timer 2. When the T2M bit is programmed to HIGH (T2M=1), (CPU CLK÷4) clock is selected to drive Timer 2. This bit has no effect when Timer 2 is programmed to work as a baud rate generator.

Table 31 T2M bit of SFR CKCON

Clock Control Register (SFR CKCON), located at 8E(hex) of the SFR map								
Bit Address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Mnemonics	Reserved		T2M	T1M	T0M	Reserved	Reserved	Reserved
Reset value	0	0	0	0	0	0	0	1

Table 32 Description of the T2M bit of SFR CKCON

MNEMONIC	BIT POSITION	FUNCTION
T2M	CKCON.5	Select Timer 2 clock frequecny. When T2M=0, Timer 2 uses (CPU CLK / 12) as clock frequency. When T2M=1, Timer 2 uses (CPU CLK / 4) as clock frequency.

For detailed description of the SFR CKCON, please refer to Table 9.

10.2.2 TIMER 2 CONTROL REGISTER (SFR T2CON)

Table 33 and Table 34 give description for SFR T2CON.

Table 33 Timer 2 Control Register (SFR T2CON, C8 hex)

Bit Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Mnemonics	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/$\overline{T2}$	CP/$\overline{RL2}$
Reset Value	0	0	0	0	0	0	0	0

Table 34 Description of Timer 2 Control Register

MNEMONIC	BIT POSITION	FUNCTION
TF2	T2CON.7	Timer 2 overflow flag. • This bit is set to HIGH when Timer 2 overflows from FFFF(hex) to 0000(hex). It must be cleared by software. • TF2 will not be set when either RCLK or TCLK is 1. That is, when Timer 2 is in Baud Rate Generator mode, TF2 will never be set. • Writing a 1 to TF2 bit forces a Timer 2 interrupt, if this interrupt function is enabled.
EXF2	T2CON.6	Timer 2 External flag. • This bit is set to HIGH when a capture or reload action is triggered by a high-to-low transition on the T2EX input pin and when EXEN2=1. • When Timer 2 interrupt is enabled, EXF2 = 1 will cause the CPU to jump to Timer 2 interrupt subroutine. It must be cleared by software. • Writing a 1 to the EXF2 bit forces a Timer 2 interrupt, if it is enabled.
RCLK	T2CON.5	UART Receiver clock selection. This bit is used to select the receiver clock of the UART. • If this bit is programmed to 1 (RCLK=1), UART uses Timer 2 overflow pulses as its receiver clock in Modes 1 and 3. • If this bit is programmed to 0 (RCLK=0) , UART uses Timer 1 overflow pulses as its receiver clock.
TCLK	T2CON.4	UART Transmitter clock selection. This bit is used to select the transmitter clock of the UART. • If this bit is programmed to 1 (TCLK=1), UART uses Timer 2 overflow pulses as its transmitter clock in Modes 1 and 3. • If this bit is programmed to 1 (TCLK=0) , UART uses Timer 1 overflow pulses as its transmitter clock.
EXEN2	T2CON.3	Timer 2 external enable. • EXEN2=1 allows a capture or reload to occur as a result of a high-to-low transition on the T2EX input, if Timer 2 is not in baud rate generator mode. • EXEN2=0 causes Timer 2 to ignore all events at T2EX input.

MNEMONIC	BIT POSITION	FUNCTION
TR2	T2CON.2	Start/Stop control for Timer 2. • TR2=1 allows clocks to be added to Timer 2. • TR2=0 prevent clocks from being added to Timer 2.
C/$\overline{T2}$	T2CON.1	Select timer function or counter function of Timer 2. • C/$\overline{T2}$= 0 selects the timer fucntion. • When used as a timer, Timer 2 runs at four CPU CLK clocks per increment or twelve CPU CLK clocks per increment, as selected by the T2M bit (CKCON.5) of the SFR CKCON, in all modes except baud rate generator mode. • When used in baud rate generator mode, Timer 2 runs at two CPU CLK per increment, independent of the state of the T2M bit. • C/$\overline{T2}$=1 selects the external event counter function; falling-edge-triggered on the T2 input.
CP/$\overline{RL2}$	T2CON.0	Selection of capture or reload function. • When this bit is programmed to HIGH (CP/$\overline{RL2}$ =1), Timer 2 is in capture mode and capture occurs on a high-to-low transitions (falling edge) at T2EX, if EXEN2=1. • When this bit is programmed to LOW (CP/$\overline{RL2}$ =0), Timer 2 is in auto-reload mode and auto-reload occurs either with Timer 2 overflows or a high-to-low transitions at T2EX when EXEN2=1. • When RCLK=1 or TCLK=1, this bit is ignored and the timer is forced to auto-reload on a Timer 2 overflow.

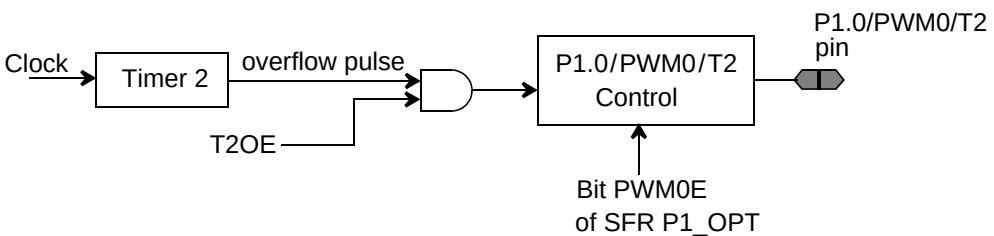
10.2.3 TIMER 2 MODE CONTROL REGISTER

Timer 2 Mode Control Register, located at C9(hex) of the SFR memory space, is a one-bit SFR. It is used to turn on Timer 2 pulse output to the P1.0/PWM0/T2 pin, when Timer 2 overflows from FFFFH.

Table 35 Timer 2 Mode Control Register (SFR T2MOD)

Timer 2 Control Register (SFR T2CON), located at C8(hex) of the SFR memory space.								
Bit Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Mnemonics							T2OE	
Reset Value	X	X	X	X	X	X	0	X

Table 36 Description of Timer 2 Control Register

MNEMONIC	BIT POSITION	FUNCTION
T2OE	T2MOD.1	Timer 2 output enable bit. Programming this bit to HIGH (T2OE=1) enables Timer 2 overflow pulse to be sent to the P1.0/PWM0/T2 pin, as illustrated in the following figure.  Fig.13 T2OE bit

10.3 16-bit Timer/Counter Mode

In this mode, SFR TL2 and SFR TH2 are cascaded into a 16-bit timer or counter. SFR RCAP2L and SFR RCAP2H are not used. This 16-bit timer can then be used to count pulses from on-chip CPU clock or off-chip external pulses, by properly programming bits T2M and C/$\overline{T2}$. The TR2 bit, Timer 2 enable bit, must always be HIGH.

When Timer 2 overflows from FFFFH to 0000H, a clock pulse with the duration of one cycle of CPU clock is sent out.This pulse then sets the Timer 2 overflow flag, which, if enabled, can generate an interrupt. The overflow pulse can also be sent to Pin1.0, if the T2OE bit is enabled.

Fig.15 shows Timer 2 configuration when it works as a 16-bit Timer/Counter.

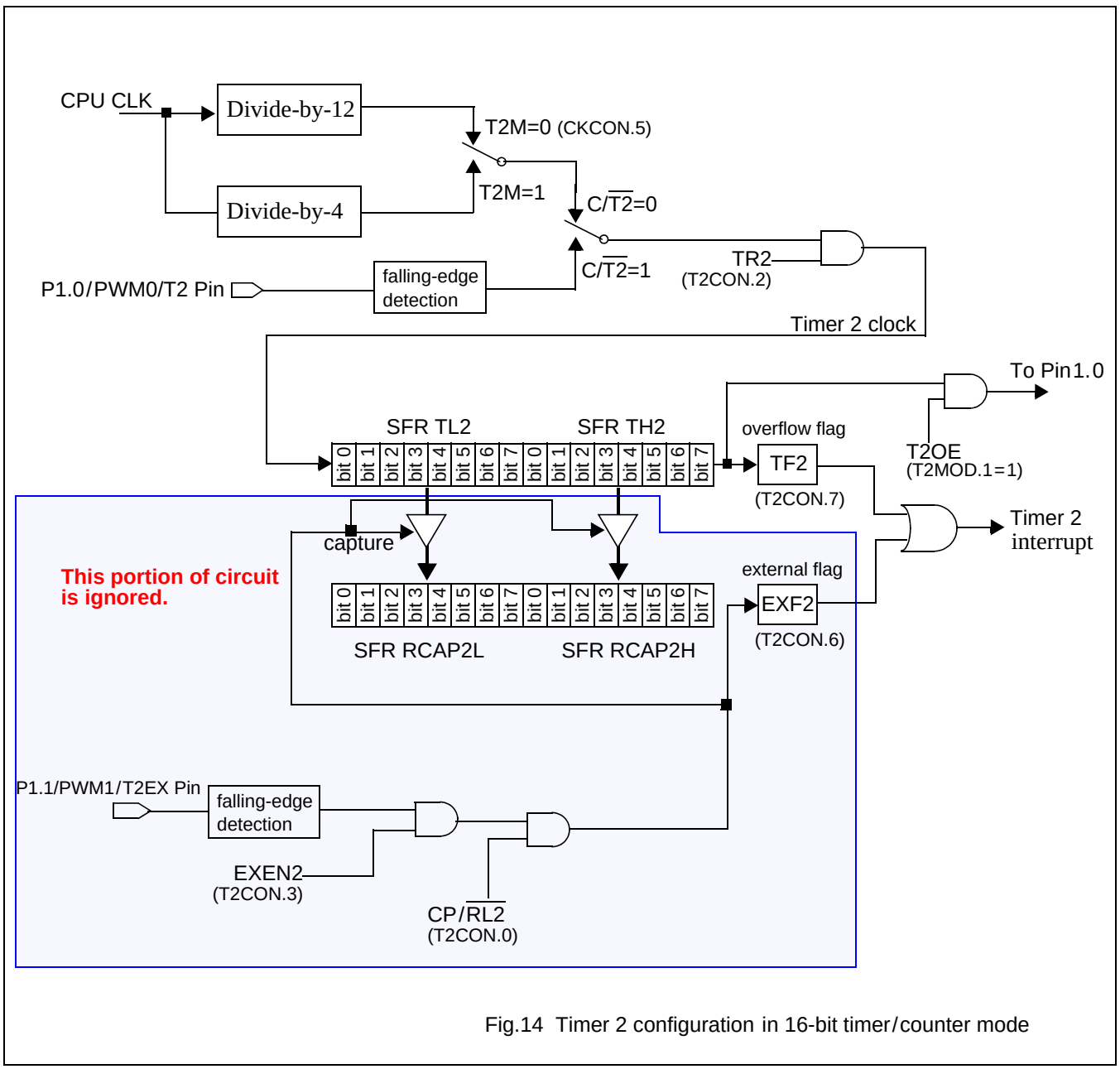


Fig.14 Timer 2 configuration in 16-bit timer/counter mode

10.4 16-bit Timer/Counter with Capture capability (Capture Mode)

When Timer 2 works in this mode, the content of SFR TL2 and SFR T2H can be captured into SFR RCAP2L and SFR RCAP2H, respectively, by an external triggering on the T2EX pin. Therefore, this mode is called Capture Mode.

Bit EXEN2 is used to enable external trigger.

- If EXEN2=0, external trigger is disabled and Timer 2 is a pure 16-bit timer/counter which, upon overflowing, sets the Timer 2 overflow flag bit TF2. This flag may then be used to generate an interrupt.
- If EXEN2=1, Timer 2 also operates as a 16-bit timer/counter, but with the additional capability that a **High-to-Low transition** at the T2EX input causes the current value in TL2 and TH2 to be captured into SFR RCAP2L and SFR RCAP2H. The falling transition at T2EX also causes the EXF2 flag bit in T2CON to be set; this flag may also be used to generate an interrupt. The triggering pulse is also conditioned by the CP/$\overline{RL2}$ bit. To enable the capture action, The CP/$\overline{RL2}$ bit must be set to HIGH.

In addition, Timer2 overflow pulse, whose duration is one cycle of Timer 2 clock, can be sent out to Pin 1.0, if T2OE=1.

Fig.15 shows Timer 2, working as a 16-bit Timer/Counter with Capture capability.

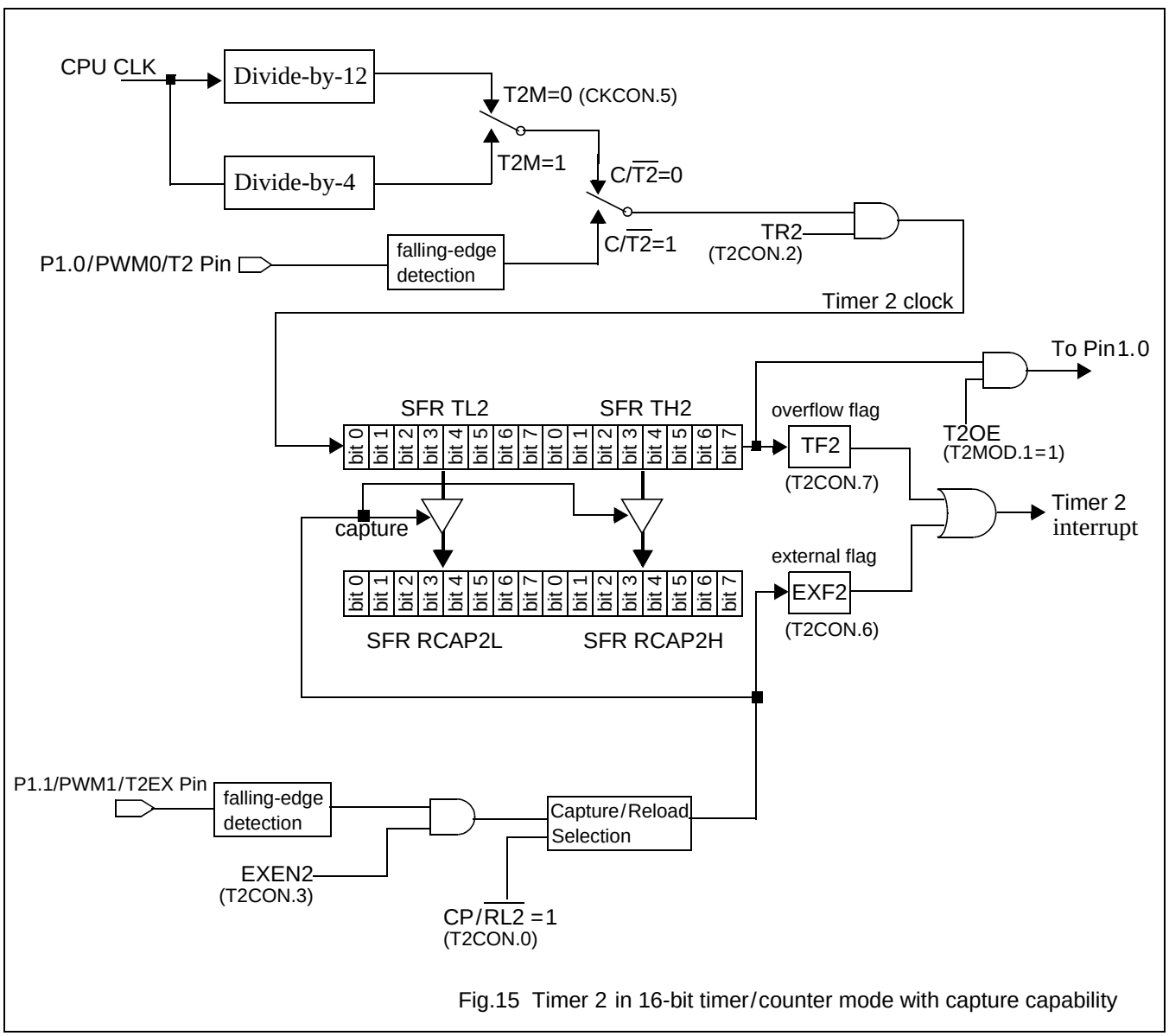


Fig.15 Timer 2 in 16-bit timer/counter mode with capture capability

10.5 16-bit Timer/Counter with Auto-Reload capability (Auto-Reload Mode)

When CP/$\overline{RL2}$=0, Timer 2 is configured into Auto-reload mode. In the Auto-Reload mode, the Timer 2's starting value is reloaded from SFR RCAP2L and SFR RCAP2H.

There are two options selected by the EXEN2 bit in T2CON.

- If EXEN2=0, then, when Timer 2 overflows from FFFFH, it sets the TF2 flag bit and also causes the Timer 2 registers to be reloaded with the 16-bit value held in SFR RCAP2L and SFR RCAP2H. The 16-bit value held in RCAP2L and RCAP2H should be pre-loaded by software.
- If EXEN2= 1, Timer 2 operates as described above, but with the additional feature that a High-to-Low transition at the external input pin T2EX will also trigger the16-bit reload and set the EXF2 flag bit.

In this mode, Timer 2 overflow pulse can also be sent to the P1.0 pin by setting the T2OE bit.

Fig.16 shows Timer 2 configuratin in Auto-reload mode.

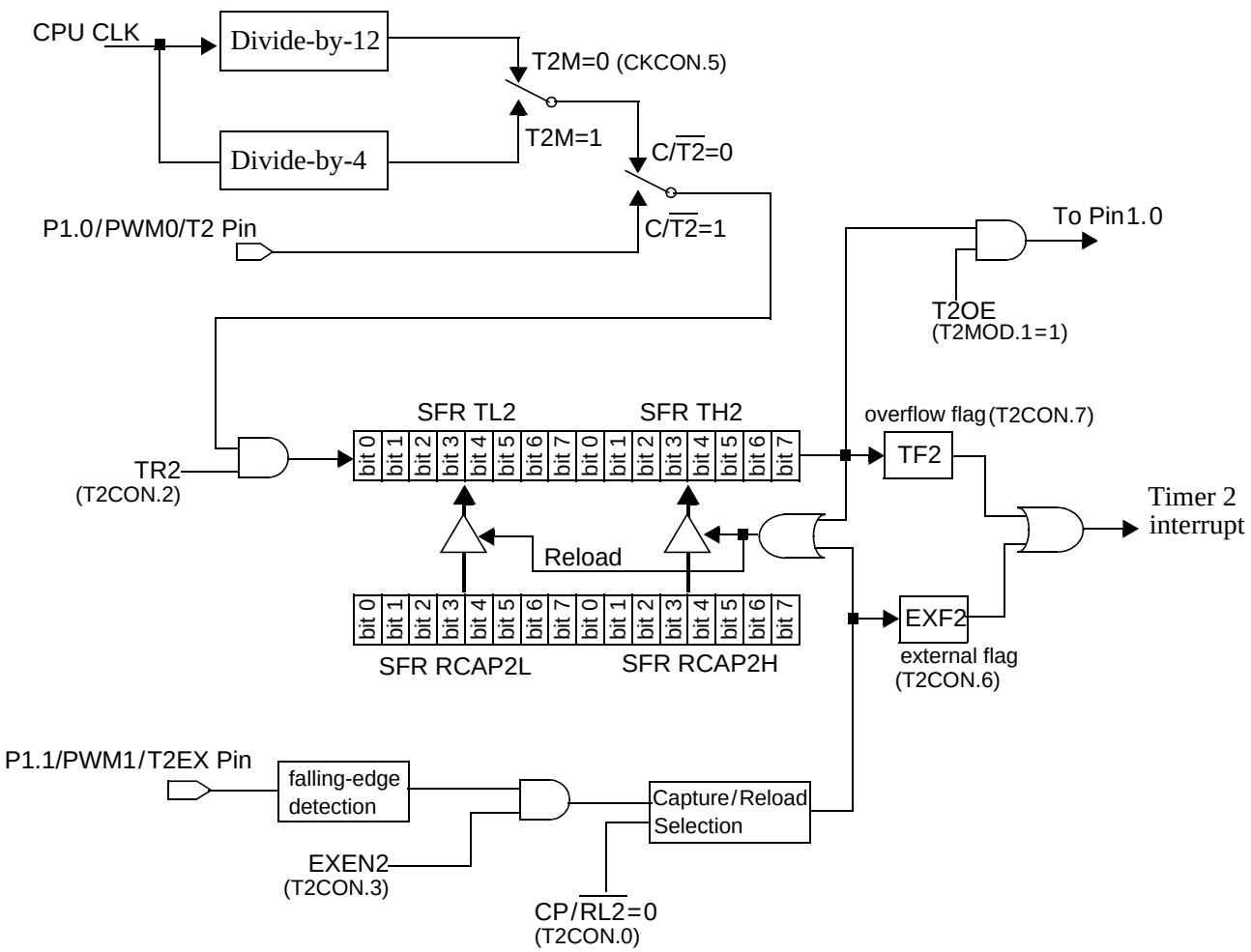


Fig.16 Timer 2 in auto-reload mode

10.6 Baud Rate Generator Mode

When either RCLK=1 or TCLK=1, Timer 2 is a baud rate generator for UART, without regard to the setting of CP/$\overline{RL2}$ bit. The overflow pulse from Timer 2, after being divided by a divided-by-16 counter, is used as the trasmitting clock or receiving clock of the UART in Mode 1 or Mode 3.

The Baud Rate Generator mode is similar to the Auto-Reload mode, in that an overflow of Timer 2 causes Timer 2 registers (SFR TH2 and SFR TL2) to be reloaded with the 16-bit value held in the registers SFR RCAP2H and SFR RCAP2L, which should be preloaded by software.

As a baud rate generator, Timer 2 counts at a frequency of 1/2 $f_{CPU\ CLK}$, as shown in Fig.17.

Baud rates of the UART in Modes 1 and 3 are determined by the following equation.

$$\text{Baud Rate} = \frac{\text{Timer 2 overflow rate}}{16} = \frac{f(\text{CPU CLK})}{(32)\times[65536-(RCAP2H;RCAP2L)]} \quad \text{-------Equation (1)}$$

In the above equation, (RCAP2H ; RCAP2L) is the content of registers RCAP2H and RCAP2L taken as a 16-bit unsigned integer. The 32 in the denominator is the result of the CPU CLK clock being divided by 2 and the Timer 2 overflow rate being divided by 16. Setting TCLK=1 or RCLK=1 automatically causes the CPU CLK clock to be divided 2.

10.6.1 CALCULATING THE VALUE OF RCAP2H AND RCAP2L FOR A DESIRED BAUD RATE

If a programmer has decided to use a certain baud rate, the required value of RCAP2H and RCAP2L and be derived from Equation (2), which is re-manipulated from the Equation (1).

$$(RCAP2H, RCAP2L) = 65536 - \frac{\text{CPU CLK}}{32\times\text{Baudrate}} \quad \text{-------Equation (2)}$$

Table 37 gives calculated value of RCAP2H and RCAP2L for some desired baud rates.

Table 37 Timer 2 reload value for UART Mode 1 and Mode 3 baud rate.

BAUD RATE	C/$\overline{T2}$	33 MHz CPU CLK		25 MHz CPU CLK		11.0592 MHz CPU CLK	
		RCAP2H	RCAP2L	RCAP2H	RCAP2L	RCAP2H	RCAP2L
57.6 Kb/s	0	FF	EE	FF	F2	FF	FA
19.2 Kb/s	0	FF	CA	FF	D7	FF	EE
9.6 Kb/s	0	FF	95	FF	AF	FF	DC
4.8 Kb/s	0	FF	29	FF	5D	FF	B8
2.4 Kb/s	0	FE	52	FE	BB	FF	70
1.2 Kb/s	0	FC	A5	FD	75	FE	E0

10.6.2 MORE ABOUT TIMER 2

When either RCLK or TCLK is set to logic high, Timer 2 overflow does not set the TF2 bit of SFR T2CON and therefore will not generate interrupt. Consequently, the Timer 2 interrupt does not need to be disabled when in the baud rate generator mode.

If EXEN2 is set to HIGH, a HIGH-to-LOW transition on T2EX will set the EXF2 bit of T2CON, but will not cause a reload from (RCAP2H; RCAP2L) to (TH2; TL2). Therefore, in this mode T2EX may still be used as an additional external interrupt.

When Timer 2 is operating in the baud rate generator mode, registers SFR TH2 and SFR TL2 should not be accessed. Because in this mode, the timer is being incremented every two CPU CLK clock and therefore the results of a read or write may not be accurate. The SFRs RCAP2H and RCAP2L, however, may be read out but not written to. A write might overlap a reload and cause write and/or reload errors. If a write operation is required, Timer 2 should first be turned off by clearing the TR2 bit.

10.6.3 TIMER 2 IN BAUD RATE GENERATOR MODE

The configuration of Timer 2 in baud rate generator mode is shown in Fig.17.

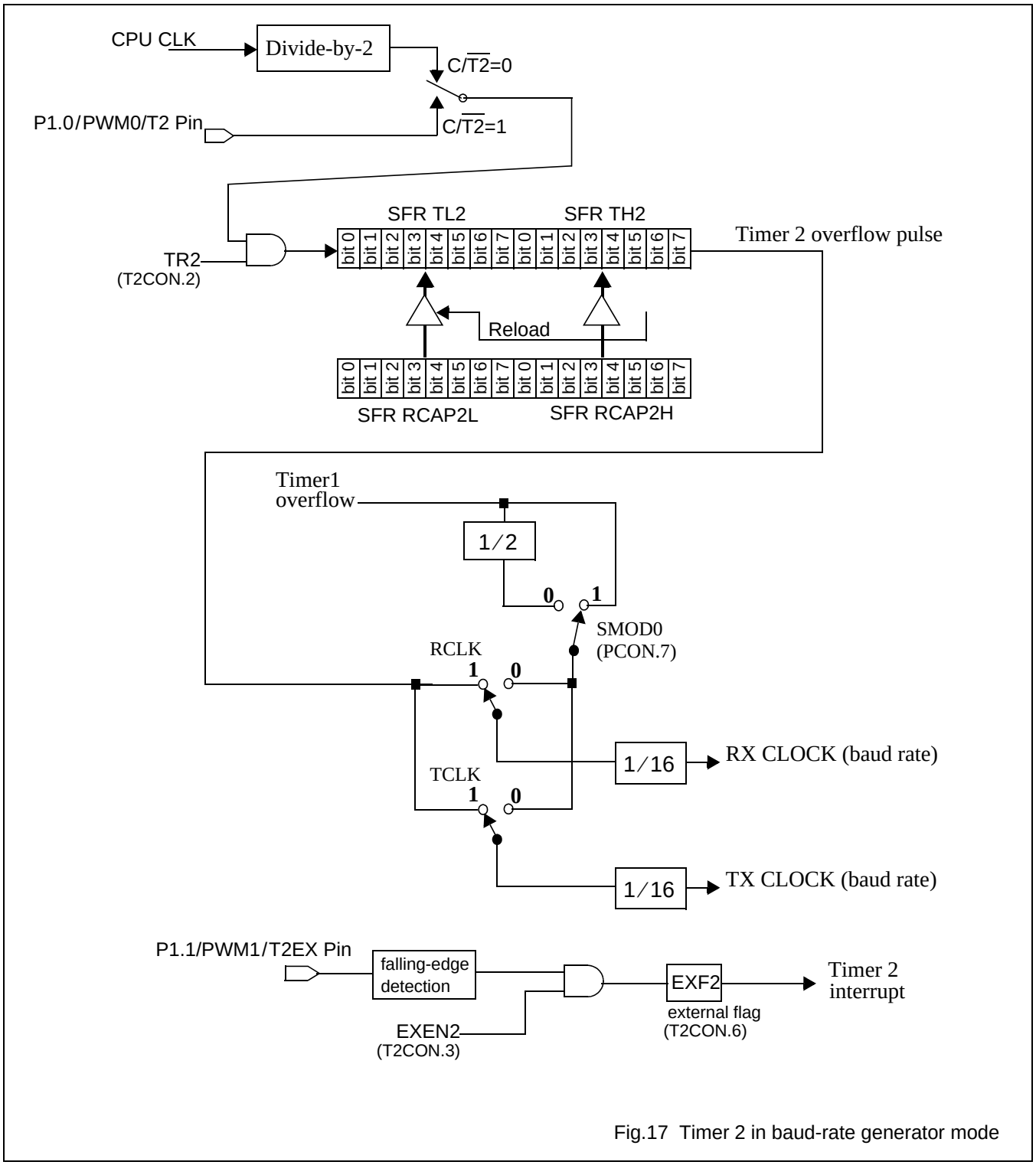


Fig.17 Timer 2 in baud-rate generator mode

Timer 3

10.7 General Description and functional block diagram

Timer 3 is mainly composed of SFR TH3, SFR TL3 and their contorl logic. The clock to Timer 3 can be XTAL1, XTAL1 divided by 3, XTAL1 divided by 48, or 2 x XTAL1. When Timer 3 overflows, it generates interrupt 2, if interrupt 2 is enabled. Enable or disable of interrupt 2 is controlled by the setting of Bit 6 (T3EN) of Chip Configuration Register (SFR CHIPCON).

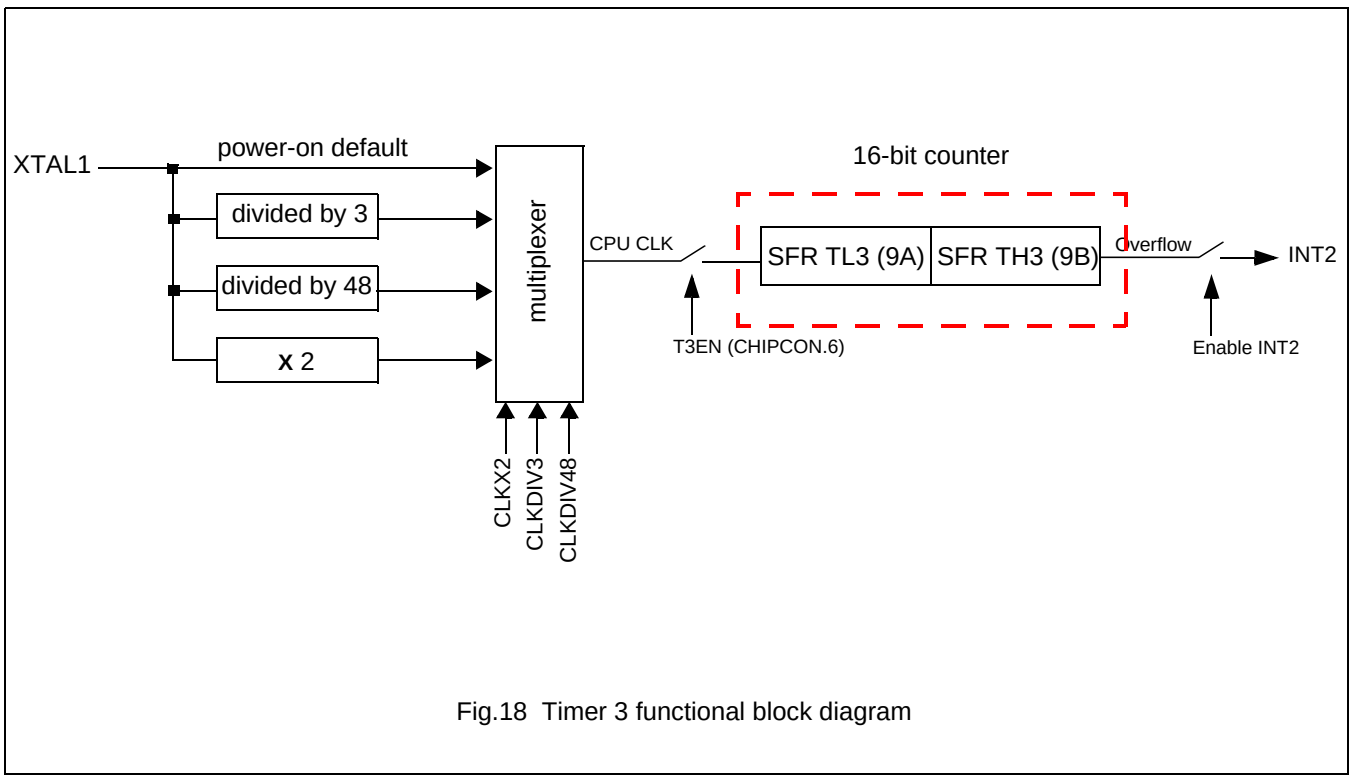


Fig.18 Timer 3 functional block diagram

10.8 Special Function Registers associated with Timer 3

Timer 3 is associated with the 3 SFRs, listed in Table 38.

Table 38 Timer 3 SFRs

ADDRESS	R/W	MNEMONICS	DESCRIPTION	VALUE AFTER RESET
BF	R/W	CHIPCON	Chip Configuration Register	x001 x000
9A	R/W	TL3	Timer 3, Low byte	0000 0000
9B	R/W	TH3	Timer 3, High byte	0000 0000

11 WATCHDOG TIMER

11.1 Functional Block Diagram

The Watchdog Timer is used to reset the STK6037 when it enters into an erroneous state, possibly due to disturbance from external world.

Only one SFR (SFR WDT), at SFR map address E1hex) is associated with the Watchdog Timer.

Fig.19 gives the functional block diagram of the Watchdog Timer.

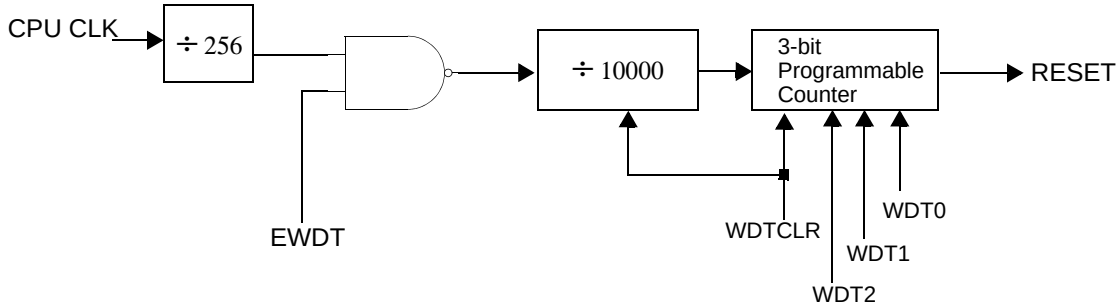


Fig.19 Watchdog Timer.

11.2 Watchdog Timer Control Register

The Watchdog Timer Control Register (SFR WDT) is the only SFR associated with the Watchdog Timer. It can be written to or read from, and is decribed in Table 39.

Table 39 Watchdog Timer Register

WATCHDOG TIMER REGISTER, SFR WDT, AT E1 (HEX) OF THE SFR MAP								
Bit Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Mnemonics	EWDT	WDTCLR	not implemented			WDT2	WDTI	WDT0
RESET value	0	0	x			0	0	0

Table 40 Description of SFR WDT

MNEMONIC	FUNCTION
EWDT (bit 7)	Enable Watchdog Timer. Setting EWDT=1 enables the Watchdog Timer. Setting EWDT=0 disables the Watchdog Timer.
WDTCLR (bit 6)	Setting WDTCLR = 1 clears the Watchdog Timer Programmable Counter and the divided-by-10000 prescaler. The Watchdog Timer must be regularly cleared before it overflows.
WDT2, WDT1, WDT0 (bits 2, 1, 0)	These 3 bits decide the overflow period of the Watchdog Timer. The following table gives the overflow period versus the programmed value of these 3 bits, assuming that XTAL1=24 MHz. Note that XTAL1 is the external crystal clock, not the CPU clock.

WDT2	WDT1	WDT0	Overflow interval	Notes
0	0	0	8 x 0.107 seconds = 0.856 seconds	Assuming XTAL1=24 MHz.
0	0	1	1 x 0.107 seconds = 0.107 seconds	
0	1	0	2 x 0.107 seconds = 0.214 seconds	
0	1	1	3 x 0.107 seconds = 0.321 seconds	
1	0	0	4 x 0.107 seconds = 0.428 seconds	
1	0	1	5 x 0.107 seconds = 0.535 seconds	
1	1	0	6 x 0.107 seconds = 0.642 seconds	
1	1	1	7 x 0.107 seconds = 0.749 seconds	

12 UART0 AND UART1

12.1 General Description

The STK6037 has two serial ports: UART1 and UART0. Both UART0 and UART1 are indentical in operation to industrial-standard 80C51's serial port, with the exception that Timer 2 can not be used as the baud rate generator of UART1. For simplicity, we illustrate only UART0 function as an example from section 12.5 to 12.9.

Both UART0 and UART1 are full-duplex serial ports. The word "full-duplex" means that that can transmit and receive simultaneously. Each of them has one receiver data pin (RXD) and one transmitter data pin (TXD). The receiver data pins share with port pins P3.0 and P1.0. The transmitter data pins share with port pins P3.1. and 1.1.

Four SFRs: SCON0, SBUF0, SCON1 and SBUF1, are associated with the UART0 and UART1. Their functions are given in Table 41.

Table 41 SFRs associated with UART0 and UART1.

Nemonics	Address (Hex)	Function
SFR SCON0	98	Control and status register of UART0.
SFR SBUF0	99	Data buffer for both transmission and reception of UART0.
SFR SCON1	C0	Control and status register of UART1.
SFR SBUF1	C1	Data buffer for both transmission and reception of UART1.

From software point of view, data transmission and reception are both through the SFR SBUF0 (SFR SBUF1). Writing to SFR SBUF0 (SFR SBUF1) loads data to be transmitted to SFR SBUF0 (SFR SBUF1). Reading SFR SBUF0 (SFR SBUF1) reads received data.

But, physically, writing to SFR SBUF0 (SFR SBUF1) loads data to a physical Transmit Register and reading SFR SBUF0 (SFR SBUF1) reads a physical Receive Register.

A programmer's model of UART0 is shown in Fig.20. The model for UART1 is the same.

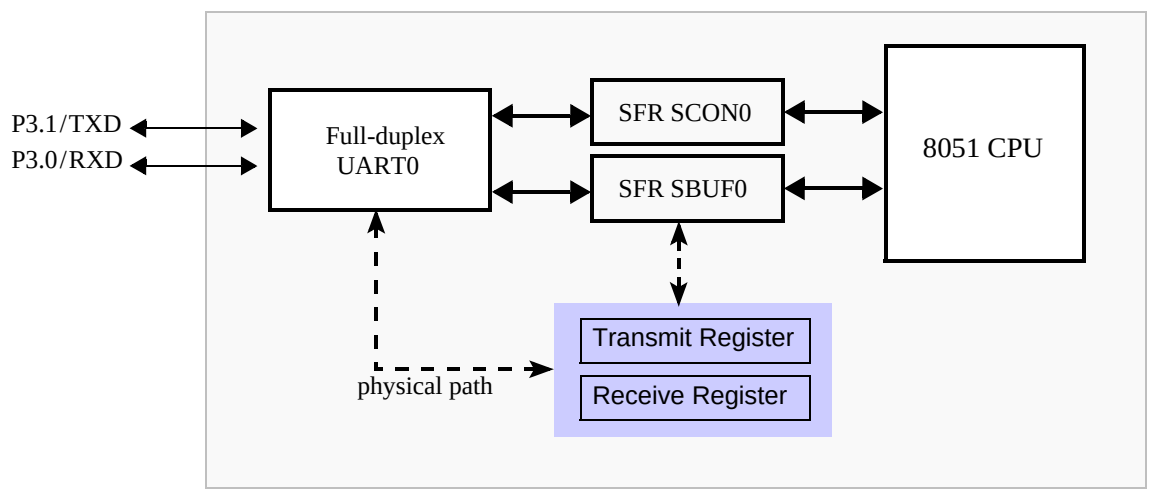


Fig.20 Programmer's model of the UART0

12.2 Summary of operation modes of UART0 and UART1

Each of UART0 and UART1 has four operating modes. These modes are summarized in Table 42:

Table 42 Operating modes of UART0 and UART1

Mode	Operation	Sync/ Async	Baud clock	Data bits	Start/Stop	9th-bit function
0	8-bit shift register.	Sync	clk/4 or clk/12	8	None	None
1	10-bit data transmission and reception	Async	For UART0, Timer 1 or Timer 2. For UART1, Timer 1 only.	8	1 start, 1 stop	None
2	11-bit data transmission and reception	Async	clk/32 or clk/clk64	9	1 start, 1 stop	0, 1, parity
3	11-bit data transmission and reception	Async	For UART0, Timer 1 or Timer 2. For UART1, Timer 1 only.	9	1 start, 1 stop	0, 1, parity

12.3 Control/Status Register and operaton mode of UART0

12.3.1 Operation modes of UART0

Table 43 gives detailed description of UART0's operation modes.

The selection of operation modes is decided by the setting of the SM0_0 bit and the SM1_0 bit of SFR SCON0.

Table 43 UART0 Operation Modes.

Mode	SM0_0	SM1_0	Description
0	0	0	**8-bit serial transmission or reception.** In this mode, the UART is actually an 8-bit shift register. 8 bits of data enters or exits through the P3.0/RXD pin. The P3.1/TxD pin always outputs the shift clock. The Least Significant Bit (LSB) is received or transmitted first. The baud rate is either 1/4 or 1/12 of the CPU clock frequency, controlled by the setting of SM2_0 bit of SFR SCON0.
1	0	1	**10-bit serial transmission or reception.** In this mode, 10 binary bits are transmitted (through P3.1/TXD) or received (through P3.0/RXD). The 10 binary bits are composed of a **start bit**(1), 8 **data bits** (LSB first), and a **stop bit**(1). On reception, the stop bit goes into bit RB8_0 of the SFR SCON0. The baud rate comes from Timer 1 or Timer 2 overflow.
2	1	0	**11-bit serial transmission or reception.** In this mode, 11 binary bits are transmitted (through P3.1/TXD) or received (through P3.0/RXD). The 11 binary bits are composed of a **start bit**(1), 8 **data bits** (LSB first), a programmable 9th data bit, and a **stop bit**(1). On transmission, the 9th data bit (TB8_0 in SCON0) can be programmed to be 1 or 0. For example, in application, the **parity bit P** of SFR PSW can be moved into TB8_0 of SCON0. On reception, the 9th data bit goes into RB8_0 of SFR SCON0. The **stop bit** is ignored. The baud rate can be 1/32 or 1/64 of CLK frequency, selected by the setting of the SMOD0 bit of SFR PCON.
3	1	1	**11-bit serial transmission or reception.** In this mode, 11 binary bits are transmitted (through P3.1/TXD) or received (through P3.0/RXD). The 11 binary bits are composed of a **start bit**(1), 8 **data bits** (LSB first), a programmable 9th data bit, and a **stop bit**(1). Actually, Mode 3 is a combination of Mode 2 protocol and Mode 1 baud rate. The baud rate in Mode 3 comes from Timer 1 or Timer 2 overflow.

12.3.2 CONTROL/STATUS REGISTER (SFR SCON0) OF UART0

The Control/Status Register of UART0 is SFR SCON0, located at address 98H of the SFR memory space.

Table 44 UART0 Control/Status Register (SFR SCON0, 98h)

Bit Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Mnemonics	SM0_0	SM1_0	SM2_0	REN_0	TB8_0	RB8_0	TI_0	RI_0

Table 45 Description of SFR SCON0

<table>
<tr><th>Mnemonic</th><th>Bit position</th><th>Function</th></tr>
<tr><td>SM0_0</td><td>SCON0.7</td><td rowspan="2">These two bits are used to select an operation mode.
<table><tr><th>SM0_0</th><th>SM1</th><th>Modes</th></tr><tr><td>0</td><td>0</td><td>Mode 0</td></tr><tr><td>0</td><td>1</td><td>Mode 1</td></tr><tr><td>1</td><td>0</td><td>M0de 2</td></tr><tr><td>1</td><td>1</td><td>Mode 3</td></tr></table></td></tr>
<tr><td>SM1_0</td><td>SCON0.6</td></tr>
<tr><td>SM2_0</td><td>SCON0.5</td><td>Multiprocessor Communication Enable.
In Mode 0, SM2_0 decides the baud rate. When SM2_0 = 0, the baud rate is $f_{clk}/12$. When SM2 = 1, the baud rate is $f_{clk}/4$, where f_{clk} is the CPU clock.
In Mode 1:
• if SM2_0=1, then RI_0 will be set to high only when a HIGH stop bit has been received.
• if SM2_0=0, then RI_0 will always be set to high without regard to the state of the received stop bit.
In modes 2 and 3, SM2_0 enables the multiprocessor communication feature. SM2_0 is used to disable interrupt to the un-addressed slave receivers, when data bytes are transmitted from the master.</td></tr>
<tr><td>REN_0</td><td>SCON0.4</td><td>Reception Enable.
When REN_0=1, UART0 is enabled for reception.
When REN_0=0, UART0 is disabled from reception.</td></tr>
<tr><td>TB8_0</td><td>SCON0.3</td><td>TB8_0 is the 9th data bit that will be transmitted in Mode 2 or Mode 3. Set or cleared by software as desired.</td></tr>
<tr><td>RB8_0</td><td>SCON0.2</td><td>In Mode 0, RB8_0 is not used.
In Mode 1, RB8_0 indicates the state of the received stop bit.
In Mode 2 and Mode 3, RB8_0 is the 9th data bit received.</td></tr>
<tr><td>TI_0</td><td>SCON0.1</td><td>Transmit Interrupt Flag bit.
In mode 0, this bit is set to logic HIGH by hardware at the end of the 8th bit time.
In mode 1, mode 2, and mode 3, this bit is set to logic HIGH by hardware at the beginning of the stop bit time.
This bit can only be cleared by software.</td></tr>
</table>

Mnemonic	Bit position	Function
RI_0	SCON0.0	Receive Interrupt Flag bit. **In mode 0**, this bit is set to a logic HIGH by hardware at the end of the 8th bit time. **In mode 1**, this bit is set to logic HIGH after the last sampling of the stop bit, subject to the state of SM2. **In mode 2, and mode 3**, this bit is set to a logic 1 by hardware at the last sampling of the stop bit. This flag bit can only be cleared by software.

12.4 Control/status Register and operaton mode of UART1

12.4.1 OPERATION MODES OF UART1

Table 46 gives detailed description for each of the four operation modes of UART1.

The selection of operation modes depends on the setting of the SM0_1 bit and the SM1 1 bit of SFR SCON1.

Table 46 UART1 Operation Modes.

Mode	SM0_1	SM1_1	Description
0	0	0	**8-bit serial transmission or reception.** In this mode, 8 bits of data enters or exits through the P1.0/RXD1/PWM0 pin. The P1.1/TxD1/PWM1 pin always outputs the shift clock. The Least Significant Bit (LSB) is received or transmitted first. The baud rate can be either 1/4 or 1/12 of the CPU clock frequency, selected by the setting of the SM2_1 bit of SFR SCON1.
1	0	1	**10-bit serial transmission or reception.** In this mode, 10 binary bits are transmitted (through P1.1/TXD1/PWM1) or received (through P1.0/RXD1/PWM0). The 10 binary bits are composed of a **start bit**(1), 8 **data bits** (LSB first), and a **stop bit**(1). On reception, the stop bit goes into bit RB8_1 of SFR SCON1. The baud rate only comes from Timer 1 overflow. Timer 2 overflow can not be used as baud rate for UART1. The two UARTs can run at the same baud rate, using Timer 1 only. If Timer 2 is used for UART0 and Timer 1 is used for UART1, then the two UARTs can run at the same baud rate.
2	1	0	**11-bit serial transmission or reception.** In this mode, 11 binary bits are transmitted (through P1.1/TXD1/PWM1) or received (through P1.0/RXD1/PWM0)). The 11 binary bits are composed of a **start bit**(1), 8 **data bits** (LSB first), a programmable 9th data bit, and a **stop bit**(1). On transmission, the 9th data bit (TB8_1 in SCON1) can be programmed to be 1 or 0. For example, in application, the **parity bit P** of SFR PSW can be moved into TB8_1 of SCON1. On reception, the 9th data bit goes into RB8_1 of SFR SCON1, while the **stop bit** is ignored. The baud rate is programmable to be 1/32 or 1/64 of CPU clock frequency, controlled by the setting of SMOD0 bit of SFR PCON or SMOD1 bit of SFR EICON.
3	1	1	**11-bit serial transmission or reception.** In this mode, 11 binary bits are transmitted (through P1.1/TXD1/PWM1) or received (through P1.0/RXD1/PWM0). The 11 binary bits are composed of a **start bit**(1), 8 **data bits** (LSB first), a programmable 9th data bit, and a **stop bit**(1). Actually, Mode 3 is a combination of Mode 2 protocol and Mode 1 baud rate. The baud rate in Mode 3 only comes from Timer 1 overflow.

12.4.2 CONTROL/STATUS REGISTER (SFR SCON1) OF UART1

The Control/Status Register of UART1 is SFR SCON1, located at address C0(hex) of the SFR memory space.

Table 47 UART1Control and Status Register (SFR SCON1, C0h)

Bit Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Mnemonics	SM0_1	SM1_1	SM2_1	REN_1	TB8_1	RB8_1	TI_1	RI_1

Table 48 Description of SFR SCON1

<table>
<tr><th>Mnemonic</th><th>Bit position</th><th>Function</th></tr>
<tr><td>SM0_1</td><td>SCON1.7</td><td rowspan="2">These two bits are used to select an operation mode.
<table><tr><th>SM0_1</th><th>SM1_1</th><th>Modes</th></tr><tr><td>0</td><td>0</td><td>Mode 0</td></tr><tr><td>0</td><td>1</td><td>Mode 1</td></tr><tr><td>1</td><td>0</td><td>M0de 2</td></tr><tr><td>1</td><td>1</td><td>Mode 3</td></tr></table></td></tr>
<tr><td>SM1_1</td><td>SCON1.6</td></tr>
<tr><td>SM2_1</td><td>SCON1.5</td><td>Multiprocessor Communication Enable.
In Mode 0, SM2_1 decides the baud rate. When SM2_1 = 0, the baud rate is $f_{CLK}/12$. When SM2_1 = 1, the baud rate is $f_{CLK}/4$.
In Mode 1:
• if SM2_1=1, then RI_1 will be set to high only when a HIGH stop bit has been received.
• if SM2_1=0, then RI_1 will always be set to high without regard to the state of the received stop bit.
In modes 2 and 3, SM2_1 enables the multiprocessor communication feature. SM2_1 is used to disable interrupt to the un-addressed slave receivers, when data bytes are transmitted from the master.</td></tr>
<tr><td>REN_1</td><td>SCON1.4</td><td>Reception Enable.
When REN_1=1, UART1 is enabled for reception.
When REN_1=0, UART1 is disabled from reception.</td></tr>
<tr><td>TB8_1</td><td>SCON1.3</td><td>TB8_1 is the 9th data bit that will be transmitted in Mode 2 or Mode 3. Set or cleared by software as desired.</td></tr>
<tr><td>RB8_1</td><td>SCON1.2</td><td>In Mode 0, RB8_1 is not used.
In Mode 1, RB8_1 indicates the state of the received stop bit.
In Mode 2 and Mode 3, RB8 is the 9th data bit received.</td></tr>
<tr><td>TI_1</td><td>SCON1.1</td><td>The Transmit Interrupt Flag.
In mode 0, this bit is set to a logic 1 by hardware at the end of the 8th bit time.
In mode 1, mode 2, and mode 3, this bit is set to a logic 1 by hardware at the beginning of the stop bit time.
This flag can only be cleared by software.</td></tr>
</table>

Mnemonic	Bit position	Function
RI_1	SCON1.0	The Receive Interrupt Flag. **In mode 0**, this bit is set to a logic HIGH by hardware at the end of the 8th bit time. **In mode 1**, this bit is set to logic HIGH after the last sampling of the stop bit, subject to the state of SM2. **In mode 2, and mode 3**, this bit is set to a logic HIGH by hardware at the last sampling of the stop bit. This flag can only be cleared by software.

12.5 Mode 0

12.5.1 TRANSMISSION AND RECEPTION OF MODE 0

When operating in mode 0, the UART0 is an 8-bit data shift register. Eight bits of data can be shifted into or out from SFR SBUF0, via the P3.0/RXD pin. The shifting clock always comes out from the P3.1/TXD pin, without regard to if the data is shifted into or out from SFR SBUF0.

12.5.2 BAUD RATE OF MODE 0

In mode 0, the UART0's baud rate is either $f_{xtal1}/12$ or $f_{xtal1}/4$, depending on the value of the SM2 bit. If SM2 = 1, the baud rate (i.e., shifting clock frequency) is $f_{xtal1}/4$. If SM2 = 0, then the baud rate is $f_{xtal1}/12$.

12.5.3 TRANSMISSION TIMING OF MODE 0

Data transmission begins when an instruction writes to SFR SBUF0. That is, whenever an instruction with SFR SBUF0 as its destination operand is executed, data transmission will be initiated. The UART0 shifts the data out, LSB first, at the selected baud rate, until all 8 bits of data have been shifted out.

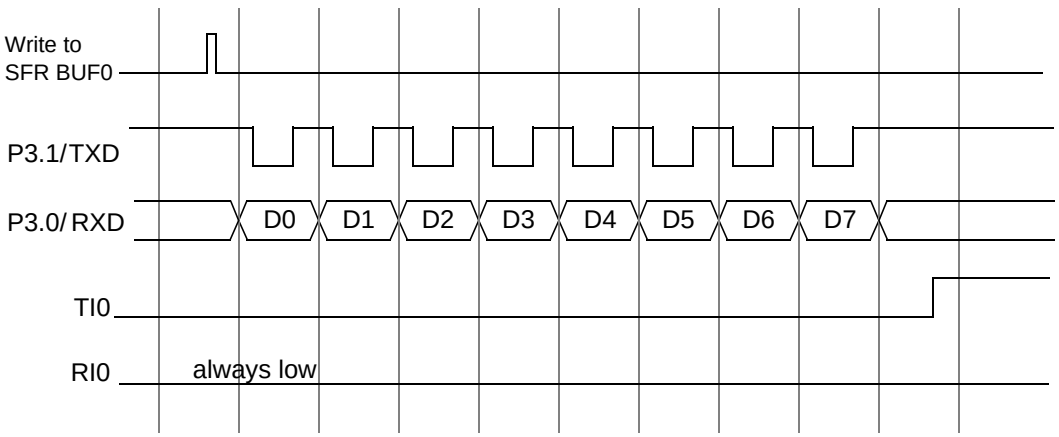


Fig.21 UART0 mode 0 transmission timing when baud rate is XTAL1/4.

12.5.4 RECEPTION TIMING OF MODE 0

To enable data reception, the REN0 bit must first be set to logic HIGH. Data reception begins when the RI0 bit is cleared. Shifting clock is then sent out from the P3.1/TXD pin to shift in data, LSB first, until all 8 bits of external data have been shifted in. Each bit of data is shifted in on the rising edge of the shifting clock. Four XTAL1 clocks after the 8th data bit has been shifted in, the RI0 bit is set to logic HIGH. The RI0=1 indicates that 8 bits of data have been received.

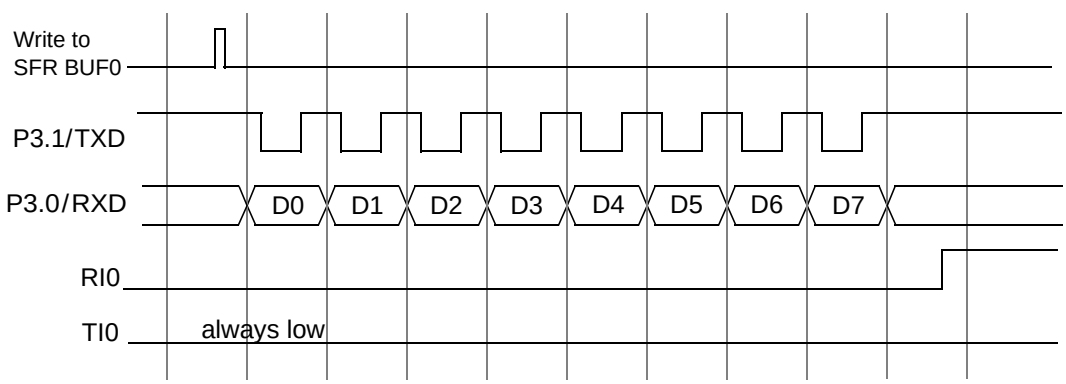


Fig.22 UART0 mode 0 reception timing when baud rate is XTAL1/4.

12.6 Mode 1

12.6.1 Operation of mode 1

Mode 1 provides 10-bits, asynchronous, full-duplex transmission or reception. One transmission or reception word is composed of the following bits:

- one start bit,
- eight data bits (D0~D7), and
- one stop bit.

The 10-bits word format is shown below:

	START	D0	D1	D2	D3	D4	D5	D6	D7	STOP

The data bits are transmitted and received LSB first.

For receive operations, the received stop bit is stored to the RB8 bit of SFR SCON0.

12.6.2 Baud rate of mode 1

Mode 1 baud rate can be from timer 1 overflow or timer 2 overflow.

Please refer to Section 12.9 “Baud Rate Generation for Mode 1 and Mode 3”

12.6.3 Data transmission timing in mode 1

A data transmission session in mode 1 involve two steps:

1. Application program issues a write to SFR SBUF0,
2. Transmission begins immediately after the first overflow of the divided-by-16 counter of the Baud Rate Generation circuit (please refer to Fig.27).
3. The UART0 transmits data out from the P3.1/ TXD pin in the following order: START bit, data bits (D0~D7), and STOP bit. The START bit is transmitted out first. The TI0 (SCON0.1) bit of SFR SCON0 is set to HIGH two XTAL1 clocks after the stop bit has been transmitted.

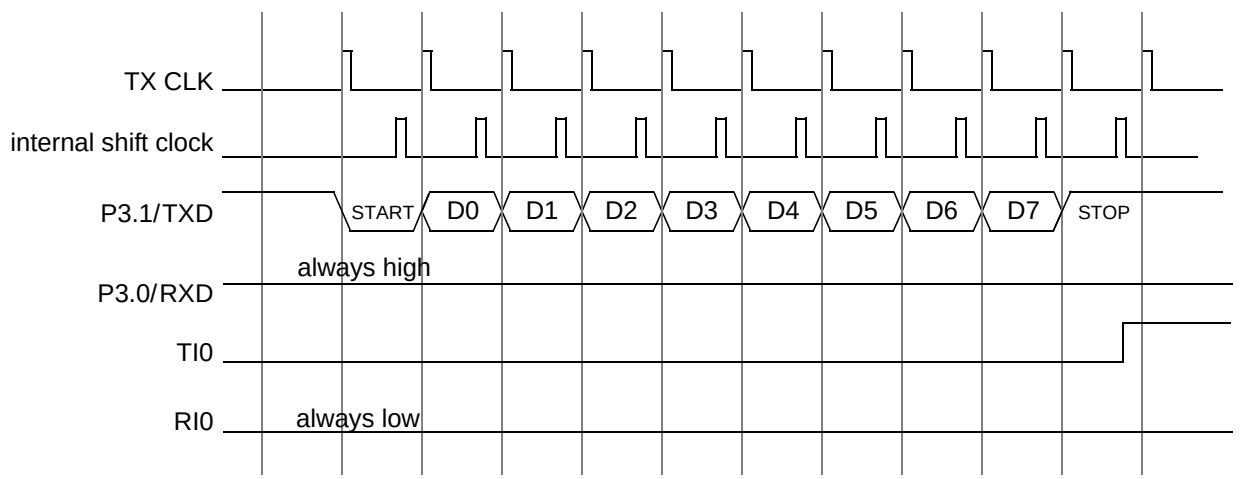


Fig.23 UART0 mode 1 transmission timing

12.6.4 DATA RECEPTION TIMING IN MODE 1

A data reception session in mode 1 is as follows:

1. First, the reception function of the UART0 must be enabled by setting REN0=1 and then the UART0 starts detecting if there is a falling edge on the P3.0/RXD input. For detecting this falling edge, UART0 samples the P3.0/RXD input pin sixteen times per bit time for any baud rate.
2. When a falling edge on the P3.0/RXD pin is detected, the divided-by-16 counter of the baud rate generation circuit is reset. The output of the divided-by-16 counter is the receiver clock, RX CLK. This action is for aligning Timer 1 or Timer 2 overflow to bit boundaries. Please refer to Fig.27 for baud rate generation circuit.
3. For noise rejection, the UART0 decides the value of each received bit by *majority decision* of three consecutive samples in the middle of each bit time. That is, if three consecutive sampled values are 110, then the received bit value is regarded as HIGH. Similarly, if three consecutive sampled values are 101, then the received bit value is still regarded as HIGH.
4. If the first received bit is not LOW, then the reception session is aborted and the UART0 waits for another falling edge on the P3.0/RXD pin.
5. If the first received bit is LOW, then a reception session is initiated and the UART0 continues to receive the following data bits (D0~D7). The bit value is decided by use of *majority decision*.
6. At the middle of the stop bit time, the UART0 checks the following conditions:
   a) RI0 must be LOW,
   b) if SM2 has been programmed to HIGH, then the received stop bit must also be HIGH. (If SM2 has been programmed to LOW, the received stop bit can be LOW or HIGH.)
7. If the above conditions are met, then the UART0 moves the received data byte from the temporary Receive Register (please refer to Fig.20) to SFR SBUF0, moves the received stop bit to the RB8 bit of SFR SCON0, and set RI0 bit to HIGH, triggering an UART0 data reception interrupt. If the above conditions are not met, the received data is ignored and the receive session is aborted.
8. After the middle of the stop bit time, the UART0 continues to wait for another high-to-low transition on the P3.0/RXD pin.

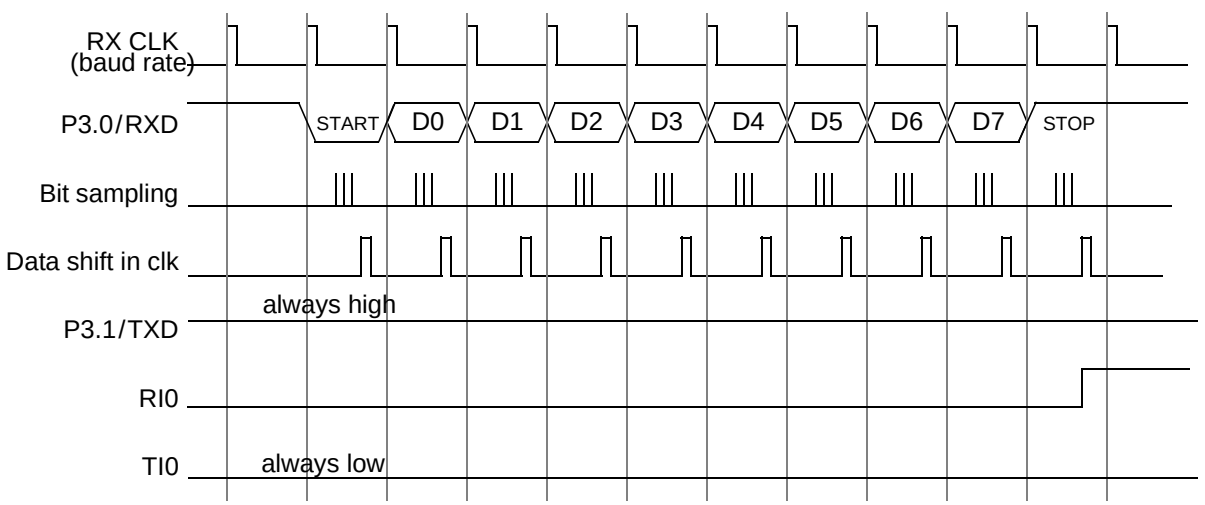


Fig.24 UART0 mode 1 reception timing

12.7 Mode 2

12.7.1 OPERATION OF MODE 2

Mode 2 provides 11-bits, asynchronous, full-duplex transmission or reception.

A transmission or reception word is composed of the following 11 bits:

- one start bit,
- eight data bits,
- one programmable 9th bit, and
- one stop bit.

The word format is shown below:

	START	D0	D1	D2	D3	D4	D5	D6	D7	TB8/RB8	STOP

The data bits are transmitted and received LSB first.

For transmission, the 9th bit is determined by the value in TB8. To use the 9th bit as a parity bit, move the value of the P bit of SFR PSW to TB8.

12.7.2 BAUD RATE OF MODE 2

In Mode 2, the baud rate is decided by the value of the SMOD0 bit in the SFR PCON (please refer to Table 48).

- If SMOD0=0, the default value of SMOD0 after reset, the baud rate is $f_{xtal1}/64$. That is, the duration of a bit time is 64 XTAL1 clocks.
- If SMOD0=1, the baud rate is $f_{xtal1}/32$. That is, the duration of a bit time is 32 XTAL1 clocks.

12.7.3 DATA TRANSMISSION TIMING IN MODE 2

A data transmission session in mode 2 involves the following steps:

1. Application program issues a write to SFR SBUF0,
2. Transmission begins immediately after the first overflow of the divided-by-16 counter of the Baud Rate Generation circuit (please refer to Fig.27).
3. The UART0 transmits data out from the P3.1/TXD pin in the following order: START bit, data bits (D0~D7), and STOP bit. The START bit is transmitted out first.
4. The TI0 (SCON0.1) bit of SFR SCON0 is set to HIGH when the stop bit is placed on the P3.1/TXD pin.

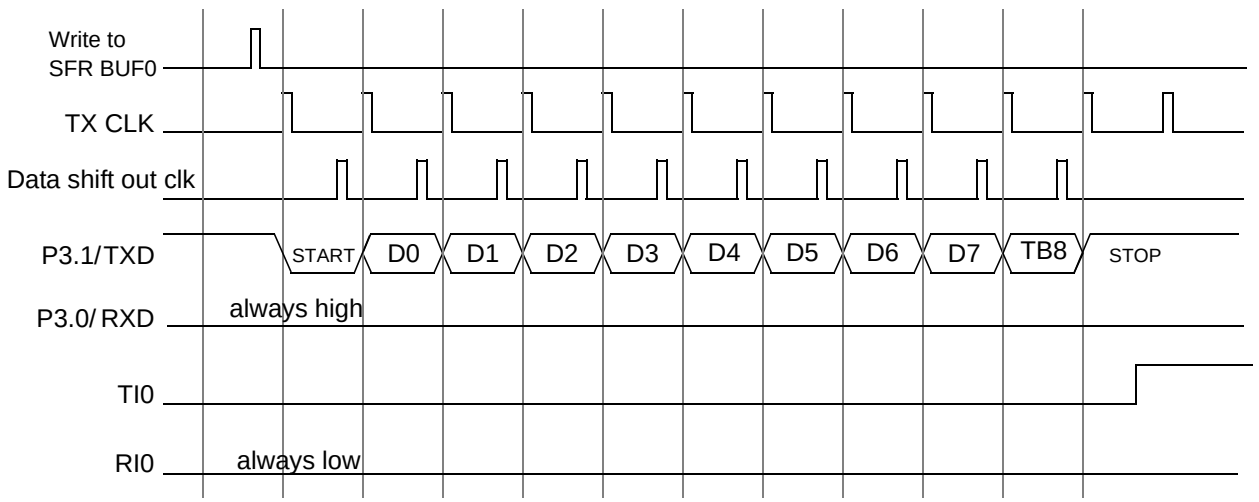


Fig.25 UART0 mode 2 transmission timing

12.7.4 DATA RECEPTION TIMING IN MODE 2

A data reception session in mode 2 is as follows:

1. First, the reception function of the UART0 must be enabled by setting REN0=1 and then the UART0 starts detecting if there is a falling edge on the P3.0/RXD input. For detecting this falling edge, UART0 samples the P3.0/RXD input pin sixteen times per bit time for any baud rate.
2. When a falling edge on the P3.0/RXD pin is detected by UART0, the divided-by-16 counter of the baud rate generation circuit is reset. The output of the divided-by-16 counter is the receiver clock, RX CLK. This action is for aligning Timer 1 or Timer 2 overflow to bit boundaries. Please refer to Fig.27 for baud rate generation circuit.
3. For noise rejection, the UART0 decides the value of each received bit by *majority decision* of three consecutive samples in the middle of each bit time. That is, if three consecutive sampled values are 110, then the received bit value is regarded as HIGH. Similarly, if three consecutive sampled values are 101, then the received bit value is still regarded as HIGH.
4. If the first received bit is not LOW, then the reception session is aborted and the UART0 waits for another falling edge on the P3.0/RXD pin.
5. If the first received bit is LOW, then a reception session is initiated and the UART0 continues to receive the following data bits (D0~D7). The bit value is decided by use of *majority decision*.
6. At the middle of the stop bit time, the UART0 checks the following conditions:
   a) RI0 must be LOW,
   b) if SM2 has been programmed to HIGH, then the received 9th bit must also be HIGH. (If SM2 has been programmed to LOW, the received 9th bit can be LOW or HIGH.)
7. If the above conditions are met, then the UART0 moves the received data byte from the temporary Receive Register (please refer to Fig.20) to SFR SBUF0, moves the received 9th bit to the RB8 bit of SFR SCON0, and set RI0 bit to HIGH, triggering an UART0 data reception interrupt. If the above conditions are not met, the received data is ignored and the receive session is aborted.
8. After the middle of the stop bit time, the UART0 continues to wait for another high-to-low transition on the P3.0/RXD pin.

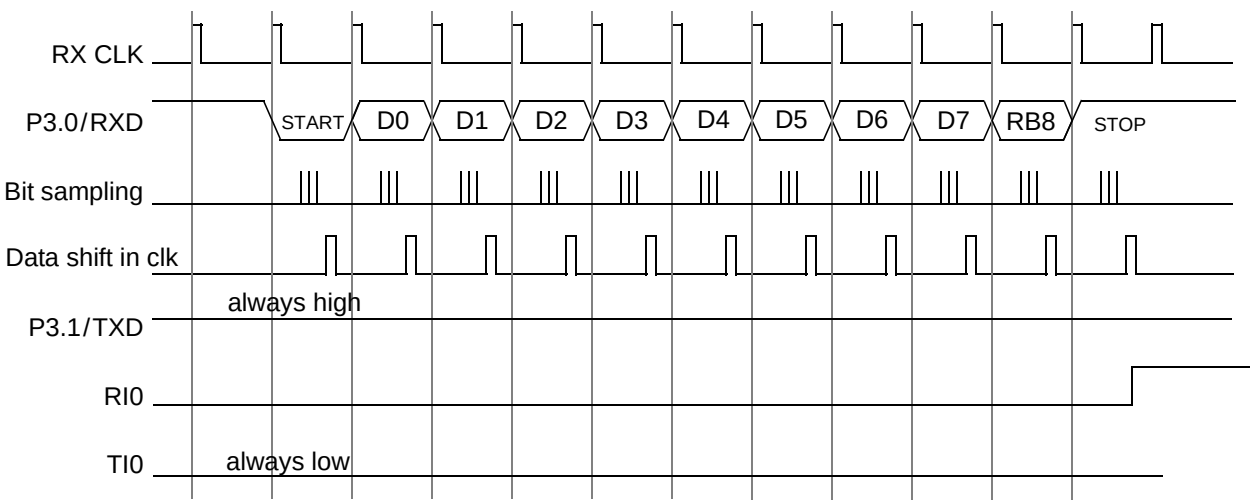


Fig.26 UART0 mode 2 reception timing

12.8 Mode 3

12.8.1 Operation of mode 3

Mode 3 provides 11-bits, asynchronous, full-duplex transmission or reception. Its transmission or reception word format is composed of:

- one start bit,
- eight data bits,
- one programmable 9th bit, and
- one stop bit.

The word format is shown below. It is actually identical to that of Mode 2.

	START	D0	D1	D2	D3	D4	D5	D6	D7	TB8/RB8	STOP

The data bits are transmitted and received LSB first.

Mode 3 operation is actually identical to Mode 2 operation, except baud rate. The Mode 3 baud rate generation is identical to Mode 1. That is, Mode 3 is a combination of Mode 2 transmission/reception protocol and Mode 1 baud rate generation.

12.8.2 Baud rate of mode 3

Mode 3 baud rate can be from timer 1 overflow or timer 2 overflow. Please refer to Section 12.9 “Baud Rate Generation for Mode 1 and Mode 3”

12.8.3 Data transmission in mode 3

Please refer to the description for mode 2.

12.8.4 Data reception in mode 3

Please refer to the description for mode 2.

12.9 Baud Rate Generation for Mode 1 and Mode 3

In both Mode 1 and Mode 3, baud rate is derived from **Timer 1** or **Timer 2** overflow. Fig.27 gives the divider circuit used to derive receiver baud rate and transmitter baud rate from Timer 1 overflow or Timer 2 overflow.

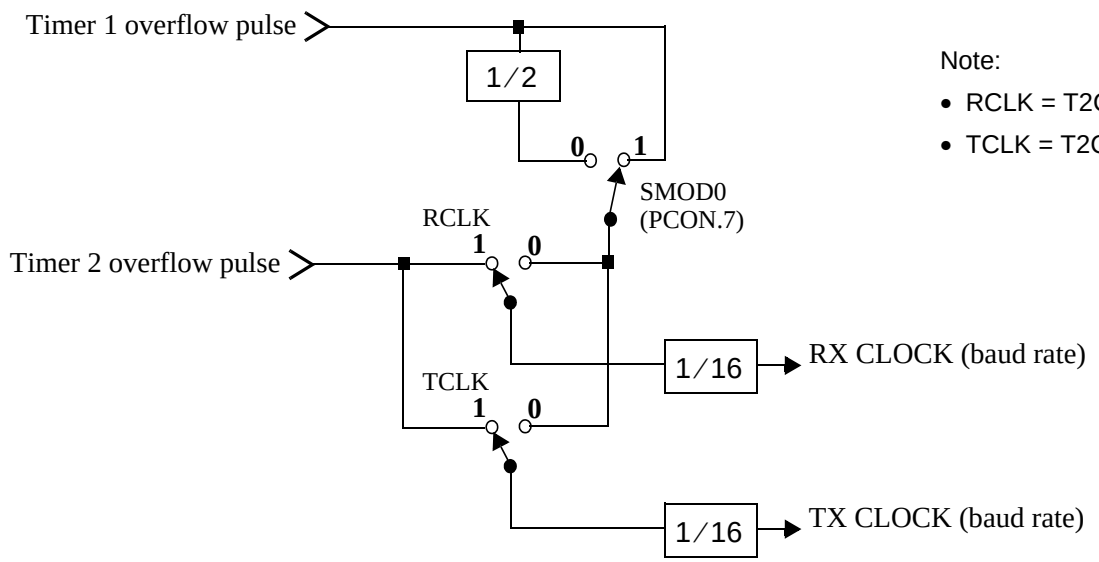


Fig.27 baud rate generation from Timer 1 or Timer 2 overflow

12.9.1 USING TIMER 1 TO GENERATE BAUD RATES

When Timer 1 is used as the baud rate generator, the baud rates in Modes 1 and 3 are determined by the Timer 1 overflow rate and the value of the SMOD0 bit of the SFR PCON, as follows:

$$\text{Baud rate} = \frac{2^{SMOD}}{32} \times \text{Timer1 overflow rate}$$

The Timer 1 interrupt should be disabled in this application.

The Timer 1 itself can be programmed for either **timer** or **counter** operation in any of its 3 running modes. In most typical applications, it is programmed for **timer** operation, in the Auto-Reload mode (high nibble of TMOD=0010B). In this case the baud rate is given by the formula:

$$\text{Baud rate} = \frac{2^{SMOD}}{32} \times XTAL1 \times \frac{1}{[12 \times (256 - TH1)]}$$

By programming Timer 1 to run as a 16-bit timer (high nibble of TMOD=0001B), and using the Timer 1 interrupt to do a 16-bit software reload, very low baud rate can be achieved

Table 49 lists sample reload values for a variety of common serial port baud rate.

Table 49 Timer 1 reload value for UART0 Mode 1 and Mode 3 baud rate.

Desired Baud rate	SMOD0 (PCON.7)	C/$\overline{T2}$ (TMOD.6)	Timer 1 Mode	33 MHz XTAL1	25 MHz XTAL1	11.0592 MHz XTAL1
57.6 Kb/s	1	0	2	FDh	FEh	FFh
19.2 Kb/s	1	0	2	F7h	F9h	FDh
9.6 Kb/s	1	0	2	EEh	F2h	FAh
4.8 Kb/s	1	0	2	DCh	E5h	F4h
2.4 Kb/s	1	0	2	B8h	CAh	E8h
1.2 Kb/s	1	0	2	71h	93h	D0h

12.9.2 USING TIMER 2 TO GENERATE BAUD RATES

Please refer to Section 11.6 “Baud Rate Generator Mode” for detailed description of using Timer 2 to generate baud rate for the UART0.

12.10 Multiprocessor communications

Mode 2 supports multiprocessor communication, in which a master transmitter can send data to one or more slave receivers. The 9th data bit is used to indicate an address byte or data byte. When the 9th data bit is HIGH, the transmitted byte is an address byte. When the 9th data bit is LOW, the transmitted byte is a data byte.

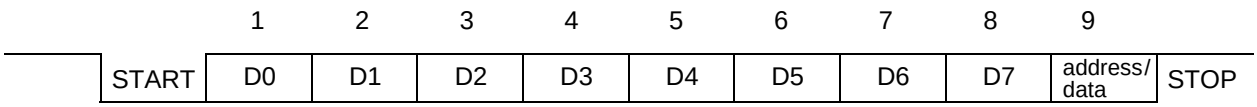


Fig.28 word format for multiprocessor communication

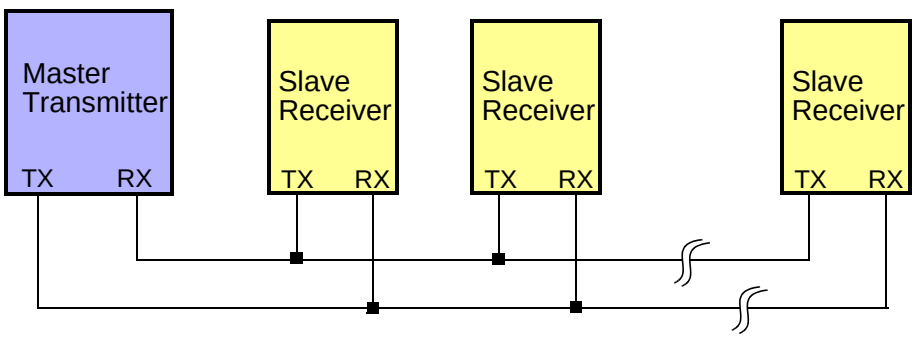


Fig.29 UART0 multiprocessor communication

A typical session of multiprocessor communication is as follows:

1. Enable all slave receivers for reception by setting REN=1 and clearing RI=0.
2. Setting SM2=1 for all slave receivers. SM=1 indicates that only an address byte, which has its 9th data bit set to HIGH, can be received by all slave receivers.
3. The master transmitter broadcasts an address byte out.
4. All the UART0s of all slave receivers receive this address byte and interrupt their respective CPU.
5. All slave receivers execute their UART0 interrupt subroutine.
6. In the interrupt subroutine, the received address is compared with the slave's pre-assigned address. If the two addresses match, then the SM2 bit is cleared to LOW. SM2=LOW indicates that the 9th bit data bit can be LOW or HIGH. That is, the addressed slave can always receive next transmitted data bytes from the master transmitter.
7. If the received address does not match with the slave's own pre-assigned address, the slave keeps its SM2 bit set to HIGH, indicating that the slave will not be able to received the next transmitted data bytes.
8. A communication channel is therefore established between the master transmitter and the addressed slave receiver. The master can continue to send data bytes to the addressed slave receiver. All other un-addressed slave receivers can not receive the following data bytes, because their SM2 bits remain at HIGH.
9. Once the entire message has been received, the addressed slave sets its SM2 bit to HIGH to block further interrupt and waits for the next address byte.

13 POWER-SAVING MODES

The STK6037 provides two power-saving modes: Idle mode and Stop mode. The bits that control entry into Idle mode and Stop modes are bits 0 (Idle mode) and bit 1 (Stop mode) of the Power Control Register (SFR PCON) at SFR adddress 87(hex). Table 50 gives a description of the Power Control Register (SFR PCON).

Table 50 Power Control Register (SFR PCON)

Bit	Mnemonics	Function
PCON.7	SMOD0	UART baud-rate doubler enable. When SMOD0=1, the baud rate for the UART is doubled. Please refer to Fig.20.
PCON. 6~4		Reserved.
PCON.3	GF1	General purpose flag 1. Bit-addressable, general-purpose flag for software control.
PCON.2	GF0	General purpose flag 0. Bit-addressable, general-purpose flag for software control.
PCON.1	STOP	STOP mode select. Setting the STOP=1 places the STK6037 in STOP mode.
PCON.0	IDLE	IDLE mode select. Setting the IDLE=1 places the STK6037 in IDLE mode.

If the STOP Mode and the Idle Mode are selected at the same time, the STOP Mode has higher priority, as can be obviously seen in Fig.30

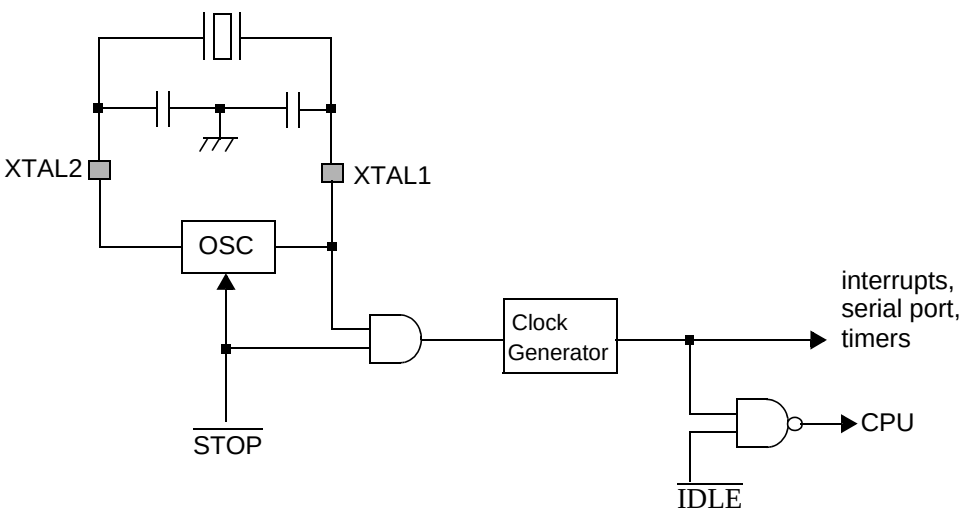


Fig.30 Power-saving modes.

13.1 Idle Mode

Idle mode operation permits the interrupt, serial ports and timers to function while the CPU is halted. The functions that are switched off when the microcontroller enters the Idle mode are:

- CPU (halted)

The functions that remain active during Idle mode are:

- Timer 0, Timer 1, Timer 2, and Watchdog Timer
- UART

- External/Internal interrupts
- External reset or power-on-reset.

The instruction that sets PCON.0 (=1) is the last instruction executed in the normal operating mode before Idle mode is activated.

Once in the Idle mode, the CPU status is preserved in its entirety: the Stack Pointer, Program Counter, Program Status Word, Accumulator, RAM and all other registers maintain their current data during Idle mode. The status of external pins during Idle mode is shown in Table 51.

There are three ways to terminate the Idle mode:

- Activation of any enabled interrupt from interrupt sources listed in Table 11 will cause PCON.0 to be cleared by hardware, terminating Idle mode, but only if there is no interrupt in service with the same or higher priority. The interrupt is serviced, and following return from interrupt instruction RETI, the next instruction to be executed will be the one which follows the instruction that wrote a logic 1 to PCON.0.

  The flag bits GF0 and GF1 may be used to determine whether the interrupt was received during normal execution or during Idle mode.

  For example, the instruction that writes to PCON.0 can also set or clear one or both flag bits.

  When Idle mode is terminated by an interrupt, the service routine can examine the status of the flag bits.
- The second way of terminating the Idle mode is with an external hardware reset. Since the oscillator is still running, the hardware reset is required to be active for two instruction cycles to complete the reset operation.
- The third way of terminating the Idle mode is by internal watchdog reset.

13.2 Stop mode

The instruction that sets PCON.1 is the last executed, prior to going into the Stop mode. Once in Stop mode, the crystal oscillator is stopped. The contents of the on-chip RAM (AUX Memory and Main Data Memory) and the SFRs are preserved.

Note that the Stop mode can not be entered when the Watchdog Timer has been enabled.

The Stop mode can be terminated only by an external reset (RAM is saved, but SFRs are cleared due to reset).

The status of the external pins during Stop mode is shown in Table 51.

In the Stop mode, Vdd supplies to the CPU can be reduced to minimize power consumption. It must be ensured, however, that Vdd is not reduced before the Stop mode is activated, and that the Vdd is restored to its normal operating level before the Stop mode is terminated by hardware reset. The reset signal that terminates the Stop mode also restarts the oscillator.The reset signal should not be activated before Vdd is restored to its normal operating level and must be held active long enough to allow the oscillator to restart and stabilize(similar to power-on reset).

13.3 Status of external pins during power-saving modes

Table 51 Status of external pins during Idle and Stop modes.

MODE	Memory	PORT 1	PORT 2	PORT 3
Idle	internal	port data	port data	port data
Stop	internal	port data	port data	port data

13.4 Summary of Power-saving Modes

Table 52 .Summary of power-saving modes

MODE	Example for enabling the mode	TERMINATED BY	REMARKS
Idle	ORL PCON, #01H	• Enabled interrupt • External hardware reset • Watchdog Timer overflow.	• CPU clock is gated off, that is, no clock is added to the CPU and CPU stays at its current state. • CPU status registers maintain their data. • Peripherals are active.
Stop	ORL PCON, #02H	External hardware reset	• Crystal oscillator is stopped. • Contents of on-chip RAM and SFRs are maintained. • However, leaving Power- Down mode means redefinition of SFR contents.

14 RESET

14.1 Sources of RESET

There are 5 sources to reset the STK6037:

- A high pulse from external RESET pin,
- Power-on reset, when power is first added to the STK6037
- Low-voltage detection reset,
- Watchdog timer overflow, and
- ISP programming is on-going.

The functional diagram of the reset sources is shown in Fig.31.

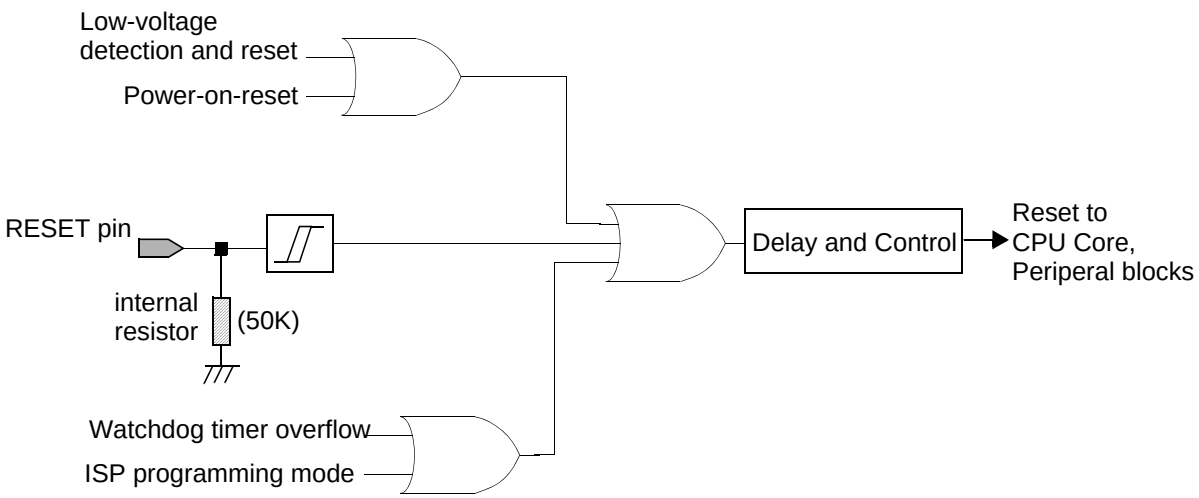


Fig.31 Functional diagram of reset circuit

14.2 Power-On- Reset (POR) with fast-rising power supply

The STK6037 can be reset by the on-chip power-on-reset, whose switching level is 3.7 ± 0.2 volts. The sequence of the power-on-reset is as follows:

1. As soon as the power supply (VDD) reaches the POR switching level, the on-chip POR generates a pulse, called POR Pulse.
2. This POR pulse then triggers an internal reset, POC. Also, this POR pulse resets the internal reset counter.
3. When the oscillator is stable enough, the oscillator clocks starts triggering the internal reset counter to count.
4. When the internal reset counter counts up to 2048 and overflows, the internal reset (POC) is released and the CPU starts executing instruction.

The above sequence is further illustrated in Fig.32.

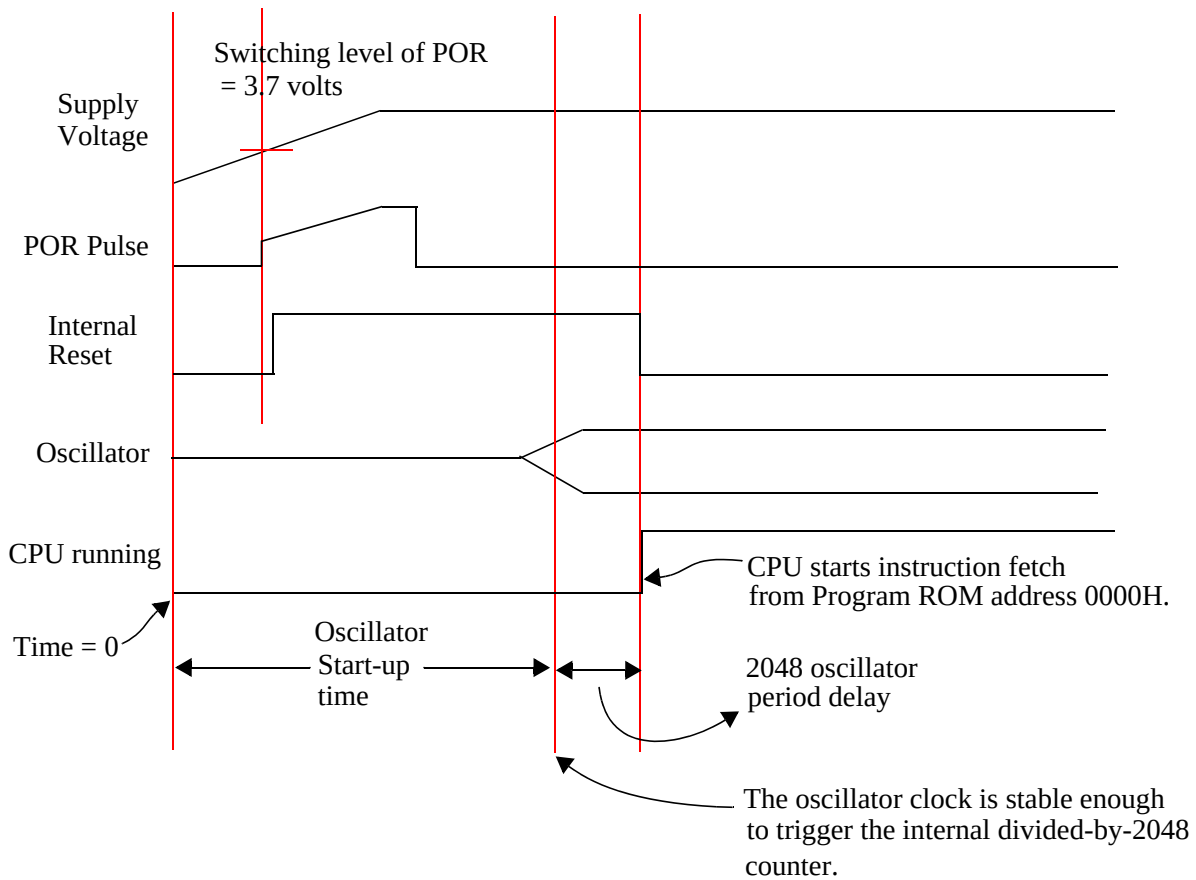


Fig.32 Timing of Power-On-Reset with fast rising VDD.

14.3 Asynchronous reset by adding a HIGH pulse to the RESET pin

The STK6037 can be reset by adding a HIGH pulse to the RESET pin. The RESET pin is an input with an internal Schmitt-trigger for noise reduction. The CPU checks if there is a reset at cycle 4 (C4) of every instruction cycle. A reset is accomplished by holding the RESET pin HIGH for at least two instruction cycles while the oscillator is running. The CPU responds by executing an internal reset.

14.4 Low-power detection and reset

The STK6037 has the capability of low-power detection and reset. The reset due to low power can be enabled or disabled by use of the LVR bit (bit 0) of SFR CHIPCON, at SFR address BF(hex). Setting LVR=0 enables low-power reset and setting LVR=1 disables low-power reset.

Due to fabrication process variations from different production lots, the threshold voltage for low-power detection is in the range of 3.2 ~ 3.4 volts, without regard to the supply voltage to the VDD pin. The typical low-power threshold voltage is 3.3 volts.

14.5 Reset from the Watchdog Timer overflow

The microcontroller can also be reset by the Watchdog Timer overflow. Please refer to Chapter 11 .

15 OSCILLATOR CIRCUIT

15.1 The Oscillator Circuit

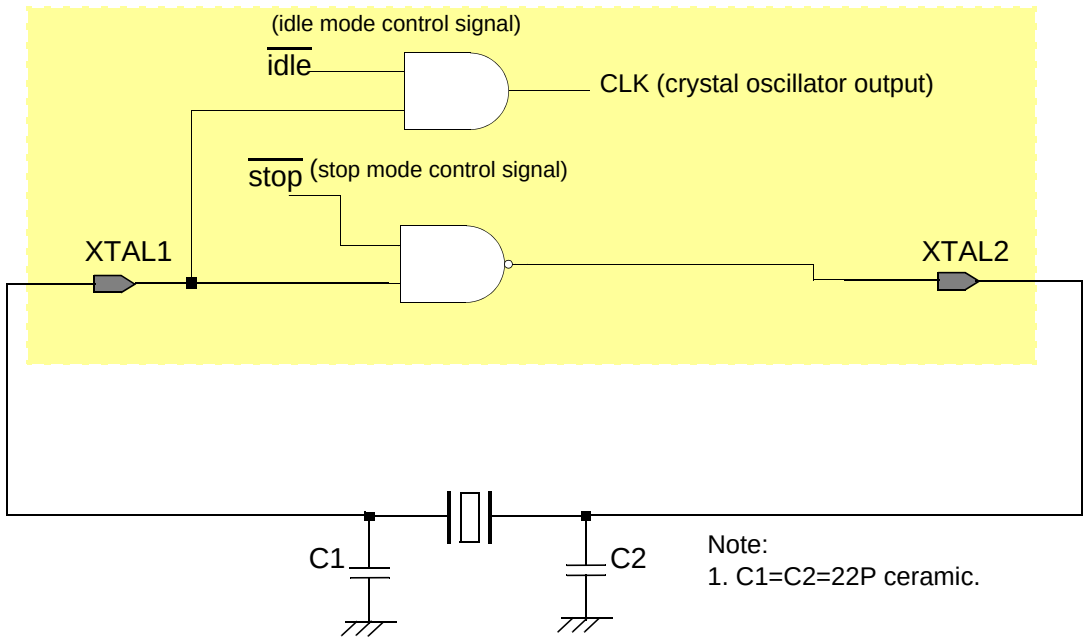


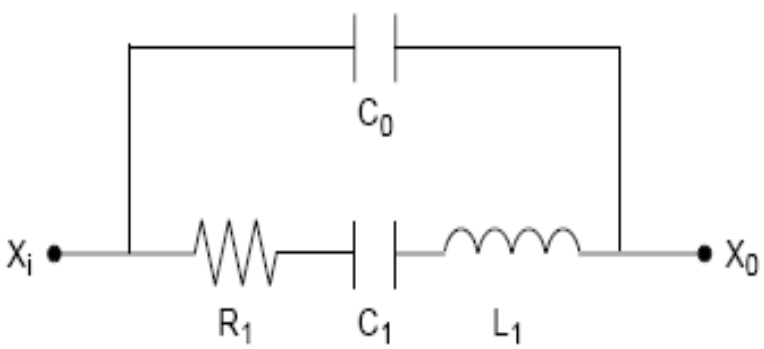
Fig.33 Oscillator Circuit.

XTAL1 is the high gain amplifier input, and XTAL2 is the output. To drive the STK6037 externally, XTAL1 is driven from an external clock source and XTAL2 is left open.

15.2 The values for R, C1, and C2

The recommended values for R, C1, and C2 given Fig.33 is for the frequency range from 2M Hz to 30M Hz.

Since the performance of the crystal oscillator is closely related to the characteristics of the crystal itself, the user should contact the crystal manufacturer for its characteristics. The crystal parameters we used for design is shown in Fig.34.



The parameter for the crystal is:
R1=10 ohm, C1=25 fF, and
C_0=7 pF.

Fig.34 crystal parameters

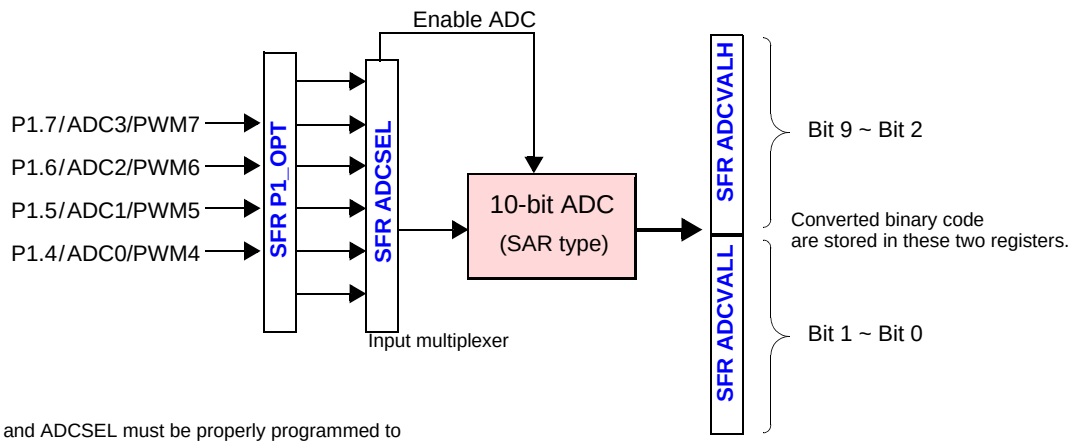
16 10-BIT ANALOG-TO-DIGITAL CONVERTER (10-BIT ADC)

16.1 ADC functional description

The STK6037 has a **10-bit successive approximation ADC with 4 multiplexed analog input channels**. ADC channel inputs share with Port 1 pins. Analog input voltage range can be from 0 V to 5.0 V.

Four SFRs (P1_OPT, ADCSEL, ADCVALH, and ADCVALL) perform the user software interface to the ADC; see Table 53 for an overview of the ADC SFRs.

Figure 35 shows the relation between SFRs and the ADC.



(1) SFRs P1_OPT and ADCSEL must be properly programmed to have propoer operation of the 10-bit ADC system.

(2) Program SFR P1_OPT to configure Port 1 pins as either a port pin or an analog input pin. Each pin can be individually programmed.

(3) Program SFR ADCSEL to select one channel of the multiplexed 4-channel input.

Fig.35 Functional block diagram of the 10-bi ADC

16.2 ADC during Idle and Stop mode

The analog-to-digital converter is active only when the microcontroller is in normal operating mode. If the Idle or Stop mode is activated, then the ADC is switched off and put into a power saving idle state - a conversion in progress is aborted. The conversion result registers (SFR ADCVALL and SFR ADCVALH) are not affected.

16.3 ADC SFRs and their reset value

Four SFRs (P1_OPT, ADCSEL, ADCVALH, and ADCVALL) are associated with the ADC. An overview of these four registers is given in Table 53.

Table 53 ADC Special Function Registers overview

ADDRESS	NAME	R/W	DESCRIPTION
D9(hex)	P1_OPT	R/W	Selection of Port 1 pin function.
DA(hex)	ADCSEL	R/W	Channel selection.
DB(hex)	ADCVALH	R/W	The upper 8 bits (bit9 ~ bit2) of the converted ADC value.
DC(hex)	ADCVALL	R/W	The lower 2 bits (bit1 and bit0) of the converted ADC value

16.3.1 P1_OPT REGISTER

The P1_OPT SFR has only 4bits. It is used to configure Port 1 pins to be either a normal I/O port pin or an analog input pin for the 10-bit SAR ADC.

Table 54 P1_OPT register (address D9 hex)

Bit Number	BIT 7	BIT 6	BIT 5	4 BIT	BIT 3	BIT 2	BIT 1	BIT 0
Bit Name	x	x	x	x	ADC3E	ADC2E	ADC1E	ADC0E
Rest Value	x	x	x	x	0	0	0	0

Note: X= don't care.

Table 55 Description of P4_OPT Register bits

BIT	SYMBOL	DESCRIPTION
Bits 4~7		Not implemented.
3	ADC3E	ADC3E=1 configures pin P1.7/ADC3/PWM7 as ADC3 input pin. ADC3E=0 configures pin P1.7/ADC3/PWM7 as P1.7 or PWM7 output.
2	ADC2E	ADC2E=1 configures pin P1.6/ADC2/PWM6 as ADC2 input pin. ADC2E=0 configures pin P1.6/ADC2/PWM6 as P1.6 or PWM6 output.
1	ADC1E	ADC1E=1 configures pin P1.5/ADC1/PWM5 as ADC1 input pin. ADC1E=0 configures pin P1.5/ADC1/PWM5 as P1.5 or PWM5 output.
0	ADC0E	ADC0E=1 configures pin P1.4/ADC0/PWM4 as ADC0 input pin. ADC0E=0 configures pin P1.4/ADC0/PWM4 as P1.4 or PWM4 output.

16.3.2 THE ADCSEL REGISTER

The ADCSEL Register is used to select an input channel for conversion. For proper conversion of the input analog voltage, do the following:

1. Select a channel for analog signal input,
2. Then, enable the ADC by setting the EADC bit to HIGH.

Table 56 ADCSEL Register (SFR address DA hex)

Bit Number	BIT 7	BIT 6	BIT 5	4 BIT	BIT 3	BIT 2	BIT 1	BIT 0
Bit Name	EADC	x	x	ADC_data_ ready	SAD3	SAD2	SAD1	SAD0
Reset Value	0	x	x	0	0	0	0	0

Note: x= don't care.

Table 57 Description of ADC Register bits

BIT	SYMBOL	DESCRIPTION
7	EADC	Enable the ADC.
6, 5		not implemented.
4	ADC_data_ready	ADC convert ready flag.
3	SADC3	SADC3=1 selects analog signal from P1.7/ADC3 pin for conversion. SADC3=0 un-selects this pin.
2	SADC2	SADC2=1 selects analog signal from P1.6/ADC2 pin for conversion. SADC2=0 un-selects this pin for conversion.
1	SADC1	SADC1=1 selects analog signal from P1.5/ADC1 pin for conversion. SADC1=0 un-selects this pin for conversion.
0	SADC0	SADC0=1 selects analog signal from P1.4/ADC0 pin for conversion. SADC0=0 un-selects this pin for conversion.

16.3.3 ADCVALH AND ADCVALL REGISTERS

The converted binary code of the 10-bit SAR ADC conversions is stored in the ADCVALH and ADCVALLRegister.

Table 58 ADCVALH Register (address DB hex)

Bit Number	BIT 7	BIT 6	BIT 5	4 BIT	BIT 3	BIT 2	BIT 1	BIT 0
Bit Name	Upper 8 bits (Bit 9 ~ Bit 2) of the converted binary code.							
Reset Value	0	0	0	0	0	0	0	0

Table 59 ADCVALL Register (address DC hex)

Bit Number	BIT 7	BIT 6	BIT 5	4 BIT	BIT 3	BIT 2	BIT 1	BIT 0
Bit Name	x	x	x	x	x	x	Lower 2 bits (Bit 1 ~ Bit 0) of the converted binary code.	
Reset Value	x	x	x	x	x	x	0	0

16.4 ADC application guide

The analog input voltage should be stable when the ADC is enabled to perform conversion. An RC low pass filter may be added to the analog input pins to filter out high frequency noises.The capacitor between an analog input pin and the ground pin should be placed as close to the pins as possible, in order to have maximum effect in minimizing input noise coupling.

17 PWM (PULSE WIDTH MODULATED OUTPUT)

17.1 SFRs associated with the PWM system

The STK6037 has 21 10-bit PWM. For mulitple functions on a specific pin, the PWM function has the higher priority.

Table 60 SFRs for PWMs

SYMBOL	DESCRIPTION	Address(Hex format)	RESET VALUE
PWM_EA0	Select Port 1 pins, P1.0 ~ P1.7, as normal P1 I/O pin or outputs of PWM0 ~ PWM7.	D2	0000 0000
PWM_EA1	Select pins P22, P21, P20, P37, P35, P34, P33, and P32 as normal port I/O pins or outputs of PWM15 ~ PWM8.	D3	0000 0000
PWM_EA2	Select pins P27 ~ P23 as as normal port I/O pin or outputs of PWM20 ~ PWM16.	D4	xxx0 0000
PCLKSEL	PWM clock Setting Register	B7	0000 0000
PWM0H	PWM0 higher 8 bits, Bit9 ~ Bit2	F9	1000 0000
PWM0L	PWM0 lower 2 bits, Bit1 and Bit0	FA	00xx xxxx
PWM1H	PWM1 higher 8 bits, Bit9 ~ Bit2	FB	1000 0000
PWM1L	PWM1 lower 2 bits, Bit1 and Bit0	FC	00xx xxxx
PWM2H	PWM2 higher 8 bits, Bit9 ~ Bit2	FD	1000 0000
PWM2L	PWM2 lower 2 bits, Bit1 and Bit0	FE	00xx xxxx
PWM3H	PWM3 higher 8 bits, Bit9 ~ Bit2	F1	1000 0000
PWM3L	PWM3 lower 2 bits, Bit1 and Bit0	F2	00xx xxxx
PWM4H	PWM4 higher 8 bits, Bit9 ~ Bit2	F3	1000 0000
PWM4L	PWM4 lower 2 bits, Bit1 and Bit0	F4	00xx xxxx
PWM5H	PWM5 higher 8 bits, Bit9 ~ Bit2	F5	1000 0000
PWM5L	PWM5 lower 2 bits, Bit1 and Bit0	F6	00xx xxxx
PWM6H	PWM6 higher 8 bits, Bit9 ~ Bit2	E9	1000 0000
PWM6L	PWM6 lower 2 bits, Bit1 and Bit0	EA	00xx xxxx
PWM7H	PWM7 higher 8 bits, Bit9 ~ Bit2	EB	1000 0000
PWM7L	PWM7 lower 2 bits, Bit1 and Bit0	EC	00xx xxxx
PWM8H	PWM8 higher 8 bits, Bit9 ~ Bit2	ED	1000 0000
PWM8L	PWM8 lower 2 bits, Bit1 and Bit0	EE	00xx xxxx
PWM9H	PWM9 higher 8 bits, Bit9 ~ Bit2	B9	1000 0000
PWM9L	PWM9 lower 2 bits, Bit1 and Bit0	BA	00xx xxxx
PWM10H	PWM10 higher 8 bits, Bit9 ~ Bit2	BB	1000 0000
PWM10L	PWM10 lower 2 bits, Bit1 and Bit0	BC	00xx xxxx
PWM11H	PWM11 higher 8 bits, Bit9 ~ Bit2	BD	1000 0000
PWM11L	PWM11 lower 2 bits, Bit1 and Bit0	BE	00xx xxxx
PWM12H	PWM12 higher 8 bits, Bit9 ~ Bit2	B1	1000 0000
PWM12L	PWM12 lower 2 bits, Bit1 and Bit0	B2	00xx xxxx
PWM13H	PWM13 higher 8 bits, Bit9 ~ Bit2	B3	1000 0000
PWM13L	PWM13 lower 2 bits, Bit1 and Bit0	B4	00xx xxxx
PWM14H	PWM14 higher 8 bits, Bit9 ~ Bit2	B5	1000 0000
PWM14L	PWM14 lower 2 bits, Bit1 and Bit0	B6	00xx xxxx

SYMBOL	DESCRIPTION	Address(Hex format)	RESET VALUE
PWM15H	PWM15 higher 8 bits, Bit9 ~ Bit2	A9	1000 0000
PWM15L	PWM15 lower 2 bits, Bit1 and Bit0	AA	00xx xxxx
PWM16H	PWM16 higher 8 bits, Bit9 ~ Bit2	AB	1000 0000
PWM16L	PWM16 lower 2 bits, Bit1 and Bit0	AC	00xx xxxx
PWM17H	PWM17 higher 8 bits, Bit9 ~ Bit2	AD	1000 0000
PWM17L	PWM17 lower 2 bits, Bit1 and Bit0	AE	00xx xxxx
PWM18H	PWM18 higher 8 bits, Bit9 ~ Bit2	A1	1000 0000
PWM18L	PWM18 lower 2 bits, Bit1 and Bit0	A2	00xx xxxx
PWM19H	PWM19 higher 8 bits, Bit9 ~ Bit2	A3	1000 0000
PWM19L	PWM19 lower 2 bits, Bit1 and Bit0	A4	00xx xxxx
PWM20H	PWM20 higher 8 bits, Bit9 ~ Bit2	A5	1000 0000
PWM20L	PWM20 lower 2 bits, Bit1 and Bit0	A6	00xx xxxx

17.2 Functional block diagram of 10-bit PWMs

Fig.36 gives functional diagram of the PWM.

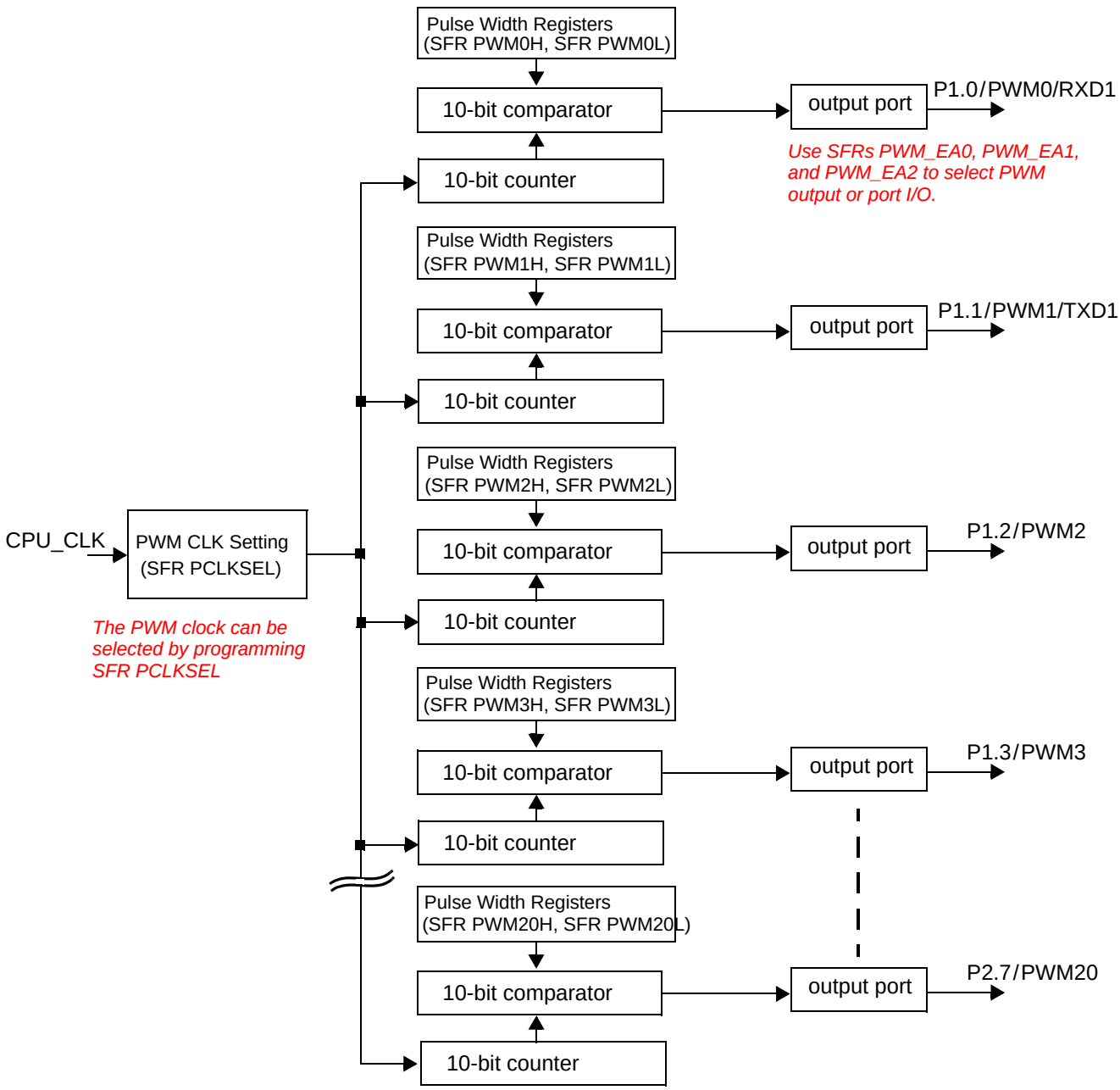


Fig.36 PWM functional block diagram

17.3 PWM/Port 1 Output Select Registers PWM_EA0, PWM_EA1, and PWM_EA2

Each bit of these three SFRs (PWM_EA0, PWM_EA1, and PWM_EA2) is used to configure a port pin to be port data I/O or a PWM output. SFR PWM_EA0 is for PWMs 0~7, SFR PWM_EA1 is for PWMs 8~15, and SFR PWM_EA2 is for PWMs 16~20.

Table 61 PWM_EA0 Register(address D2 hex)

Bit position	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	PWM_EA07	PWM_EA06	PWM_EA05	PWM_EA04	PWM_EA03	PWM_EA02	PWM_EA01	PWM_EA00
Controlled I/O pin	P1.7	P1.6	P1.5	P1.4	P1.3	P1.2	P1.1	P1.0
Controlled PWM	PWM7	PWM6	PWM5	PWM4	PWM3	PWM2	PWM1	PWM0
Reset value	0	0	0	0	0	0	0	0

Table 62 Description of SFR PWM_EA0 bits

BIT	SYMBOL	DESCRIPTION
7 to 0	PWM_EA07 to PWM_EA00	These bits are used to configure Port 1 pins to be an I/O pin or PWM output pin. When PWM_EAxx=0, the controlled port pin works as an I/O pin, xx=00 ~ 07 When PWM_EAxx=1, the controlled port pin works as PWM output pin, xx=00 ~ 07.

Table 63 PWM_EA1 Register(address D3 hex)

Bit position	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	PWM_EA17	PWM_EA16	PWM_EA15	PWM_EA14	PWM_EA13	PWM_EA12	PWM_EA11	PWM_EA10
Controlled I/O pin	P2.2	P2.1	P2.0	P3.7	P3.5	P3.4	P3.3	P3.2
Controlled PWM	PWM15	PWM14	PWM13	PWM12	PWM11	PWM10	PWM9	PWM8
Reset value	0	0	0	0	0	0	0	0

Table 64 Description of SFR PWM_EA1 bits

BIT	SYMBOL	DESCRIPTION
7 to 0	PWM_EA17 to PWM_EA10	These bits are used to configure Port 2 or Port 3 pins to be an I/O pin or a PWM output pin. When a PWM_EAxx bit (xx=17~10) is programmed to be LOW, its controlled pin works as a normal I/O pin. When PWM_EAxx bit is programmed to be HIGH, its controlled pin works as a PWM n output pin, n=8 ~ 15.

Table 65 PWM_EA2 Register(address D4 hex)

Bit position	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbols				PWM_EA24	PWM_EA23	PWM_EA22	PWM_EA21	PWM_EA20
Controlled I/O pin				P2.7	P2.6	P2.5	P2.4	P2.3
Controlled PWM				PWM20	PWM19	PWM18	PWM17	PWM16
Reset value	x(undertermined)			0	0	0	0	0

Table 66 Description of SFR PWM_EA2 bits

BIT	**SYMBOL**	**DESCRIPTION**
4 to 0	PWM_EA24 to PWM_EA20	These bits are used to configure Port 2 pins to be an I/O pin or PWM output pin. When a PWM_EAxx bit (xx=24 ~ 20) is programmed to be LOW, its controlled pin works as a normal I/O pin. When PWM_EAxx is programmed to be HIGH, its controlled pin works as output pin.

17.4 Pulse Width Registers (PWM0H, PWM0L ~ PWM20H, PWM20L)

Each PWM is composed of two SFRs. PWMnH contains higher 8 bits. PWMnL contains lower two bits, n = 0~20.

Table 67 Pulse width registers (R/W)

Register Name	Address (hex)	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
PWM0H	F9	Pulse width of PWM0 higher 8 bits.							
PWM0L	FA	Pulse width of PWM0 lower 2 bits..							
~~									
PWM20H	A5	Pulse width of PWM20 higher 8 bits.							
PWM20L	A6	Pulse width of PWM20 lower 2 bits..							
Reset value		1	0	0	0	0	0	0	0

17.5 PWM Clock Selection Register, SFR PCLKSEL

PWM Clock Selection Register, SFR PCLKSEL at address B7 hex, is for configuring the frequency of the clock added to the PWMs.

The PWM clock frequency = CPU clock frequency / [(value of SFR PCLKSEL) + 1]. For example, if the value of SFR PCLKSEL is 0, the PWM clock frequency will be equal to CPU clock frequency. The default value of SFR PCLKSEL=00.

17.6 PWM timing diagram

The value of a Pulse Width Registers indicates the HIGH pulse width within an interval of 2^{10}=1024 PWM Clocks, as illustrated in Fig.37.

When a PWM width register (PWMnL or PWMnH, n=0~20) is loaded with a new value, the associated output is updated immediately. It does not have to wait until the end of the current counter period. All PWMn output pins are driven by push-pull output drivers.

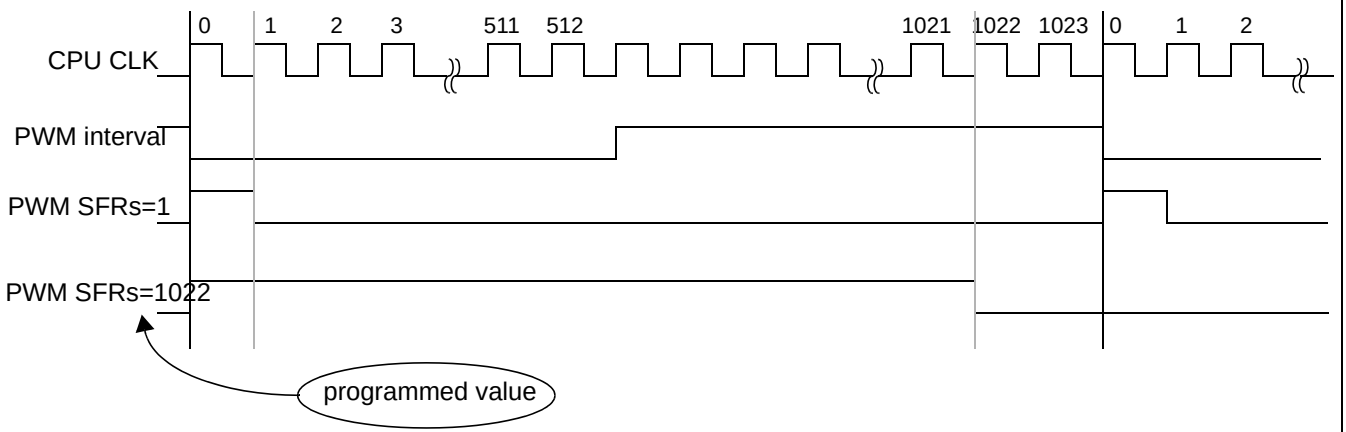


Fig.37 value of a PWM SFR and the pulse width

17.7 Selection of P1.4, P1.5, P1.6, P1.7 as PWM outputs or as ADC inputs

Each of pins Port1.4~Port1.7 has triple functions.

- P1.7/PWM7/ADC3
- P1.6/PWM6/ADC2
- P1.5/PWM5/ADC1
- P1.4/PWM4/ADC0

SFR PWM_EA0, SFR P1_OPT and SFR ADCSEL need to be correctly programmed to configure each pin to the desired funtion. Fisrt, the PWM has the higher priority, so when the PWM_EA04 to PWM_EA07 bit are set then PWM function work. Secondly, when PWM_EA04 to PWM_EA07 bit are cleared, SFR P1_OPT and SFR ADCSEL are programmed to configure a pin to be a port data I/O pin or a ADC output pin.

18 PORT 1, PORT 2, PORT 3

18.1 General Description

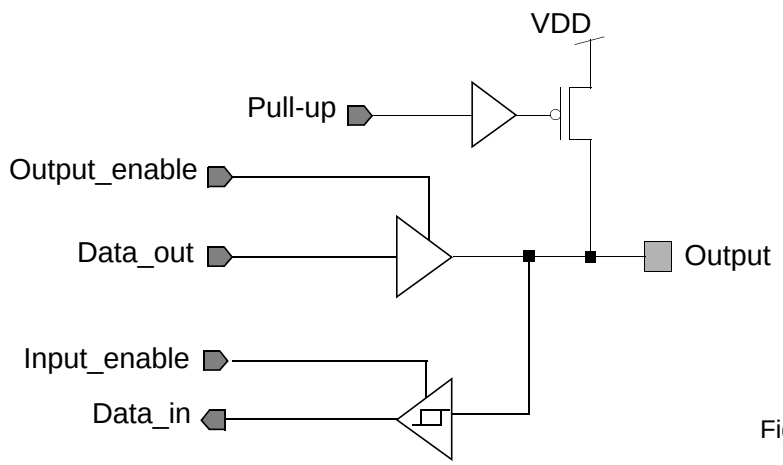
The STK6037 has two 8-bits ports (Port 1 and Port 2)and one 7-bit port (Port 3). P3.6 is not implemented. All bits of Port 1, Port 2, and Port 3 are push-pull outputs with internal weak pull-high PMOS.

18.2 Port 1, Port 2, and Port 3

Figure 38 shows Port 1, Port 2, and Port 3. They are push-pull outputs with internal weak pull-up.

SFR P1_OPT needs to be properly programmed to ensure porper operation of Port 1, because pins P1.4 ~ P1.7 are shared by port I/O, PWM and ADC input. Please refer to Section 14.2 for detailed description of SFR P1_OPT.

Port 3 is a multi-functional I/O port.



Pins of Port 1, Port 2, and Port 3 are push-pull outputs with weak internal pull-up. The output sinking and sourcing capability is 4 mA (typ.). The typical value of the equivalent resistance of the pull-up PMOS is 30K ohm.

Fig.38 Port 1, Port 2, and Port 3

18.3 MOVX instruction, Port 2, P3.6, P3.7

When executing MOVX instruction from internal program memory, an access to the internal AUX RAM will not affect Port 2, and P3.7.

18.4 Multiple-Function Port Pins

Some port pins have multiple functions. Port pins which are not used for alternate functions may be used as normal bidirectional I/O pins. The configuration of a port pin as an alternate function is carried out automatically by writing the associated SFR bit with proper value.

Please refer to Table 2 for a detailed decription of multiple-function pins.

19 ABSOLUTE MAXIMUM RATING

Table 68 Absolute Maximum Rating

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
VDD	voltage on VDD with respect to ground, and SCL, SDA to ground.	–0.3	+5.8	volts
V_I (note 1)	input voltage on any other pin with respect to ground.	–0.3	VDD + 0.3	volts
I_I, I_O	input/output current on any I/O pin	–	±19	mA
I_{total}	Absolute sum of all input currents during overload condition.		100	mA
P_{tot}	total power dissipation (note 2)	–	1.5	W
T_{stg}	storage temperature range	–40	+125	°C
T_{amb}	operating ambient temperature range.	-40	+ 85	°C

Notes

1. The following applies to the Absolute Maximum Ratings:
   a) Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device should refer to the normal DC and AC characteristics.
   b) This product includes ESD-protection circuits, specifically designed for the protection of its internal circuit. However, its suggested that conventional ESD precautions be taken.
   c) Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to ground.
2. This value is based on the maximum allowable die temperature and the thermal resistance of the package, not on device power consumption.

20 DC/AC CHARACTERISTICS

Table 69 DC and AC characteristics

Test condition: V_{DD} = 5.0 V ±10%; V_{SS} = 0 V; all voltages are with respect to V_{SS} , unless otherwise specified; T_{amb} = -40 to +85 °C; f_{XTAL1} = 12 MHz

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP	MAX.	UNIT
General						
V_{DD}	Operating supply voltage.		4.2	5.0	5.6	V
$T_{operating}$	Operating temperature range		-40		+85	°C
$F_{operating}$	Operating frequency range		2 MHz	24 MHz	30 MHz	
$I_{DD(NORMAL)}$	Operating supply current in normal mode, at CPU clock= 12 MHz.	notes 1, 2 and 3		6.4		mA
	Operating supply current in normal mode, at CPU clock= 12 x 2 MHz, double clock option..			8.4		
	Operating supply current in normal mode, at CPU clock= 12 / 3 MHz, divided-by-3 clock option..			5.0		
	Operating supply current in normal mode, at CPU clock= 12 / 48 MHz, divided-by-48 clock option..			4.3		
$I_{DD(IDLE)}$	supply current in Idle mode, at CPU clock= 12 MHz.	notes 1 ,2 and 3		3.9		mA
	supply current in normal mode, at CPU clock= 12 x 2 MHz, double clock option..			6.0		
	supply current in normal mode, at CPU clock= 12 / 3 MHz, divided-by-3 clock option..			2.5		
	supply current in normal mode, at CPU clock= 12 / 48 MHz, divided-by-48 clock option..			1.8		
$I_{DD(STOP)}$	supply current in Stop mode	notes 1 ,2 and 3		5.7		µA
Current sourcing/sinking capability of Ports 1, 2, 3, at VDD=5.0 volts						
I_{P1_source}	The PMOS sourcing current of Port 1.			170		µA
I_{P1_sink}	The NMOS sinking current of Port 1.			19		mA
I_{P2_source}	The PMOS sourcing current of Port 2.			170		µA
I_{P2_sink}	The NMOS sinking current of Port 2.			19		mA
I_{P3_source}	The PMOS sourcing current of Port 3.			170		µA
I_{P3_sink}	The NMOS sinking current of Port 3.			19		mA
Inputs HIGH/LOW voltage, Output HIGH/LOW voltage at VDD=5.0 volts.						
V_{IL}	Input LOW voltage to Port 1, Port 2, Port 3				1.8	volts

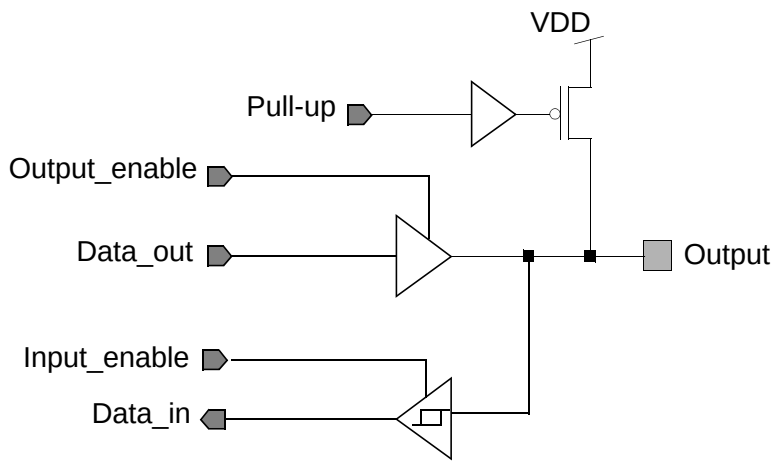
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP	MAX.	UNIT
V_{IH}	Input HIGH voltage to Port 1, Port 2, Port 3		3.7			volts
V_{OL}	Output LOW voltage of Port 1, Port 2, Port 3	I_{OL} = 3.2 mA		0.14		volts
V_{OH}	Output HIGH voltage of Port 1, Port 2, Port 3	I_{OH} = -25 µA		4.9		volts
V_{IH_RST}	Input HIGH voltage to RESET pin.		3.7			volts
V_{IL_RST}	Input LOW voltage to RESET pin.				1.8	volts
$C_{I/O}$	I/O pin capacitance	Frequency = 1 MHz; T_{amb} = 25 °C			10	pF

Notes to the DC characteristics

1. The operating supply current is measured with all output pins disconnected; XTAL1 driven with $t_r = t_f$ = 5ns; $V_{IL} = V_{SS}$ + 0.5 V; $V_{IH} = V_{DD}$ - 0.5 V.
2. The Idle mode supply current is measured with all output pins disconnected; XTAL1 driven with $t_r = t_f$ = 5ns; $V_{IL} = V_{SS}$ + 0.5 V; $V_{IH} = V_{DD}$ - 0.5 V; XTAL2 not connected.
3. The Stop mode current is measured with all output pins disconnected; XTAL2 not connected.
4. Pins of Ports 1, 2, and 3 source a transition current when they are being externally driven from HIGH to LOW. The transition current reaches its maximum value when V_{IN} is approximately 2.6 V.

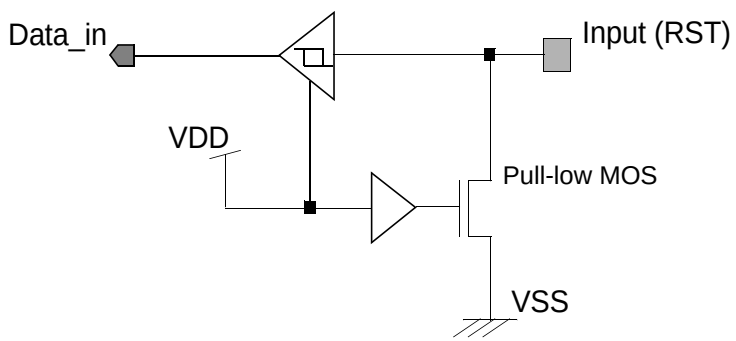
21 PIN CIRCUITS

21.1 Port 1 (P1.0 ~ P1.7), Port 2 (P2.0 ~ P2.7), Port 3 (P3.0 ~ P3.5, and P3.7)) circuit (Bidirectional I/O, with weak Pull-up)



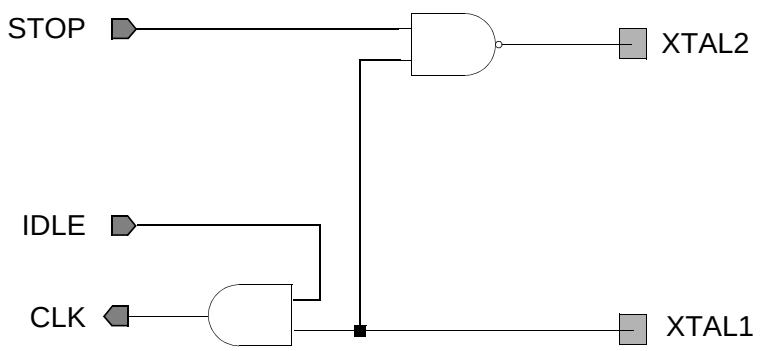
Pins of Port 1, Port 2, and Port 3 are push-pull outputs with weak internal pull-up. The output sinking and sourcing capability is 4 mA (typ.). The typical value of the equivalent resistance of the pull-up PMOS is 30K ohm.

21.2 RST (Input)



Note: This pin is weakly pulled down via internal pull-low MOS.

21.3 XTAL1, XTAL2



Please refer to Fig.36 for detail.

22 REDUCING ELECTROMAGNETIC EMISSION

There are two recommended ways to reduce chip's EMI emission: filtering and turning off ALE (not bonded out).

22.1 Filtering

Primary attention has been paid to the reduction of electromagnetic emission in the design of the STK6037. For example, the internal clock routing has been carefully arranged and internal decoupling capacitance has been added. However, in application, it is recommended that external capacitors should be connected across VDD and VSS pins. Lead length should be as short as possible. Ceramic chip capacitors are recommended (100 nF).

22.2 Turning off ALE (not bonded out)

For applications that require no external memory or temporarily no external memory: the ALE output (pulses at a frequency of $\frac{1}{4} \times f_{OSC}$) can be disabled by setting CHIPCON.3=1 (bit 3 of SFR CHIPCON at SFR address BF hex); if disabled, no ALE pulse will occur. ALE pin will be weakly pulled high internally, switching an external address latch to a quiet state. The MOVX instruction will still toggle ALE (when external Data Memory is accessed).

Additionally during internal access ($\overline{EA}$ = 1) ALE will toggle normally when the address exceeds the internal Program Memory size. During external access ($\overline{EA}$ = 0) ALE will always toggle normally, without regard to if bit 3 of SFR CHIPCON is set or not.

For detailed description of the SFR CHIPCON, please refer to Table 3 and Table 4.

23 IN-APPLICATION PROGRAMMING(IAP)

23.1 IAP programming

The STK6037 has a total of 16384 bytes (16K) of flash memory for user program, but not all user programs completely use up these memory. Un-used flash program memory can be used to stored user data. After power-off, the data remain stored in the flash memory for future use at the next power-on. This function is called I**n-Application Programming (IAP**).

64 bytes of AUX memory, from address 0100 (hex) to 0139 (hex), is used as a *temporary buffer*. Data stored in this buffer can be programmed to the flash memory. Similarily, data stored in the flash program memory can be read back to this buffer. The starting address for the flash memory IAP is a cascade of the content of the SFR IAP_ADRH and SFR IAP_ADRL

The overall concept of IAP is illustrated in Figure 39.

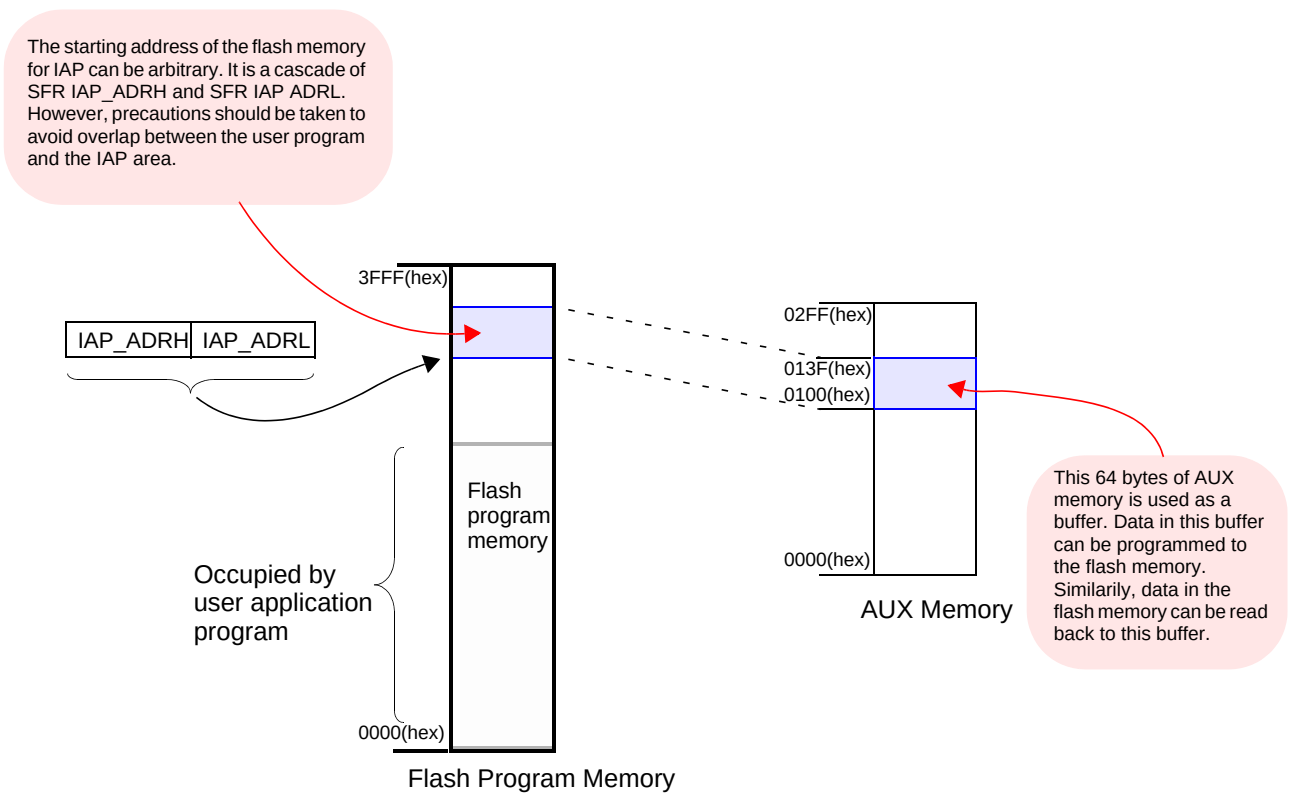


Fig.39 IAP function

23.2 SFRs associated with IAP

Three SFRs are associated with the IAP function. They are:

- SFR IAPEN (E4 hex)
- SFR IAP_ADRL (E5 hex)
- SFR IAP_ADRH (E6 hex)

A description of these 3 SFRs are given in Table 70.

Table 70 SFRs associated with IAP

NEMONICS	DESCRIPTION	ADDRESS	RESET VALUE
IAP_ADRH	High-byte address of the flash memory location for IAP.	E6 (Hex)	0000 0000
IAP_ADRL	Low-byte address of the flash memory location for IAP.	E5 (Hex)	0000 0000
IAPEN	IAP ENable register.	E4 (Hex)	0000 xxxx

23.3 SFR IAPEN

Table 71 IAPEN Register(address E4H)

Bit position	7	6	5	4	3	2	1	0
Mnemonics	IAPEN	APROG	AREAD	AERASE	x	x	x	x
Reset value	0	0	0	0	x	x	x	x

Table 72 Description of SFR IAPEN bits

OPERATION	DESCRIPTION
Erase	If this SFR is programmed with “1001 0000”, 512 bytes of the 16K flash memory is erased, starting from the address pointed to by SFR IAP_ADRL and SFR IAP_ADRH.
Programming	If this SFR is programmed with “1100 0000”, 64 bytes of data stored in the AUX memory buffer is programmed to the 16K flash memory, starting from the address pointed to by SFR IAP_ADRL and SFR IAP_ADRH
Read	If this SFR is programmed with “1010 0000”, 64 bytes of data stored in the flash memory, starting from the address pointed to by SFR IAP_ADRL and SFR IAP_ADRH, is read back to the AUX memory buffer.

23.4 SFR IAP_ADRL and SFR IAP_ADR_H

Table 73 IAP_ADRL Register(address E5H)

Bit position	7	6	5	4	3	2	1	0
Mnemonics	Initial low byte address of flash memory for Erase, Programming, and Read.							
Reset value	0	0	0	0	x	x	x	x

Table 74 IAP_ADRH Register(address E6H)

Bit position	7	6	5	4	3	2	1	0
Mnemonics	Initial hig byte address of flash memory for Erase, Programming, and Read.							
Reset value	0	0	0	0	x	x	x	x

23.5 Programming caution

It is recommended that at least two NOP instructions be added immediately after a write operation to SFR LDSV.

24 INSTRUCTION SET

The STK6037's instruction set is binary-code-compatible with industrial standard 80C51. It consists of:

- 49 single byte,
- 45 two byte, and
- 17 three byte instructions.

A summary of the instruction set is given in Table 76, Table 77, Table 78, Table 79 and Table 80.

24.1 Addressing modes

Most instructions have a destination, source field that specifies the data type, addressing modes and operands involved. For all these instructions, except for MOVs, the destination operand is also the source operand (e.g. ADD A,R7).

There are five kinds of addressing modes:

- Register Addressing
  - R0 to R7 (4 banks)
  - A,B,C (bit), AB (2 bytes), DPTR (double byte)
- Direct Addressing
  - lower 128 bytes of internal main RAM (including the four R0 to R7 register banks)
  - Special Function Registers
  - 128 bits in a subset of the internal main RAM
  - 128 bits in a subset of the Special Function Registers
- Register-Indirect Addressing
  - internal main RAM (@R0, @R1, @SP [PUSH/POP])
  - internal auxiliary RAM (@R0, @R1, @DPTR)
  - external auxiliary RAM (@R0, @R1, @DPTR)
- Immediate Addressing
  - Program Memory (in-code 8 bit or 16 bit constant)
- Base-Register-plus-Index-Register-Indirect Addressing
  - Program Memory look-up table (@DPTR+A, @PC+A).

The first three addressing modes are usable for destination operands.

24.2 80C51 family instruction set

Table 75 Instructions that affect flag settings; note 1

INSTRUCTION	FLAG[2]		
	C	OV	AC
ADD	X	X	X
ADDC	X	X	X
SUBB	X	X	X
MUL	0	X	
DIV	0	X	
DA	X	X	
RRC	X		
RLC	X		
SETB C	1		
CLR C	0		
CPL C	X		
ANL C, bit	X		
ANL C,/bit	X		
ORL C, bit	X		
ORL C,/bit	X		
MOV C, bit	X		
CJNE	X		

Note

1. Note that operations on SFR byte address 208 or bit addresses 209 to 215 (i.e. the PSW or bits in the PSW) will also affect flag settings.
2. X = dont care.

24.3 Instruction set description

For the description of the **Data Addressing Modes** and **Hexadecimal opcode cross-reference** see Table 80.

Table 76 Instruction set description: Arithmetic operations

MNEMONIC		DESCRIPTION	BYTES	CYCLES	OPCODE (HEX)
Arithmetic operations					
ADD	A,Rr	Add register to A	1	1	2*
ADD	A,direct	Add direct byte to A	2	2	25
ADD	A,@Ri	Add indirect RAM to A	1	1	26, 27
ADD	A,#data	Add immediate data to A	2	2	24
ADDC	A,Rr	Add register to A with carry flag	1	1	3*
ADDC	A,direct	Add direct byte to A with carry flag	2	2	35
ADDC	A,@Ri	Add indirect RAM to A with carry flag	1	1	36, 37
ADDC	A,#data	Add immediate data to A with carry flag	2	2	34
SUBB	A,Rr	Subtract register from A with borrow	1	1	9*
SUBB	A,direct	Subtract direct byte from A with borrow	2	2	95
SUBB	A,@Ri	Subtract indirect RAM from A with borrow	1	1	96, 97
SUBB	A,#data	Subtract immediate data from A with borrow	2	2	94
INC	A	Increment A	1	1	04
INC	Rr	Increment register	1	1	0*
INC	direct	Increment direct byte	2	2	05
INC	@Ri	Increment indirect RAM	1	1	06, 07
DEC	A	Decrement A	1	1	14
DEC	Rr	Decrement register	1	1	1*
DEC	direct	Decrement direct byte	2	2	15
DEC	@Ri	Decrement indirect RAM	1	1	16, 17
INC	DPTR	Increment data pointer	1	3	A3
MUL	AB	Multiply A and B	1	5	A4
DIV	AB	Divide A by B	1	5	84
DA	A	Decimal adjust A	1	1	D4

Table 77 Instruction set: Logic operations

MNEMONIC		DESCRIPTION	BYTES	CYCLES	OPCODE (HEX)
Logic operations					
ANL	A,Rr	AND register to A	1	1	5*
ANL	A,direct	AND direct byte to A	2	2	55
ANL	A,@Ri	AND indirect RAM to A	1	1	56, 57
ANL	A,#data	AND immediate data to A	2	2	54
ANL	direct,A	AND A to direct byte	2	2	52
ANL	direct,#data	AND immediate data to direct byte	3	3	53
ORL	A,Rr	OR register to A	1	1	4*
ORL	A,direct	OR direct byte to A	2	2	45
ORL	A,@Ri	OR indirect RAM to A	1	1	46, 47
ORL	A,#data	OR immediate data to A	2	2	44
ORL	direct,A	OR A to direct byte	2	2	42
ORL	direct,#data	OR immediate data to direct byte	3	3	43
XRL	A,Rr	Exclusive-OR register to A	1	1	6*
XRL	A,direct	Exclusive-OR direct byte to A	2	2	65
XRL	A,@Ri	Exclusive-OR indirect RAM to A	1	1	66, 67
XRL	A,#data	Exclusive-OR immediate data to A	2	2	64
XRL	direct,A	Exclusive-OR A to direct byte	2	2	62
XRL	direct,#data	Exclusive-OR immediate data to direct byte	3	2	63
CLR	A	Clear A	1	1	E4
CPL	A	Complement A	1	1	F4
RL	A	Rotate A left	1	1	23
RLC	A	Rotate A left through the carry flag	1	1	33
RR	A	Rotate A right	1	1	03
RRC	A	Rotate A right through the carry flag	1	1	13
SWAP	A	Swap nibbles within A	1	1	C4

Table 78 Instruction set: Data transfer

MNEMONIC		DESCRIPTION	BYTES	CYCLES	OPCODE (HEX)
Data transfer					
MOV	A,Rr	Move register to A	1	1	E*
MOV	A,direct (note 1)	Move direct byte to A	2	2	E5
MOV	A,@Ri	Move indirect RAM to A	1	1	E6, E7
MOV	A,#data	Move immediate data to A	2	2	74
MOV	Rr,A	Move A to register	1	1	F*
MOV	Rr,direct	Move direct byte to register	2	2	A*
MOV	Rr,#data	Move immediate data to register	2	2	7*
MOV	direct,A	Move A to direct byte	2	2	F5
MOV	direct,Rr	Move register to direct byte	2	2	8*
MOV	direct,direct	Move direct byte to direct	3	2	85
MOV	direct,@Ri	Move indirect RAM to direct byte	2	2	86, 87
MOV	direct,#data	Move immediate data to direct byte	3	3	75
MOV	@Ri,A	Move A to indirect RAM	1	1	F6, F7
MOV	@Ri,direct	Move direct byte to indirect RAM	2	2	A6, A7
MOV	@Ri,#data	Move immediate data to indirect RAM	2	2	76, 77
MOV	DPTR,#data 16	Load data pointer with a 16-bit constant	3	3	90
MOVC	A,@A+DPTR	Move code byte relative to DPTR to A	1	3	93
MOVC	A,@A+PC	Move code byte relative to PC to A	1	3	83
MOVX	A,@Ri	Move external RAM (8-bit address) to A	1	2 ~ 9	EB, E3
MOVX	A,@DPTR	Move external RAM (16-bit address) to A	1	2 ~ 9	E0
MOVX	@Ri,A	Move A to external RAM (8-bit address)	1	2 ~ 9	F2, F3
MOVX	@DPTR,A	Move A to external RAM (16-bit address)	1	2 ~ 9	F0
PUSH	direct	Push direct byte onto stack	2	2	C0
POP	direct	Pop direct byte from stack	2	2	D0
XCH	A,Rr	Exchange register with A	1	1	C*
XCH	A,direct	Exchange direct byte with A	2	2	C5
XCH	A,@Ri	Exchange indirect RAM with A	1	1	C6, C7
XCHD	A,@Ri	Exchange LOW-order digit indirect RAM with A	1	1	D6, D7

Note

1. MOV A,ACC is not permitted.

Table 79 Instruction set: Boolean variable manipulation, Program flow control

MNEMONIC		DESCRIPTION	BYTES	CYCLES	OPCODE (HEX)
Boolean variable manipulation					
CLR	C	Clear carry flag	1	1	C3
CLR	bit	Clear direct bit	2	2	C2
SETB	C	Set carry flag	1	1	D3
SETB	bit	Set direct bit	2	2	D2
CPL	C	Complement carry flag	1	1	B3
CPL	bit	Complement direct bit	2	2	B2
ANL	C,bit	AND direct bit to carry flag	2	2	82
ANL	C,/bit	AND complement of direct bit to carry flag	2	2	B0
ORL	C,bit	OR direct bit to carry flag	2	2	72
ORL	C,/bit	OR complement of direct bit to carry flag	2	2	A0
MOV	C,bit	Move direct bit to carry flag	2	2	A2
MOV	bit,C	Move carry flag to direct bit	2	2	92
Branching					
ACALL	addr11	Absolute subroutine call	2	3	•1
LCALL	addr16	Long subroutine call	3	4	12
RET		Return from subroutine	1	4	22
RETI		Return from interrupt	1	4	32
AJMP	addr11	Absolute jump	2	3	♦1
LJMP	addr16	Long jump	3	4	02
SJMP	rel	Short jump (relative address)	2	3	80
JMP	@A+DPTR	Jump indirect relative to the DPTR	1	3	73
JZ	rel	Jump if A is zero	2	3	60
JNZ	rel	Jump if A is not zero	2	3	70
JC	rel	Jump if carry flag is set	2	3	40
JNC	rel	Jump if carry flag is not set	2	3	50
JB	bit,rel	Jump if direct bit is set	3	4	20
JNB	bit,rel	Jump if direct bit is not set	3	4	30
JBC	bit,rel	Jump if direct bit is set and clear bit	3	4	10
CJNE	A,direct,rel	Compare direct to A and jump if not equal	3	4	B5
CJNE	A,#data,rel	Compare immediate to A and jump if not equal	3	4	B4
CJNE	Rr,#data,rel	Compare immediate to register and jump if not equal	3	4	B*
CJNE	@Ri,#data,rel	Compare immediate to indirect and jump if not equal	3	4	B6, B7
DJNZ	Rr,rel	Decrement register and jump if not zero	2	3	D*
DJNZ	direct,rel	Decrement direct and jump if not zero	3	4	D5
NOP		No operation	1	1	00
All mnemonics are copyright © Intel Corporation 1980.					

Table 80 Description of the mnemonics in the Instruction set

MNEMONIC	DESCRIPTION
Data addressing modes	
Rr	Working register R0-R7.
direct	128 internal RAM locations and any special function register (SFR).
@Ri	Indirect internal RAM location addressed by register R0 or R1 of the actual register bank.
#data	8-bit constant included in instruction.
#data 16	16-bit constant included as bytes 2 and 3 of instruction.
bit	Direct addressed bit in internal RAM or SFR.
addr16	16-bit destination address. Used by LCALL and LJMP. The branch will be anywhere within the 64 kbytes Program Memory address space.
addr11	11-bit destination address. Used by ACALL and AJMP. The branch will be within the same 2 kbytes page of Program Memory as the first byte of the following instruction.
rel	Signed (two's complement) 8-bit offset byte. Used by SJMP and all conditional jumps. Range is –128 to +127 bytes relative to first byte of the following instruction.
Hexadecimal opcode cross-reference	
*	8, 9, A, B, C, D, E, F.
•	1, 3, 5, 7, 9, B, D, F.
♦	0, 2, 4, 6, 8, A, C, E.

First hexadecimal character of opcode ← **Second hexadecimal character of opcode** →

↓	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	NOP	AJMP addr11	LJMP addr16	RR A	INC A	INC direct	INC @Ri 0	INC @Ri 1	INC Rr 0	INC Rr 1	INC Rr 2	INC Rr 3	INC Rr 4	INC Rr 5	INC Rr 6	INC Rr 7
1	JBC bit,rel	ACALL addr11	LCALL addr16	RRC A	DEC A	DEC direct	DEC @Ri 0	DEC @Ri 1	DEC Rr 0	DEC Rr 1	DEC Rr 2	DEC Rr 3	DEC Rr 4	DEC Rr 5	DEC Rr 6	DEC Rr 7
2	JB bit,rel	AJMP addr11	RET	RL A	ADD A,#data	ADD A,direct	ADD A,@Ri 0	ADD A,@Ri 1	ADD A,Rr 0	ADD A,Rr 1	ADD A,Rr 2	ADD A,Rr 3	ADD A,Rr 4	ADD A,Rr 5	ADD A,Rr 6	ADD A,Rr 7
3	JNB bit,rel	ACALL addr11	RETI	RLC A	ADDC A,#data	ADDC A,direct	ADDC A,@Ri 0	ADDC A,@Ri 1	ADDC A,Rr 0	ADDC A,Rr 1	ADDC A,Rr 2	ADDC A,Rr 3	ADDC A,Rr 4	ADDC A,Rr 5	ADDC A,Rr 6	ADDC A,Rr 7
4	JC rel	AJMP addr11	ORL direct,A	ORL direct,#data	ORL A,#data	ORL A,direct	ORL A,@Ri 0	ORL A,@Ri 1	ORL A,Rr 0	ORL A,Rr 1	ORL A,Rr 2	ORL A,Rr 3	ORL A,Rr 4	ORL A,Rr 5	ORL A,Rr 6	ORL A,Rr 7
5	JNC rel	ACALL addr11	ANL direct,A	ANL direct,#data	ANL A,#data	ANL A,direct	ANL A,@Ri 0	ANL A,@Ri 1	ANL A,Rr 0	ANL A,Rr 1	ANL A,Rr 2	ANL A,Rr 3	ANL A,Rr 4	ANL A,Rr 5	ANL A,Rr 6	ANL A,Rr 7
6	JZ rel	AJMP addr11	XRL direct,A	XRL direct,#data	XRL A,#data	XRL A,direct	XRL A,@Ri 0	XRL A,@Ri 1	XRL A,Rr 0	XRL A,Rr 1	XRL A,Rr 2	XRL A,Rr 3	XRL A,Rr 4	XRL A,Rr 5	XRL A,Rr 6	XRL A,Rr 7
7	JNZ rel	ACALL addr11	ORL C,bit	JMP @A+DPTR	MOV A,#data	MOV direct,#data	MOV @Ri,#data 0	MOV @Ri,#data 1	MOV Rr,#data 0	MOV Rr,#data 1	MOV Rr,#data 2	MOV Rr,#data 3	MOV Rr,#data 4	MOV Rr,#data 5	MOV Rr,#data 6	MOV Rr,#data 7
8	SJMP rel	AJMP addr11	ANL C,bit	MOVC A,@A+PC	DIV AB	MOV direct,direct	MOV direct,@Ri 0	MOV direct,@Ri 1	MOV direct,Rr 0	MOV direct,Rr 1	MOV direct,Rr 2	MOV direct,Rr 3	MOV direct,Rr 4	MOV direct,Rr 5	MOV direct,Rr 6	MOV direct,Rr 7
9	MOV DTPR,#data16	ACALL addr11	MOV bit,C	MOVC A,@A+DPTR	SUBB A,#data	SUBB A,direct	SUBB A,@Ri 0	SUBB A,@Ri 1	SUB A,Rr 0	SUB A,Rr 1	SUB A,Rr 2	SUB A,Rr 3	SUB A,Rr 4	SUB A,Rr 5	SUB A,Rr 6	SUB A,Rr 7
A	ORL C,/bit	AJMP addr11	MOV bit,C	INC DPTR	MUL AB		MOV @Ri,direct 0	MOV @Ri,direct 1	MOV Rr,direct 0	MOV Rr,direct 1	MOV Rr,direct 2	MOV Rr,direct 3	MOV Rr,direct 4	MOV Rr,direct 5	MOV Rr,direct 6	MOV Rr,direct 7
B	ANL C,/bit	ACALL addr11	CPL bit	CPL C	CJNE A,#data,rel	CJNE A,direct,rel	CJNE @Ri,#data,rel 0	CJNE @Ri,#data,rel 1	CJNE Rr,#data,rel 0	CJNE Rr,#data,rel 1	CJNE Rr,#data,rel 2	CJNE Rr,#data,rel 3	CJNE Rr,#data,rel 4	CJNE Rr,#data,rel 5	CJNE Rr,#data,rel 6	CJNE Rr,#data,rel 7
C	PUSH direct	AJMP addr11	CLR bit	CLR C	SWAP A	XCH A,direct	XCH A,@Ri 0	XCH A,@Ri 1	XCH A,Rr 0	XCH A,Rr 1	XCH A,Rr 2	XCH A,Rr 3	XCH A,Rr 4	XCH A,Rr 5	XCH A,Rr 6	XCH A,Rr 7
D	POP direct	ACALL addr11	SETB bit	SETB C	DA A	DJNZ direct,rel	XCHD A,@Ri 0	XCHD A,@Ri 1	DJNZ Rr,rel 0	DJNZ Rr,rel 1	DJNZ Rr,rel 2	DJNZ Rr,rel 3	DJNZ Rr,rel 4	DJNZ Rr,rel 5	DJNZ Rr,rel 6	DJNZ Rr,rel 7

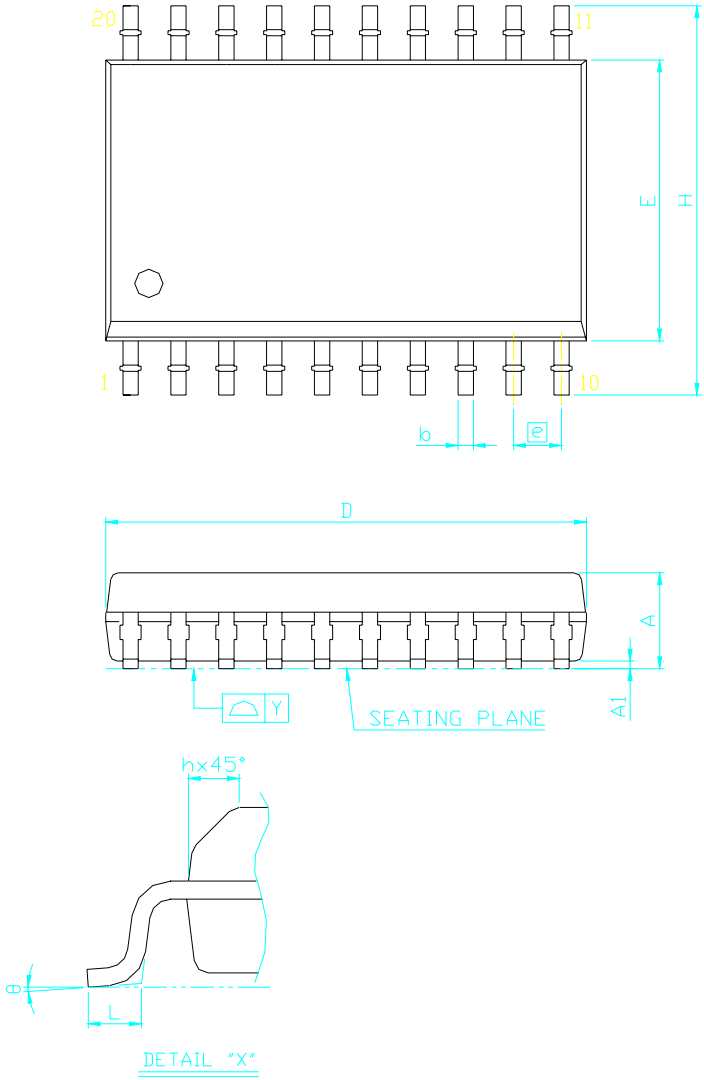
First hexadecimal character of opcode ← **Second hexadecimal character of opcode** →

↓	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
E	MOVX A,@DTPR	AJMP addr11	MOVX A,@Ri 0	MOVX A,@Ri 1	CLR A	MOV A,direct (1)	MOV A,@Ri 0	MOV A,@Ri 1	MOV A,Rr 0	MOV A,Rr 1	MOV A,Rr 2	MOV A,Rr 3	MOV A,Rr 4	MOV A,Rr 5	MOV A,Rr 6	MOV A,Rr 7
F	MOVX @DTPR,A	ACALL addr11	MOVX @Ri,A 0	MOVX @Ri,A 1	CPL A	MOV direct,A	MOV @Ri,A 0	MOV @Ri,A 1	MOV Rr,A 0	MOV Rr,A 1	MOV Rr,A 2	MOV Rr,A 3	MOV Rr,A 4	MOV Rr,A 5	MOV Rr,A 6	MOV Rr,A 7

Note

1. MOV A, ACC is not a valid instruction.

25 SOP20 PACKAGE OUTLINE DWRAWING



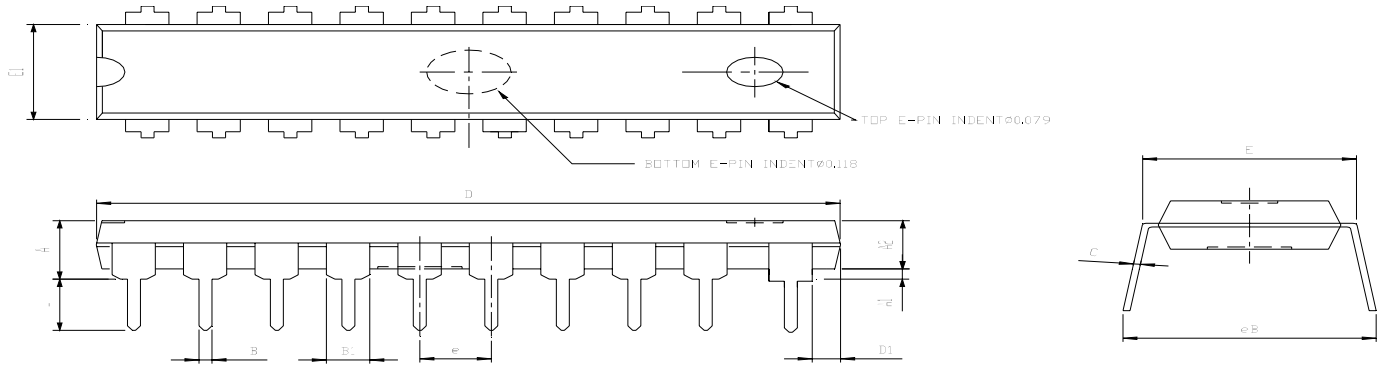
SYMBOL	DIMENSION (MM)			DIMENSION (MIL)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	2,36	2,54	2,64	93	100	104
A1	0,10	0,20	0,30	4	8	12
b	0,35	0,406	0,48	14	16	19
c	0,23	0,254	0,31	9	10	12
D	12,60	12,80	13,00	496	504	512
E	7,40	7,50	7,60	291	295	299
e		1,27 BSC			50 BSC	
H	10,00	10,31	10,65	394	406	419
h	0,25	0,66	0,75	10	26	30
L	0,51	0,76	1,02	20	30	40
Y			0,075			3
θ	0°		8°	0°		8°

NOTES:

1. REFER TO JEDEC STD. MS-013 AC.
2. DIMENSION "D" DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED 0,15mm (6mil) PER SIDE.
3. DIMENSION "E" DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTER-LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED 0,25mm (10mil) PER SIDE.
4. CONTROLLING DIMENSION: MILLIMETER

Fig.40 STK6037 SOP20 Package Outline Drawing

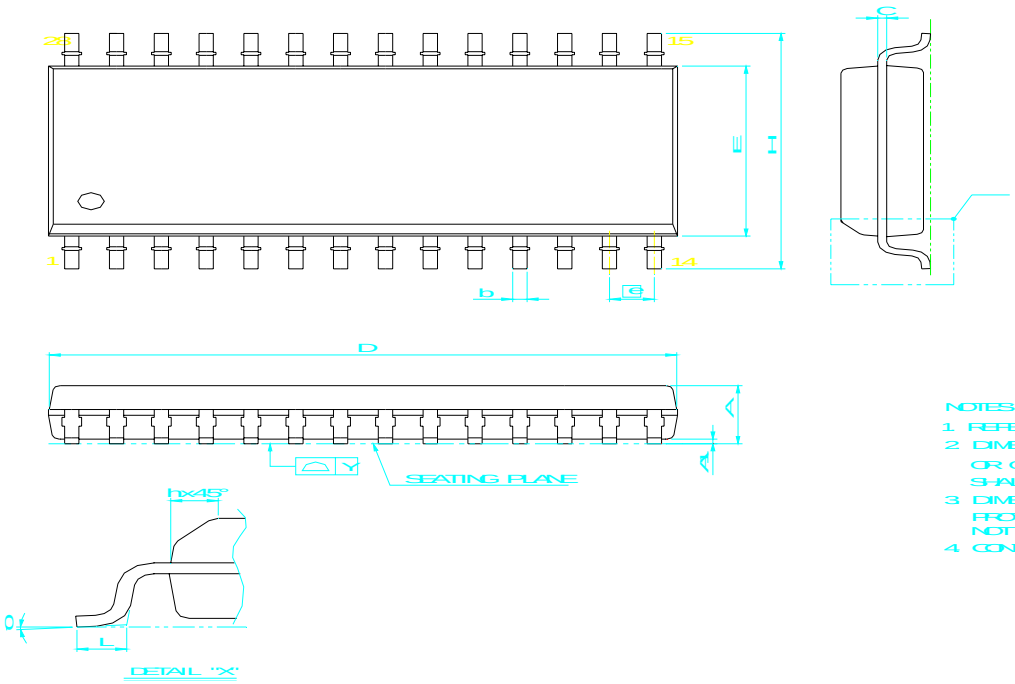
26 DIP20 PACKAGE OUTLINE DWRAWING



SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	—	—	4.57	—	—	0.180
A1	0.38	—	—	0.015	—	—
A2	—	3.30	3.56	—	0.130	0.140
B	0.36	0.46	0.56	0.014	0.018	0.022
B1	1.27	1.52	1.78	0.050	0.060	0.070
C	0.20	0.25	0.33	0.008	0.010	0.013
D	26.00	26.25	26.50	1.024	1.033	1.04
D1	0.70	0.83	0.96	0.028	0.033	0.038
E	7.62	—	8.26	0.300	—	0.325
E1	6.26	6.36	6.46	0.252	0.256	0.262
e	—	2.54	—	—	0.100	—
L	3.18	—	—	0.125	—	—
eB	8.6	—	9.4	0.339	—	0.37

Fig.41 DIP20 package outline drawing

27 SOP28 PACKAGE OUTLINE DWRAWING

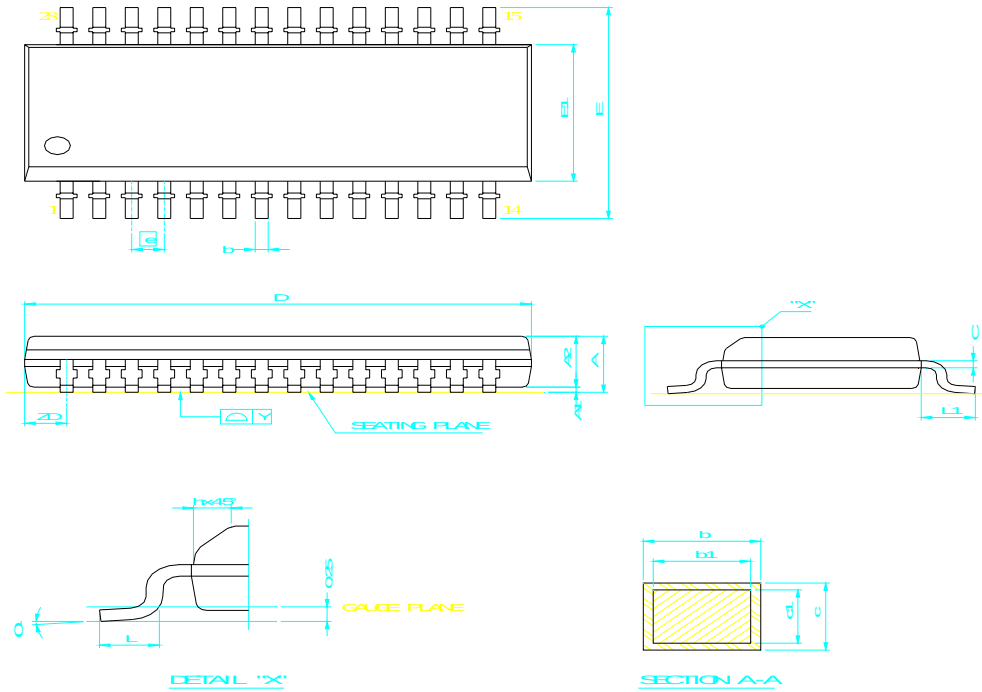


SYMBOL	DIMENSION (MM)			DIMENSION (MIL)		
	MIN	NOM	MAX	MIN	NOM	MAX
A	2,36	2,54	2,64	93	100	104
A1	0,10	0,20	0,30	4	8	12
b	0,35	0,406	0,48	14	16	19
c	0,23	0,254	0,31	9	10	12
D	17,70	17,83	18,10	697	702	713
E	7,40	7,50	7,60	291	295	299
e	1,27 BSC			50 BSC		
H	10,00	10,31	10,65	394	406	419
h	0,25	0,66	0,75	10	26	30
L	0,51	0,76	1,02	20	30	40
Y			0,075			3
θ	0°		8°	0°		8°

NOTES
1 REFER TO JEDEC STD MS-013 AE
2 DIMENSION "D" DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED 0,15mm (6mil) PER SIDE.
3 DIMENSION "E" DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTER-LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED 0,25mm (10mil) PER SIDE.
4 CONTROLLING DIMENSION: MILLIMETER

Fig.42 STK6037 SOP28 Package Outline Drawing

28 SSOP28 PACKAGE OUTLINE DWRAWING

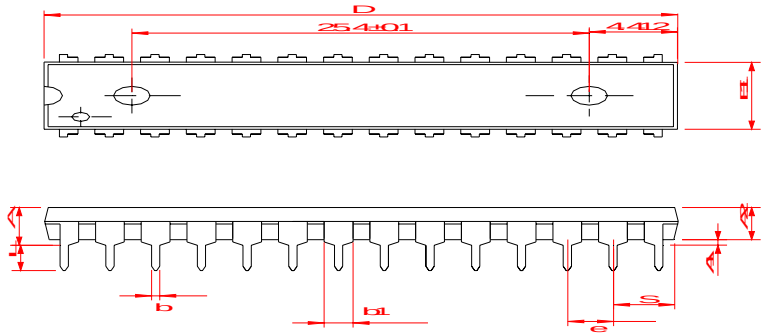


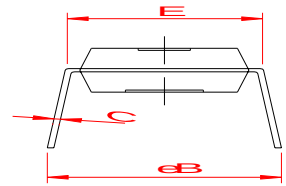
SYMBOL	DIMENSION (MM)			DIMENSION (MIL)		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.35	1.60	1.75	53	63	69
A1	0.10	0.15	0.25	4	6	10
A2			1.50			59
b	0.20		0.30	8		12
b1	0.20	0.254	0.28	8	10	11
c	0.18		0.25	7		10
c1	0.18	0.203	0.23	7	8	9
D	9.80	9.90	10.00	386	390	394
E	5.80	6.00	6.20	228	236	244
E1	3.80	3.90	4.00	150	154	157
e	0.635 BSC			25 BSC		
h	0.25	0.42	0.50	10	17	20
L	0.40	0.635	1.27	16	25	50
L1	1.00	1.05	1.10	39	41	43
ZD	0.823 REF			32.5 REF		
Y			0.10			4
θ	0°		8°	0°		8°

NOTE:
1. REFER TO JEDEC STD MO-137 AD
2. DIMENSION "D" DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED 0.15mm (6 MIL) PER SIDE. PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED 0.15mm (6 MIL) PER SIDE
3. DIMENSION "E1" DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTER-LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED 0.25mm (10mil) PER SIDE
4. CONTROLLING DIMENSION: MILLIMETER

Fig.43 STK6037 SSOP28 Package Outline Drawing

29 SKINNY28 PACKAGE OUTLINE DWRAWING





SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	3.67	3.69	3.70	0.144	0.145	0.146
A1	0.33	0.39	0.46	0.013	0.015	0.018
A2	3.27	3.30	3.31	0.129	0.130	0.131
b	-	0.46	-	-	0.018	-
b1	1.52	1.55	1.61	0.060	0.061	0.063
C	0.24	-	0.26	0.009	-	0.01
D	34.96	35.18	35.30	1.376	1.385	1.389
S	3.34	3.38	3.40	0.131	0.133	0.134
E	8.12	8.13	8.15	0.319	0.320	0.321
E1	7.32	7.38	7.40	0.288	0.290	0.291
e	-	2.54	-	-	0.1	-
L	-	3.23	3.25	-	0.127	0.128
eB	8.4	8.9	9.4	0.330	0.350	0.370

Fig.44 SKINNY 28 package outline drawing