SMDK2450 Evaluation Board for S3C2450X

1. PCB Revision

Revision	Date	Description
Rev 0.0	2007. 11. 22	Preliminary Version
Rev 0.1	2008. 2. 21	Modified in Cam/LCD(ref Red Circle/Rectangle)
Rev 0.2	2008. 4. 07	Modified in CLK/Buffers/USB/PMIC/LCD/Audio/Connectors/ETC.(ref Red/Blue Circle/Rectangle)
	2008. 5. 14	Modified in B0D. UART/IrDA(ref Red Circle)
	2008. 5. 29	Modified in C05. Memory(OneNand)/JTAG/CLK(ref Green Rectangle)
	2008. 6. 30	Modified in C06. Buffers(SROM IF), C0A. B2B Connector(CPU) (ref Red Circle)
	2008. 7. 02	Modified in C08. CPU B'D Power(ARM, INT) (ref Red Circle)

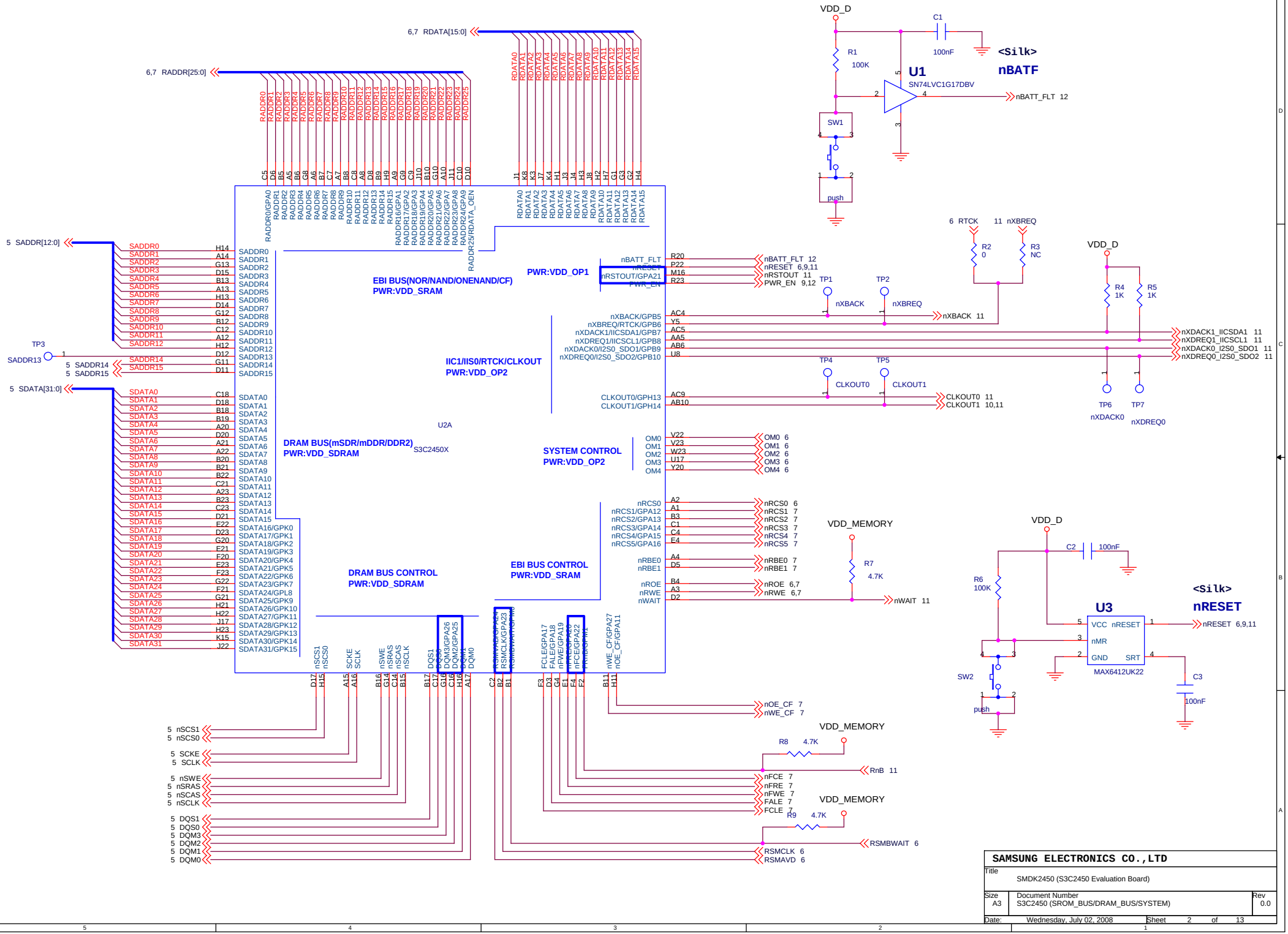
2. Table of Contents

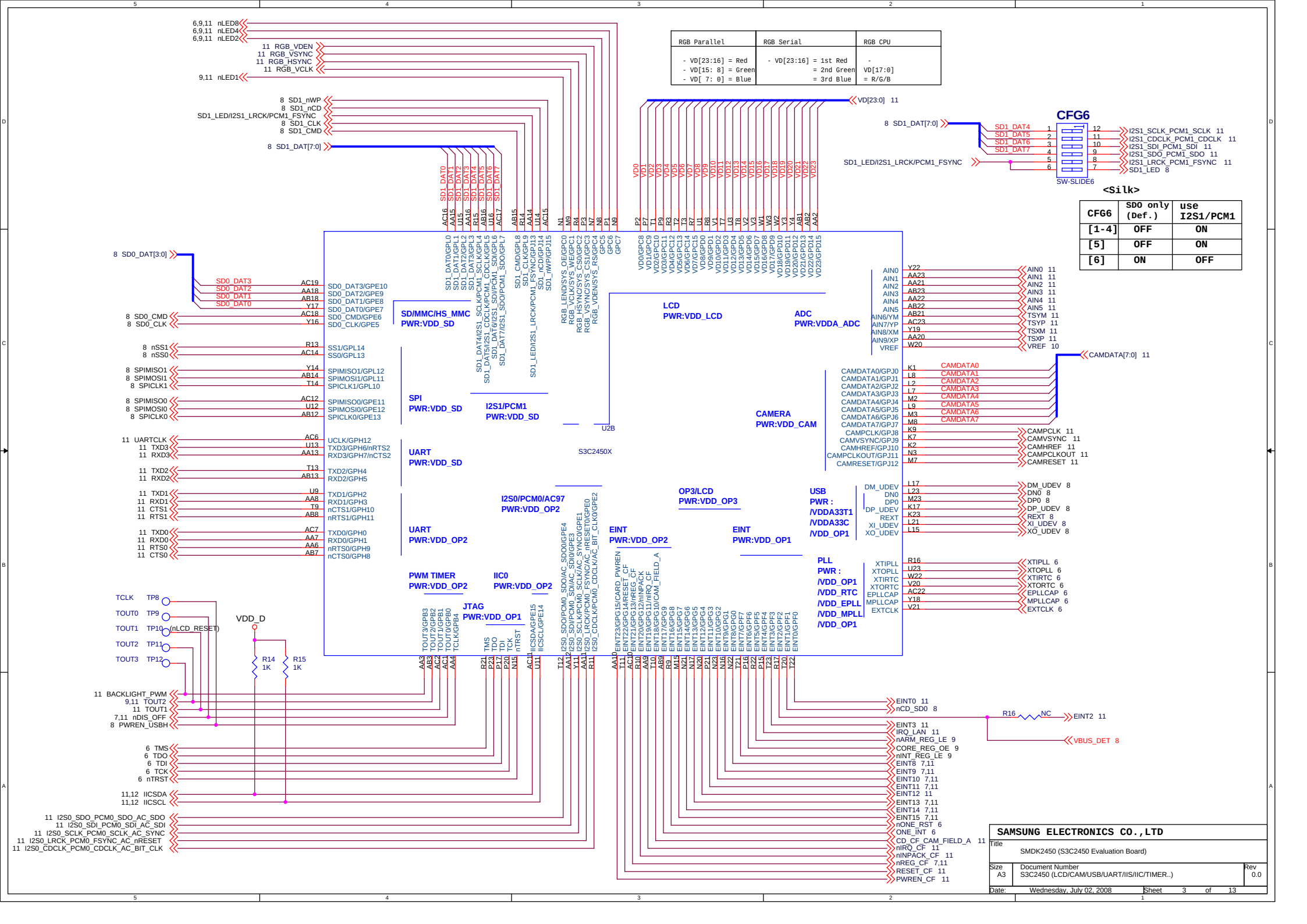
3. Part Reference

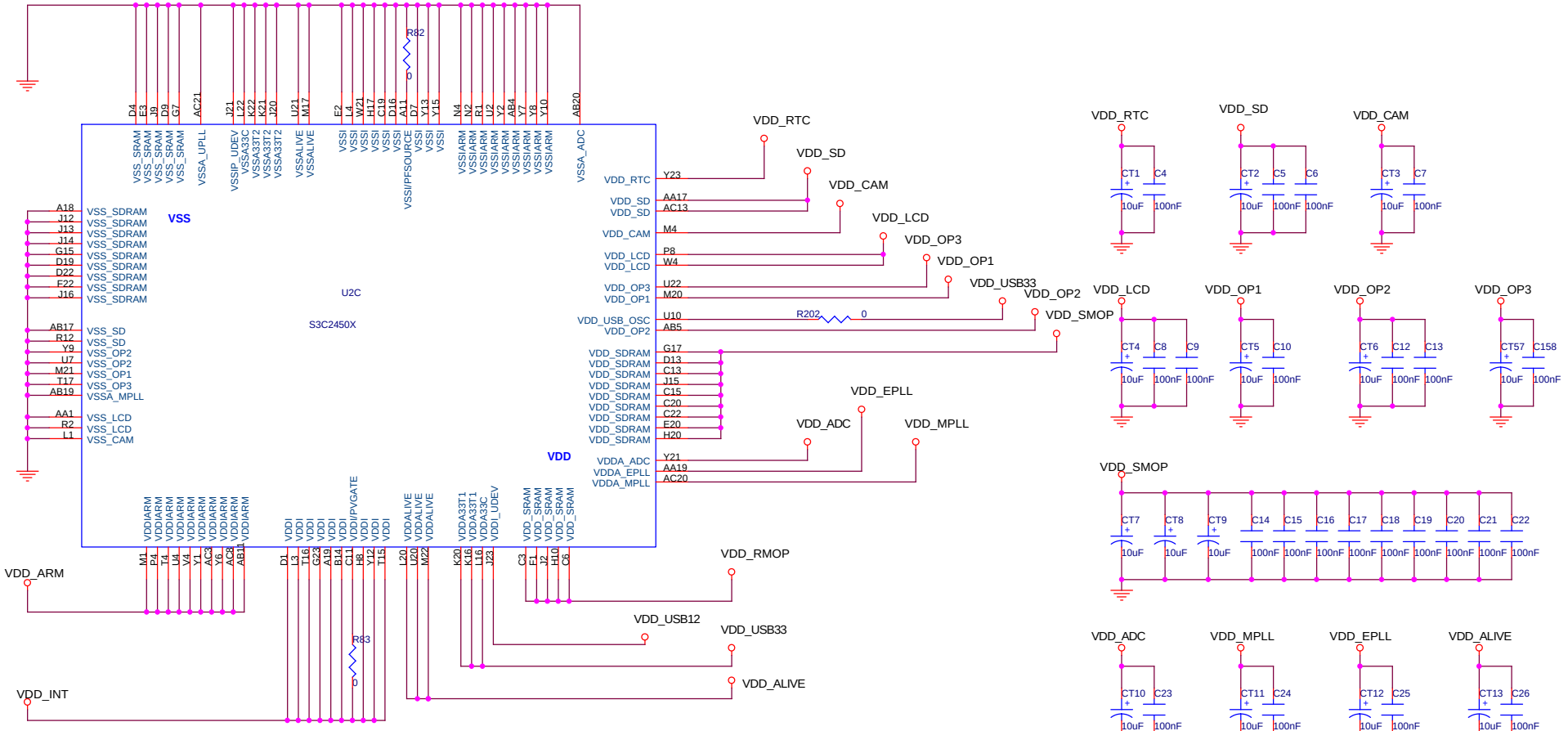
<Component><Number>

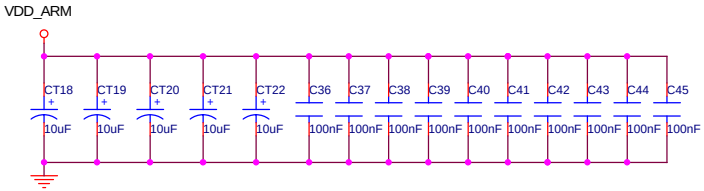
- U - COMPONENT IC & REGURATOR IC
- C - CAPACITOR
- CT- TANTAL CAPACITOR
- R - RESISTER
- RP - RESISTOR PACK
- VR - VARIABLE RESISTER
- J - JUMPER
- L - INDUCTOR
- F - FERRITE BEAD
- Y - OSCILLATOR
- X - CRYSTAL
- Q - TRANSISTOR/FET
- D - DIODE
- SW - TACT/PUSH SWITCH
- CON - CONNECTOR
- CFG - DIP SWITCH

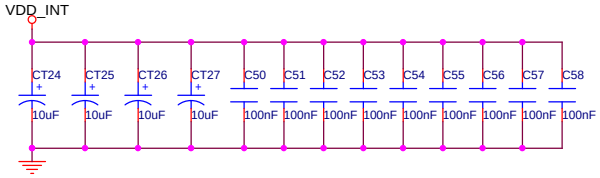
SAMSUNG ELECTRONICS CO.,LTD		
Title: SMDK2450 (S3C2450 Evaluation Board)		
Size: A3	Document Number: TITLE BLOCK	Rev: 0.1
Date: Wednesday, July 02, 2008	Sheet 1 of 13	

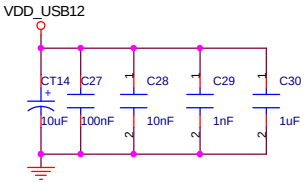

6,7 RDATA[15:0]
6,7 RADDR[25:0]
5 SADDR[12:0]
5 SDATA[31:0]
SADDR13
5 SADDR14
5 SADDR15
TP3
EBI BUS(NOR/NAND/ONENAND/CF)
PWR:VDD_SRAM
PWR:VDD_OP1
IIC1/IIS0/RTCK/CLKOUT
PWR:VDD_OP2
U2A
S3C2450X
DRAM BUS(mSDR/mDDR/DDR2)
PWR:VDD_SDRAM
SYSTEM CONTROL
PWR:VDD_OP2
DRAM BUS CONTROL
PWR:VDD_SDRAM
EBI BUS CONTROL
PWR:VDD_SRAM
VDD_D
R1
100K
C1
100nF
SW1
push
U1
SN74LVC1G17DBV
<Silk>
nBATF
nBATT_FLT 12
6 RTCK
11 nXBREQ
R2
0
R3
NC
TP1
TP2
nXBACK
nXBREQ
nXBACK 11
R4
1K
R5
1K
nXDACK1_IICSDA1 11
nXDREQ1_IICSCL1 11
nXDACK0_I2S0_SDO1 11
nXDREQ0_I2S0_SDO2 11
TP4
TP5
CLKOUT0
CLKOUT1
CLKOUT0 11
CLKOUT1 10,11
TP6
TP7
nXDACK0
nXDREQ0
nBATT_FLT 12
nRESET 6,9,11
nRSTOUT 11
PWR_EN 9,12
OM0 6
OM1 6
OM2 6
OM3 6
OM4 6
nRCS0 6
nRCS1 7
nRCS2 7
nRCS3 7
nRCS4 7
nRCS5 7
nRBE0 7
nRBE1 7
nROE 6,7
nRWE 6,7
nWAIT 11
VDD_MEMORY
R7
4.7K
VDD_D
C2
100nF
R6
100K
U3
MAX6412UK22
VCC
nRESET
nMR
GND
SRT
<Silk>
nRESET
nRESET 6,9,11
SW2
push
C3
100nF
nOE_CF 7
nWE_CF 7
VDD_MEMORY
R8
4.7K
RnB 11
nFCE 7
nFRE 7
nFWE 7
FALE 7
FCLE 7
VDD_MEMORY
R9
4.7K
RSMBWAIT 6
RSMCLK 6
RSMAVD 6
5 nSCS1
5 nSCS0
5 SCKE
5 SCLK
5 nSWE
5 nSRAS
5 nSCAS
5 nSCLK
5 DQS1
5 DQS0
5 DQM3
5 DQM2
5 DQM1
5 DQM0
SAMSUNG ELECTRONICS CO.,LTD
Title
SMDK2450 (S3C2450 Evaluation Board)
Size
A3
Document Number
S3C2450 (SROM_BUS/DRAM_BUS/SYSTEM)
Rev
0.0
Date:
Wednesday, July 02, 2008
Sheet
2
of
13

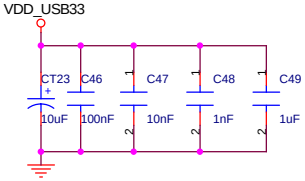

RGB Parallel
- VD[23:16] = Red
- VD[15: 8] = Green
- VD[7: 0] = Blue
RGB Serial
- VD[23:16] = 1st Red
= 2nd Green
= 3rd Blue
RGB CPU
- VD[17:0] = R/G/B
CFG6
SW-SLIDE6
<Silk>
CFG6 | SD0 only (Def.) | use I2S1/PCM1
[1-4] | OFF | ON
[5] | OFF | ON
[6] | ON | OFF
S3C2450X
U2B
SD/MMC/HS_MMC PWR:VDD_SD
SPI PWR:VDD_SD
I2S1/PCM1 PWR:VDD_SD
UART PWR:VDD_SD
I2S0/PCM0/AC97 PWR:VDD_OP2
UART PWR:VDD_OP2
PWM TIMER PWR:VDD_OP2
IIC0 PWR:VDD_OP2
JTAG PWR:VDD_OP1
LCD PWR:VDD_LCD
ADC PWR:VDDA_ADC
CAMERA PWR:VDD_CAM
OP3/LCD PWR:VDD_OP3
USB PWR : /VDDA33T1 /VDDA33C /VDD_OP1
EINT PWR:VDD_OP2
EINT PWR:VDD_OP1
PLL PWR : /VDD_OP1 /VDD_RTC /VDD_EPLL /VDD_MPLL /VDD_OP1
SAMSUNG ELECTRONICS CO.,LTD
Title SMDK2450 (S3C2450 Evaluation Board)
Size A3
Document Number S3C2450 (LCD/CAM/USB/UART/IIS/IIC/TIMER..)
Rev 0.0
Date: Wednesday, July 02, 2008
Sheet 3 of 13

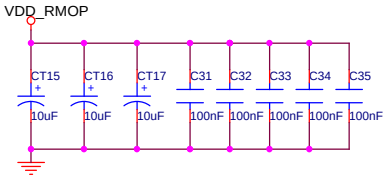




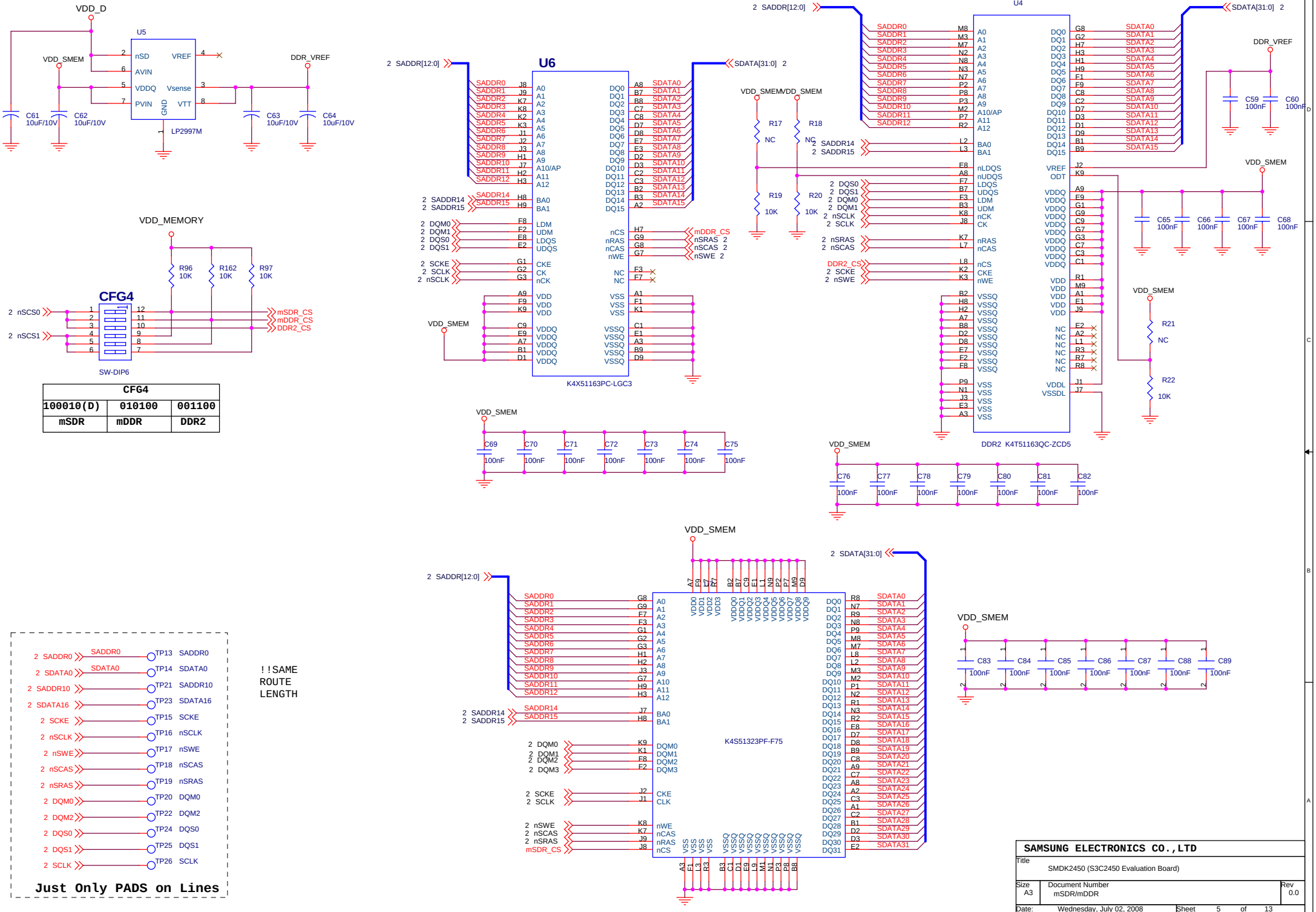


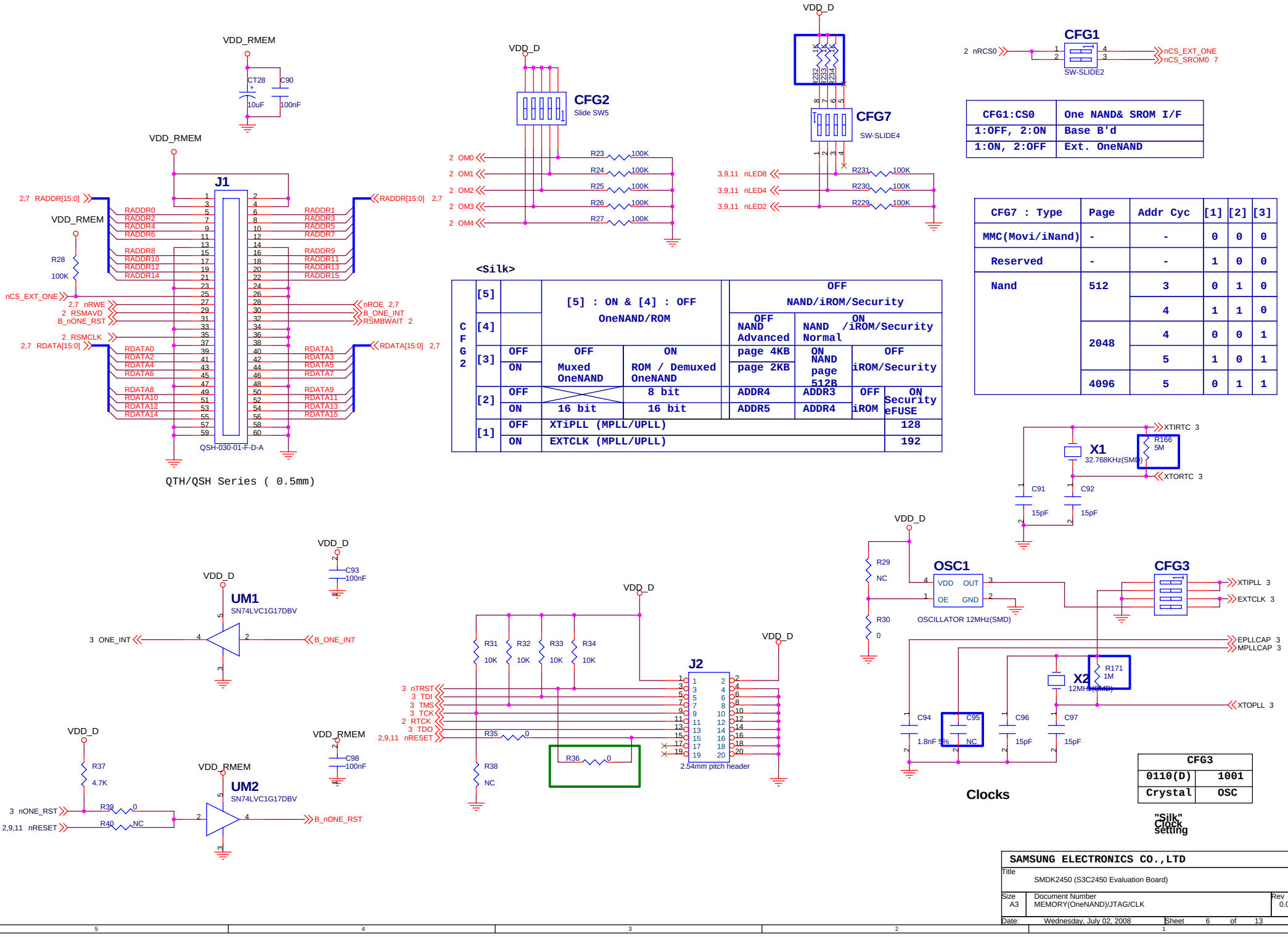






SAMSUNG ELECTRONICS CO.,LTD		
Title: SMDK2450 (S3C2450 Evaluation Board)		
Size: A3	Document Number: S3C2450 (POWER)	Rev: 0.0
Date: Wednesday, July 02, 2008	Sheet 4 of 13	


VDD_D
U5
VDD_SMEM
DDR_VREF
nSD
AVIN
VDDQ
PVIN
VREF
Vsense
VTT
GND
LP2997M
C61 10uF/10V
C62 10uF/10V
C63 10uF/10V
C64 10uF/10V
VDD_MEMORY
R96 10K
R162 10K
R97 10K
CFG4
2 nSCS0
2 nSCS1
mSDR_CS
mDDR_CS
DDR2_CS
SW-DIP6
CFG4
100010(D) 010100 001100
mSDR mDDR DDR2
U6
2 SADDR[12:0]
SDATA[31:0] 2
SADDR0 SADDR1 SADDR2 SADDR3 SADDR4 SADDR5 SADDR6 SADDR7 SADDR8 SADDR9 SADDR10 SADDR11 SADDR12
SADDR14 SADDR15
2 DQM0 2 DQM1 2 DQS0 2 DQS1
2 SCKE 2 SCLK 2 nSCLK
nCS nRAS nCAS nWE
mDDR_CS nSRAS 2 nSCAS 2 nSWE 2
VDD VDD VDD
VDDQ VDDQ VDDQ VDDQ VDDQ
VSS VSS VSS
VSSQ VSSQ VSSQ VSSQ VSSQ
K4X51163PC-LGC3
VDD_SMEM
C69 C70 C71 C72 C73 C74 C75 100nF
U4
SADDR0 SADDR1 SADDR2 SADDR3 SADDR4 SADDR5 SADDR6 SADDR7 SADDR8 SADDR9 SADDR10 SADDR11 SADDR12
2 SADDR14 2 SADDR15
2 DQS0 2 DQS1 2 DQM0 2 DQM1 2 nSCLK 2 SCLK
2 nSRAS 2 nSCAS
DDR2_CS 2 SCKE 2 nSWE
DQ0 DQ1 DQ2 DQ3 DQ4 DQ5 DQ6 DQ7 DQ8 DQ9 DQ10 DQ11 DQ12 DQ13 DQ14 DQ15
A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10/AP A11 A12
BA0 BA1
nLDQS nUDQS LDQS UDQS LDM UDM nCK CK
nRAS nCAS
nCS CKE nWE
VSSQ VSS
VDDQ VDD
VREF ODT
VDDL VSSDL
DDR2 K4T51163QC-ZCD5
VDD_SMEM/VDD_SMEM
R17 NC
R18 NC
R19 10K
R20 10K
DDR_VREF
C59 100nF
C60 100nF
VDD_SMEM
C65 C66 C67 C68 100nF
R21 NC
R22 10K
C76 C77 C78 C79 C80 C81 C82 100nF
VDD_SMEM
2 SADDR[12:0]
2 SDATA[31:0]
SADDR0 SADDR1 SADDR2 SADDR3 SADDR4 SADDR5 SADDR6 SADDR7 SADDR8 SADDR9 SADDR10 SADDR11 SADDR12
2 SADDR14 2 SADDR15
2 DQM0 2 DQM1 2 DQM2 2 DQM3
2 SCKE 2 SCLK
2 nSWE 2 nSCAS 2 nSRAS mSDR_CS
A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 A11 A12
BA0 BA1
DQM0 DQM1 DQM2 DQM3
CKE CLK
nWE nCAS nRAS nCS
DQ0 DQ1 DQ2 DQ3 DQ4 DQ5 DQ6 DQ7 DQ8 DQ9 DQ10 DQ11 DQ12 DQ13 DQ14 DQ15 DQ16 DQ17 DQ18 DQ19 DQ20 DQ21 DQ22 DQ23 DQ24 DQ25 DQ26 DQ27 DQ28 DQ29 DQ30 DQ31
K4S51323PF-F75
VDD_SMEM
C83 C84 C85 C86 C87 C88 C89 100nF
2 SADDR[12:0]
SADDR0 SADDR0
SDATA0 SDATA0
SADDR10 SADDR10
SDATA16 SDATA16
SCKE SCKE
nSCLK nSCLK
nSWE nSWE
nSCAS nSCAS
nSRAS nSRAS
DQM0 DQM0
DQM2 DQM2
DQS0 DQS0
DQS1 DQS1
SCLK SCLK
TP13 TP14 TP21 TP23 TP15 TP16 TP17 TP18 TP19 TP20 TP22 TP24 TP25 TP26
Just Only PADS on Lines
!!SAME ROUTE LENGTH
SAMSUNG ELECTRONICS CO.,LTD
Title
SMDK2450 (S3C2450 Evaluation Board)
Size A3
Document Number mSDR/mDDR
Rev 0.0
Date: Wednesday, July 02, 2008
Sheet 5 of 13



CFG1:CS0	One NAND& SROM I/F
1:OFF, 2:ON	Base B'd
1:ON, 2:OFF	Ext. OneNAND

CFG7 : Type	Page	Addr Cyc	[1]	[2]	[3]
MMC(Movi/iNand)	-	-	0	0	0
Reserved	-	-	1	0	0
Nand	512	3	0	1	0
		4	1	1	0
	2048	4	0	0	1
		5	1	0	1
	4096	5	0	1	1

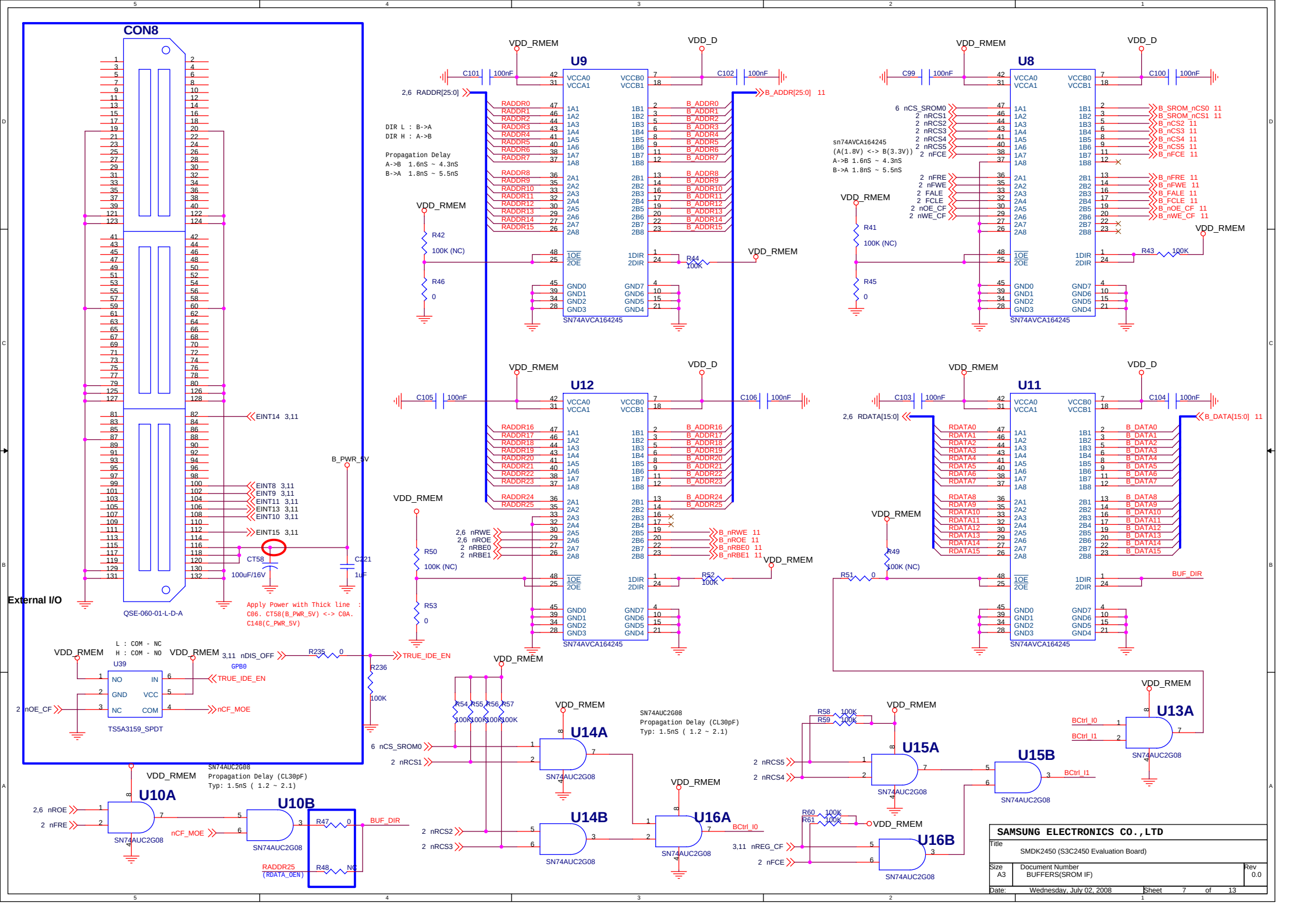
CFG2							
[5]		[5] : ON & [4] : OFF OneNAND/ROM		OFF NAND/iROM/Security			
[4]				OFF NAND Advanced	ON NAND /iROM/Security Normal		
[3]	OFF	OFF Muxed OneNAND	ON ROM / Demuxed OneNAND	page 4KB	ON NAND page 512B	OFF iROM/Security	
	ON			page 2KB			
[2]	OFF		8 bit	ADDR4	ADDR3	OFF iROM	ON Security eFUSE
	ON	16 bit	16 bit	ADDR5	ADDR4		
[1]	OFF	XTiPLL (MPLL/UPLL)					128
	ON	EXTCLK (MPLL/UPLL)					192

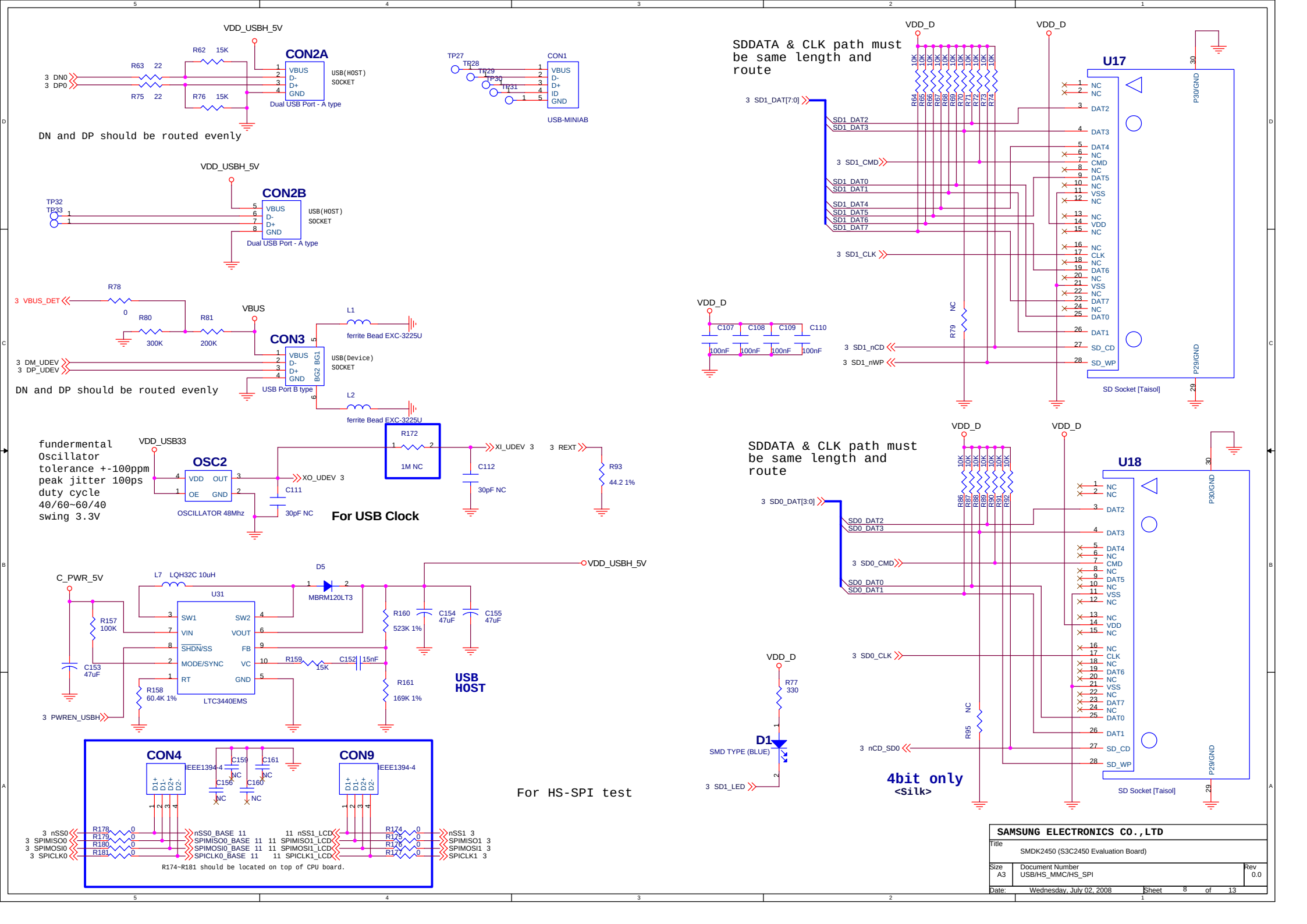
CFG3	
0110(D)	1001
Crystal	OSC

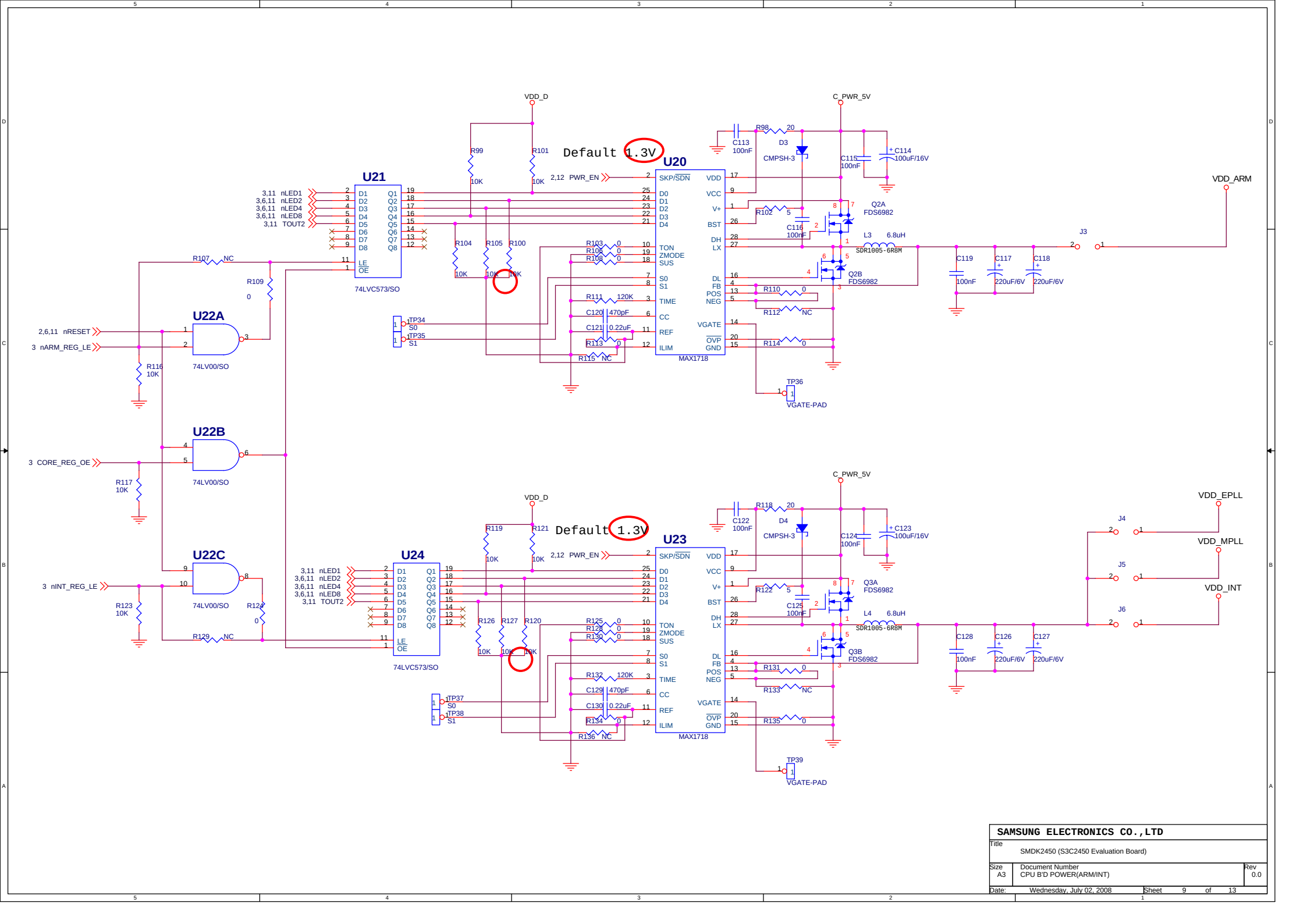
Clocks

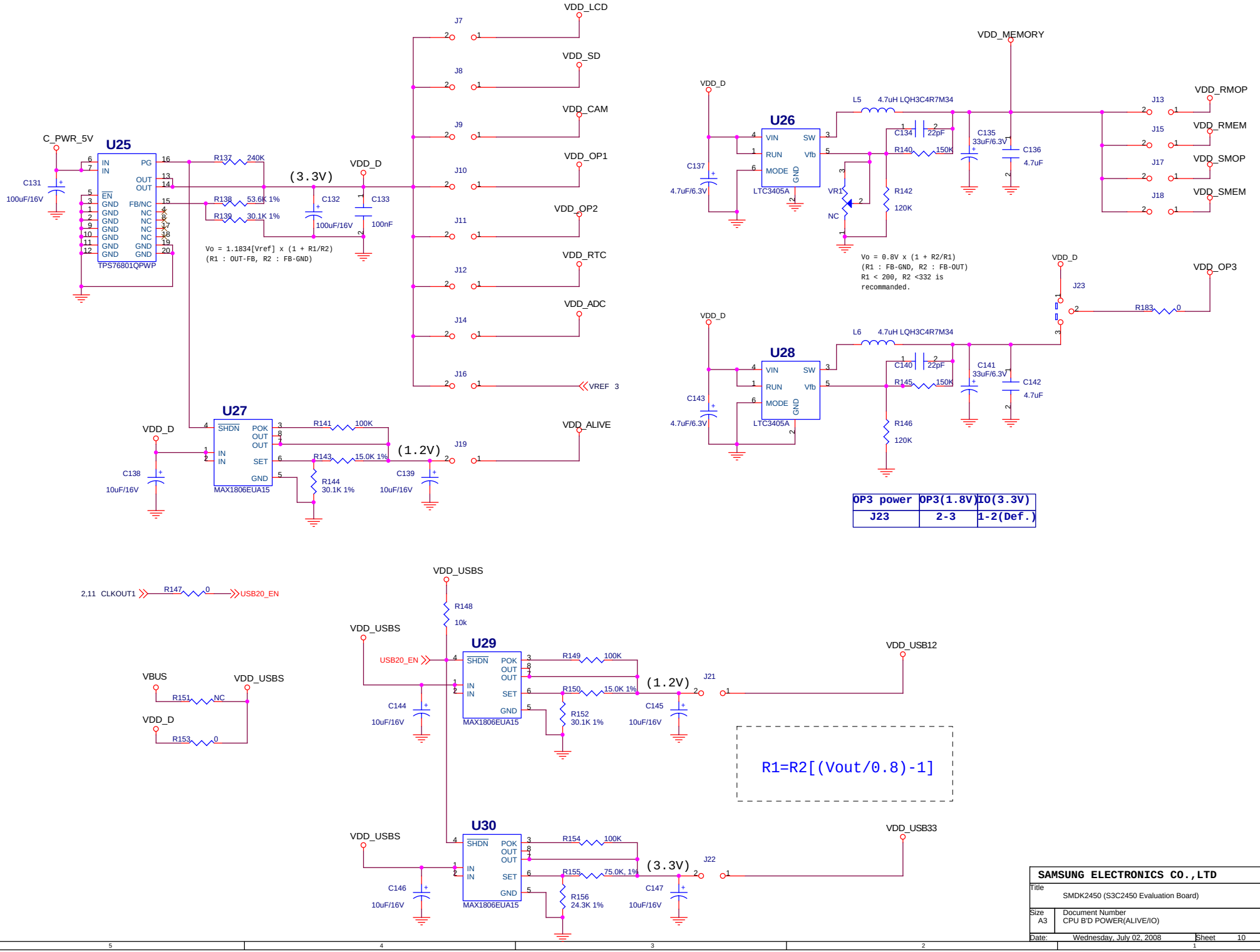
"Silk" Clock Setting

SAMSUNG ELECTRONICS CO.,LTD		
Title: SMDK2450 (S3C2450 Evaluation Board)		
Size: A3	Document Number: MEMORY(OneNAND)/JTAG/CLK	Rev: 0.0
Date: Wednesday, July 02, 2008	Sheet 6 of 13	

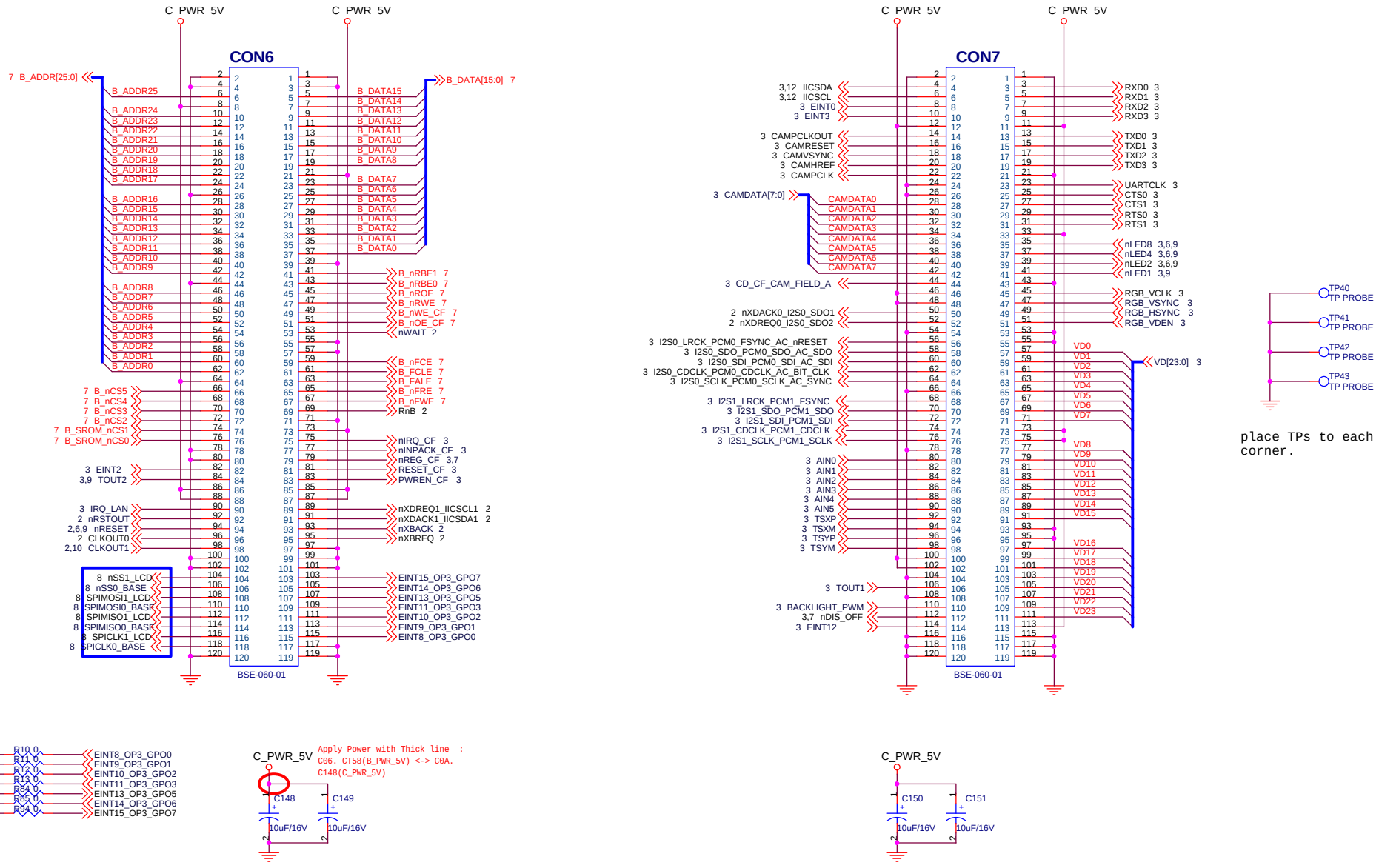

CON8
QSE-060-01-L-D-A
External I/O
EINT14 3,11
EINT8 3,11
EINT9 3,11
EINT11 3,11
EINT13 3,11
EINT10 3,11
EINT15 3,11
B_PWR_5V
CT58
100uF/16V
C221
1uF
Apply Power with Thick line : C06. CT58(B_PWR_5V) <-> C0A. C148(C_PWR_5V)
U9
U8
U12
U11
SN74AVCA164245
VDD_RMEM
VDD_D
C101 100nF
C102 100nF
C99 100nF
C100 100nF
C105 100nF
C106 100nF
C103 100nF
C104 100nF
2,6 RADDR[25:0]
B_ADDR[25:0] 11
DIR L : B->A
DIR H : A->B
Propagation Delay
A->B 1.6nS ~ 4.3nS
B->A 1.8nS ~ 5.5nS
sn74AVCA164245
(A(1.8V) <-> B(3.3V))
A->B 1.6nS ~ 4.3nS
B->A 1.8nS ~ 5.5nS
6 nCS_SROM0
2 nRCS1
2 nRCS2
2 nRCS3
2 nRCS4
2 nRCS5
2 nFCE
2 nFRE
2 nFWE
2 FALE
2 FCLE
2 nOE_CF
2 nWE_CF
B_SROM_nCS0 11
B_SROM_nCS1 11
B_nCS2 11
B_nCS3 11
B_nCS4 11
B_nCS5 11
B_nFCE 11
B_nFRE 11
B_nFWE 11
B_FALE 11
B_FCLE 11
B_nOE_CF 11
B_nWE_CF 11
2,6 nRWE
2,6 nROE
2 nRBE0
2 nRBE1
B_nRWE 11
B_nROE 11
B_nRBE0 11
B_nRBE1 11
2,6 RDATA[15:0]
B_DATA[15:0] 11
BUF_DIR
R41 100K (NC)
R42 100K (NC)
R43 100K
R44 100K
R45 0
R46 0
R49 100K (NC)
R50 100K (NC)
R51 0
R52 100K
R53 0
L : COM - NC
H : COM - NO
U39
TS5A3159_SPDT
3,11 nDIS_OFF
GPB0
R235 0
R236 100K
TRUE_IDE_EN
nCF_MOE
SN74AUC2G08
Propagation Delay (CL30pF)
Typ: 1.5nS (1.2 ~ 2.1)
U10A
U10B
U14A
U14B
U15A
U15B
U16A
U16B
U13A
R54 R55 R56 R57 100K
R58 100K
R59 100K
R60 100K
R61 100K
BCtrl_I0
BCtrl_I1
3,11 nREG_CF
2 nFCE
2,6 nROE
2 nFRE
R47 0
R48 NC
RADDR25
(RDATA_OEN)
SAMSUNG ELECTRONICS CO.,LTD
Title
SMDK2450 (S3C2450 Evaluation Board)
Size A3
Document Number BUFFERS(SROM IF)
Rev 0.0
Date: Wednesday, July 02, 2008
Sheet 7 of 13


VDD_USBH_5V
R62 15K
R63 22
3 DN0
3 DP0
R75 22
R76 15K
CON2A
VBUS
D-
D+
GND
USB(HOST)
SOCKET
Dual USB Port - A type
DN and DP should be routed evenly
TP27
TP28
TP29
TP30
TP31
CON1
VBUS
D-
D+
ID
GND
USB-MINIAB
VDD_USBH_5V
TP32
TP33
CON2B
VBUS
D-
D+
GND
USB(HOST)
SOCKET
Dual USB Port - A type
R78
3 VBUS_DET
0
R80
300K
R81
200K
VBUS
L1
ferrite Bead EXC-3225U
CON3
VBUS
D-
D+
GND
BG2 BG1
USB(Device)
SOCKET
USB Port B type
3 DM_UDEV
3 DP_UDEV
DN and DP should be routed evenly
L2
ferrite Bead EXC-3225U
fundermental
Oscillator
tolerance +-100ppm
peak jitter 100ps
duty cycle
40/60~60/40
swing 3.3V
VDD_USB33
OSC2
VDD
OUT
OE
GND
OSCILLATOR 48Mhz
XO_UDEV 3
C111
30pF NC
R172
1M NC
XI_UDEV 3
C112
30pF NC
3 REXT
R93
44.2 1%
For USB Clock
C_PWR_5V
L7 LQH32C 10uH
U31
SW1
SW2
VIN
VOUT
SHDN/SS
FB
MODE/SYNC
VC
RT
GND
LTC3440EMS
D5
MBRM120LT3
VDD_USBH_5V
R157
100K
C153
47uF
R158
60.4K 1%
3 PWREN_USBH
R160
523K 1%
C154
47uF
C155
47uF
R159
15K
C152
15nF
R161
169K 1%
USB
HOST
CON4
IEEE1394-4
CON9
IEEE1394-4
C159
C161
C156
C160
NC
3 nSS0
3 SPIMISO0
3 SPIMOSI0
3 SPICLK0
R178
R179
R180
R181
nSS0_BASE 11
SPIMISO0_BASE 11
SPIMOSI0_BASE 11
SPICLK0_BASE 11
11 nSS1_LCD
11 SPIMISO1_LCD
11 SPIMOSI1_LCD
11 SPICLK1_LCD
R174
R175
R176
R177
nSS1 3
SPIMISO1 3
SPIMOSI1 3
SPICLK1 3
R174~R181 should be located on top of CPU board.
For HS-SPI test
SDDATA & CLK path must be same length and route
VDD_D
3 SD1_DAT[7:0]
SD1_DAT2
SD1_DAT3
3 SD1_CMD
SD1_DAT0
SD1_DAT1
SD1_DAT4
SD1_DAT5
SD1_DAT6
SD1_DAT7
3 SD1_CLK
3 SD1_nCD
3 SD1_nWP
R64 10K
R65 10K
R66 10K
R67 10K
R68 10K
R70 10K
R71 10K
R72 10K
R73 10K
R74 10K
R79 NC
C107 100nF
C108 100nF
C109 100nF
C110 100nF
U17
NC
CLK
CMD
DAT0
DAT1
DAT2
DAT3
DAT4
DAT5
DAT6
DAT7
VDD
VSS
P30/GND
P29/GND
SD Socket [Taisol]
SDDATA & CLK path must be same length and route
3 SD0_DAT[3:0]
SD0_DAT2
SD0_DAT3
3 SD0_CMD
SD0_DAT0
SD0_DAT1
3 SD0_CLK
3 nCD_SD0
R86 10K
R87 10K
R88 10K
R89 10K
R90 10K
R91 10K
R92 10K
R95 NC
U18
SD Socket [Taisol]
R77
330
D1
SMD TYPE (BLUE)
3 SD1_LED
4bit only
<Silk>
SAMSUNG ELECTRONICS CO.,LTD
Title
SMDK2450 (S3C2450 Evaluation Board)
Size
A3
Document Number
USB/HS_MMC/HS_SPI
Rev
0.0
Date:
Wednesday, July 02, 2008
Sheet
8
of
13

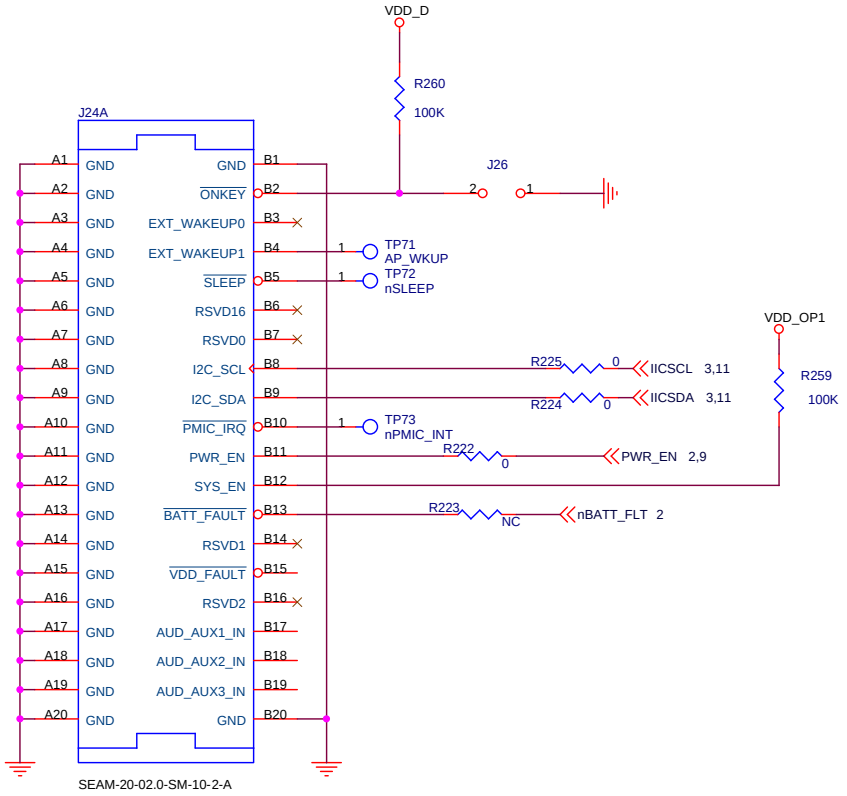

VDD_D
C_PWR_5V
VDD_ARM
U21
U20
U22A
U22B
U22C
U24
U23
Default 1.3V
74LVC573/SO
74LV00/SO
MAX1718
VGATE-PAD
VDD_EPLL
VDD_MPLL
VDD_INT
SAMSUNG ELECTRONICS CO.,LTD
SMDK2450 (S3C2450 Evaluation Board)
CPU B'D POWER(ARM/INT)
Wednesday, July 02, 2008

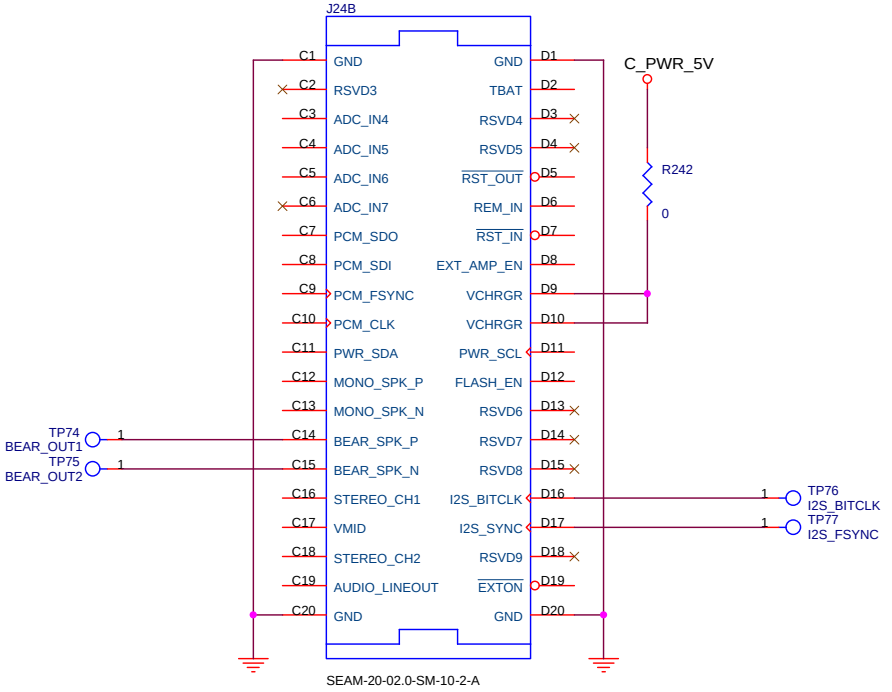


SAMSUNG ELECTRONICS CO.,LTD		
Title: SMDK2450 (S3C2450 Evaluation Board)		
Size: A3	Document Number: CPU B'D POWER(ALIVE/IO)	Rev: 0.0
Date: Wednesday, July 02, 2008	Sheet 10 of 13	

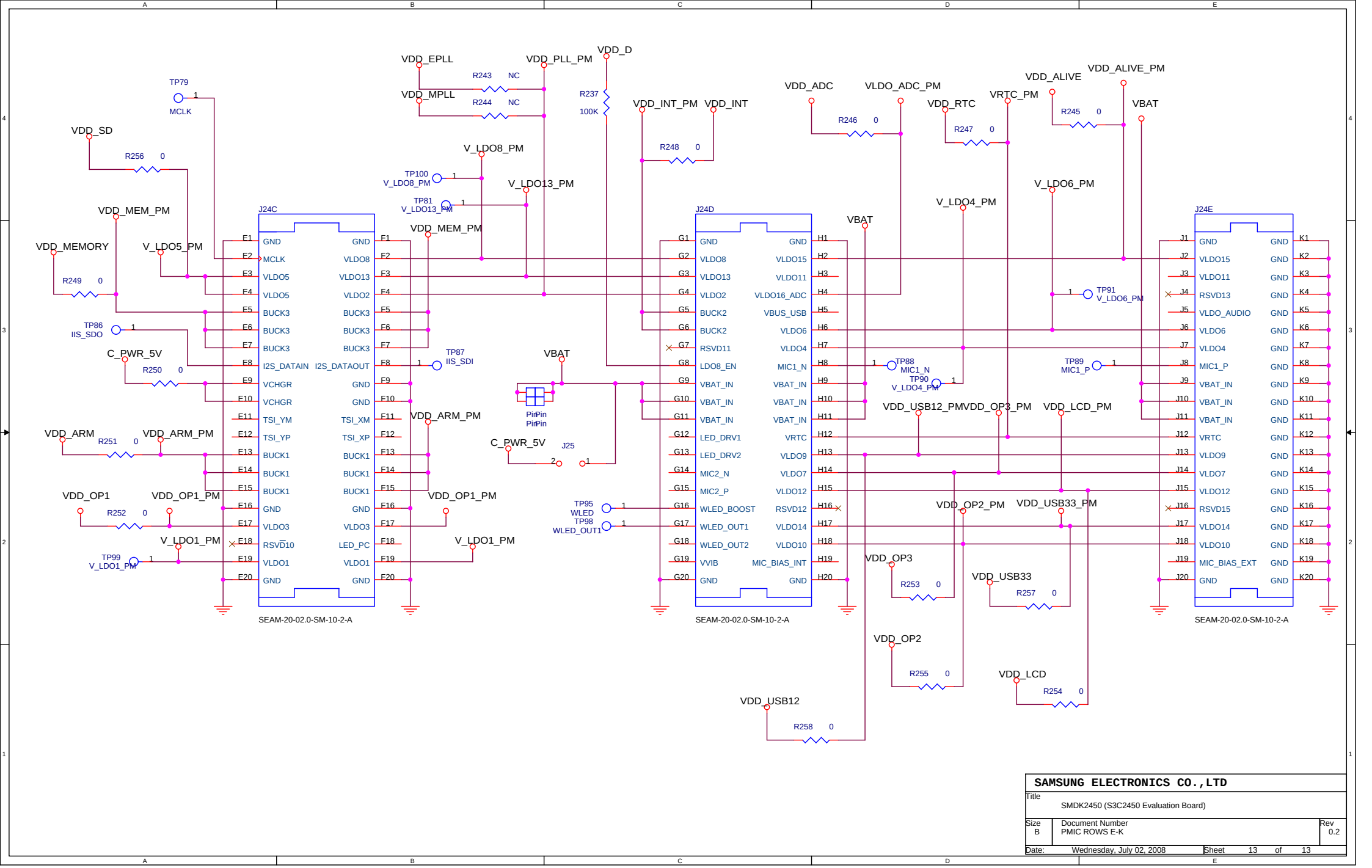


SAMSUNG ELECTRONICS CO.,LTD		
Title: SMDK2450 (S3C2450 Evaluation Board)		
Size: A3	Document Number: C0A. B2B Connector(CPU)	Rev: 0.0
Date: Wednesday, July 02, 2008	Sheet 11 of 13	



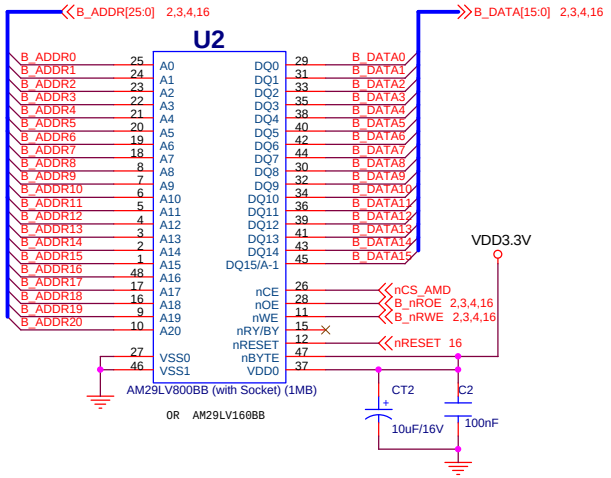


SAMSUNG ELECTRONICS CO.,LTD		
Title: SMDK2450 (S3C2450 Evaluation Board)		
Size: B	Document Number: PMIC ROWS A-D	Rev: 0.2
Date: Wednesday, July 02, 2008	Sheet 12 of 13	

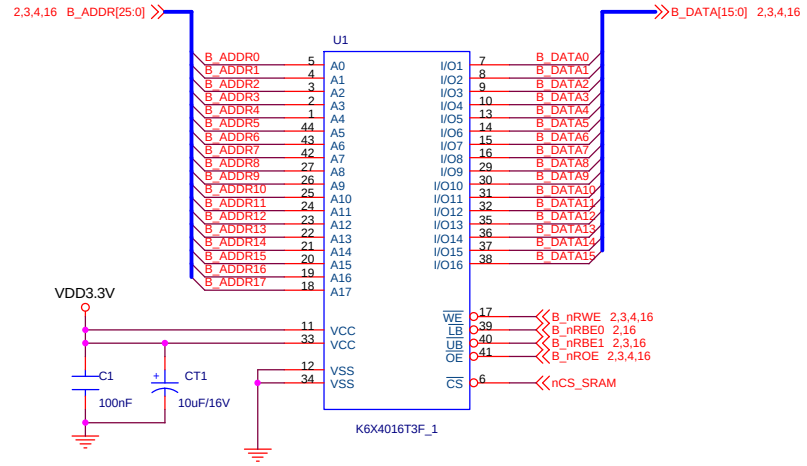


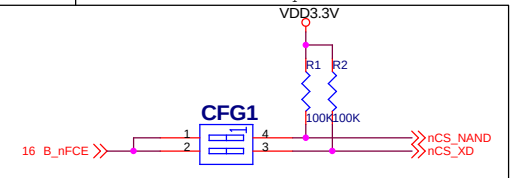
SAMSUNG ELECTRONICS CO.,LTD		
Title: SMDK2450 (S3C2450 Evaluation Board)		
Size: B	Document Number: PMIC ROWS E-K	Rev: 0.2
Date: Wednesday, July 02, 2008	Sheet 13 of 13	

AMD Flash Memory(SOCKET)



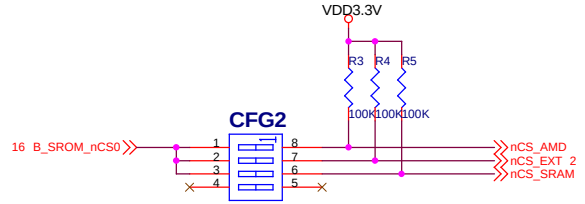
SRAM





<Silk>

CFG1: nFCE	SROM Selector
[2]	XD card
[1]	NAND



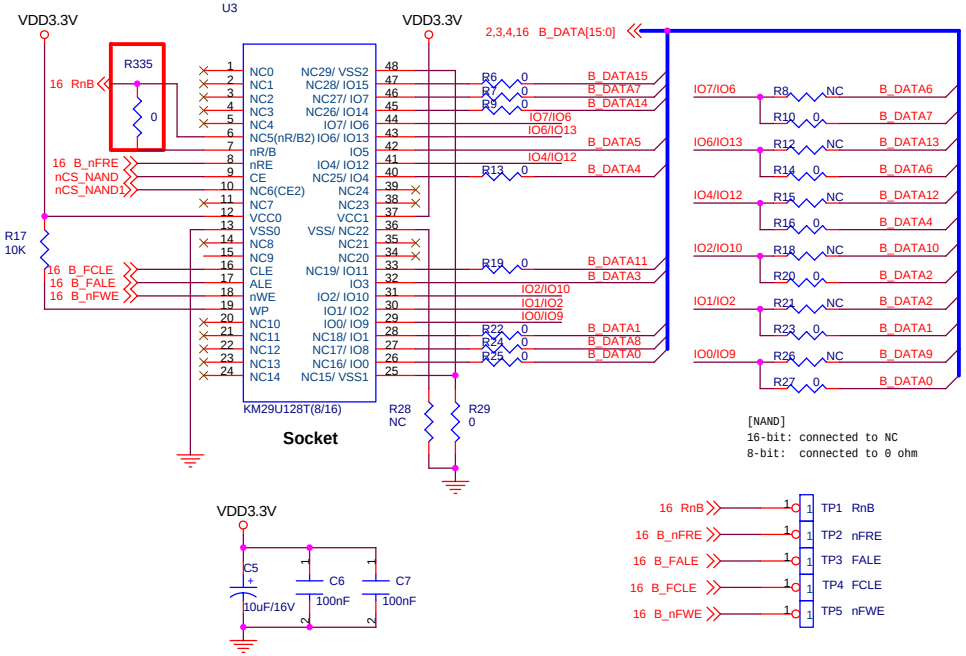
<Silk>

CFG2: nCS0	SROM Selector
[3]	External
[2]	SRAM
[1]	NOR(AMD)

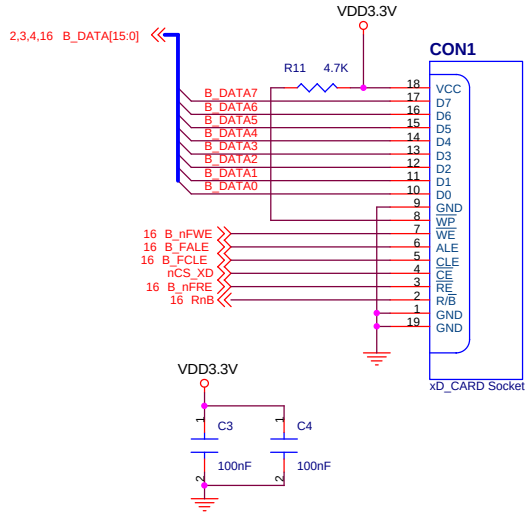
S3C2450
Addition : NAND CS1 & RnB1

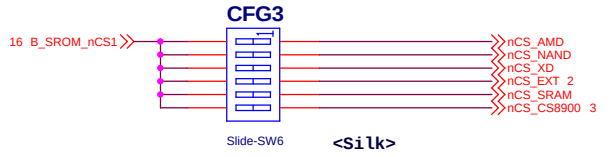
S3C2450
Addition : NAND CS1
SW(To Select Ethernet or Additional Nand CS)

NAND Flash memory (SOCKET)



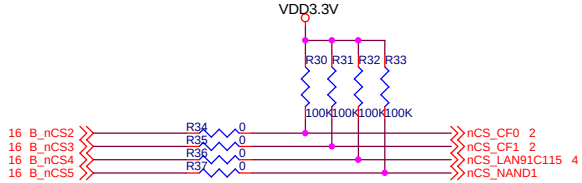
XD PICTURE CARD





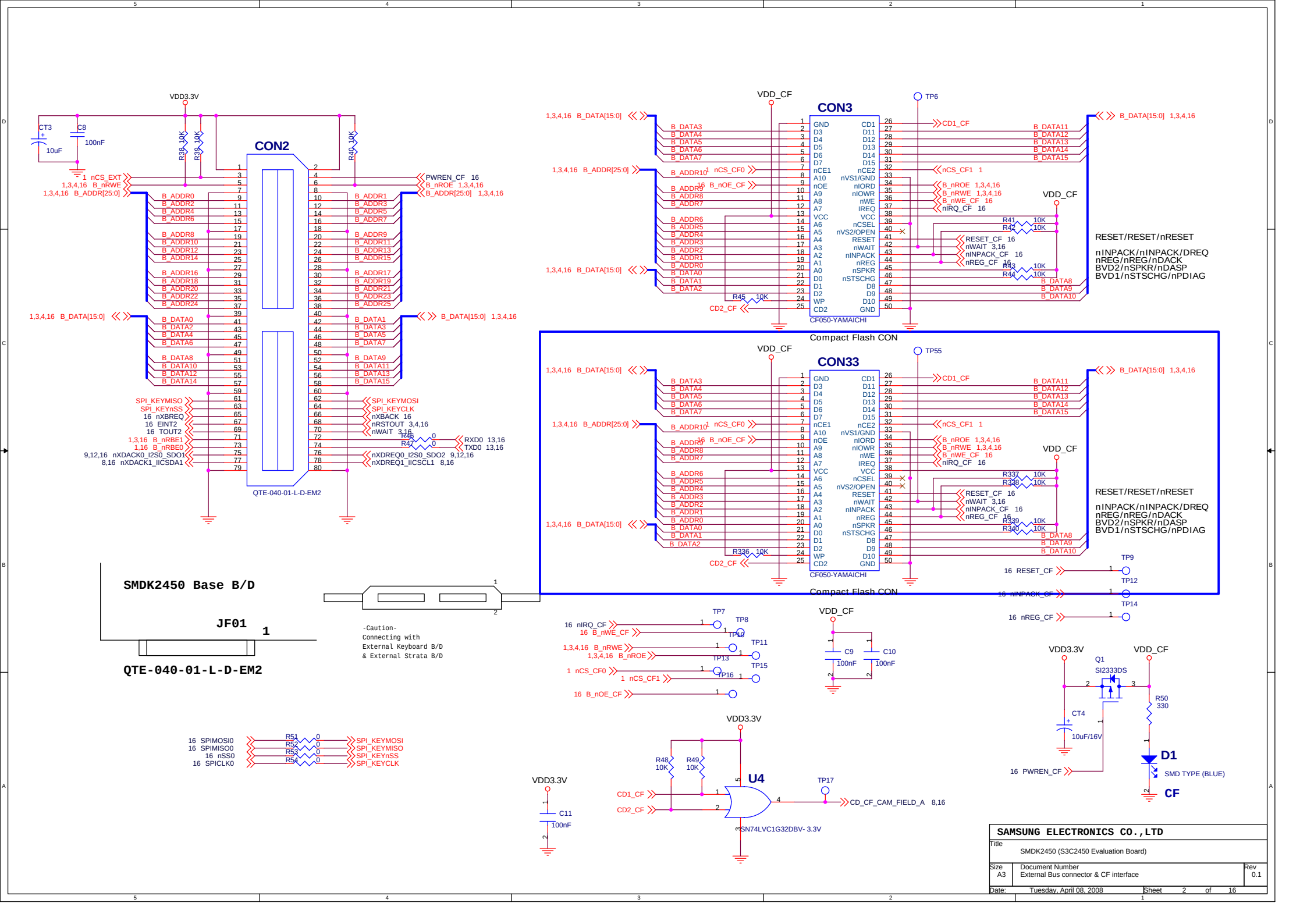
<Silk>

CFG3: nCS1	SROM Selector
[6]	CS8900(CS1)
[5]	SRAM
[4]	External
[3]	XD card
[2]	NAND
[1]	NOR(AMD)

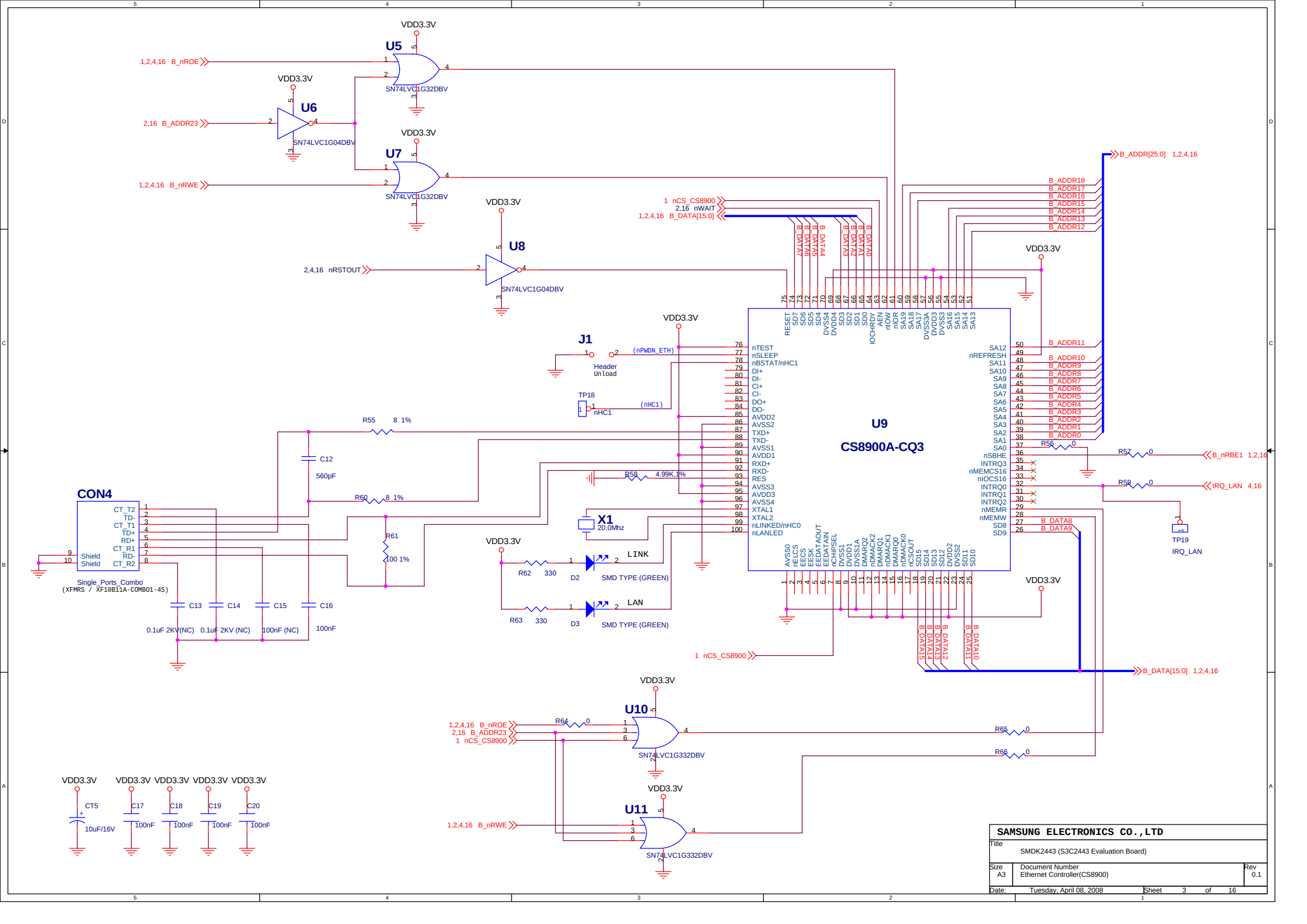


R281~R284 place on top

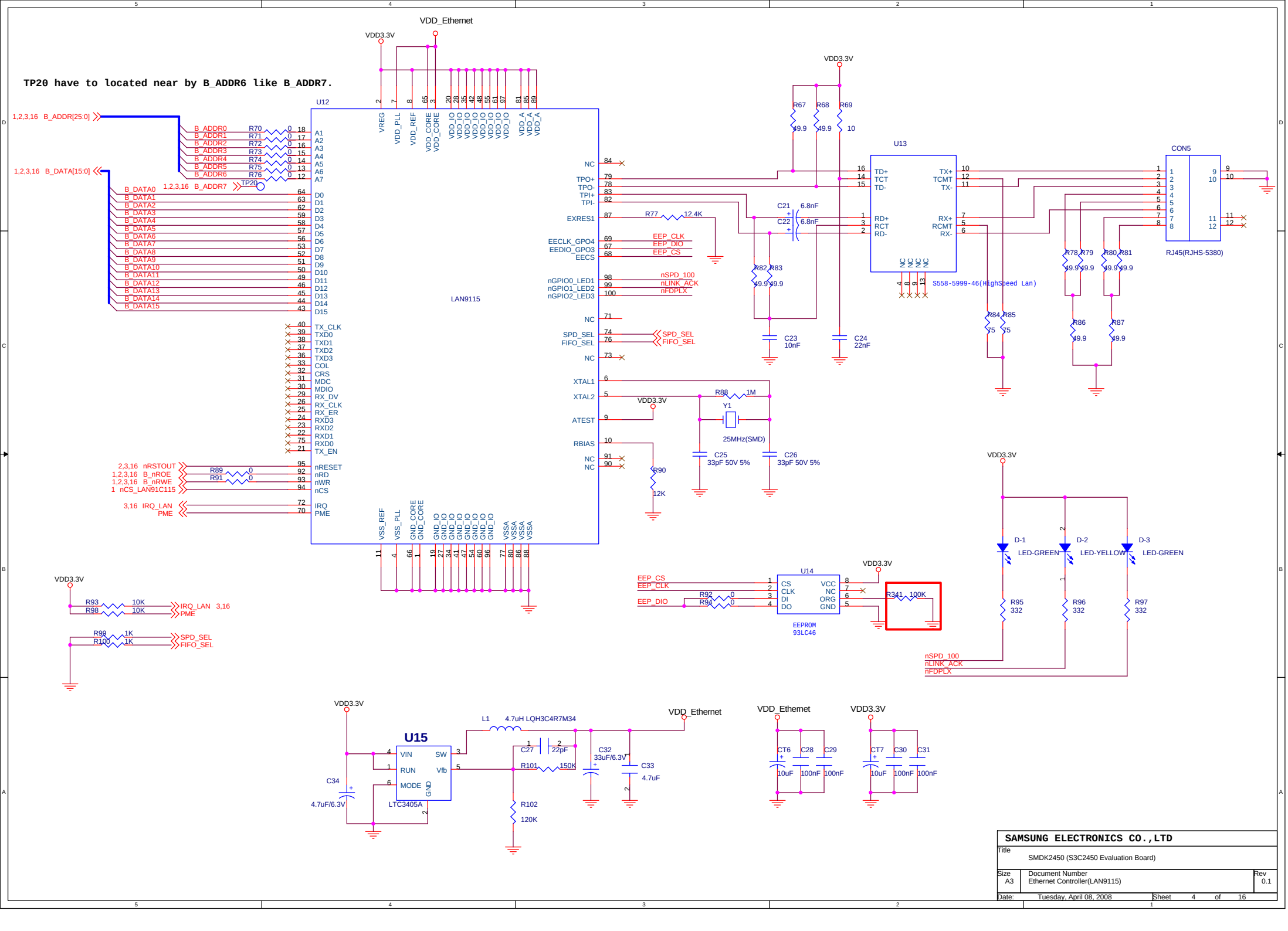
SAMSUNG ELECTRONICS CO.,LTD		
Title: SMDK2450 (S3C2450 Evaluation Board)		
Size: A3	Document Number: NOR/NAND/SRAM/CONFIG	Rev: 0.1
Date: Tuesday, April 08, 2008	Sheet 1 of 16	

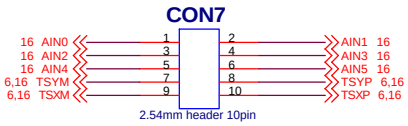


SAMSUNG ELECTRONICS CO.,LTD	
Title	SMDK2450 (S3C2450 Evaluation Board)
Size A3	Document Number: External Bus connector & CF interface
Rev	0.1
Date:	Tuesday, April 08, 2008
Sheet	2 of 16

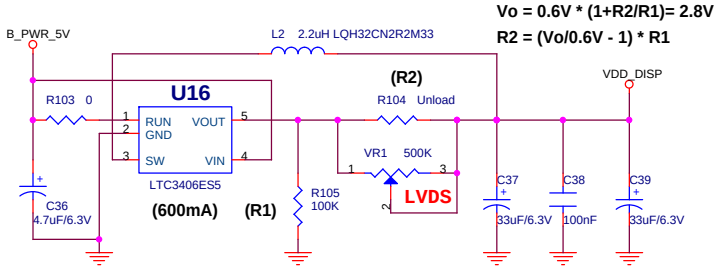


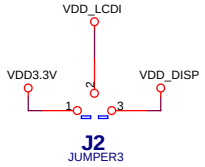
SAMSUNG ELECTRONICS CO.,LTD		
Title: SMDK2443 (S3C2443 Evaluation Board)		
Size: A3	Document Number: Ethernet Controller(CS8900)	Rev: 0.1
Date: Tuesday, April 08, 2008	Sheet 3 of 16	

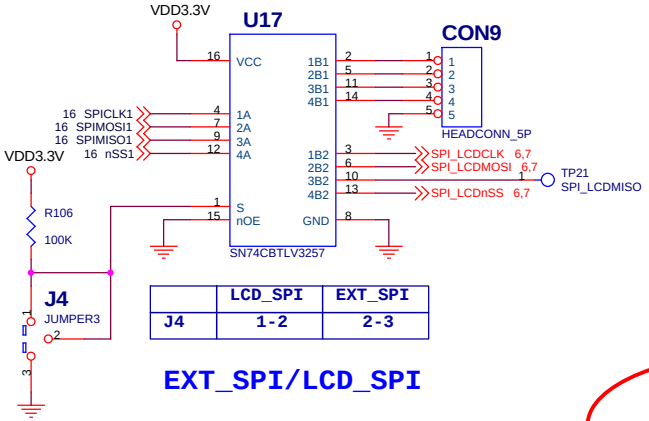

TP20 have to located near by B_ADDR6 like B_ADDR7.
VDD_Ethernet
VDD3.3V
U12
LAN9115
1,2,3,16 B_ADDR[25:0]
1,2,3,16 B_DATA[15:0]
B_ADDR0
B_ADDR1
B_ADDR2
B_ADDR3
B_ADDR4
B_ADDR5
B_ADDR6
1,2,3,16 B_ADDR7
TP20
B_DATA0
B_DATA1
B_DATA2
B_DATA3
B_DATA4
B_DATA5
B_DATA6
B_DATA7
B_DATA8
B_DATA9
B_DATA10
B_DATA11
B_DATA12
B_DATA13
B_DATA14
B_DATA15
TX_CLK
TXD0
TXD1
TXD2
TXD3
COL
CRS
MDC
MDIO
RX_DV
RX_CLK
RX_ER
RXD3
RXD2
RXD1
RXD0
TX_EN
2,3,16 nRSTOUT
1,2,3,16 B_nROE
1,2,3,16 B_nRWE
1 nCS_LAN91C115
3,16 IRQ_LAN
PME
nRESET
nRD
nWR
nCS
IRQ
PME
EEPROM
93LC46
U13
S558-5999-46(HighSpeed Lan)
CON5
RJ45(RJHS-5380)
25MHz(SMD)
D-1
LED-GREEN
D-2
LED-YELLOW
D-3
LED-GREEN
nSPD_100
nLINK_ACK
nFDPLX
U15
LTC3405A
4.7uF/6.3V
SAMSUNG ELECTRONICS CO.,LTD
Title
SMDK2450 (S3C2450 Evaluation Board)
Size
A3
Document Number
Ethernet Controller(LAN9115)
Rev
0.1
Date:
Tuesday, April 08, 2008
Sheet
4
of
16



ADC

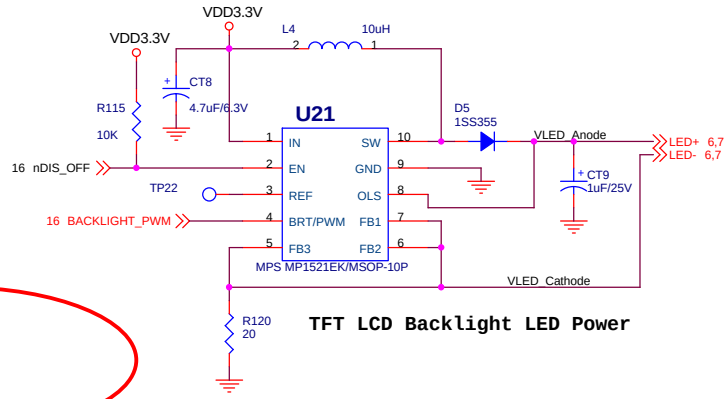




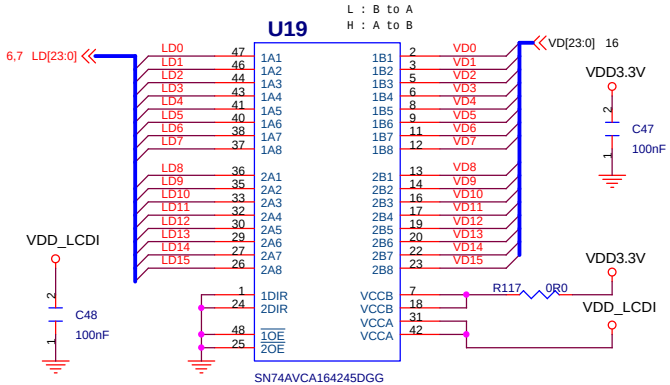


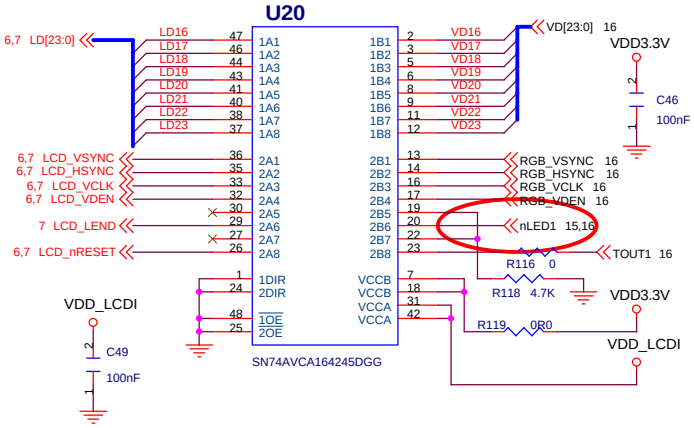
	LCD_SPI	EXT_SPI
J4	1-2	2-3

EXT_SPI/LCD_SPI

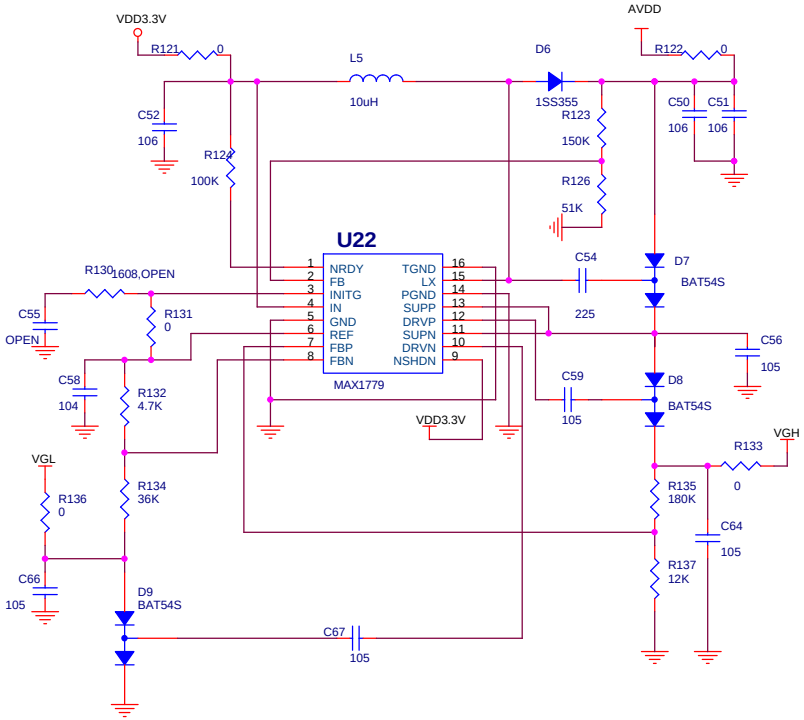


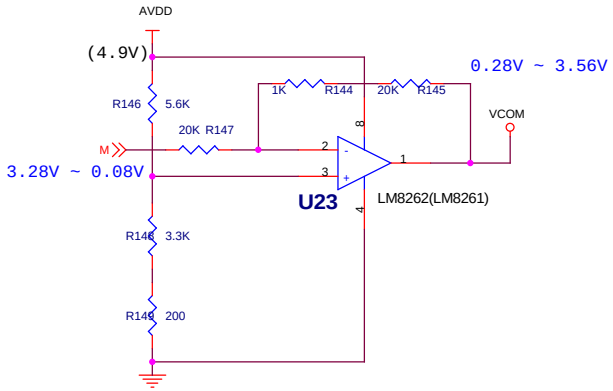
TFT LCD Backlight LED Power

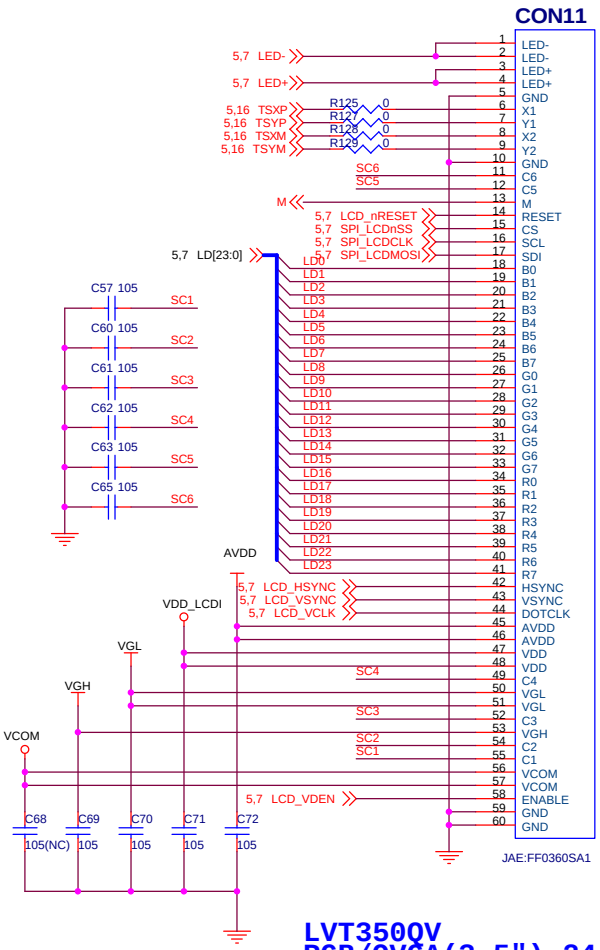




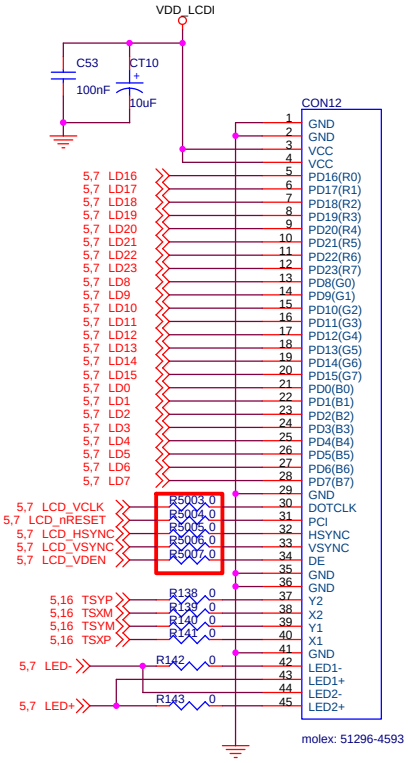
SAMSUNG ELECTRONICS CO.,LTD		
Title: SMDK2450 (S3C2450 Evaluation Board)		
Size: A3	Document Number: B05. LCD General/SPI/ADC	Rev: 0.1
Date: Tuesday, April 08, 2008	Sheet 5 of 16	





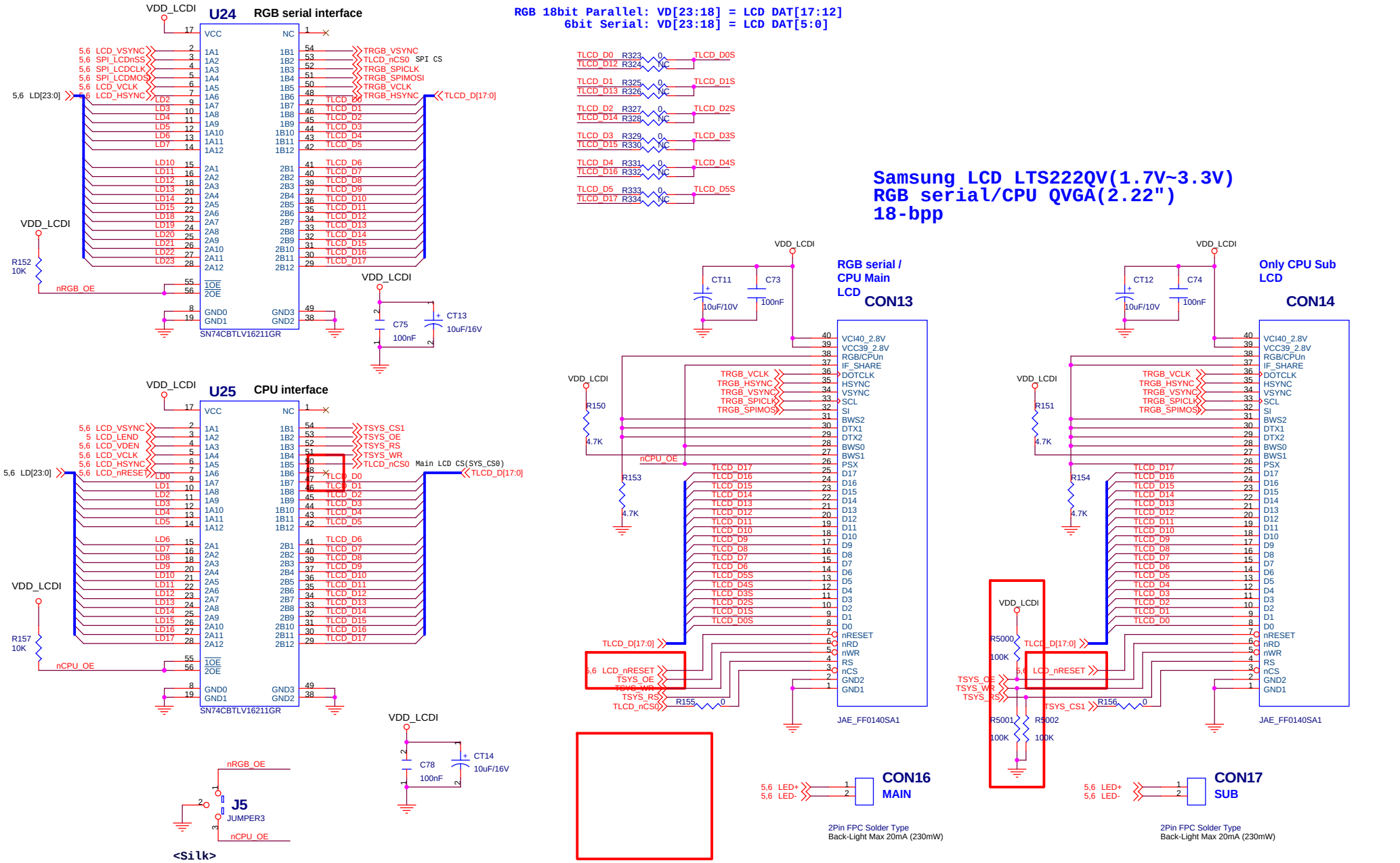


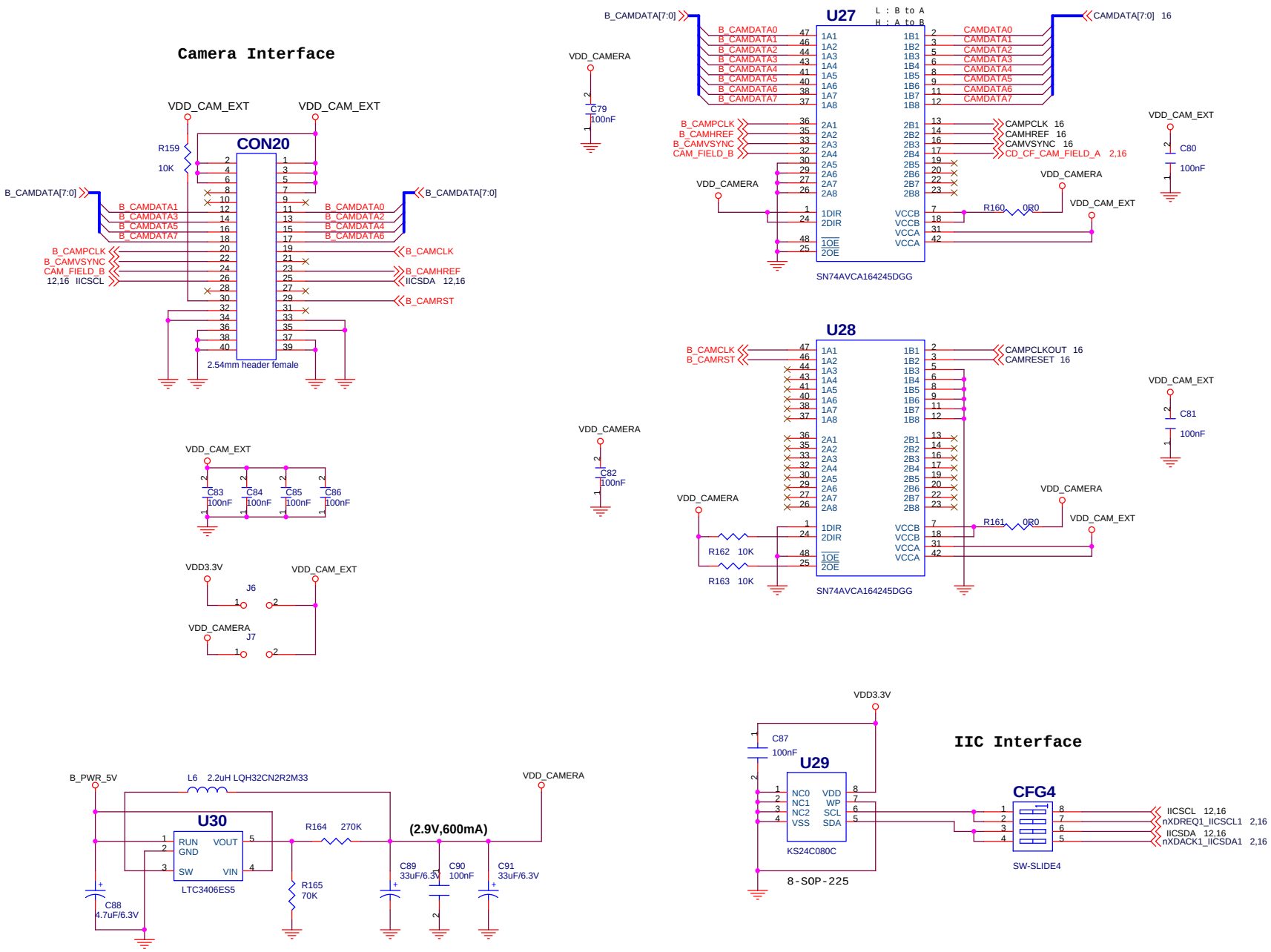
LVT350QV
RGB/QVGA(3.5") 24-bpp



LTE480WE
RGB/WVGA(4.8") 24-bpp
- Default

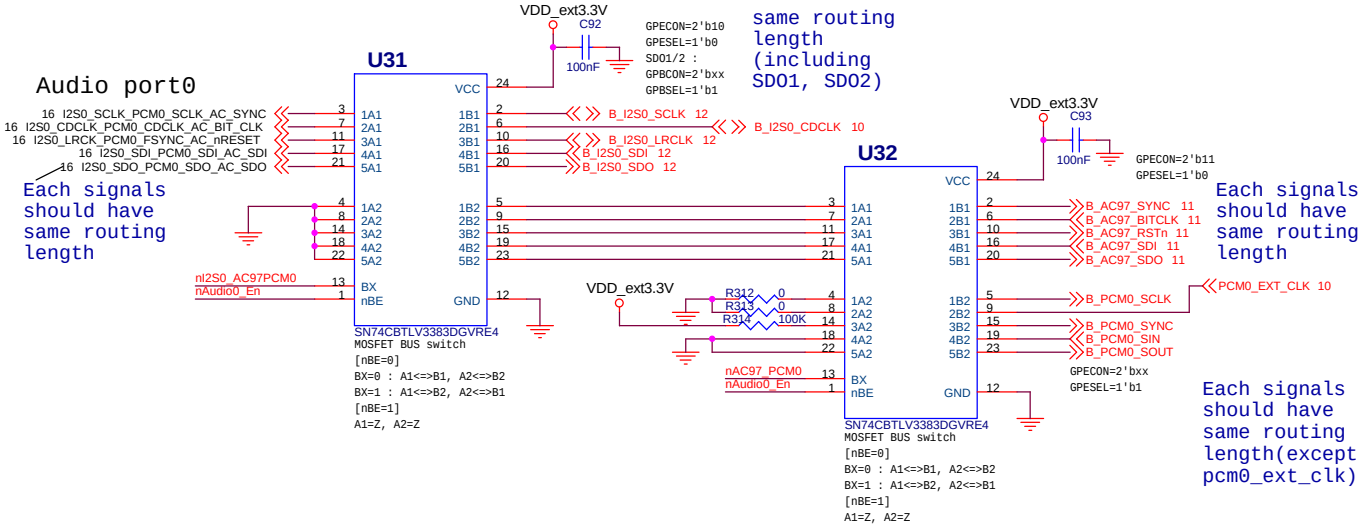
SAMSUNG ELECTRONICS CO.,LTD		
Title: SMDK2450 (S3C2450 Evaluation Board)		
Size: A3	Document Number: LCD interface & TFT LCD(Landscape type)	Rev: 0.1
Date: Tuesday, April 08, 2008	Sheet 6 of 16	

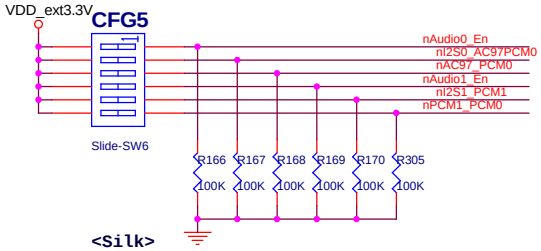

RGB 18bit Parallel: VD[23:18] = LCD DAT[17:12]
6bit Serial: VD[23:18] = LCD DAT[5:0]
U24 RGB serial interface
U25 CPU interface
SN74CBTLV16211GR
SPI CS
Main LCD CS(SYS_CS0)
Samsung LCD LTS222QV(1.7V~3.3V)
RGB serial/CPU QVGA(2.22")
18-bpp
RGB serial / CPU Main LCD
CON13
Only CPU Sub LCD
CON14
JAE_FF0140SA1
CON16
MAIN
CON17
SUB
2Pin FPC Solder Type
Back-Light Max 20mA (230mW)
J5
JUMPER3
<Silk>
LCD IF | 1-2 | 2-3
J5 | RGB Serial IF | CPU IF (Main/Sub)
SAMSUNG ELECTRONICS CO.,LTD
SMDK2450 (S3C2450 Evaluation Board)
TFT LCD(CPU/RGB portrait type) / CSTN LCD
Rev 0.1
Date: Tuesday, April 08, 2008
Sheet 7 of 16



SAMSUNG ELECTRONICS CO.,LTD		
Title: SMDK2450 (S3C2450 Evaluation Board)		
Size: A3	Document Number: Camera Interface	Rev: 0.1
Date: Tuesday, April 08, 2008	Sheet 8 of 16	

Audio port0





<Silk>

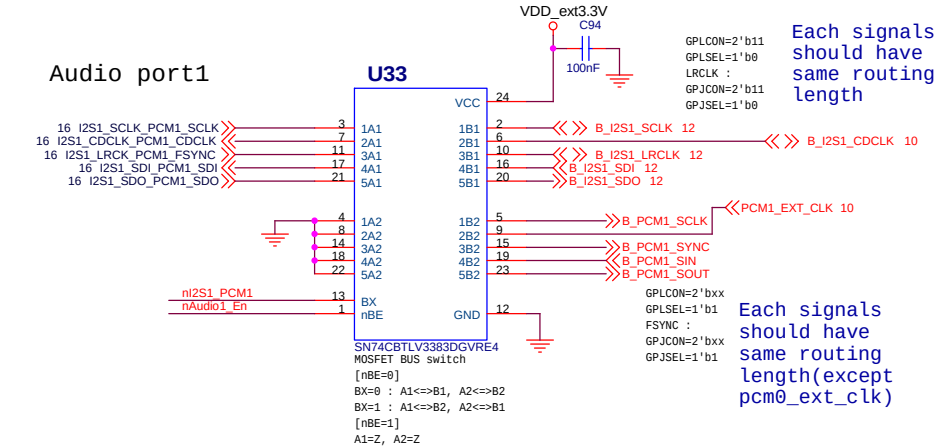
<Pcm0/1 select>

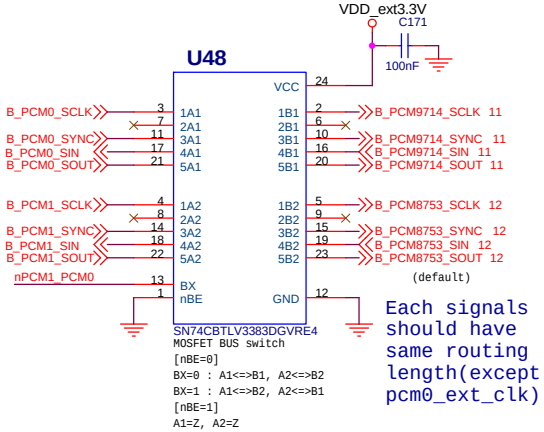
Port 0	CFG5	Enable [1]	Select [2]	Select [3]	Select [6]
	I2S0 (Def)	OFF (Def.)	OFF	X	X
	AC97		ON	OFF	X
	PCM0		ON	ON	ON (8753)
	Disable	ON	X		

Port 1	CFG5	Enable [4]	Select [5]	Select [6]
	IIS1* (Def)	OFF (Def.)	OFF	X
	PCM1*		ON	OFF (8753)
	Disable	ON	X	

* set CFG6 switch of CPU b'd

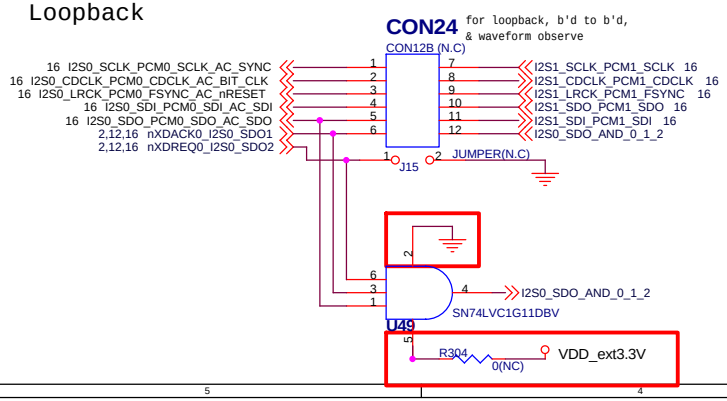
Audio port1





Pcm0/1 are verified by 8753 codec(default)
but can be verified by 9714(sw setting is needed)

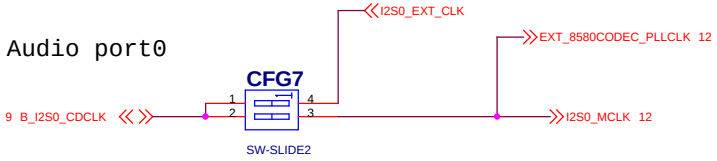
Loopback



SAMSUNG ELECTRONICS CO.,LTD			
Title: SMDK2450 (S3C2450 Evaluation Board)			
Size: A3	Document Number: Audio(Demux)		Rev: 0.1
Date: Tuesday, April 08, 2008	Sheet 9 of 16		

<i2s cdclk select/codec operating clk supply>

Audio port0

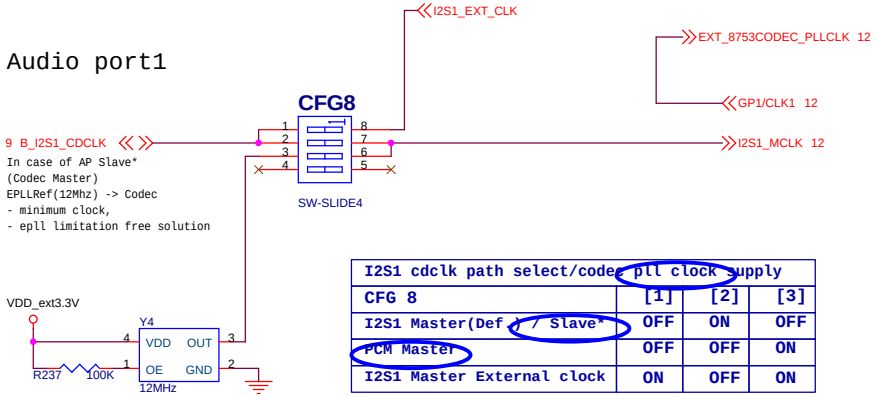


<Silk>

I2S0 cdclk path select		
CFG 7	[1]	[2]
I2S0 Master(Def.)	OFF	ON
I2S0 Slave	OFF	OFF
I2S0 Master External clock	ON	ON*

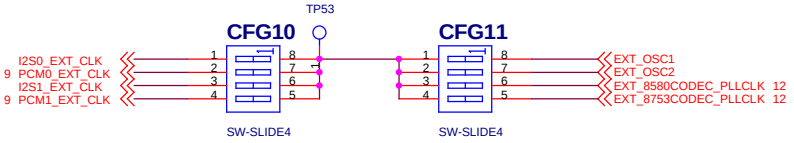
On* : without crystal to codec
off : codec pll clock
with crystal
(sw setting is needed)

Audio port1

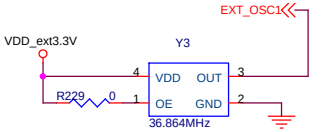


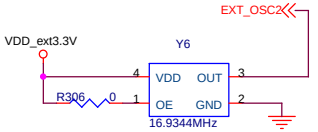
I2S1 cdclk path select/codec pll clock supply			
CFG 8	[1]	[2]	[3]
I2S1 Master(Def.) / Slave*	OFF	ON	OFF
PCM Master	OFF	OFF	ON
I2S1 Master External clock	ON	OFF	ON

<External Clock select part>

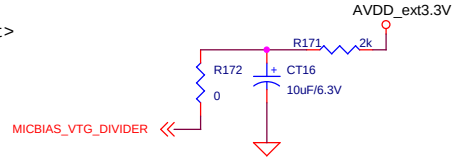


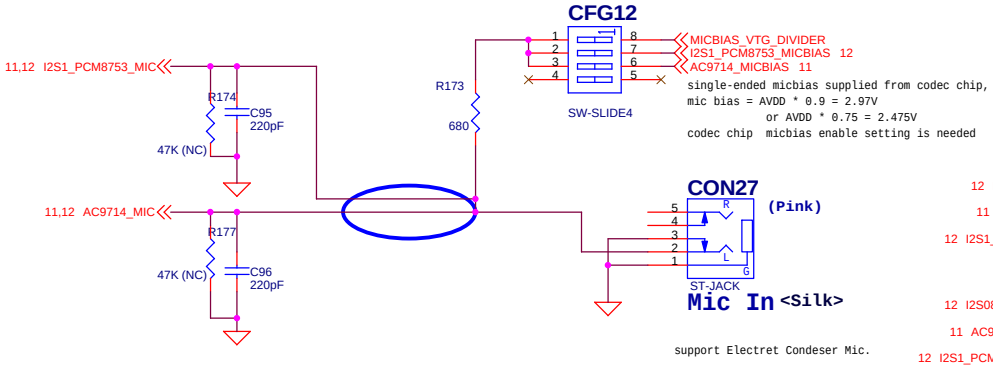
Ext. Clk Sel.	CFG10 To.	CFG11 From
[1]	I2S0	OSC1 36.864MHz
[2]	PCM0	OSC2 16.9344MHz
[3]	I2S1	8580PLL
[4]	PCM1	8753PLL
All Off (Default)		





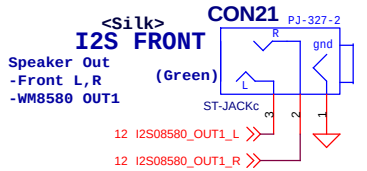
<mic bias part>

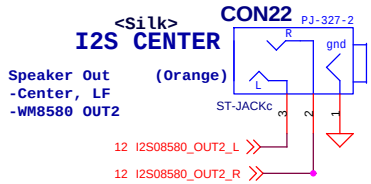


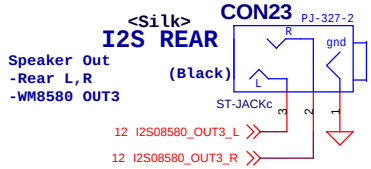


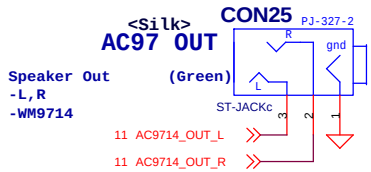
<Silk>

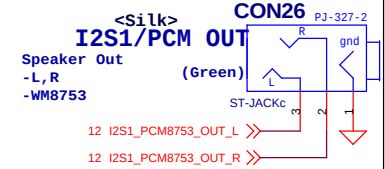
CFG12	Mic bias source
[1]	VTG div. (Def.)
[2]	8753 Codec
[3]	9714 Codec

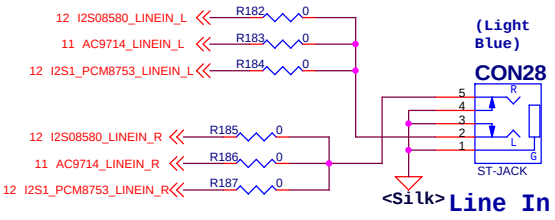












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Title: SMDK2450 (S3C2450 Evaluation Board)		
Size: A3	Document Number: Audio(Ext. Clk & Conn)	Rev: 0.1
Date: Tuesday, April 08, 2008	Sheet 10 of 16	

Adopted from 6400/2450 io b'd
- modified library as datasheet
- removed capacitors as reference

U34

WM9714LGEFL
for test Audio port0 (AC97)
(extraly can test PCM1)

DBVDD, DCVDD, DGND2, DGND1, AVDD, SPKVDD, HPVDD, AVDD2, AGND3, HPGND, SPKGND, AGND, AGND2, GNDPADDLE, MCLKA, MCLKB, SDATAOUT, BITCLK, SDATAIN, SYNC, RESETB, GPIO1/PCMCLK, GPIO3/PCMFS, GPIO4/PCMDAC, GPIO5/PCMADC, AUX4, NC, NC, NC, NC, SPKL, OUT4, SPKR, OUT3, MONO, HPL, HPR, GPIO2/IRQ, MICBIAS, CAP2, VREF, LINEL, LINER, PCBEEP, MONOIN, MIC1, MIC2A, MIC2B, MICCM

VDD_ext3.3V, VDD_ext1.8V, AVDD_ext3.3V

Y2: VDD, OUT, OE, GND, 24.576MHz, R188 100K

CT19 4.7uF/6.3V, CT20 4.7uF/6.3V, CT21 4.7uF/6.3V, CT22 4.7uF/6.3V, CT23 4.7uF/6.3V, CT24 4.7uF/6.3V

R189 0, R190 100K (NC), R191 0

9 B_AC97_SDO, 9 B_AC97_BITCLK, 9 B_AC97_SDI, 9 B_AC97_SYNC, 9 B_AC97_RSTn
R192 47, R193 47, R194 47, R195 0, R197 0

9 B_PCM9714_SCLK, 9 B_PCM9714_SYNC, 9 B_PCM9714_SOUT, 9 B_PCM9714_SIN
R307 0, R308 0, R309 0, R310 0

8.2K divided network :
to prevent codec chip
for full 2Vrms input
signal,
(7dB attenuation)

CT27 1uF/6.3V

10 AC9714_LINEIN_L, R199 8.2K, C97 220pF, R200 8.2K
10 AC9714_LINEIN_R, R201 8.2K, C100 220pF, R202 8.2K
10,12 AC9714_MIC, R205 0

C98 1uF, C99 1uF, C101 100nF, C102 100nF, C103 1uF, C104 100nF, R207 NC, C105 100nF, R208 NC, C106 1uF, R209 47K (NC), C107 220pF

CT28 100uF/6.3V, CT29 100uF/6.3V
AC9714_OUT_L 10, AC9714_OUT_R 10
16 or 32 ohm hp
R203 47K, R204 47K

R206 100K

AC9714_MICBIAS 10

CT30 4.7uF/6.3V, CT31 4.7uF/6.3V, CT32 4.7uF/6.3V

CT19~24, 30~32 should be placed as close as to the codec chip

Power

VDD_ext5V, AVDD_ext5V, VDD_ext3.3V, AVDD_ext3.3V

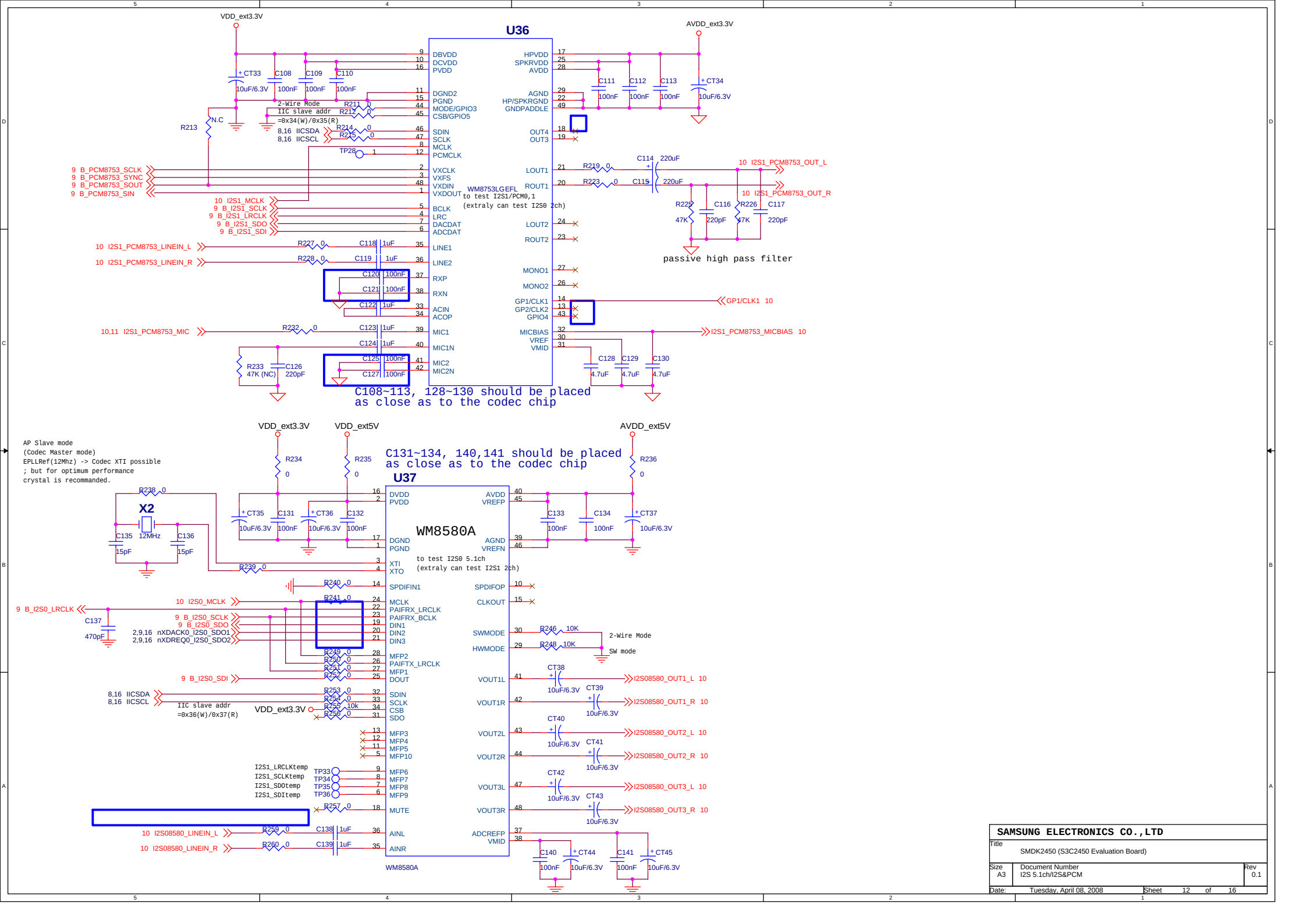
L7 BLM18PG121, L8 BLM18PG121, L9 BLM18PG121
<--LINE!!
CT17 10uF/6.3V, CT18 10uF/6.3V

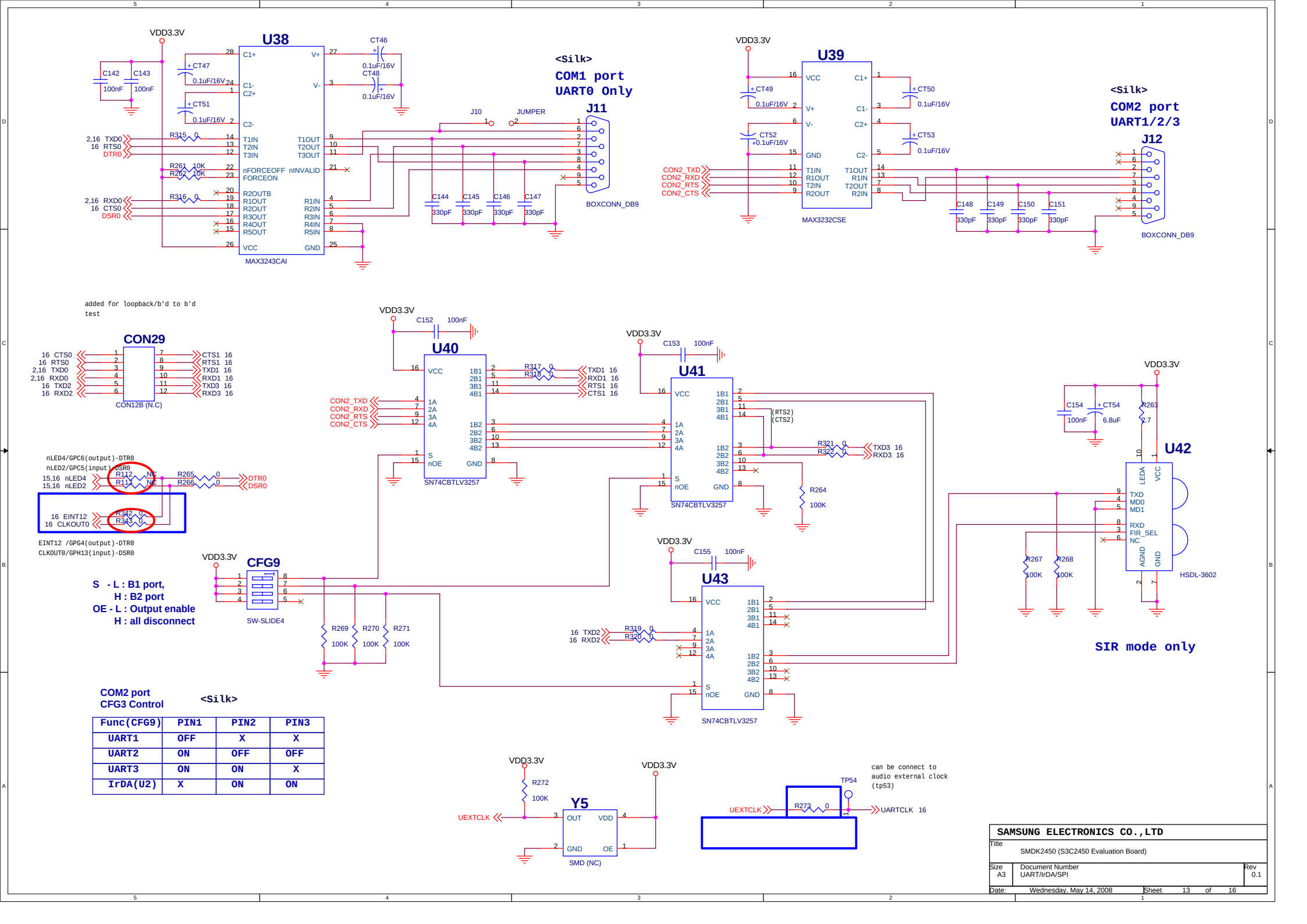
U35

MIC5219BM5: IN, OUT, GND, EN, ADJ
VDD_ext5V, VDD_ext1.8V, Vout
CT25 10uF/6.3V, CT26 10uF/6.3V
R196 220K 1%, R198 100K 1%
280K => 3.3V

Vout = 1.24V(1+R2/R1)

SAMSUNG ELECTRONICS CO.,LTD		
Title: SMDK2450 (S3C2450 Evaluation Board)		
Size: A3	Document Number: AC97&Power	Rev: 0.1
Date: Tuesday, April 08, 2008	Sheet 11 of 16	

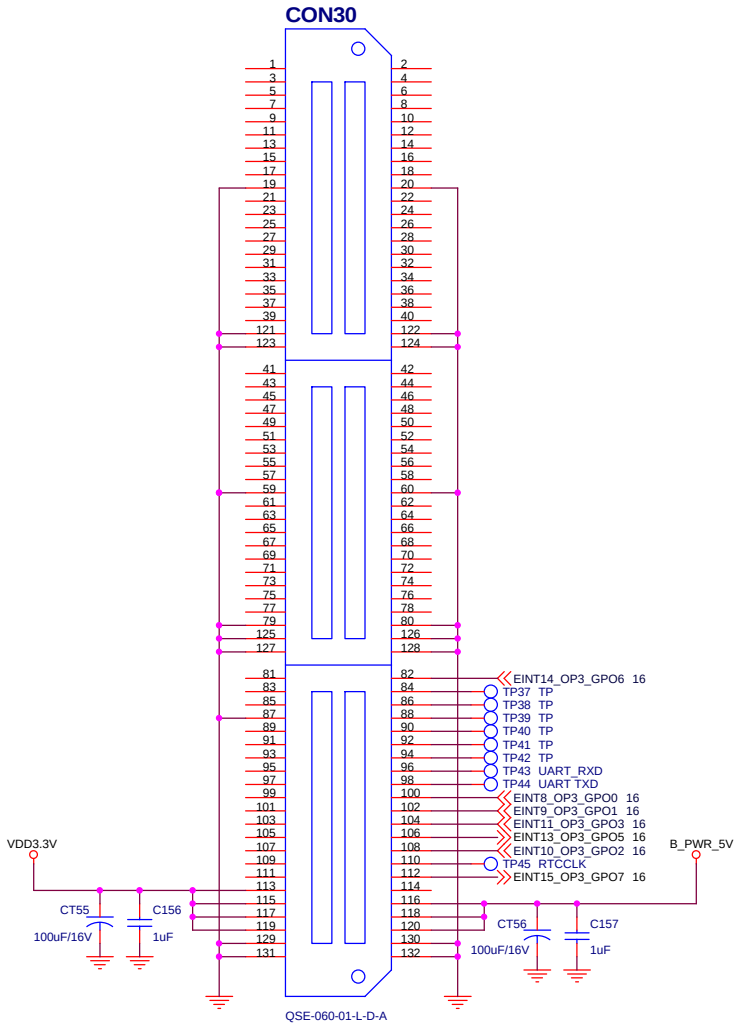

U36
WM8753LGEFL
to test I2S1/PCM0,1
(extraly can test I2S0 2ch)
passive high pass filter
C108~113, 128~130 should be placed
as close as to the codec chip
AP Slave mode
(Codec Master mode)
EPLLRef(12Mhz) -> Codec XTI possible
; but for optimum performance
crystal is recommanded.
C131~134, 140,141 should be placed
as close as to the codec chip
U37
WM8580A
to test I2S0 5.1ch
(extraly can test I2S1 2ch)
IIC slave addr
=0x34(W)/0x35(R)
IIC slave addr
=0x36(W)/0x37(R)
2-Wire Mode
SW mode
SAMSUNG ELECTRONICS CO.,LTD
SMDK2450 (S3C2450 Evaluation Board)
I2S 5.1ch/I2S&PCM
Tuesday, April 08, 2008



COM2 port
CFG3 Control

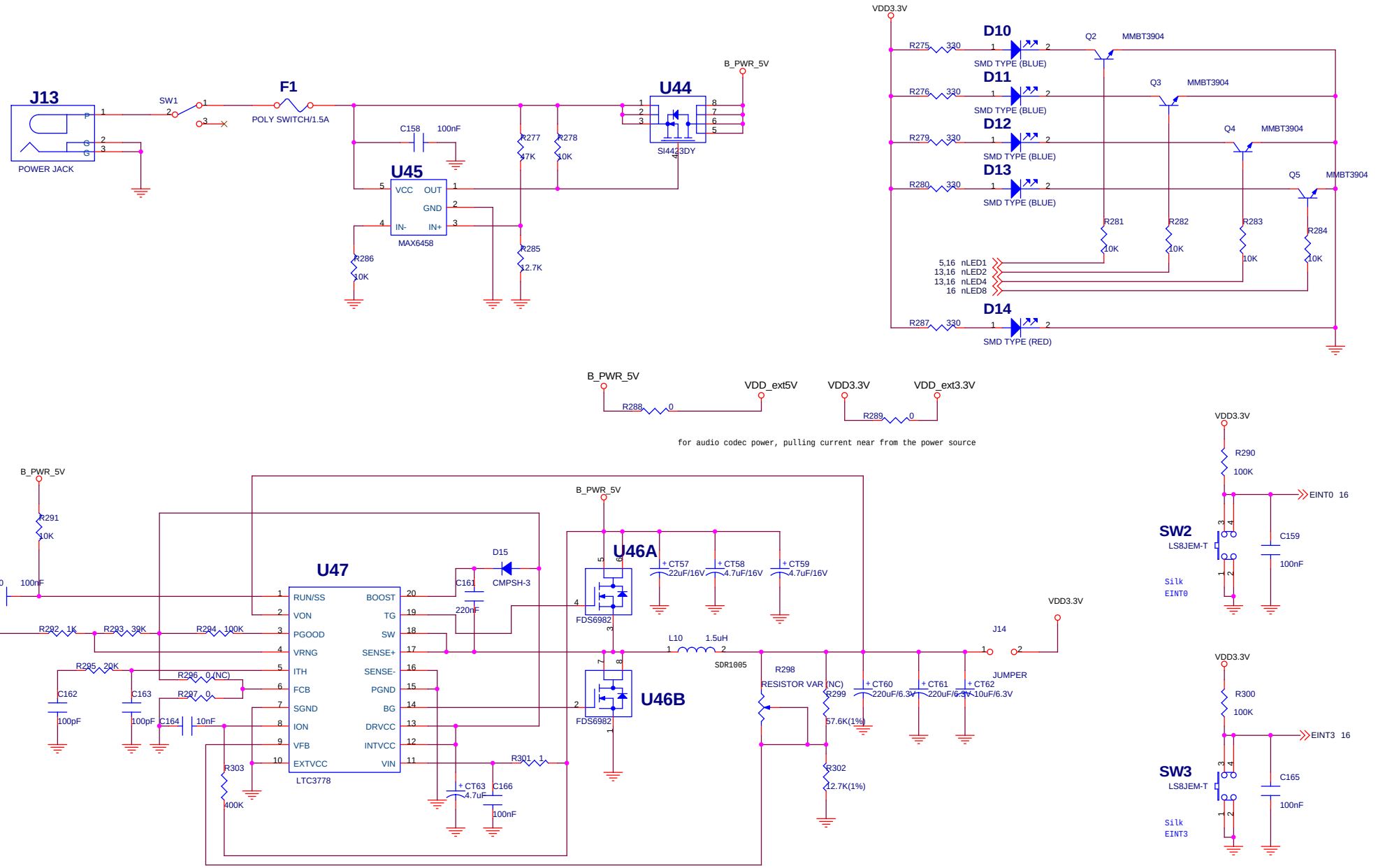
<Silk>

Func(CFG9)	PIN1	PIN2	PIN3
UART1	OFF	X	X
UART2	ON	OFF	OFF
UART3	ON	ON	X
IrDA(U2)	X	ON	ON

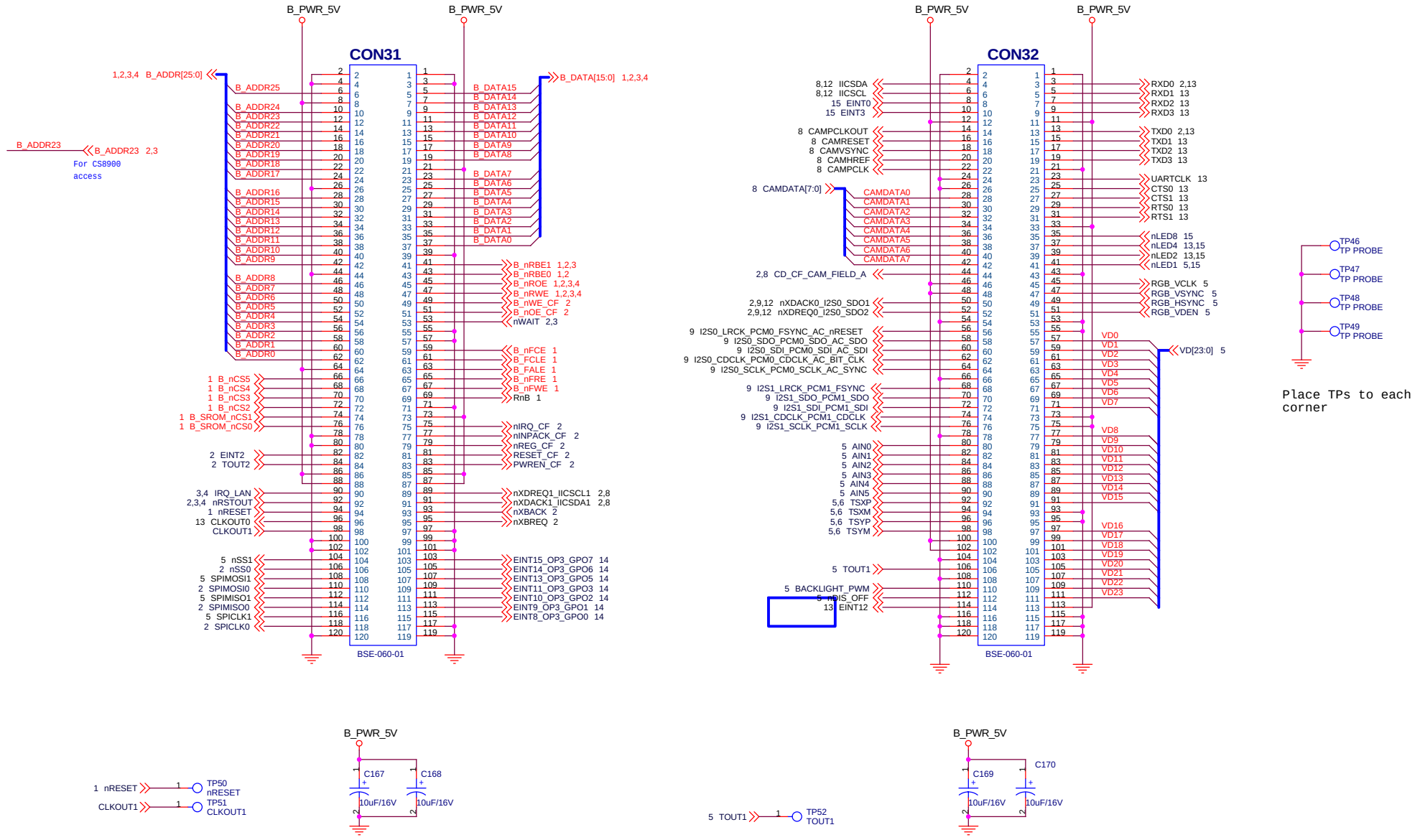


External I/O

SAMSUNG ELECTRONICS CO.,LTD		
Title: SMDK2450 (S3C2450 Evaluation Board)		
Size: A3	Document Number: External I/O	Rev: 0.1
Date: Tuesday, April 08, 2008	Sheet 14 of 16	



SAMSUNG ELECTRONICS CO.,LTD		
Title: SMDK2450 (S3C2450 Evaluation Board)		
Size: A3	Document Number: Base board Power & LED	Rev: 0.1
Date: Tuesday, April 08, 2008	Sheet 15 of 16	



SAMSUNG ELECTRONICS CO.,LTD		
Title: SMDK2450 (S3C2450 Evaluation Board)		
Size: A3	Document Number: Board to Board connector	Rev: 0.1
Date: Tuesday, April 08, 2008	Sheet 16 of 16	