# 7. SPI Core

NII51011-9.0.0

## Core Overview

SPI is an industry-standard serial protocol commonly used in embedded systems to connect microprocessors to a variety of off-chip sensor, conversion, memory, and control devices. The SPI core with Avalon® interface implements the SPI protocol and provides an Avalon Memory-Mapped (Avalon-MM) interface on the back end.

The SPI core can implement either the master or slave protocol. When configured as a master, the SPI core can control up to 32 independent SPI slaves. The width of the receive and transmit registers are configurable between 1 and 32 bits. Longer transfer lengths can be supported with software routines. The SPI core provides an interrupt output that can flag an interrupt whenever a transfer completes.

The SPI core is SOPC Builder ready and integrates easily into any SOPC Builder-generated system. This chapter contains the following sections:



## Functional Description

The SPI core communicates using two data lines, a control line, and a synchronization clock:

- Master Out Slave In (`mosi`)—Output data from the master to the inputs of the slaves
- Master In Slave Out (`miso`)—Output data from a slave to the input of the master
- Serial Clock (`sclk`)—Clock driven by the master to slaves, used to synchronize the data bits
- Slave Select (`ss_n`)— Select signal (active low) driven by the master to individual slaves, used to select the target slave

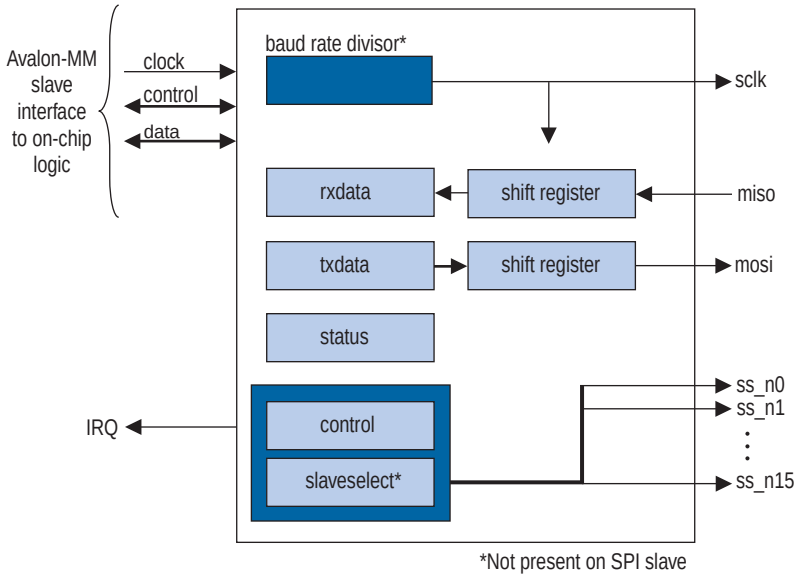
The SPI core has the following user-visible features:

- A memory-mapped register space comprised of five registers: `rxdata`, `txdata`, `status`, `control`, and `slaveselect`
- Four SPI interface ports: `sclk`, `ss_n`, `mosi`, and `miso`

The registers provide an interface to the SPI core and are visible via the Avalon-MM slave port. The `sclk`, `ss_n`, `mosi`, and `miso` ports provide the hardware interface to other SPI devices. The behavior of `sclk`, `ss_n`, `mosi`, and `miso` depends on whether the SPI core is configured as a master or slave.

Figure 7–1 shows a block diagram of the SPI core in master mode.

**Figure 7–1.** SPI Core Block Diagram



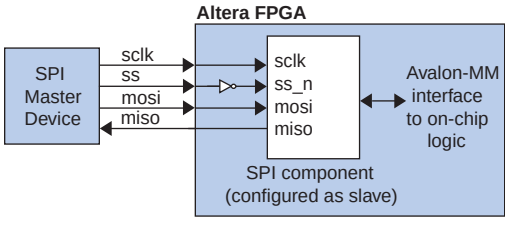

The SPI core logic is synchronous to the clock input provided by the Avalon-MM interface. When configured as a master, the core divides the Avalon-MM clock to generate the SCLK output. When configured as a slave, the core's receive logic is synchronized to SCLK input. The core's Avalon-MM interface is capable of Avalon-MM transfers with flow control. The SPI core can be used in conjunction with a DMA controller with flow control to automate continuous data transfers between, for example, the SPI core and memory.

For more details, refer to the *Interval Timer Core* chapter in volume 5 of the *Quartus II Handbook*.

## Example Configurations

Figure 7–1 and Figure 7–2 show two possible configurations. In Figure 7–2, the SPI core provides a slave interface to an off-chip SPI master.

**Figure 7–2.** SPI Core Configured as a Slave




In Figure 7–1, the SPI core provides a master interface driving multiple off-chip slave devices. Each slave device in Figure 7–1 must tristate its `miso` output whenever its select signal is not asserted.

The ss_n signal is active-low. However, any signal can be inverted inside the FPGA, allowing the slave-select signals to be either active high or active low.

## Transmitter Logic

The SPI core transmitter logic consists of a transmit holding register (txdata) and transmit shift register, each *n* bits wide. The register width *n* is specified at system generation time, and can be any integer value from 1 to 32. After a master peripheral writes a value to the txdata register, the value is copied to the shift register and then transmitted when the next operation starts.

The shift register and the txdata register provide double buffering during data transmission. A new value can be written into the txdata register while the previous data is being shifted out of the shift register. The transmitter logic automatically transfers the txdata register to the shift register whenever a serial shift operation is not currently in process.

In master mode, the transmit shift register directly feeds the mosi output. In slave mode, the transmit shift register directly feeds the miso output. Data shifts out LSB first or MSB first, depending on the configuration of the SPI core.

## Receiver Logic

The SPI core receive logic consists of a receive holding register (rxdata) and receive shift register, each *n* bits wide. The register width *n* is specified at system generation time, and can be any integer value from 1 to 16. A master peripheral reads received data from the rxdata register after the shift register has captured a full *n*-bit value of data.

The shift register and the rxdata register provide double buffering while receiving data. The rxdata register can hold a previously received data value while subsequent new data is shifting into the shift register. The receiver logic automatically transfers the shift register content to the rxdata register when a serial shift operation completes.

In master mode, the shift register is fed directly by the miso input. In slave mode, the shift register is fed directly by the mosi input. The receiver logic expects input data to arrive LSB first or MSB first, depending on the configuration of the SPI core.

## Master and Slave Modes

At system generation time, the designer configures the SPI core in either master mode or slave mode. The mode cannot be switched at runtime.

### Master Mode Operation

In master mode, the SPI ports behave as shown in Table 7–1.

**Table 7–1.** Master Mode Port Configurations (Part 1 of 2)

| Name | Direction | Description |
|---|---|---|
| mosi | output | Data output to slave(s) |
| miso | input | Data input from slave(s) |

**Table 7–1.** Master Mode Port Configurations (Part 2 of 2)

| Name | Direction | Description |
|---|---|---|
| sclk | output | Synchronization clock to all slaves |
| ss_n*M* | output | Slave select signal to slave *M*, where M is a number between 0 and 15. |

In master mode, an intelligent host (for example, a microprocessor) configures the SPI core using the `control` and `slaveselect` registers, and then writes data to the `txdata` buffer to initiate a transaction. A master peripheral can monitor the status of the transaction by reading the `status` register. A master peripheral can enable interrupts to notify the host whenever new data is received (for example, a transfer has completed), or whenever the transmit buffer is ready for new data.

The SPI protocol is full duplex, so every transaction both sends and receives data at the same time. The master transmits a new data bit on the `mosi` output and the slave drives a new data bit on the `miso` input for each active edge of `sclk`. The SPI core divides the Avalon-MM system clock using a clock divider to generate the `sclk` signal.

When the SPI core is configured to interface with multiple slaves, the core has one `ss_n` signal for each slave, up to a maximum of sixteen slaves. During a transfer, the master asserts `ss_n` to each slave specified in the `slaveselect` register. Note that there can be no more than one slave transmitting data during any particular transfer, or else there will be a contention on the `miso` input. The number of slave devices is specified at system generation time.

## Slave Mode Operation

In slave mode, the SPI ports behave as shown in Table 7–2.

**Table 7–2.** Slave Mode Port Configurations

| Name | Direction | Description |
|---|---|---|
| mosi | input | Data input from the master |
| miso | output | Data output to the master |
| sclk | input | Synchronization clock |
| ss_n | input | Select signal |

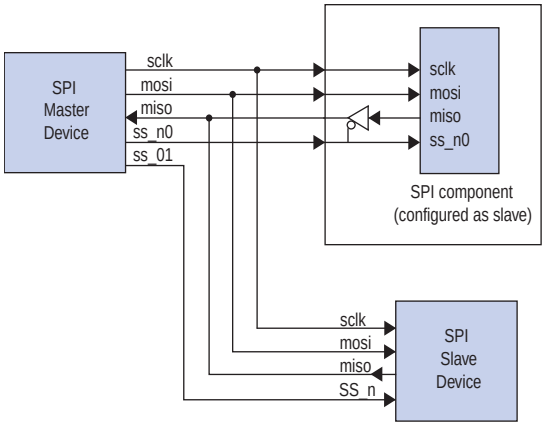
In slave mode, the SPI core simply waits for the master to initiate transactions. Before a transaction begins, the slave logic continuously polls the `ss_n` input. When the master asserts `ss_n`, the slave logic immediately begins sending the transmit shift register contents to the `miso` output. The slave logic also captures data on the `mosi` input, and fills the receive shift register simultaneously.

An intelligent host such as a microprocessor writes data to the `txdata` registers, so that it is transmitted the next time the master initiates an operation. A master peripheral reads received data from the `rxdata` register. A master peripheral can enable interrupts to notify the host whenever new data is received, or whenever the transmit buffer is ready for new data.

### Multi-Slave Environments

When `ss_n` is not asserted, typical SPI cores set their `miso` output pins to high impedance. The Altera®-provided SPI slave core drives an undefined high or low value on its `miso` output when not selected. Special consideration is necessary to avoid signal contention on the `miso` output, if the SPI core in slave mode is connected to an off-chip SPI master device with multiple slaves. In this case, the `ss_n` input should be used to control a tristate buffer on the `miso` signal. Figure 7–3 shows an example of the SPI core in slave mode in an environment with two slaves.

**Figure 7–3.** SPI Core in a Multi-Slave Environment




## Avalon-MM Interface

The SPI core's Avalon-MM interface consists of a single Avalon-MM slave port. In addition to fundamental slave read and write transfers, the SPI core supports Avalon-MM read and write transfers with flow control.

# Instantiating the SPI Core in SOPC Builder

You can use the MegaWizard™ interface for the SPI core in SOPC Builder to configure the hardware feature set. The following sections describe the available options.

## Master/Slave Settings

The designer can select either master mode or slave mode to determine the role of the SPI core. When master mode is selected, the following options are available: **Number of select (SS_n) signals, SPI clock rate**, and **Specify delay**.

### Number of Select (SS_n) Signals

This setting specifies how many slaves the SPI master connects to. The range is 1 to 32. The SPI master core presents a unique `ss_n` signal for each slave.

### SPI Clock (sclk) Rate

This setting determines the rate of the `sclk` signal that synchronizes data between master and slaves. The target clock rate can be specified in units of Hz, kHz or MHz. The SPI master core uses the Avalon-MM system clock and a clock divisor to generate `sclk`.

The actual frequency of sclk may not exactly match the desired target clock rate. The achievable clock values are:

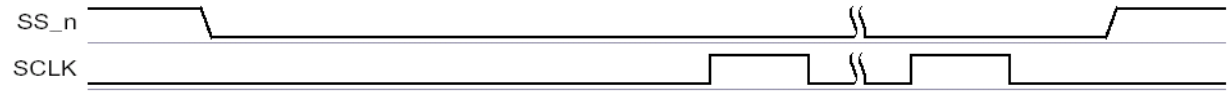
*<Avalon-MM system clock frequency>* / [2, 4, 6, 8, ...]

The actual frequency achieved will not be greater than the specified target value. For example, if the system clock frequency is 50 MHz and the target value is 25 MHz, the clock divisor is 2 and the actual sclk frequency achieves exactly 25 MHz.

### Specify Delay

Turning on this option causes the SPI master to add a time delay between asserting the ss_n signal and shifting the first bit of data. This delay is required by certain SPI slave devices. If the delay option is on, you must also specify the delay time in units of ns, µs or ms. An example is shown in Figure 7–4.

**Figure 7–4.** Time Delay Between Asserting ss_n and Toggling sclk




The delay generation logic uses a granularity of half the period of sclk. The actual delay achieved is the desired target delay rounded up to the nearest multiple of half the sclk period, as shown in Equation 7–1 and Equation 7–2:

**Equation 7–1.**

$$p = \frac{1}{2} \times (\text{period of sclk})$$

**Equation 7–2.**

$$\text{actual delay} = \text{ceiling} \times \left( \frac{\text{desired delay}}{p} \right) \times p$$

## Data Register Settings

The data register settings affect the size and behavior of the data registers in the SPI core. There are two data register settings:

- **Width**—This setting specifies the width of rxdata, txdata, and the receive and transmit shift registers. The range is from 1 to 32.
- **Shift direction**—This setting determines the direction that data shifts (MSB first or LSB first) into and out of the shift registers.

## Timing Settings

The timing settings affect the timing relationship between the `ss_n`, `sclk`, `mosi` and `miso` signals. In this discussion the `mosi` and `miso` signals are referred to generically as *data*. There are two timing settings:

- **Clock polarity**—This setting can be 0 or 1. When clock polarity is set to 0, the idle state for `sclk` is low. When clock polarity is set to 1, the idle state for `sclk` is high.
- **Clock phase**—This setting can be 0 or 1. When clock phase is 0, data is latched on the leading edge of `sclk`, and data changes on trailing edge. When clock phase is 1, data is latched on the trailing edge of `sclk`, and data changes on the leading edge.

Figure 7–5 through Figure 7–8 demonstrate the behavior of signals in all possible cases of clock polarity and clock phase.

**Figure 7–5.** Clock Polarity = 0, Clock Phase = 0

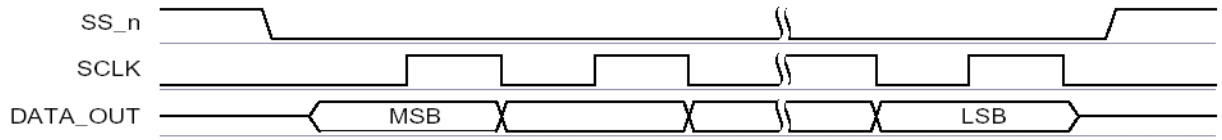



**Figure 7–6.** Clock Polarity = 0, Clock Phase = 1

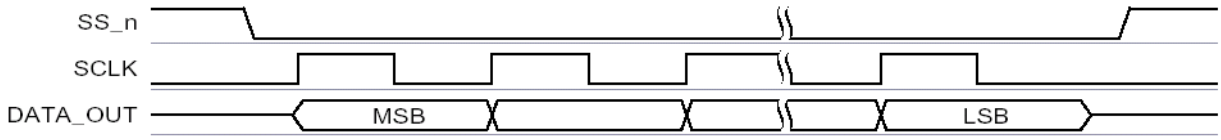



**Figure 7–7.** Clock Polarity = 1, Clock Phase = 0

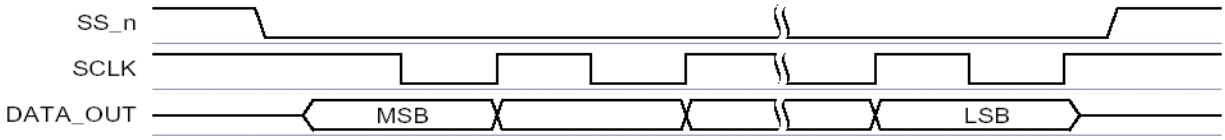
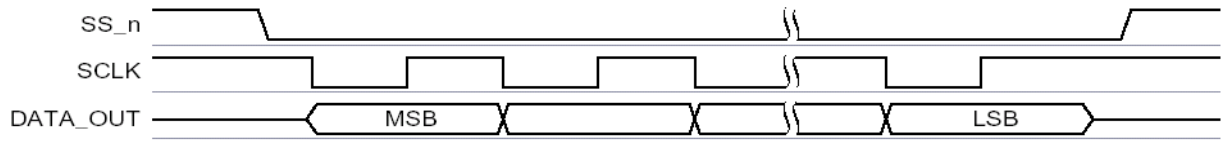



**Figure 7–8.** Clock Polarity = 1, Clock Phase = 1



# Device Support

The SPI core supports all Altera® device families.

# Software Programming Model

The following sections describe the software programming model for the SPI core, including the register map and software constructs used to access the hardware. For Nios® II processor users, Altera provides the HAL system library header file that defines the SPI core registers. The SPI core does not match the generic device model categories supported by the HAL, so it cannot be accessed via the HAL API or the ANSI C standard library. Altera provides a routine to access the SPI hardware that is specific to the SPI core.

## Hardware Access Routines

Altera provides one access routine, `alt_avalon_spi_command()`, that provides general-purpose access to an SPI core configured as a master.

## alt_avalon_spi_command()

| | |
|---|---|
| Prototype: | `int alt_avalon_spi_command(alt_u32 base, alt_u32 slave, alt_u32 write_length, const alt_u8* wdata, alt_u32 read_length, alt_u8* read_data, alt_u32 flags)` |
| Thread-safe: | No. |
| Available from ISR: | No. |
| Include: | <altera_avalon_spi.h> |
| Description: | `alt_avalon_spi_command()` is used to perform a control sequence on the SPI bus. This routine is designed for SPI masters of 8-bit data width or less. Currently, it does not support SPI hardware with data-width greater than 8 bits. A single call to this function writes a data buffer of arbitrary length out the MOSI port, and then reads back an arbitrary amount of data from the MISO port. The function performs the following actions:<br>(1) Asserts the slave select output for the specified slave. The first slave select output is numbered 0, the next is 1, etc.<br>(2) Transmits `write_length` bytes of data from `wdata` through the SPI interface, discarding the incoming data on MISO.<br>(3) Reads `read_length` bytes of data, storing the data into the buffer pointed to by `read_data`. MOSI is set to zero during the read transaction.<br>(4) De-asserts the slave select output, unless the flags field contains the value `ALT_AVALON_SPI_COMMAND_MERGE`. If you want to transmit from scattered buffers then you can call the function multiple times, specifying the merge flag on all the accesses except the last.<br>This function is not thread safe. If you want to access the SPI bus from more than one thread, you should use a semaphore or mutex to ensure that only one thread is executing within this function at any time. |
| Returns: | The number of bytes stored in the `read_data` buffer. |

## Software Files

The SPI core is accompanied by the following software files. These files provide a low-level interface to the hardware.

- **altera_avalon_spi.h**—This file defines the core's register map, providing symbolic constants to access the low-level hardware.
- **altera_avalon_spi.c**—This file implements low-level routines to access the hardware.

## Register Map

An Avalon-MM master peripheral controls and communicates with the SPI core via the six 32-bit registers, shown in Table 7–3. The table assumes an *n*-bit data width for `rxdata` and `txdata`.

**Table 7–3.** Register Map for SPI Master Device

| Internal Address | Register Name | 32..11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | rxdata *(1)* | RXDATA (n-1..0) | | | | | | | | | | | |
| 1 | txdata *(1)* | TXDATA (n-1..0) | | | | | | | | | | | |
| 2 | status *(2)* | | | | E | RRDY | TRDY | TMT | TOE | ROE | | | |
| 3 | control | | SSO *(3)* | | IE | IRRDY | ITRDY | | ITOE | IROE | | | |
| 4 | Reserved | | | | | | | | | | | | |
| 5 | slaveselect *(3)* | Slave Select Mask | | | | | | | | | | | |

**Notes to Table 7–3:**

(1) Bits 15 to *n* are undefined when *n* is less than 16.

(2) A write operation to the status register clears the ROE, TOE, and E bits.

(3) Present only in master mode.

Reading undefined bits returns an undefined value. Writing to undefined bits has no effect.

### rxdata Register

A master peripheral reads received data from the rxdata register. When the receive shift register receives a full *n* bits of data, the status register's RRDY bit is set to 1 and the data is transferred into the rxdata register. Reading the rxdata register clears the RRDY bit. Writing to the rxdata register has no effect.

New data is always transferred into the rxdata register, whether or not the previous data was retrieved. If RRDY is 1 when data is transferred into the rxdata register (that is, the previous data was not retrieved), a receive-overrun error occurs and the status register's ROE bit is set to 1. In this case, the contents of rxdata are undefined.

### txdata Register

A master peripheral writes data to be transmitted into the txdata register. When the status register's TRDY bit is 1, it indicates that the txdata register is ready for new data. The TRDY bit is set to 0 whenever the txdata register is written. The TRDY bit is set to 1 after data is transferred from the txdata register into the transmitter shift register, which readies the txdata holding register to receive new data.

A master peripheral should not write to the txdata register until the transmitter is ready for new data. If TRDY is 0 and a master peripheral writes new data to the txdata register, a transmit-overrun error occurs and the status register's TOE bit is set to 1. In this case, the new data is ignored, and the content of txdata remains unchanged.

As an example, assume that the SPI core is idle (that is, the txdata register and transmit shift register are empty), when a CPU writes a data value into the txdata holding register. The TRDY bit is set to 0 momentarily, but after the data in txdata is transferred into the transmitter shift register, TRDY returns to 1. The CPU writes a second data value into the txdata register, and again the TRDY bit is set to 0. This time the shift register is still busy transferring the original data value, so the TRDY bit remains at 0 until the shift operation completes. When the operation completes, the second data value is transferred into the transmitter shift register and the TRDY bit is again set to 1.

### status Register

The status register consists of bits that indicate status conditions in the SPI core. Each bit is associated with a corresponding interrupt-enable bit in the control register, as discussed in "control Register" on page 7–12. A master peripheral can read status at any time without changing the value of any bits. Writing status does clear the ROE, TOE and E bits. Table 7–4 describes the individual bits of the status register.

**Table 7–4.** status Register Bits

| # | Name | Description |
|---|---|---|
| 3 | ROE | **Receive-overrun error**<br>The ROE bit is set to 1 if new data is received while the rxdata register is full (that is, while the RRDY bit is 1). In this case, the new data overwrites the old. Writing to the status register clears the ROE bit to 0. |
| 4 | TOE | **Transmitter-overrun error**<br>The TOE bit is set to 1 if new data is written to the txdata register while it is still full (that is, while the TRDY bit is 0). In this case, the new data is ignored. Writing to the status register clears the TOE bit to 0. |
| 5 | TMT | **Transmitter shift-register empty**<br>In master mode, the TMT bit is set to 0 when a transaction is in progress and set to 1 when the shift register is empty.<br>In slave mode, the TMT bit is set to 0 when the slave is selected (SS_n is low) or when the SPI Slave register interface is not ready to receive data. |
| 6 | TRDY | **Transmitter ready**<br>The TRDY bit is set to 1 when the txdata register is empty. |
| 7 | RRDY | **Receiver ready**<br>The RRDY bit is set to 1 when the rxdata register is full. |
| 8 | E | **Error**<br>The E bit is the logical OR of the TOE and ROE bits. This is a convenience for the programmer to detect error conditions. Writing to the status register clears the E bit to 0. |

# control Register

The `control` register consists of data bits to control the SPI core's operation. A master peripheral can read `control` at any time without changing the value of any bits.

Most bits (`IROE`, `ITOE`, `ITRDY`, `IRRDY`, and `IE`) in the `control` register control interrupts for status conditions represented in the `status` register. For example, bit 1 of `status` is `ROE` (receiver-overrun error), and bit 1 of control is `IROE`, which enables interrupts for the `ROE` condition. The SPI core asserts an interrupt request when the corresponding bits in `status` and `control` are both 1.

The `control` register bits are shown in Table 7–5.

**Table 7–5.** control Register Bits

| # | Name | Description |
|---|---|---|
| 3 | IROE | Setting IROE to 1 enables interrupts for receive-overrun errors. |
| 4 | ITOE | Setting ITOE to 1 enables interrupts for transmitter-overrun errors. |
| 6 | ITRDY | Setting ITRDY to 1 enables interrupts for the transmitter ready condition. |
| 7 | IRRDY | Setting IRRDY to 1 enables interrupts for the receiver ready condition. |
| 8 | IE | Setting IE to 1 enables interrupts for any error condition. |
| 10 | SSO | Setting SSO to 1 forces the SPI core to drive its ss_n outputs, regardless of whether a serial shift operation is in progress or not. The slaveselect register controls which ss_n outputs are asserted. SSO can be used to transmit or receive data of arbitrary size, for example, greater than 32 bits. |

After reset, all bits of the `control` register are set to 0. All interrupts are disabled and no `ss_n` signals are asserted.

### slaveselect Register

The `slaveselect` register is a bit mask for the `ss_n` signals driven by an SPI master. During a serial shift operation, the SPI master selects only the slave device(s) specified in the `slaveselect` register.

The `slaveselect` register is only present when the SPI core is configured in master mode. There is one bit in `slaveselect` for each `ss_n` output, as specified by the designer at system generation time.

A master peripheral can set multiple bits of `slaveselect` simultaneously, causing the SPI master to simultaneously select multiple slave devices as it performs a transaction. For example, to enable communication with slave devices 1, 5, and 6, set bits 1, 5, and 6 of `slaveselect`. However, consideration is necessary to avoid signal contention between multiple slaves on their `miso` outputs.

Upon reset, bit 0 is set to 1, and all other bits are cleared to 0. Thus, after a device reset, slave device 0 is automatically selected.

# Referenced Documents

This chapter references the following documents:

- *AN 350: Upgrading Nios Processor Systems to the Nios II Processor*
- *Interval Timer Core* chapter in volume 5 of the *Quartus II Handbook*

# Document Revision History

Table 7–6 shows the revision history for this chapter.

**Table 7–6.** Document Revision History

| Date and Document Version | Changes Made | Summary of Changes |
|---|---|---|
| March 2009<br>v9.0.0 | No change from previous release. | — |
| November 2008<br>v8.1.0 | Changed to 8-1/2 x 11 page size. Updated the width of the parameters and signals from 16 to 32. | — |
| May 2008<br>v8.0.0 | Updated the description of the TMT bit. | Updates made to comply with the Quartus II software version 8.0 release. |

For previous versions of the *Quartus II Handbook*, refer to the Quartus II Handbook Archive.