Setting up the MMA7660FC for Orientation, Shake, Auto-Wake/Sleep and Tap Detection

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ACRONYMS

PMP: Portable Media Player
PDA: Personal Digital Assistant
INT: Interrupt
TILT: MMA7660FC Internal register 0x03: Tilt Status
SR: MMA7660FC Internal register 0x08: Sample rate register, Auto-Wake and Active Mode Portrait/Landscape Samples per Seconds Register
INTSU: MMA7660FC Internal register 0x06: Interrupt Setup Register
ODR: Output Data Rate
Auto-Wake: Sleep state
Auto-Sleep: Wake state

ABSTRACT

The MMA7660FC is a ±1.5 g 3-Axis Accelerometer with Digital Output (I^2C). It is a very low power, low profile capacitive MEMS sensor featuring a low pass filter, compensation for 0g offset and gain errors, and conversion to 6-bit digital values at a user configurable sample rate. The device can be used for sensor data changes, product orientation, shake detection, tap detection, and gesture detection through an interrupt pin (INT). This application note will describe how to set up the MMA7660FC registers for orientation, shake, auto-wake/sleep and tap detection.

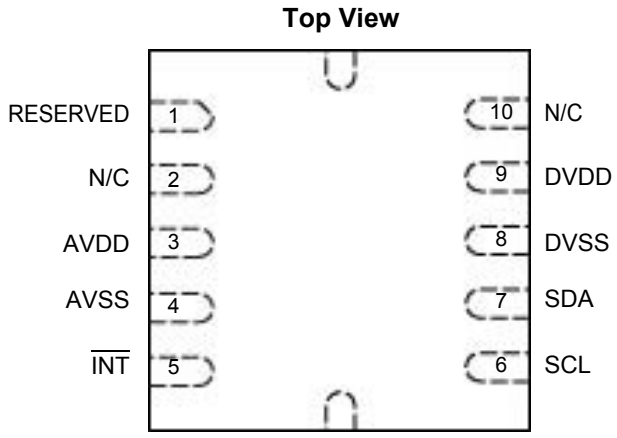
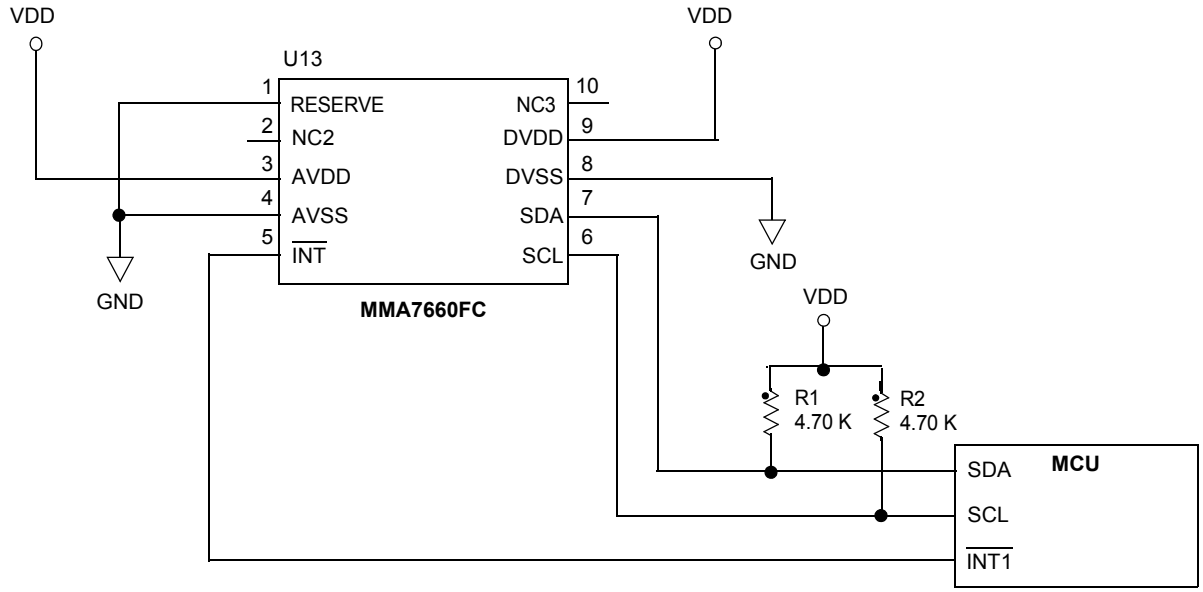


Figure 1. Pinout

Table 1. Pin Description

Pin #	Pin Name	Description	Pin Status
1	RESERVED	Connect to AVSS	Input
2	N/C	No Internal Connection, leave unconnected or connect to Ground	Input
3	AVDD	Device Power	Input
4	AVSS	Device Ground	Input
5	INT	Interrupt/Data Ready	Output
6	SCL	I^2C Serial Clock	Input
7	SDA	I^2C Serial Data	Open Drain
8	DVSS	Digital I/O Ground	Input
9	DVDD	Digital I/O Power	Input
10	N/C	No Internal Connection, recommended to connect to Ground	Input



NOTE: A 10 μF ceramic capacitor can be placed connecting pin 3 (AVDD) to pin 4 (AVSS). In addition, another 10 μF ceramic capacitor can be place connecting pin 9 (DVDD) to pin 8 (DVSS). The capacitors should be placed close to the pins of the MMA7660FC and is recommended for testing and to adequately decouple the accelerometer from noise on the power supply.

Figure 2. I^2C Connection to MCU

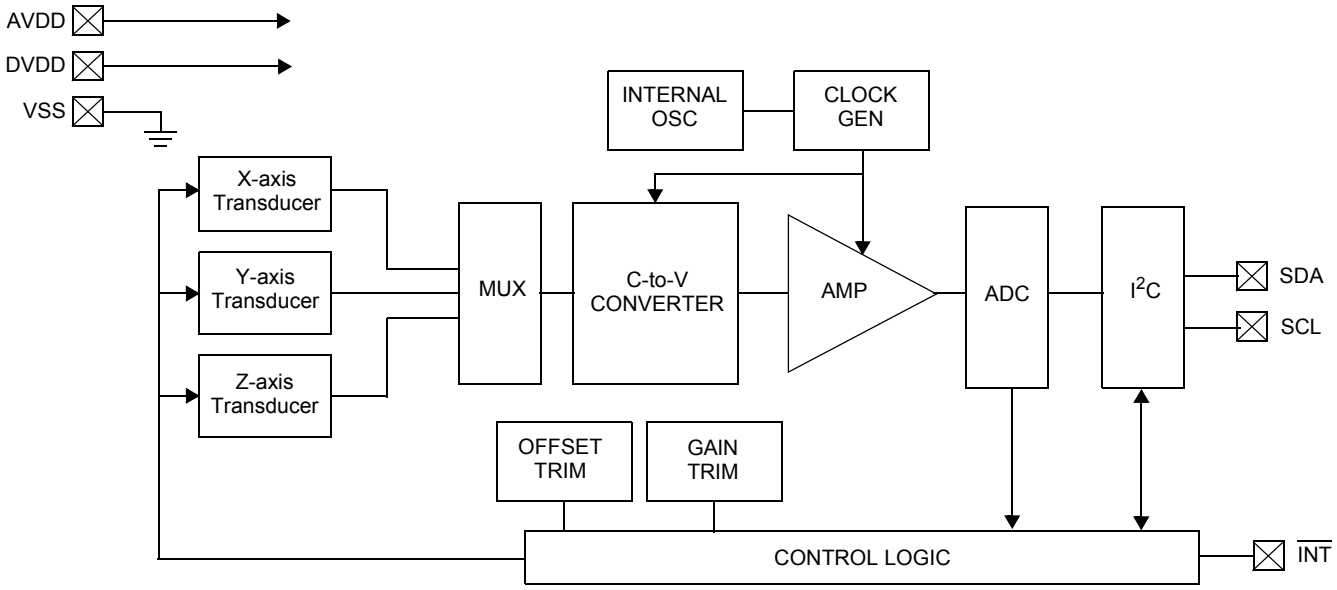


Figure 3. Simplified Accelerometer Functional Block Diagram

REGISTER OVERVIEW

The following are the registers that will be used and/or configured for orientation, shake, auto-wake/sleep and tap detection.

Address	Name	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x00	XOUT	6 bits output value X	-	Alert	XOUT[5]	XOUT[4]	XOUT[3]	XOUT[2]	XOUT[1]	XOUT[0]
0x01	YOUT	6 bits output value Y	-	Alert	YOUT[5]	YOUT[4]	YOUT[3]	YOUT[2]	YOUT[1]	YOUT[0]
0x02	ZOUT	6 bits output value Z	-	Alert	ZOUT[5]	ZOUT[4]	ZOUT[3]	ZOUT[2]	ZOUT[1]	ZOUT[0]
0x03	TILT	Tilt Status	Shake	Alert	Tap	PoLa[2]	PoLa[1]	PoLa[0]	BaFro[1]	BaFro[0]
0x04	SRST	Sampling Rate Status	0	0	0	0	0	0	AWSRS	AMSRS
0x05	SPCNT	Sleep Count	SC[7]	SC[6]	SC[5]	SC[4]	SC[3]	SC[2]	SC[1]	SC[0]
0x06	INTSU	Interrupt Setup	SHINTX	SHINTY	SHINTZ	GINT	ASINT	PDINT	PLINT	FBINT
0x07	MODE	Mode	IAH	IPP	SCPS	ASE	AWE	TON	-	MODE
0x08	SR	Auto-Sleep and Active Mode Portrait/Landscape Sample Rates and Debounce Filter	FILT[2]	FILT[1]	FILT[0]	AWSR [1]	AWSR [0]	AMSR [2]	AMSR [1]	AMSR [0]
0x09	PDET	Tap Detection	ZDA	YDA	XDA	PDTH[4]	PDTH[3]	PDTH[2]	PDTH[1]	PDTH[0]
0x0A	PD	Tap Debounce Count	PD[7]	PD[6]	PD[5]	PD[4]	PD[3]	PD[2]	PD[1]	PD[0]
0x0B to 0x1F	Factory	Reserved	-	-	-	-	-	-	-	-

REGISTER DEFINITIONS

0x00: XOUT: 6 bits Output Value X

D7	D6	D5	D4	D3	D2	D1	D0
—	Alert	XOUT[5]	XOUT[4]	XOUT[3]	XOUT[2]	XOUT[1]	XOUT[0]
0	0	0	0	0	0	0	0

Signed byte 6 bit 2's complement data with allowable range of +31 to -32

XOUT[5] is 0 if the g direction is positive, 1 if the g direction is negative.

If the Alert bit is set, the register was read at the same time as the device was attempting to update the contents. The register must be read again.

0x01: YOUT: 6 bits Output Value Y

D7	D6	D5	D4	D3	D2	D1	D0
—	Alert	YOUT[5]	YOUT[4]	YOUT[3]	YOUT[2]	YOUT[1]	YOUT[0]
0	0	0	0	0	0	0	0

Signed byte 6 bit 2's complement data with allowable range of +31 to -32.

YOUT[5] is 0 if the g direction is positive, 1 if the g direction is negative.

If the Alert bit is set, the register was read at the same time as the device was attempting to update the contents. The register must be read again.

0x02: ZOUT: 6 bits Output Value Z

D7	D6	D5	D4	D3	D2	D1	D0
—	Alert	ZOUT[5]	ZOUT[4]	ZOUT[3]	ZOUT[2]	ZOUT[1]	ZOUT[0]
0	0	0	0	0	0	0	0

Signed byte 6 bit 2's complement data with allowable range of +31 to -32.

ZOUT[5] is 0 if the g direction is positive, 1 if the g direction is negative.

If the Alert bit is set, the register was read at the same time as the device was attempting to update the contents. The register must be read again.

0x03: TILT: Tilt Status (Read only)

D7	D6	D5	D4	D3	D2	D1	D0
Shake	Alert	Tap	PoLa[2]	PoLa[1]	PoLa[0]	BaFro[1]	BaFro[0]
0	0	0	0	0	0	0	0

BaFro[1:0]
00:Unknown condition of front or back
01:Front:Equipment is lying on its front
10:Back:Equipment is lying on its back

PoLa[2:0]
000:Unknown condition of up or down or left or right
001:Left:Equipment standing vertically in normal orientation (any markings are the right way up)
010:Right:Equipment standing vertically in inverted orientation (any markings are the wrong way up)
101:Down:Equipment is in landscape mode to the right
110:Up:Equipment is in landscape mode to the left

Tap
0:Equipment has detected a tap
1:Equipment has not detected a tap

Alert
0:Register data is valid
1:The register was read at the same time as MMA7660FC was attempting to update the contents. Re-read the register

Shake
0:Equipment is not experiencing shaking in one or more of the axes enabled by SHINTX, SHINTY, and SHINTZ
1:Equipment is experiencing shake in one or more of the axes enabled by SHINTX, SHINTY, and SHINTZ

0x04: SRST: Sampling Rate Status (Read Only)

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	AWSRS	AWSRS
0	0	0	0	0	0	0	0

AMSRS

0:Sample rate specified in AMSR[2:0] is not active
1:Sample rate specified in AMSR[2:0] is active

AWSRS

0:Sample rate specified in AWSR[1:0] is not active
1:Sample rate specified in AWSR[1:0] is active

0x05: SPCNT: Sleep Count Register (Read/Write)

D7	D6	D5	D4	D3	D2	D1	D0
SC[7]	SC[6]	SC[5]	SC[4]	SC[3]	SC[2]	SC[1]	SC[0]
0	0	0	0	0	0	0	0

Writing Sleep Count register resets the internal sleep counter

SC[7:0]

8 bit maximum count value for the 8 bit internal sleep counter in Auto-Sleep. When the 8 bit internal sleep counter reaches value set by SC[7:0], MMA7660FC will exit Auto-Sleep and switch to the sample rate specified in AWSR[1:0] of the SR register.

0x06: INTSU: Interrupt Setup

D7	D6	D5	D4	D3	D2	D1	D0
SHINT X	SHINT Y	SHINT Z	GINT	ASINT	PDINT	PLINT	FBINT
0	0	0	0	0	0	0	0

FBINT

0:Front/Back position change does not cause an interrupt
1:Front/Back position change (Front bit toggling or Back bit toggling) causes an interrupt

PLINT

0:Up/Down/Right/Left position change does not cause an interrupt
1:Up/Down/Right/Left position change (Up bit toggling or Down bit toggling) causes an interrupt

ASINT

0:Exiting Auto-Sleep does not cause an interrupt
1:Exiting Auto-Sleep causes an interrupt

PDINT

0:Successful tap detection does not cause an interrupt
1:Successful tap detection causes an interrupt

GINT

0:There is not an automatic interrupt after every measurement
1:There is an automatic interrupt after every measurement, when G-cell readings are updated in XOUT, YOUT, ZOUT registers, regardless of whether the readings have changed or not. This interrupt does not affect the Auto-Sleep or Auto-Wake functions.

SHINTX

0:Shake on the X axis does not cause an interrupt or set the Shake bit in the TILT register
1:Shake detected on the X axis causes an interrupt, and sets the Shake bit in the TILT register

SHINTY

0:Shake on the Y axis does not cause an interrupt or set the Shake bit in the TILT register
1:Shake detected on the Y axis causes an interrupt, and sets the Shake bit in the TILT register

SHINTZ

0:Shake on the Z axis does not cause an interrupt or set the Shake bit in the TILT register
1:Shake detected on the Z axis causes an interrupt, and sets the Shake bit in the TILT register

The active interrupt condition (IRQ = 0 if IAH = 0, IRQ = 1 if IAH = 1) is released during the acknowledge bit of the slave address transmission of the first subsequent I^2C to MMA7660FC after the interrupt was asserted.

0x07: MODE: Mode Register (Read/Write)

D7	D6	D5	D4	D3	D2	D1	D0
IAH	IPP	SCPS	ASE	AWE	TON	—	MODE
0	0	0	0	0	0	0	0

When [TON,MODE] = [0,1], MMA7660FC will only allow write access to the Mode register 0x07.
Writing Mode register resets sleep timing, and clears the XOUT, YOUT, ZOUT, TILT registers.
Reading Mode register resets sleep timing.

MODE
0: Standby mode or Test Mode depending on state of TON
1: Active mode
Existing state of TON bit must be 0 (MMA7660FC must not be in Test Mode) to write MODE = 1
MMA7660FC always enters Active Mode using the sample rate specified in AMSR[2:0] of the SR register.
When MMA7660FC enters Active Mode with [ASE:AWE] = 11, MMA7660FC operates Auto-Sleep functionality first.

TON
0:Standby Mode or Active Mode depending on state of MODE
1:Test Mode
Existing state of MODE bit must be 0 (MMA7660FC must be in Standby Mode) to write TON = 1

AWE
0:Auto-Wake is disabled
1:Auto-Wake is enabled.
When Auto-Wake functionality is operating, the AWSRS bit is the SRST register is set and MMA7660FC uses the sample rate specified in AWSR[1:0] of the SR register.
When MMA7660FC automatically exits Auto-Wake by a selected interrupt, MMA7660FC will then switch to the sample rate specified in AMSR[2:0] of the SR register. If ASE = 1, then Auto-Sleep functionality is now enabled.

ASE
0:Auto-Sleep is disabled
1:Auto-Sleep is enabled
When Auto-Sleep functionality is operating, the AMSRS bit is the SRST register is set and MMA7660FC uses the sample rate specified in AMSR[2:0] of the SR register.
When MMA7660FC automatically exits Auto-Sleep because the Sleep Counter times out, MMA7660FC will then switch to the sample rate specified in AWSR[1:0] of the SR register. If AWE = 1, the Auto-Wake functionality is now enabled.

SCPS
0:Prescaler is divide-by-1. The 8 bit internal Sleep Counter input clock is the sample rate set by AMSR[2:0], so the clock range is 64Hz to 1Hz depending on AMSR[2:0] setting. Sleep Counter time-out range is 256 times the prescaled clock (Table 2.)
1:Prescaler is divide-by-16. The 8 bit Sleep Counter input clock is the sample rate set by AMSR[2:0] divided by 16, so the clock range is 4Hz to 1/16Hz depending on AMSR[2:0] setting. Sleep Counter time-out range is 256 times the prescaled clock (Table 2.).

IPP
0:Interrupt output INT is open-drain. **Note:** do not connect pull-up resistor from INT to higher voltage than DVDD
1:Interrupt output INT is push-pull

IAH
0:Interrupt output INT is active low
1:Interrupt output INT is active high
The active interrupt condition (IRQ = 0 if IAH = 0, IRQ = 1 if IAH = 1) is released during the acknowledge bit of the slave address transmission of the first subsequent I^2C MMA7660FC after the interrupt was asserted.

Table 2. Sleep Counter Timeout Ranges

AMSR	SCPS = 0		SCPS = 1	
	Minimum Range (2^0)	Maximum Range (2^8)	Minimum Range (2^0)	Maximum Range (2^8)
1 SPS	1 s	256 s	16 s	4096 s
2 SPS	0.5 s	128 s	8 s	2048 s
4 SPS	0.25 s	34 s	4 s	1024 s
8 SPS	0.125 s	32 s	2 s	512 s
16 SPS	0.625 s	16 s	1 s	256 s
32 SPS	0.03125 s	8 s	0.5 s	128 s
64 SPS	0.0156 s	4 s	0.25 s	64 s
120 SPS	0.00836 s	2.14 s	0.133 s	34.24 s

0x08: SR: Auto-Wake and Active Mode Portrait/Landscape Sample Rates Register (Read/Write)

D7	D6	D5	D4	D3	D2	D1	D0
FILT[2]	FILT[1]	FILT[0]	AWSR[1]	AWSR[0]	AMSR[2]	AMSR[1]	AMSR[0]
0	0	0	0	0	0	0	1

AMSR[2:0]	NAME	DESCRIPTION
000	AMPD	Tap Detection Mode and 120 Samples/Second Active and Auto-Sleep Mode **Tap Detection Sampling Rate**: The device takes readings continually at a rate of nominally 3846 g-cell measurements a second. It then filters these high speed measurements by maintaining continuous rolling averages of the current and last g-cell measurements. The averages are updated every 260 µs to track fast moving accelerations. Tap detection: Compares the two filtered axis responses (fast and slow) described above for each axis. The absolute (unsigned) difference between the fast and slow axis responses is compared against the tap detection delta threshold value PDTH[4:0] in the PDET (0x09) register. **For portrait/landscape detection:** The device takes and averages 32 g-cell measurements every 8.36 ms in Active Mode and Auto-Sleep. The update rate is 120 samples per second. These measurements update the XOUT (0x00), YOUT (0x01), and ZOUT (0x02) registers also.
001	AM64	64 Samples/Second Active and Auto-Sleep Mode **For portrait/landscape detection**: The device takes and averages 32 g-cell measurements every 15.625 ms in Active Mode and Auto-Sleep. The update rate is 64 samples per second. These measurements update the XOUT (0x00), YOUT (0x01), and ZOUT (0x02) registers also.
010	AM32	32 Samples/Second Active and Auto-Sleep Mode **For portrait/landscape detection:** The device takes and averages 32 g-cell measurements every 31.25 ms in Active Mode and Auto-Sleep. The update rate is 32 samples per second. These measurements update XOUT (0x00), YOUT (0x01), and ZOUT (0x02) registers also.
011	AM16	16 Samples/Second Active and Auto-Sleep Mode **For portrait/landscape detection:** The device takes and averages 32 g-cell measurements every 62.5 ms in Active Mode and Auto-Sleep. The update rate is 16 samples per second. These measurements update the XOUT (0x00), YOUT (0x01), and ZOUT (0x02) registers also.
100	AM8	8 Samples/Second Active and Auto-Sleep Mode **For portrait/landscape detection:** The device takes and averages 32 g-cell measurements every 125 ms in Active Mode and Auto-Sleep. The update rate is 8 samples per second. These measurements update the XOUT (0x00), YOUT (0x01), and ZOUT (0x02) registers also.
101	AM4	4 Samples/Second Active and Auto-Sleep Mode **For portrait/landscape detection:** The device takes and averages 32 g-cell measurements every 250 ms in Active Mode and Auto-Sleep. The update rate is 4 samples per second. These measurements update the XOUT (0x00), YOUT (0x01), and ZOUT (0x02) registers also.
110	AM2	2 Samples/Second Active and Auto-Sleep Mode **For portrait/landscape detection:** The device takes and averages 32 g-cell measurements every 500 ms in Active Mode and Auto-Sleep. The update rate is 2 samples per second. These measurements update the XOUT (0x00), YOUT (0x01), and ZOUT (0x02) registers also.
111	AM1	1 Sample/Second Active and Auto-Sleep Mode **For portrait/landscape detection:** The device takes and averages 32 g-cell measurements every 1000 ms in Active Mode and Auto-Sleep. The update rate is 1 sample per second. These measurements update the XOUT (0x00), YOUT (0x01), and ZOUT (0x02) registers also.

AWSR[1:0]	NAME	DESCRIPTION
00	AW32	32 Samples/Second Auto-Wake Mode **For portrait/landscape detection:** The device takes and averages 32 g-cell measurements every 31.25 ms in Auto-Wake. The update rate is 32 samples per second. These measurements update the XOUT (0x00), YOUT (0x01), and ZOUT (0x02) registers also.
01	AW16	16 Samples/Second Auto-Wake Mode **For portrait/landscape detection**: The device takes and averages 32 g-cell measurements every 62.5 ms in Auto-Wake. The update rate is 16 samples per second. These measurements update the XOUT (0x00), YOUT (0x01), and ZOUT (0x02) registers also.
10	AW8	8 Samples/Second Auto-Wake Mode **For portrait/landscape detection:** The device takes and averages 32 g-cell measurements every 125 ms in Auto-Wake. The update rate is 8 samples per second. These measurements update the XOUT (0x00), YOUT (0x01), and ZOUT (0x02) registers also.
11	AW1	1 Sample/Second Auto-Wake Mode **For portrait/landscape detection**: The device takes and averages 32 g-cell measurements every 1000 ms in Auto-Wake. The update rate is 1 sample per second. These measurements update the XOUT (0x00), YOUT (0x01), and ZOUT (0x02) registers also.

FILT[2:0]	DESCRIPTION
000	Tilt debounce filtering is disabled. The device updates portrait/landscape every reading at the rate set by AMSR[2:0] or AWSR[1:0]
001	2 measurement samples at the rate set by AMSR[2:0] or AWSR[1:0] have to match before the device updates portrait/landscape data in TILT (0x03) register.
010	3 measurement samples at the rate set by AMSR[2:0] or AWSR[1:0] have to match before the device updates portrait/landscape data in TILT (0x03) register.
011	4 measurement samples at the rate set by AMSR[2:0] or AWSR[1:0] have to match before the device updates portrait/landscape data in TILT (0x03) register.
100	5 measurement samples at the rate set by AMSR[2:0] or AWSR[1:0] have to match before the device updates portrait/landscape data in TILT (0x03) register.
101	6 measurement samples at the rate set by AMSR[2:0] or AWSR[1:0] have to match before the device updates portrait/landscape data in TILT (0x03) register.
110	7 measurement samples at the rate set by AMSR[2:0] or AWSR[1:0] have to match before the device updates portrait/landscape data in TILT (0x03) register.
111	8 measurement samples at the rate set by AMSR[2:0] or AWSR[1:0] have to match before the device updates portrait/landscape data in TILT (0x03) register.

$09: PDET: Tap/Pulse Detection Register (Read/Write)

D7	D6	D5	D4	D3	D2	D1	D0
ZDA	YDA	XDA	PDTH[4]	PDTH[3]	PDTH[2]	PDTH[1]	PDTH[0]
0	0	0	0	0	0	0	0

PDTH[4:0]	DESCRIPTION
00000	Tap detection threshold is ±1 count
00001	
00010	Tap detection threshold is ±2 counts
00011	Tap detection threshold is ±3 counts
...	... and so on up to...
11101	Tap detection threshold is ±29 counts
11110	Tap detection threshold is ±30 counts
11111	Tap detection threshold is ±31 counts

XDA

1:X-axis is disabled for tap detection
0:X-axis is enabled for tap detection

YDA

1: Y-axis is disabled for tap detection
0: Y-axis is enabled for tap detection

ZDA

1: Z-axis is disabled for tap detection
0: Z-axis is enabled for tap detection

$0A: Tap/Pulse Debounce Count Register (Read/Write)

PD

D7	D6	D5	D4	D3	D2	D1	D0
PD[7]	PD[6]	PD[5]	PD[4]	PD[3]	PD[2]	PD[1]	PD[0]
0	0	0	0	0	0	0	0

PD[4:0]	DESCRIPTION
00000000	The tap detection debounce filtering requires 2 adjacent tap detection tests to be the same to trigger a tap event and set the Tap bit in the TILT (0x03) register, and optionally set an interrupt if PDINT is set in the INTSU (0x06) register. Tap detection response time is nominally 0.52 ms
00000001	
00000010	Tap detection debounce filtering requires 3 adjacent tap detection tests to be the same to trigger a tap event and set the Tap bit in the TILT (0x03) register, and optionally set an interrupt if PDINT is set in the INTSU (0x06) register. Tap detection response time is nominally 0.78 ms
00000011	Tap detection debounce filtering requires 4 adjacent tap detection tests to be the same to trigger a tap event and set the Tap bit in the TILT (0x03) register, and optionally set an interrupt if PDINT is set in the INTSU (0x06) register. Tap detection response time is nominally 1.04 ms
...	... and so on up to...
11111101	Tap detection debounce filtering requires 254 adjacent tap detection tests to be the same to trigger a tap event and set the Tap bit in the TILT (0x03) register, and optionally set an interrupt if PDINT is set in the INTSU (0x06) register. Tap detection response time is nominally 66.04 ms
11111110	Tap detection debounce filtering requires 255 adjacent tap detection tests to be the same to trigger a tap event and set the Tap bit in the TILT (0x03) register, and optionally set an interrupt if PDINT is set in the INTSU (0x06) register. Tap detection response time is nominally 66.3 ms
11111111	Tap detection debounce filtering requires 256 adjacent tap detection tests to be the same to trigger a tap event and set the Tap bit in the TILT (0x03) register, and optionally set an interrupt if PDINT is set in the INTSU (0x06) register. Tap detection response time is nominally 66.56 ms

Table 3. Orientation Detection Logic of when Interrupt will Occur

Orientation	Xg	Yg	Zg
Shake	|X| > +1.3g or	|Y| > +1.3g or	|Z| > +1.3g
Up	|Z| < 0.8g and |X| > |Y| and X < 0		
Down	|Z| < 0.8g and |X| > |Y| and X > 0		
Right		|Z| < 0.8g and |Y| > |X| and Y < 0	
Left		|Z| < 0.8g and |Y| > |X| and Y > 0	
Back			Z < -0.25g
Front			Z > 0.25g

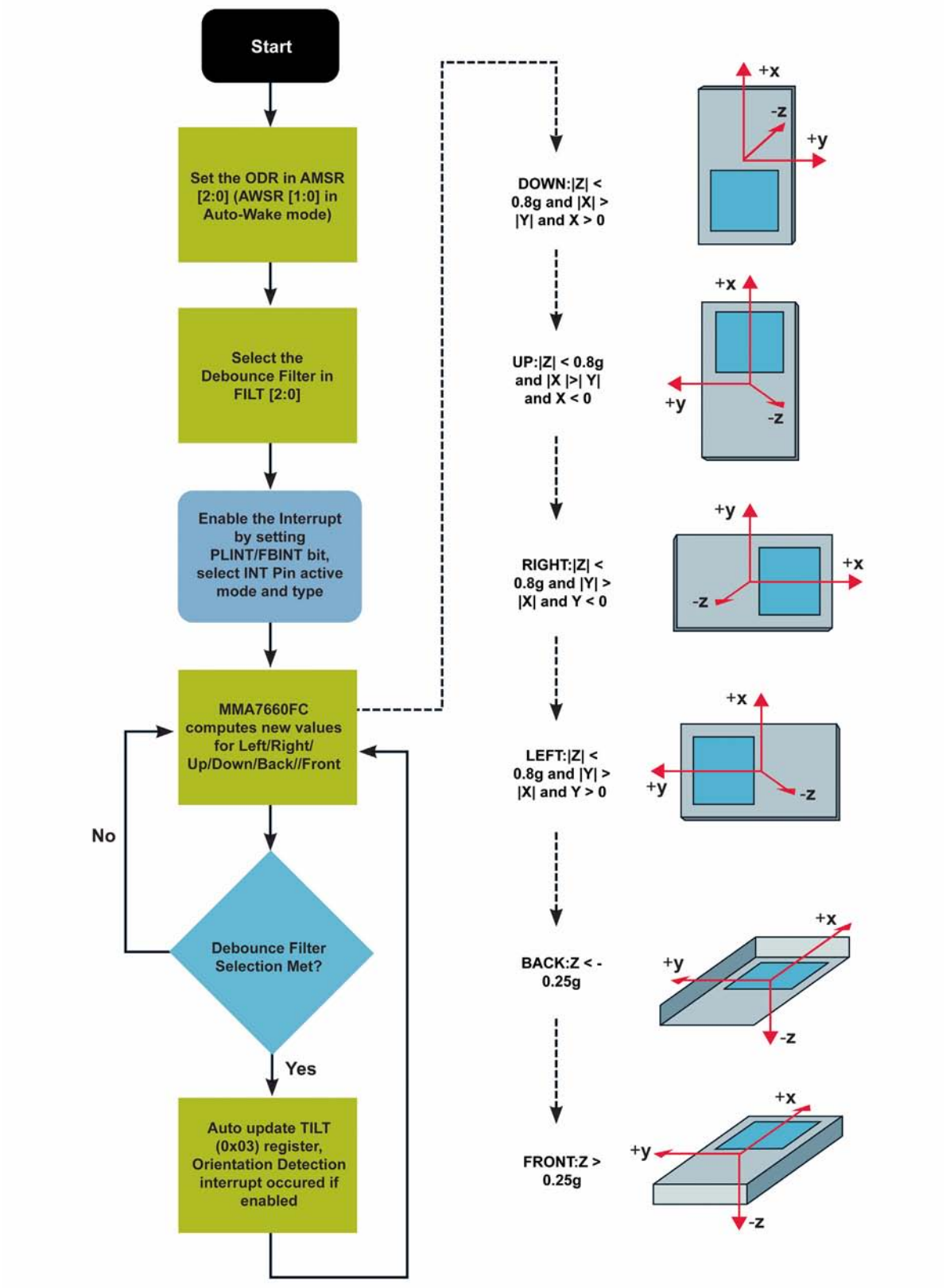


Figure 4. Flow Chart of Orientation Detection

SAMPLE RATE

The sampling rate can be selected based on the targeted power consumption per the application specification or the desired response rate of the orientation detection. The following are the sample rates available in the MMA7660FC sensor with the corresponding approximate power consumption rates.

NOTE: These power consumption rates were tested in the factory and could vary depending on the PCB board design.

Table 4. Sample Rate vs. Current Consumption

Sampling Rate	Current Consumption
Stand By	2.33 μA
1 SPS	46.9 μA
2 SPS	49.3 μA
4 SPS	54 μA
8 SPS	65.8 μA
16 SPS	89.2 μA
64 SPS	221 μA
32 SPS	133 μA
120 SPS	294 μA

ORIENTATION DETECTION

The MMA7660FC has the built in capability to do orientation detection. This feature gives the customer the capability to do applications such as portrait/landscape in mobile phones/PMP/PDAs. The tilt orientation of the device is in 3 dimensions and is identified in its last known static position. This allows a product to set its display orientation appropriately to either portrait or landscape mode or to turn off the display when the device is placed upside down. The sensor provides 6 different positions: left, right, up, down, back, and front. This application note will explain how to configure the MMA7660FC to do orientation detection given the desired sample rate or targeted power consumption.

Setting up the INSU[0x06] Register for Orientation Detection Only

Based on the application specification of the MMA7660FC sensor can be configured to report back/front interrupts and/or up/down/left/right interrupts. If the application targets to use back and front the FBINT bit must be set to 1. If the back and front interrupt is not desired than set the FBINT bit to 0. If the application targets Up/Down/Left/Right interrupts then the PLINT bit must be set to 1. If the Up/Down/Left/Right interrupt is not desired then set the PLINT bit should be set to 0.

$06: Interrupt Setup Register
INTSU

D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	X	PLINT	FBLINT
0	0	0	0	0	0	0	0

Setting up the SR (0x08) Register for Orientation Detection Only

The sample rate must be selected based on target power consumption level and/or desired response rate for the orientation detection application. To set up the sample rate the AMSR[3:0] must be configured. Given the selected sample rate a debounce filter setting (FILT[3:0]) must be set also. Application testing has been done to correlate the sample rate and the recommended debounce filter setting. Refer to “Sample Rate vs. Debounce Filter Table”.

$08: Auto-Wake and Active Mode Portrait/Landscape Output Data Rates Register (Read/Write)
SR - Sample Rate Register

D7	D6	D5	D4	D3	D2	D1	D0
FILT[2]	FILT[1]	FILT[0]	X	X	AMSR[2]	AMSR[1]	AMSR[0]
0	0	0	0	0	0	0	0

Table 5. Sample Rate vs. Debounce Filter Table

Sample Rate	Debounce Filter Setting
1 SPS	4
2 SPS	6
4 SPS	8
8 SPS	8
16 SPS	8
32 SPS	8
64 SPS	External Debounce Filter
120 SPS	External Debounce Filter

NOTE: The recommended values were tested on the RD3803MMA7660FC. The values may change given the mounting and position of the sensor on the PCB design.

HANDLING THE ORIENATION DETECTION INTERRUPT

When an interrupt occurs the application must read the TILT (0x03) register. When reading the TILT register the bits of interest are the following POLA[4:2] and BAFRO[1:0]. The interrupt will be cleared when the TILT register is read.

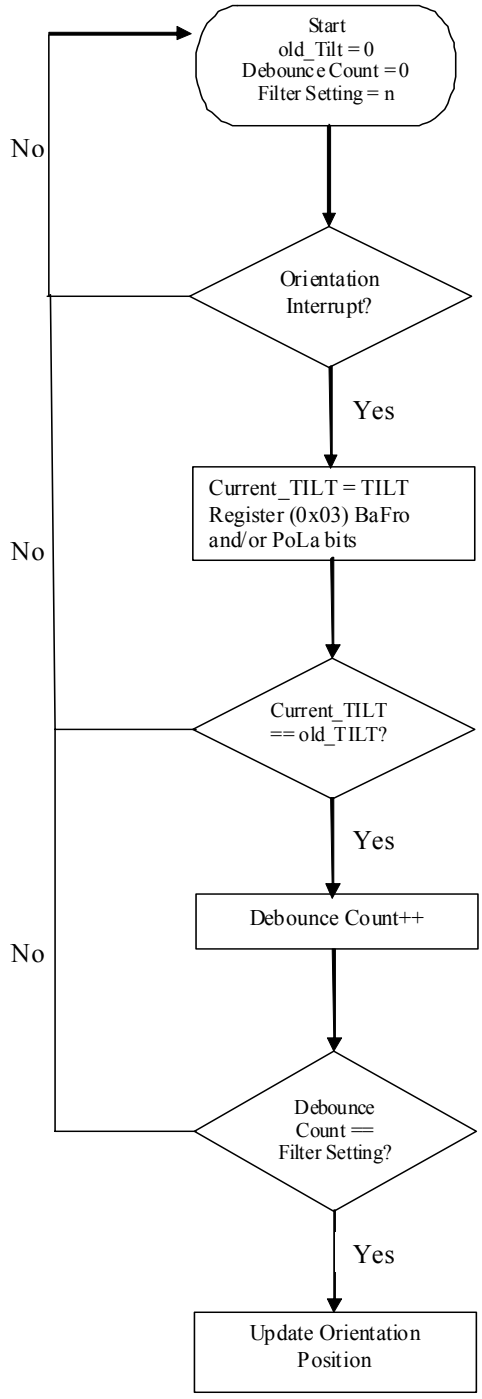
$03: Tilt Status (Read Only)
TILT

D7	D6	D5	D4	D3	D2	D1	D0
X	ALERT	X	PoLa[2]	PoLa[1]	PoLa[0]	BaFro[1]	BaFro[0]
0	0	0	0	0	0	0	0

NOTE: For further description of the INTSU (0x06), SR (0x08) and TILT (0x03) register, please refer to the MMA7660FC Data Sheet.

External Debounce Filter

When using the MMA7660FC and sample rates higher than 32 SPS an external debounce filter must be added to avoid flickering between positions due to involuntary human movement. The external debounce filter must be added to the application microcontroller. Below is a flow chart AND Pseudocode for the debounce filter.




```
PSEUDOCODE:

//Configure Orientation Detection
Interrupts
FILTER_SETTING = n
If(TILT_Interrupt occurs)
            read TILT Register
            if(old_TILT ==
current_TILT)
                        Debounce
Count++
If(Debounce Count == FILTER_SETTING)
            //orientation =
current_TILT
```

Figure 5. External Debounce Filter

REFERENCE CODE:

```
//Configure MMA7660FC as Portrait/Landscape Detection
Write to the MODE register = 0x00       //Standby Mode
Write to the SPCNT register = 0x00      //No sleep count
Write to the INTSU register = 0x03      //Configure GINT Interrupt
Write to the PDET register = 0xE0       //No tap detection enabled
Write to the SR register = 0x34         //8 samples/s, TILT debounce filter = 2
Write to the PD register = 0x00         //No tap detection debounce count enabled
Write to the MODE register = 0x41       //Active Mode, INT = push-pull and active low

//Interrupt service routine
  If (Orientation INT occurs)
     REGTILT=Read TILT Register;                //Read TILT Register value

     Switch (Pola [2:0])                        //Judge the sensor position
     Case 1: Orientation=Left;
     Case 2: Orientation=Right;
     Case 5: Orientation=Down;
     Case 6: Orientation=UP;

     Switch (BaFro [1:0])                       //Judge the sensor position
     Case 1: Orientation=Front;
     Case 2: Orientation=Back;
```

SHAKE DETECTION

The shake feature can be used as a button replacement to perform functions such as scrolling through images or web pages on a Mobile Phone/PMP/PDA. The customer can enable the shake interrupt on any of the 3 axes, by enabling the SHINTX, SHINTY, and/or SHINTZ in the INTSU (0x06) register.

MMA7660FC detects shake by examining the current 6-bit measurement for each axis in XOUT, YOUT, and ZOUT. The axes that are tested for shake detection are the ones enabled by SHINTX, SHINTY, and/or SHINTZ. If a selected axis measures greater than 1.3g or less than -1.3g, then a shake is detected for that axis and an interrupt occurs. All three axes are checked independently, but a common Shake bit in the TILT register is set when shake is detected in any one of the selected axes. Therefore when all 3 axes (SHINTX, SHINTY, and/or SHINTZ) are selected the sensor will not know what axis the shake occurred. When the TILT register is read the Shake bit is cleared during the acknowledge bit of the read access to that register and shake detection monitoring starts again.

Setting up the INSU[0x06] Register for Shake Detection

Based on the application specification of the MMA7660FC sensor can be configured to report shake interrupts. It can be configured as individual axis or combined axes shake detection. If SHINTX/SHINTY/SHINTZ is set to 1, X/Y/Z axis is enabled for shake detection; and if SHINTX/SHINTY/SHINTZ is set to 0, X/Y/Z axis is not desired for shake detection.

$06: Interrupt Setup Register Tilt Status
INTSU

D7	D6	D5	D4	D3	D2	D1	D0
SHINTX	SHINTY	SHINTZ	X	X	X	X	X
0	0	0	0	0	0	0	0

Setting up the SR(0x08) Register for Shake Detection

The sample rate must be selected based on target power consumption level and/or desired response rate for the shake detection application. To set up the sample rate the AMSR[3:0] bits in the SR register must be configured.

$08: Auto-Wake and Active Mode Portrait/Landscape Output Data Rates Register (Read/Write)
SR - Sample Rate Register

D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	AMSR[2]	AMSR[1]	AMSR[0]
0	0	0	0	0	0	0	0

HANDLING THE SHAKE DETECTION INTERRUPT

When an interrupt occurs, the application must read the TILT (0x03) register. When reading the TILT register, the bit of interest is the shake. If the alert bit is high, the data is invalid.

$03: Tilt Status (Read Only)
TILT

D7	D6	D5	D4	D3	D2	D1	D0
Shake	Alert	X	X	X	X	X	X
0	0	0	0	0	0	0	0

NOTE: For further description of the INTSU (0x06), SR (0x08) and TILT (0x03) register, please refer to the MMA7660FC Data Sheet.

PLEASE NOTE: All three axes are checked independently, but a common Shake bit in the TILT register is set when shake is detected in any one of the selected axes. Therefore when all 3 (SHINTX, SHINTY, and/or SHINTZ) are selected the sensor will not know what axis the shake occurred.

Figure 6 shows the flowchart of shake detection.

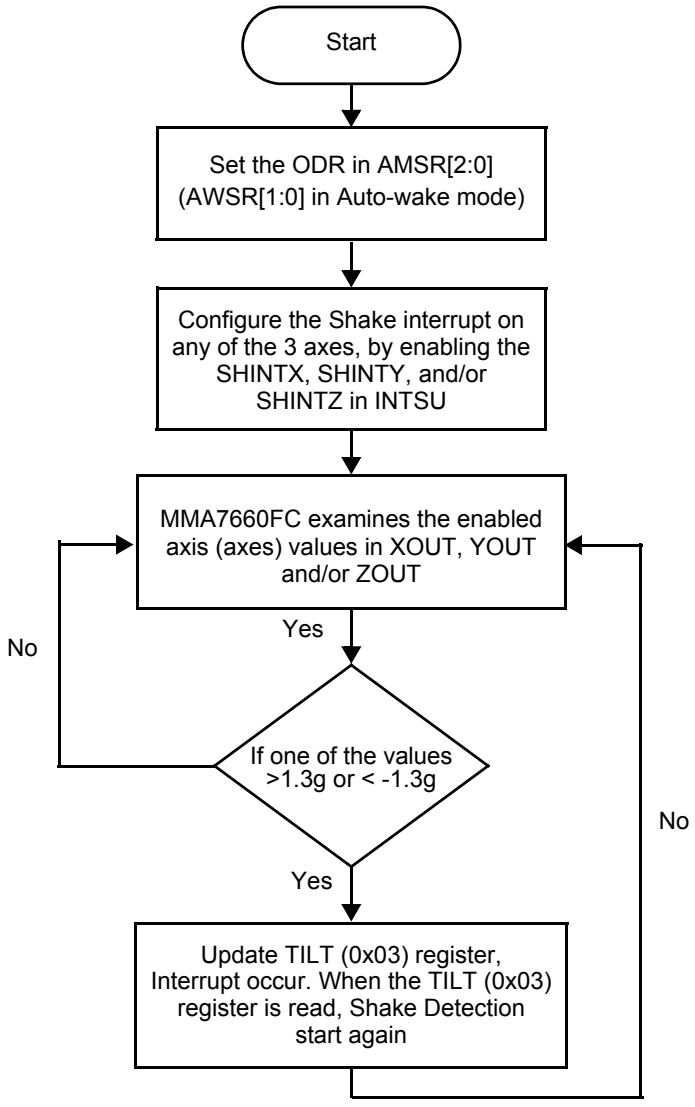


Figure 6. Flow Chart of Shake Detection Algorithm

REFERENCE CODE

```
//Configure MMA7660FC as Shake Detection
Write to the MODE register = 0x00              //Standby Mode
Write to the SPCNT register = 0x00             //No sleep count
Write to the INTSU register = 0xE0             //Configure Shake Interrupt on 3 axes
Write to the PDET register = 0xE0              //No tap detection enabled
Write to the SR register = 0x02                //32 samples/s
Write to the PD register = 0x00                //No tap detection debounce count enabled
Write to the MODE register = 0x41              //Active Mode, INT = push-pull and active low

//Interrupt service routine
  If (Shake INT occurs)
     REGTILT=Read TILT Register;               //Read TILT Register value
     If (Shake =1)                             //Verify "Shake" bit in TILT register
     Shake occurs
```

TAP DETECTION

The MMA7660FC also includes a Tap Detection feature that can be used for a number of different customer applications such as button replacement. For example, a single tap can stop a song from playing and a double tap can play a song. This function detects a fast transition that exceeds a user-defined threshold (PDET (0x09) register) for a certain duration of time (PD (0x0A) register).

Tap Detection Setup

In order to enable Tap detection in the device the user must enable the Tap Interrupt in the INTSU (0x06) register and set the AMSR[2:0] = 000 in the SR (0x08) register. In this mode, TILT (0x03) register, XOUT (0x00), YOUT (0x01), and ZOUT (0x02) registers will update at the 120 samples/second.

NOTE: Delta G is available with any AMSR setting, when XDA = YDA = ZDA = 1 (PDET = 1). When the sampling rate is less than 120 samples/second, the device cannot detect tapping, but can detect small tilt angles (30 degree angle change) which can not be detected by orientation detection.

Setting up the INSU [0x06] Register for Tap Detection

The MMA7660FC sensor can be configured to report tap interrupt by configuring PDINT bit to 1; if the bit is set to 0, tap detection is disabled.

$06: Interrupt Setup Register
INTSU

D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	PDINT	X	X	X
0	0	0	0	0	0	0	0

Setting up the SR (0x08) Register for Tap Detection

The sample rate must be set at 120 samples/second, AMSR [3:0] must be 000.

$08: Auto-Wake and Active Mode Portrait/Landscape Output Data Rates Register (Read/Write)
SR - Sample Rate Register

D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	AMSR[2]	AMSR[1]	AMSR[0]
0	0	0	0	0	0	0	0

Setting up PDET (0x09) Register for Tap Detection

The user can configure Tap Detection to be detected on X and/or Y and/or Z axes. The Customer can configure this by changing the XDA, YDA, and/or ZDA bit in the PDET (0x09) register. The bits PDTH [4:0] is used to set the tap threshold form ±1 count to ±31 counts.

0x09: Tap Detection Register (Read/Write)
PDET

D7	D6	D5	D4	D3	D2	D1	D0
ZDA	YDA	XDA	PDTH[4]	PDTH[3]	PDTH[2]	PDTH[1]	PDTH[0]
0	0	0	0	0	0	0	0

Setting up PD (0x0A) Register for Tap Detection:

The user can configure Tap Debounce Count by PD [7:0] in the PD register to avoid some error trigger, Tap detection debounce filtering requires 2 to 256 adjacent tap detection tests (0.52ms to 66.56ms) to be the same to trigger a tap event and set the Tap bit in the TILT (0x03) register to high, and optionally set an interrupt if PDINT is set in the INTSU (0x06) register.

0x0A: Tap Debounce Count Register (Read/Write)
PD

D7	D6	D5	D4	D3	D2	D1	D0
PD[7]	PD[6]	PD[5]	X	X	X	X	X
0	0	0	0	0	0	0	0

HANDLING THE TAP DETECTION INTERRUPT

Detection for enabled axes is decided on an OR basis: If the PDINT bit is set in the INTSU (0x06) register, the device reports the first axis for which it detects a tap by the Tap bit in the TILT (0x03) register. When the Tap bit in the TILT (0x03) register is set, tap detection ceases, but the device will continue to process orientation detection data. Tap detection will resume when the TILT (0x03) register is read.

$03: Tilt Status (Read only)
TILT

D7	D6	D5	D4	D3	D2	D1	D0
X	Alert	TAP	X	X	X	X	X
0	0	0	0	0	0	0	0

NOTE: For further description of the INTSU (0x06), SR (0x08), PDET (0x09), PD (0x0A) and TILT (0x03) register, please refer to the MMA7660FC Data Sheet.

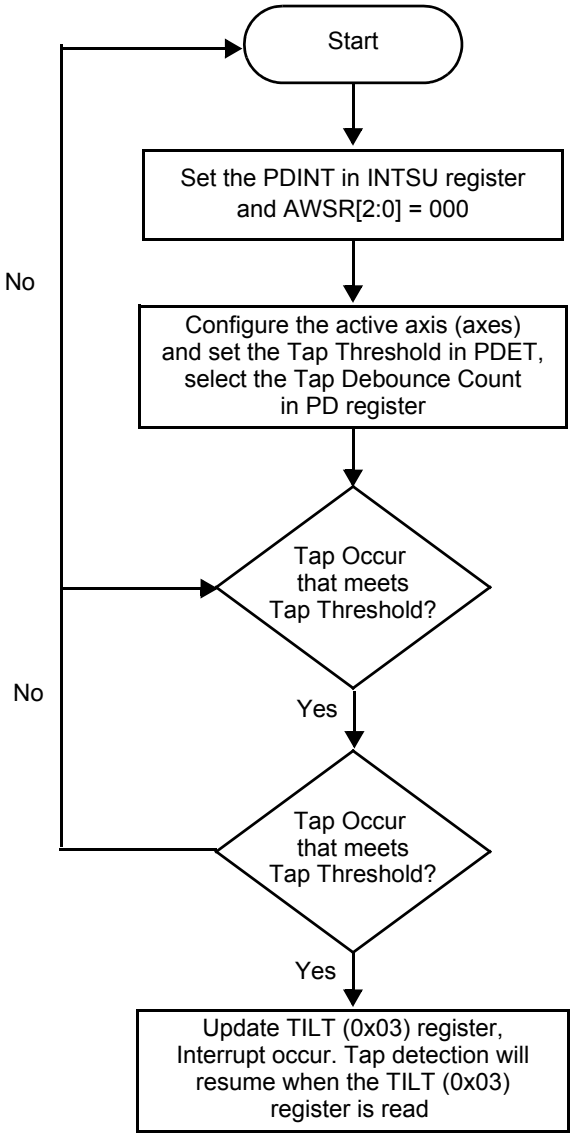


Figure 7. Flow Chart of Tap Detection Algorithm

REFERENCE CODE

```
//Configure MMA7660FC as Tap Detection
Write to the MODE register = 0x00              //Standby Mode
Write to the SPCNT register = 0x00             //No sleep count
Write to the INTSU register = 0x04             // Configure tap detection Interrupt
Write to the PDET register = 0x6C              // Only Z axis tap detection on, threshold ±12
                                               //counts
Write to the SR register = 0x00                //120 samples/s
Write to the PD register = 0x08                // Tap detection debounce count = 9
Write to the MODE register = 0x41              //Active Mode, INT = push-pull and active low

//Interrupt service routine
     If (Tap INT occurs)
     REGTILT=Read TILT Register;               //Read TILT Register value

     If (Tap =1)           //Verify "Tap" bit in TILT register
         Tap occurs
```

AUTO-WAKE/SLEEP

The MMA7660FC has the Auto-Wake/Sleep feature that can be enabled for power saving. In the Auto-Wake (sleep state) function, the device is put into a user specified low sample rate (1 sample/second, 8 samples/second, 16 samples/second, or 32 samples/second) in order to minimize power consumption. When the Auto-Wake is enabled and activity is detected such as a change in orientation, pulse event, Delta G acceleration or a shake event, then the device wakes up (Table 4). Auto-Wake will automatically enable Auto-Sleep when the device is in wake mode and can therefore be configured to cause an interrupt on wake-up, by configuring the part to either wake up with a change in orientation, shake, or if using the part at 120 samples/second tap detection.

When the device is in Auto-Wake mode, the MODE (0x07) register, bit AWE is high. When the device has detected a change in orientation, a tap, a shake, or Delta G (change in acceleration) the device will enter Auto-Sleep mode. In the Auto-Sleep (wake state) function, the device is put into any of the following user specified sample rate (1 sample/second, 2 samples/second, 4 samples/second, 8 samples/second, 16 samples/second, 32 samples/second, 64 samples/second, and 120 samples/second). In the Auto-Sleep mode, if there is no change in the orientation, shake or tap has been detected and the sleep counter has elapsed, the device will go into the Auto-Wake mode. When the device is in the Auto-Sleep mode, the MODE (0x07) register, bit ASE is high. The device can be programmed to continually cycle between Auto-Wake/Sleep.

Table 6. Auto-Wake/Sleep Truth Table

	Trigger Wake-up Reset	Sleep Counter Trigger	Sleep Mode
Orientation Detection Change	Yes	Yes	No
Shake	Yes	Yes	No
Delta G (set with PD (0x0A) and PDET (0x09))	Yes (XDA = YDA = ZDA = 0)	Yes	No
Pulse Detect (120 samples/second)	Yes	Yes	No
Sleep Counter Elapse	No	No	Yes

Setting up the MODE[0x07] Register for Auto-Sleep and Auto-Wake

Based on the application specification of the MMA7660FC sensor can be configured to auto-sleep and auto-wake. When Auto-Wake functionality is desired AWE must be set to 1. When the device enters Auto-Wake mode, the AWSRS bit in the SRST register is set and the device uses the samples per second specified in AWSR[1:0] of the SR (0x08) register. When the device exits Auto-Wake mode by any of the selected interrupts, the device will then enter Auto-Sleep Mode (the ASE bit must be set to 1). The device will switch to the samples per second specified in AMSR[2:0] of the SR (0x08) register.

When Auto-Sleep functionality is operating, the AMSRS bit in the SRST register is set and the device uses the sample rate specified in AMSR[2:0] of the SR (0x08) register. When MMA7660FC automatically exits Auto-Sleep mode because the Sleep Counter times out, the device will then switch to the samples per second specified in AWSR[1:0] of the SR register. If AWE = 1, then Auto-Wake functionality is enabled.

If SCPS bit is set to 1 the sleep counter input clock is the sample rate set by AMSR divided by 16. When selected the sleep counter time-out ranges from 64s to 4096s (68 minutes).

If SCPS bit is set to 0, the prescaler is divide-by-1. The 8-bit internal Sleep Counter input clock is the samples per second set by AMSR[2:0], so the sleep Counter time-out range is 2.13s to 256s (4.25 minutes).

Setting up the SRST Register

When an interrupt occurs, read the SRST register. If AMSRS bit is high, the Auto-Sleep in enabled. If AWSRS is high the Auto-Wake is enabled.

$04: Sample Rate Status Register (Read only)
SRST

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	AWSRS	AWSRS
0	0	0	0	0	0	0	0

Setting up the SPCNT (0x05) Register for Auto-Sleep and Auto-Wake

The user can set the 8-bit maximum count value for the 8-bit internal sleep counter in Auto-Sleep. When the 8-bit internal sleep counter reaches the value set by SC[7:0], MMA7660FC will exit Auto-Sleep and switch to the samples per second specified in AWSR[1:0} of the SR (0x08) register.

$05: Sleep Count Register (Read/Write)
SPCNT

D7	D6	D5	D4	D3	D2	D1	D0
SC[7]	SC[6]	SC[5]	SC[4]	SC[3]	SC[2]	SC[1]	SC[0]
0	0	0	0	0	0	0	0

Setting up the INTSU [0x06] Register Auto-Sleep and Auto-Wake

The MMA7660FC sensor can be configured to report on exiting auto-sleep interrupts. If the ASINT bit is set, exiting Auto-Sleep would cause an interrupt.

$06: Interrupt Setup Register
INTSU

D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	ASINT	X	X	X
0	0	0	0	0	0	0	0

Setting up the MODE Register

The bits of interest are the ASE, AWE, SCPS and IPP bit. If the ASE is set to high, then Auto-Sleep is enabled and AMSR sample rate is used. If low, then Auto-Sleep is disabled. If the AWE = 1, then Auto-Wake is enabled and AWSR sample is used. If AWE = 0, then Auto-Wake is disabled. SCPS bit sets the clock prescaler to divide-by-1 (SCPS= 0) or divide-by-16 (SCPS = 1) (Table 2.). The IPP bit sets the interrupt output to open-drain (IPP = 0) or push-pull (IPP = 1).

$07: Mode Register (Read/Write)
MODE

D7	D6	D5	D4	D3	D2	D1	D0
X	IPP	SCPS	ASE	AWE	X	X	X
0	0	0	0	0	0	0	0

Setting up the SR (0x08) Register for Auto-Sleep and Auto-Wake

The sample rate must be selected based on target power consumption level and/or desired response rate for the applications. To setup the sample rate, the AMSR[3:0] bits for Auto-Sleep mode and AWSR[2:0] for Auto-Wake mode in the SR register must be configured.

$08: Auto-Wake and Active Mode Portrait/Landscape Samples per Seconds Register (Read/Write)
SR - Sample Rate Register

D7	D6	D5	D4	D3	D2	D1	D0
FILT[2]	FILT[1]	FILT[0]	AWSR[1]	AWSR[0]	AMSR[2]	AMSR[1]	AMSR[0]
0	0	0	0	0	0	0	0

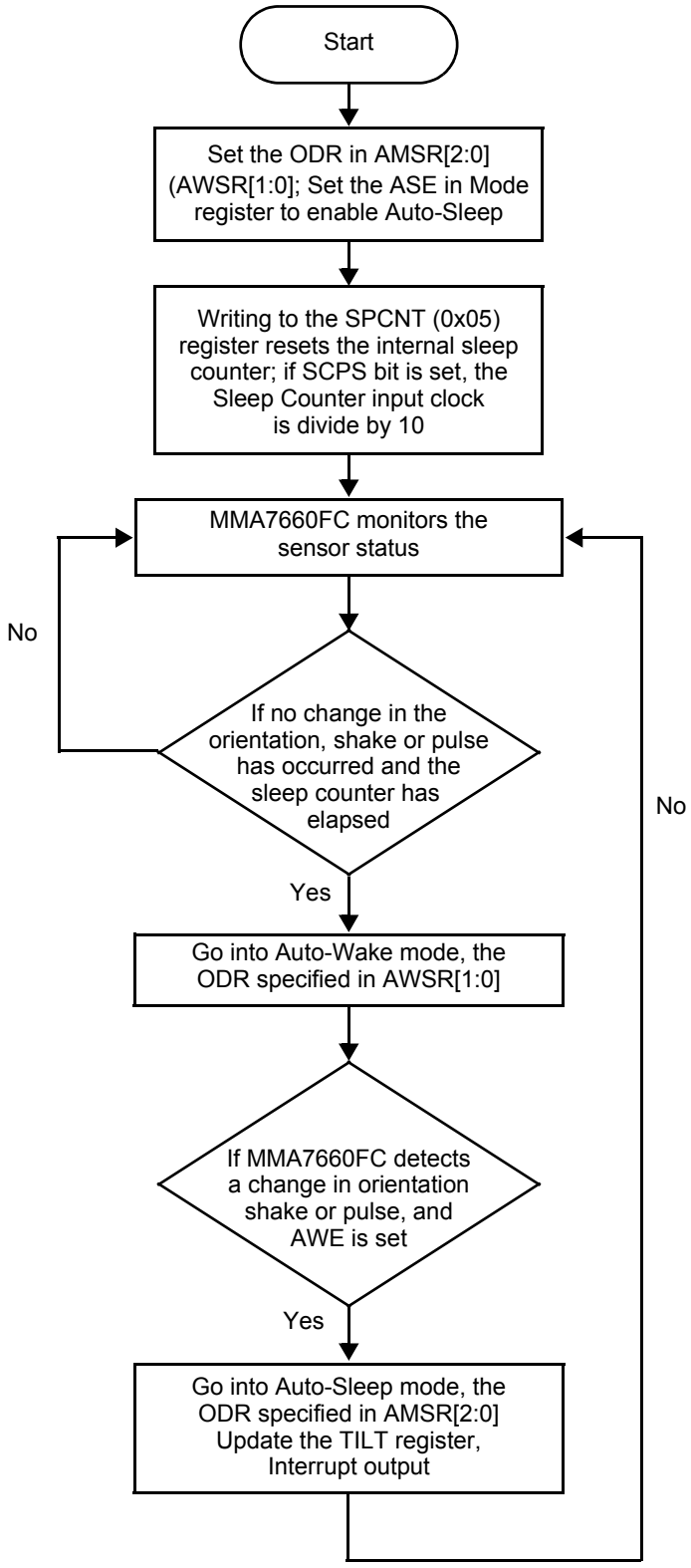


Figure 8. Flow Chart of Auto-Sleep/Wake Algorithm

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