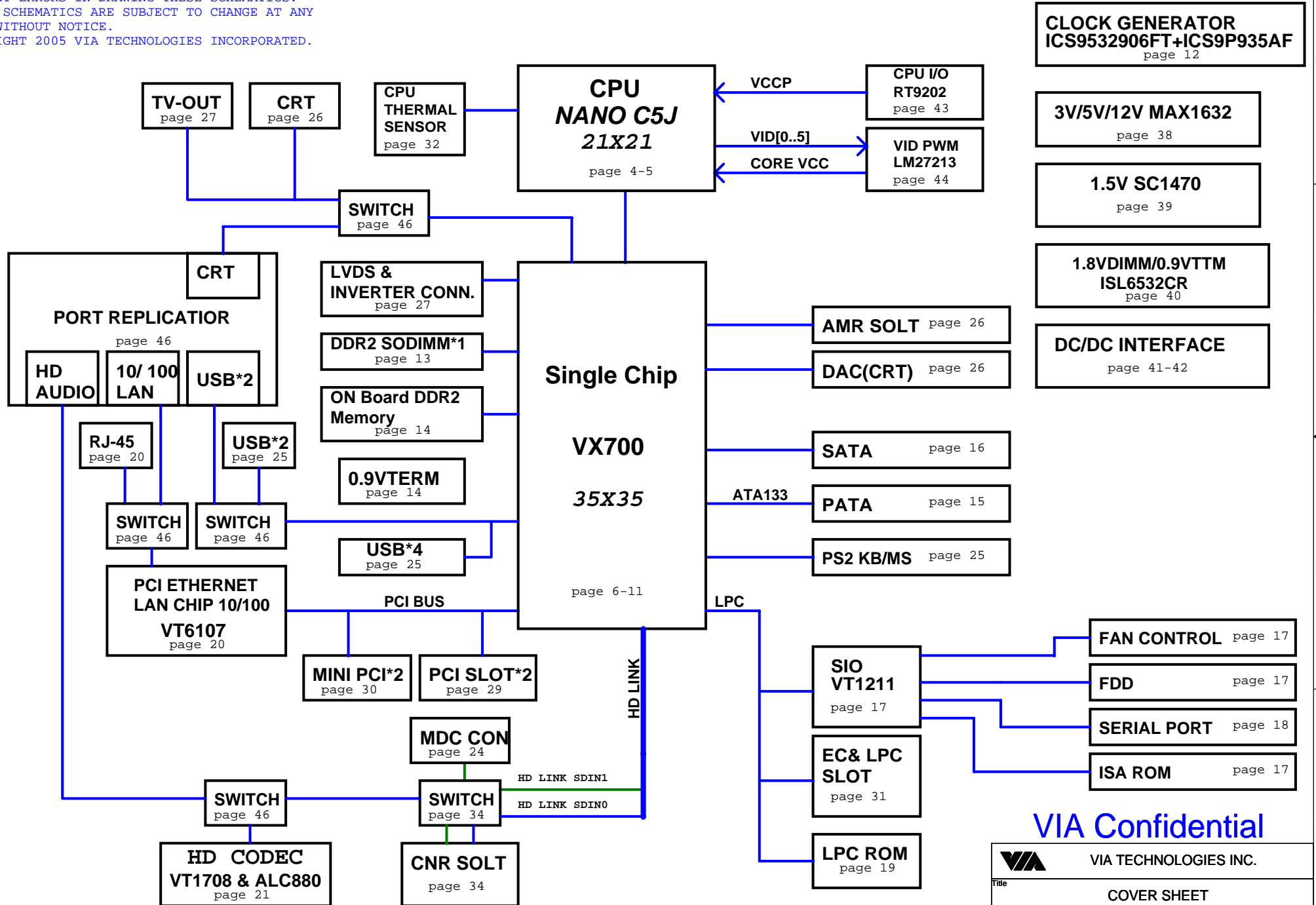


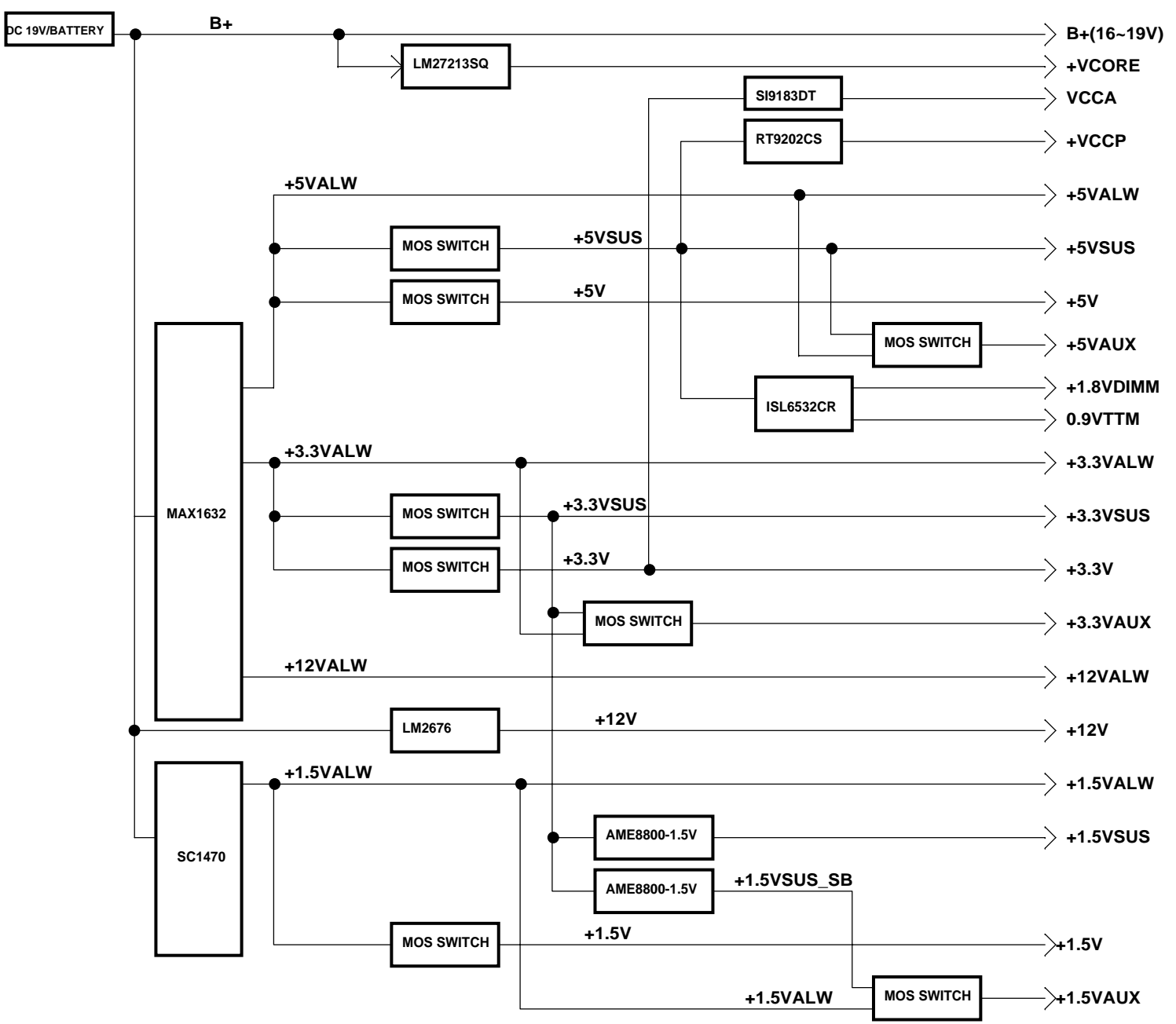
MODEL: VT6304A3 REV.: 3.1

VIA TECHNOLOGIES ASSUMES NO RESPONSIBILITY FOR ANY ERRORS IN DRAWING THESE SCHEMATICS. THESE SCHEMATICS ARE SUBJECT TO CHANGE AT ANY TIME WITHOUT NOTICE. COPYRIGHT 2005 VIA TECHNOLOGIES INCORPORATED.



VIA Confidential

		VIA TECHNOLOGIES INC.	
Title: COVER SHEET			
Size: C	Document Number: VT6304A3	Rev: 3.1	
Date: Wednesday, August 02, 2006	Sheet: 1	of 53	



S0/S1	S3	S4	S5	DEVICE
X	X	X	X	B+(16~19V)
X				+VCORE CPU
X				VCCA CPU (1.5V)
X				+VCCP CPU (1.05V)
X	X	X	X	+5VALW (NOTE 1)
X	X			+5VSUS USB(NOTE 2)
X				+5V IDE, CODEC, AUDIO AMP. NOTE 4
X	X			+5VAUX PS2 KB/MOUSE NOTE 5
X	X			+1.8VDIMM VX700,SODIMM,BUFFER
X				0.9VTTM DDR2 SODIMM
X	X	X	X	+3.3VALW EC
X	X			+3.3VSUS VX700
X				+3.3V VX700,ISC952906, SIO ,CODEC,THERMAL SENSOR NOTE 4
X	X			+3.3VAUX VX700,VT6107(NOTE 3) NOTE 5
X	X	X	X	+12VALW
X				+12V
X	X	X	X	+1.5VALW
X	X			+1.5VSUS VX700
X				+1.5V VX700
X	X			+1.5VAUX NOTE 4
X	X	X	X	+1.5VALW VX700 NOTE 5

NOTE 1: +5VALW exist while DC 19V, but not exist while BATTERY only!
 NOTE 2: +5VSUS exist until S4 while w/ EC device, but not exist at S4 while w/o EC device!
 NOTE 3: +3.3VAUX can be switched to +3.3VALW or +3.3VSUS by J17, while w/o or w/ EC exist. (see page 41)
 NOTE 4: NOT SUPPORT S4 WHILE W/O EC
 NOTE 5: SUPPORT S4 WHILE W/ EC

Clock Generator (ICS952906)

PIN NO	PIN NAME	CONNECT TO
2	REF0/FS0	GUICLK
1	REF1/FS1	X
21	48MHz/FS3	SIICLK
22	24/48MHz	USBCLK
29	3V66_0	X
26	3V66_1	X
25	3V66_2	GUICLK
7	PCI_F0/FS2	PCICLK5
8	PCI_F1/FS4	SPCLK
9	PCI_F2	PCICLK5IO
		ROM_CLK
12	PCI0/MODE	X
13	PCI1	PCICLK1
14	PCI2	PCICLK2
15	PCI3	PCICLK3
16	PCI4	PCICLK4
19	PCI5	PCICLK9
20	PCI6	PCICLK8
39	CPUCLKT0	CPU_CLK
38	CPUCLKC0	CPU_CLK#
42	CPU2_T	HCLK
41	CPU2_C	HCLK#
36	25MHz_0	CLK250
35	25MHz_1	CLK250_1

Clock Buffer (ICS9P935AF)

PIN NO	PIN NAME	CONNECT TO
1	DDRC0	DCLK0-
2	DDRT0	DCLK0+
4	DDRT1	DCLK2+
5	DDRC1	DCLK2-
9	CLKINT	MCLKOT
10	CLKINC	MCLKOC
12	DDRT2	DCLK1+
13	DDRC2	DCLK1-
16	DDRT3	DCLK3+
15	DDRC3	DCLK3-
17	FB_OUT	DCLK3+
18	FB_IN	DCLK3-

Either One

PCI Device ID number


PCI Device	IDSEL	Device #	INT_A#	INT_B#	INT_C#	INT_D#
PCI SLOT1	AD19	08h	INT_A#	INT_B#	INT_C#	INT_D#
PCI SLOT2	AD20	09h	INT_B#	INT_C#	INT_D#	INT_A#
Mini PCI1	AD23	09h	INT_B#	INT_C#		
Mini PCI2	AD22	08h	INT_C#	INT_D#		
LAN VT6107	AD21	0Ah	INT_C#			

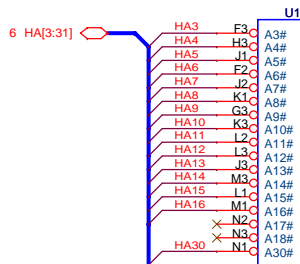
SMBus Address

Master	Address
VX700	D2
ICS952006AF	read: D4 write: D5
ICS9P935AF	A0
DDR-SODIMM1	A1
On Board DDR Memory	A1
CNR	AE

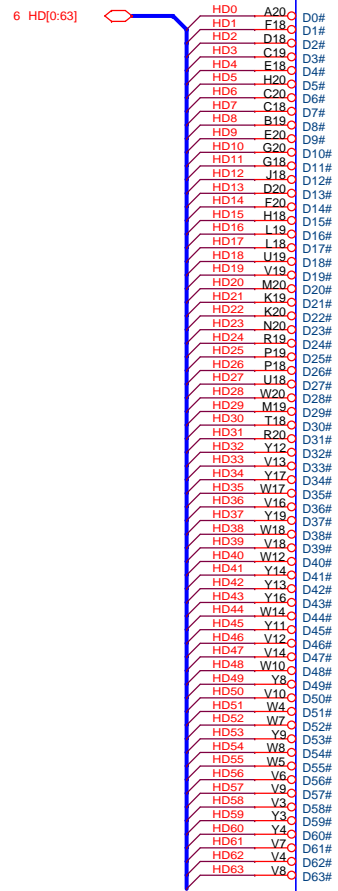
Wakeup Event

WakeUp Events	S1	S3	S4	S5	Note
PS2 KB/MS	Yes	No	No	No	
USE	Yes	Yes	Yes	No	S4 wakeup disable when there's no EC
WOL	Yes	Yes	Yes	No	
PME	Yes	Yes	Yes	No	PCI bus,
WOR	Yes	Yes	Yes	No	From HD
FWRBTN	Yes	Yes	Yes	Yes	

		VIA TECHNOLOGIES INC.	
Title		HW SPEC.	
Size	Document Number	Rev	
Custom	VT6304A3	3.1	
Date:	Wednesday, August 02, 2006	Sheet	3 of 53

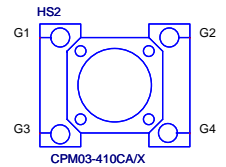
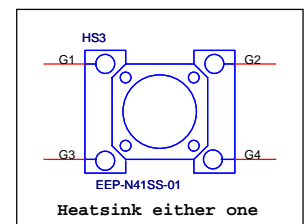


21X21 NANO BGA

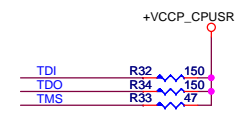
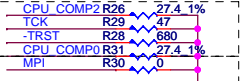
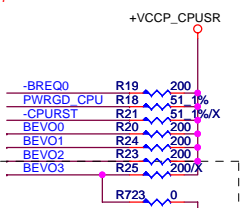
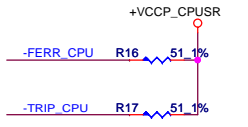
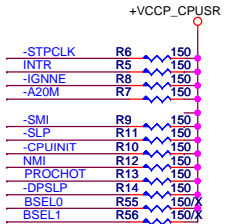
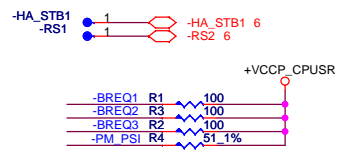
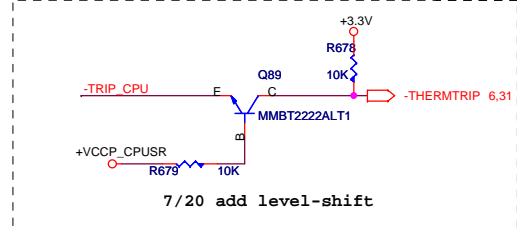
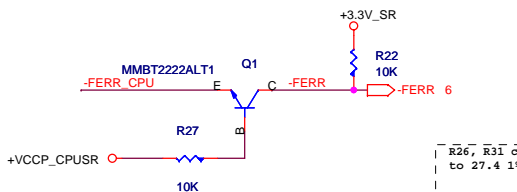
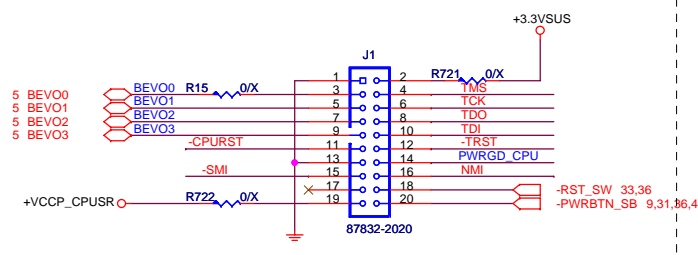


HA3	F3	A3#	A20M#	B9	-A20M	-A20M 6
HA4	H3	A4#	FERR#	A8	-FERR CPU	
HA5	J1	A5#	INTR#	A10	-CPUUNIT	-CPUUNIT 6
HA6	F2	A6#	INTR#	B8	INTR	INTR 6
HA7	J2	A7#	NMI	C9	NMI	NMI 6
HA8	K1	A8#	IGNNE#	D9	-IGNNE	-IGNNE 6
HA9	G3	A9#	SMI#	A11	-SMI	-SMI 6
HA10	K3	A10#	SLP#	B10	-STPCLK	-SLP 6,47
HA11	L2	A11#	STPCLK#	A18	-STPCLK	-STPCLK 6
HA12	L3	A12#	DPWR#	B1	-DPWR	-DPWR 6
HA13	J3	A13#	ADS#	D3	-ADS	-ADS 6
HA14	M3	A14#	BNR#	D3	-BNR	-BNR 6
HA15	L1	A15#	DBSY#	A1	-DBSY	-DBSY 6
HA16	M1	A16#	DEFER#	A2	-DEFER	-DEFER 6
N2	N2	A17#	DRDY#	B3	-DRDY	-DRDY 6
N3	N3	A18#	HIT#	C3	-HIT	-HIT 6
N1	N1	A30#	HITM#	B2	-HITM	-HITM 6
			TRDY#	B2	-HTRDY	-HTRDY 6
			BPRI#	C4	-BPRI	-BPRI 6
			BREQ0#	C1	-BREQ0	-BREQ0 6
			BREQ1#	U1	-BREQ1	-BREQ1 6
			BREQ2#	D5	-BREQ2	-BREQ2 6
			BREQ3#	D5	-BREQ3	-BREQ3 6
			LOCK#	D4		
			REQ0#	D1	-HREQ0	-HREQ0 6
			REQ1#	D2	-HREQ1	-HREQ1 6
			REQ2#	F1	-HREQ2	-HREQ2 6
			RS0#	B4	-RS0	-RS0 6
			RS1#	A3	-RS1	-RS1 6
			RS2#	E3	-RS2	-RS2 6
			ASTBN0#	G1	-HA_STBN0	-HA_STBN0 6
			ASTBP0#	G2	-HA_STBP0	-HA_STBP0 6
			DSTBN0#	E19	-HD_STBN0	-HD_STBN0 6
			DSTBN1#	E19	-HD_STBN1	-HD_STBN1 6
			DSTBN2#	U20	-HD_STBN2	-HD_STBN2 6
			DSTBN3#	T20	-HD_STBN3	-HD_STBN3 6
			BCLK#	A14	CPU_CLK+	CPU_CLK+ 12
			BCLK#	A13	CPU_CLK-	CPU_CLK- 12
			BSEL0	C14	BSEL0	BSEL0 12
			BSEL1	D14	BSEL1	BSEL1 12
			RESET#	C13	-CPURST	-CPURST 6,47
			PWRGD	C8	PWRGD_CPU	CPU_POK 35,47
			PSI#	C7	-PM_PSI	-PM_PSI 44
			COMP0	H17	CPU_COMP0	
			COMP2	T3	CPU_COMP2	
			MPI	U5	MPI	
			THERMDA	C17	THERMDA	THERMDA_CPU 32
			THERMDC	A17	THERMDC	THERMDC_CPU 32
			THERMTRIP#	A16	-TRIP_CPU	
			PROCHOT#	B18	PROCHOT	
			DP0#	J20	DPB0	DP0-1
			DP1#	R18	DPB1	DP1-1
			DP2#	V11	DPB2	DP2-1
			DP3#	Y10	DPB3	DP3-1
			DPSLP#	B11	-DPSLP	-DPSLP 6,47
			TDI	C15	TDI	
			TDO	A15	TDO	
			TMS	B15	TMS	
			TRST#	B16	-TRST	
			TCK	C16	TCK	
			VID0	B7	CPU_VID0	CPU_VID0 44
			VID1	C6	CPU_VID1	CPU_VID1 44
			VID2	A7	CPU_VID2	CPU_VID2 44
			VID3	B6	CPU_VID3	CPU_VID3 44
			VID4	A6	CPU_VID4	CPU_VID4 44
			VID5	A5	CPU_VID5	CPU_VID5 44
			DINV3#	V5	-HDBI3	-HDBI3 6
			DINV2#	V17	-HDBI2	-HDBI2 6
			DINV1#	N18	-HDBI1	-HDBI1 6
			DINV0#	H19	-HDBI0	-HDBI0 6

C5J-nano



7/20 change heatsink

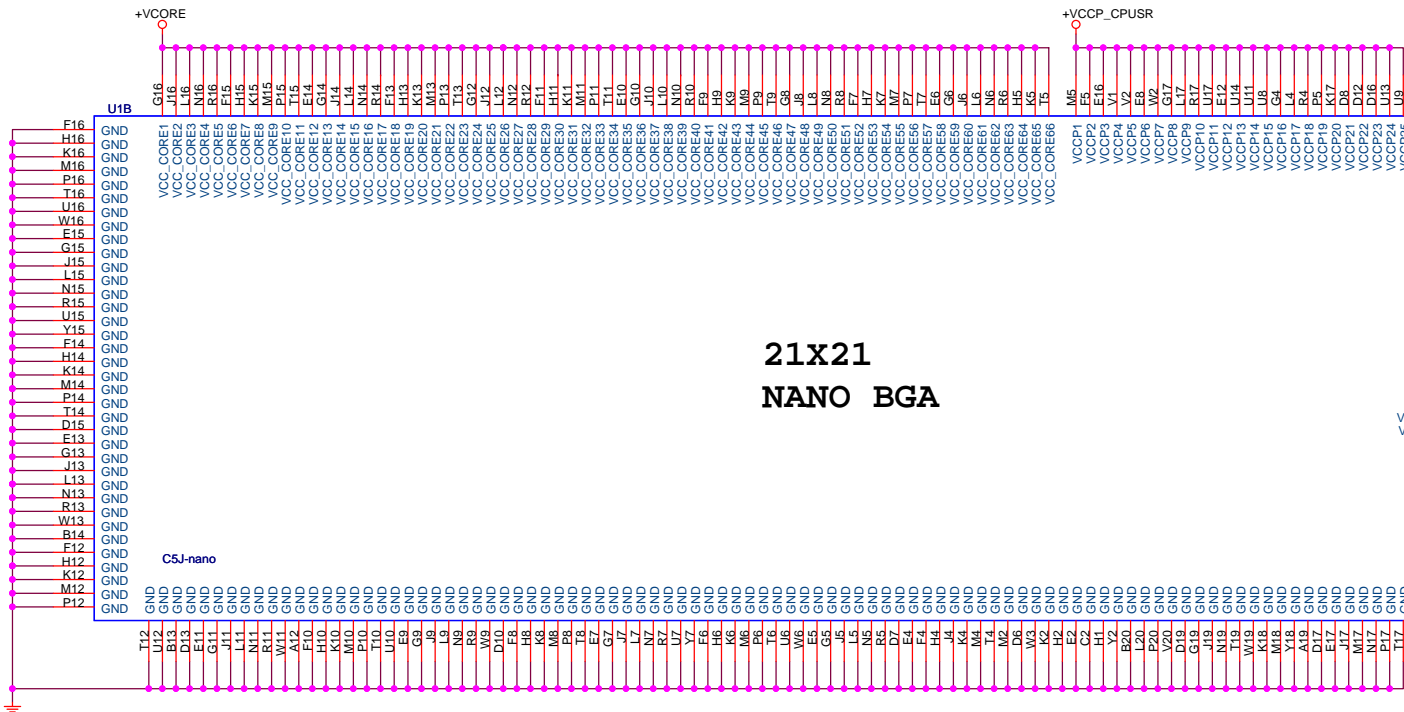


VIA VIA TECHNOLOGIES INC.

Title: Nano_C5J PART 1

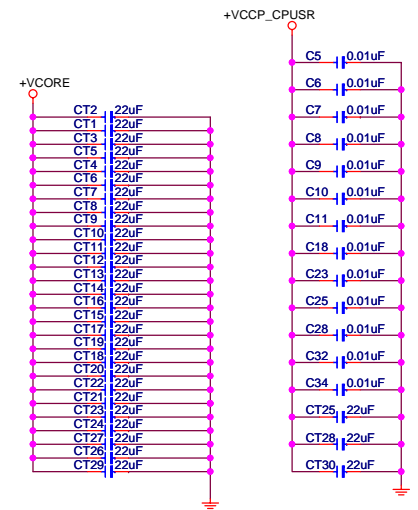
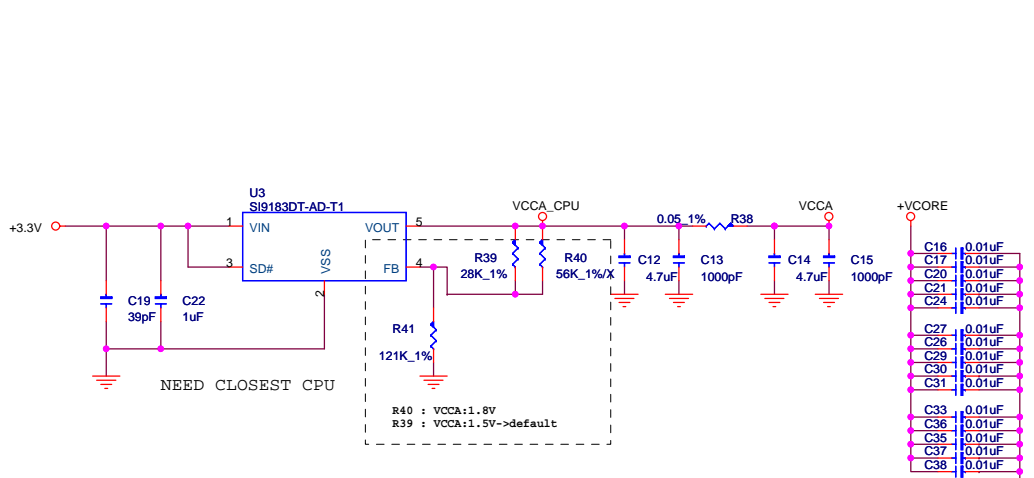
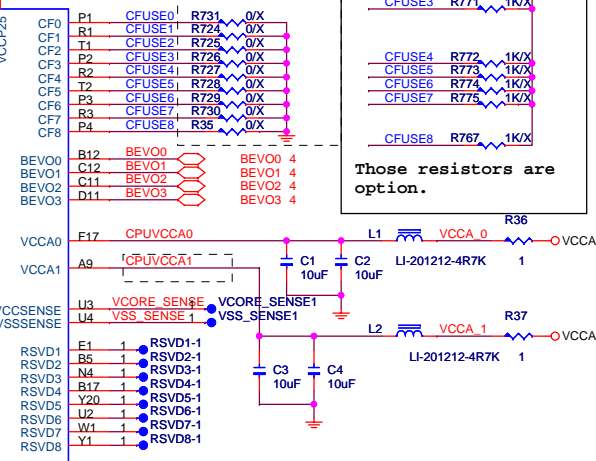
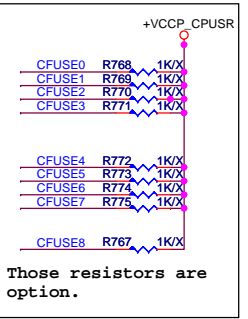
Size: Custom Document Number: VT6304A3 Rev: 3.1

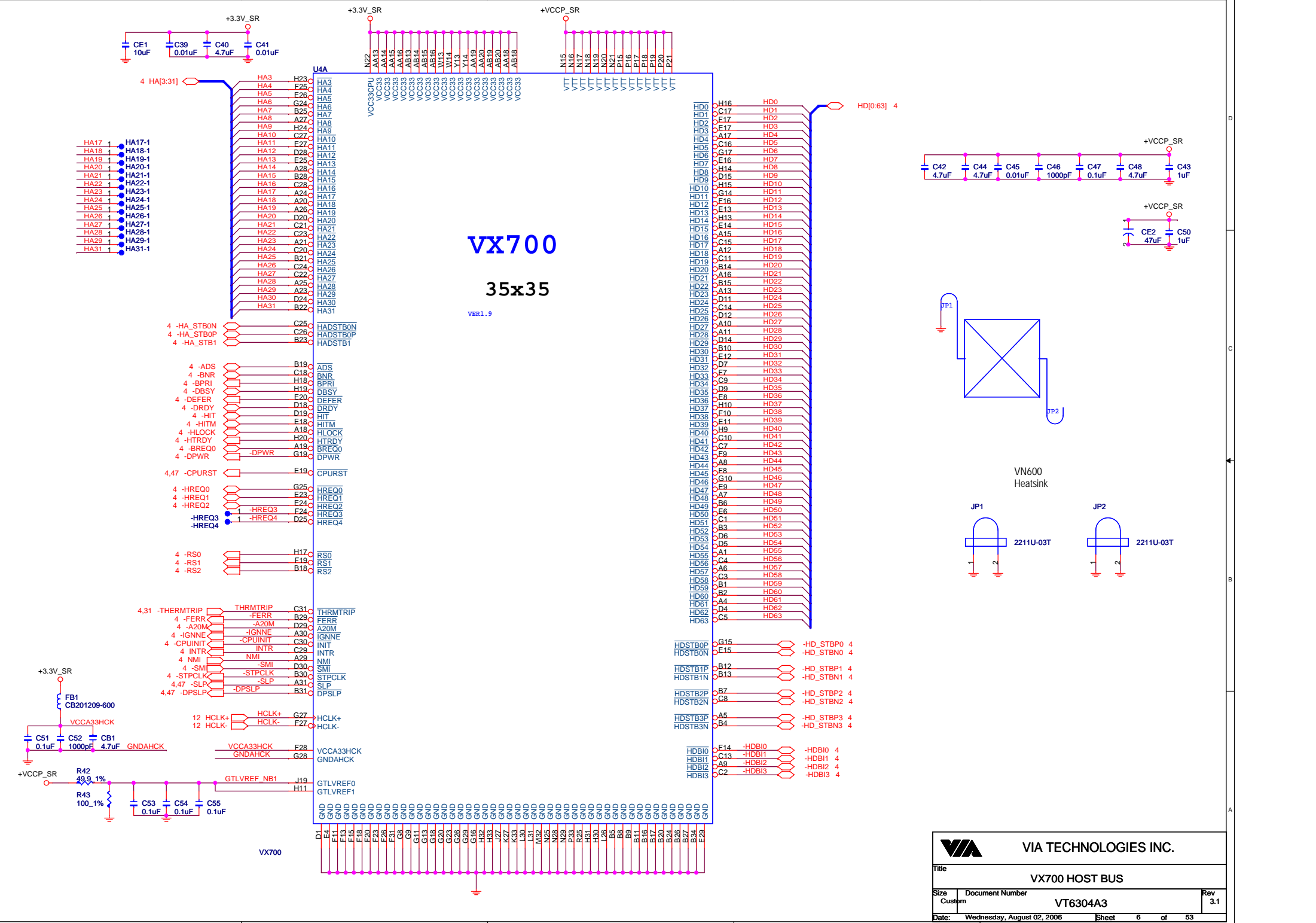
Date: Wednesday, August 02, 2006 Sheet: 4 of 53



**21X21
NANO BGA**

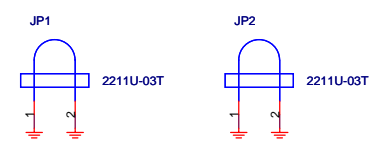
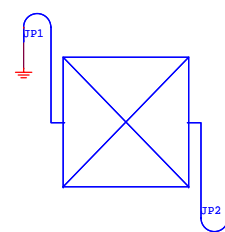
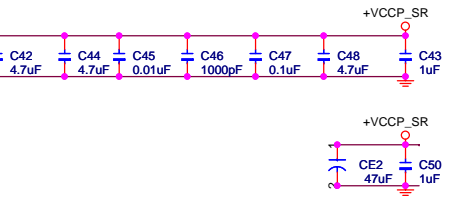
NOTE L



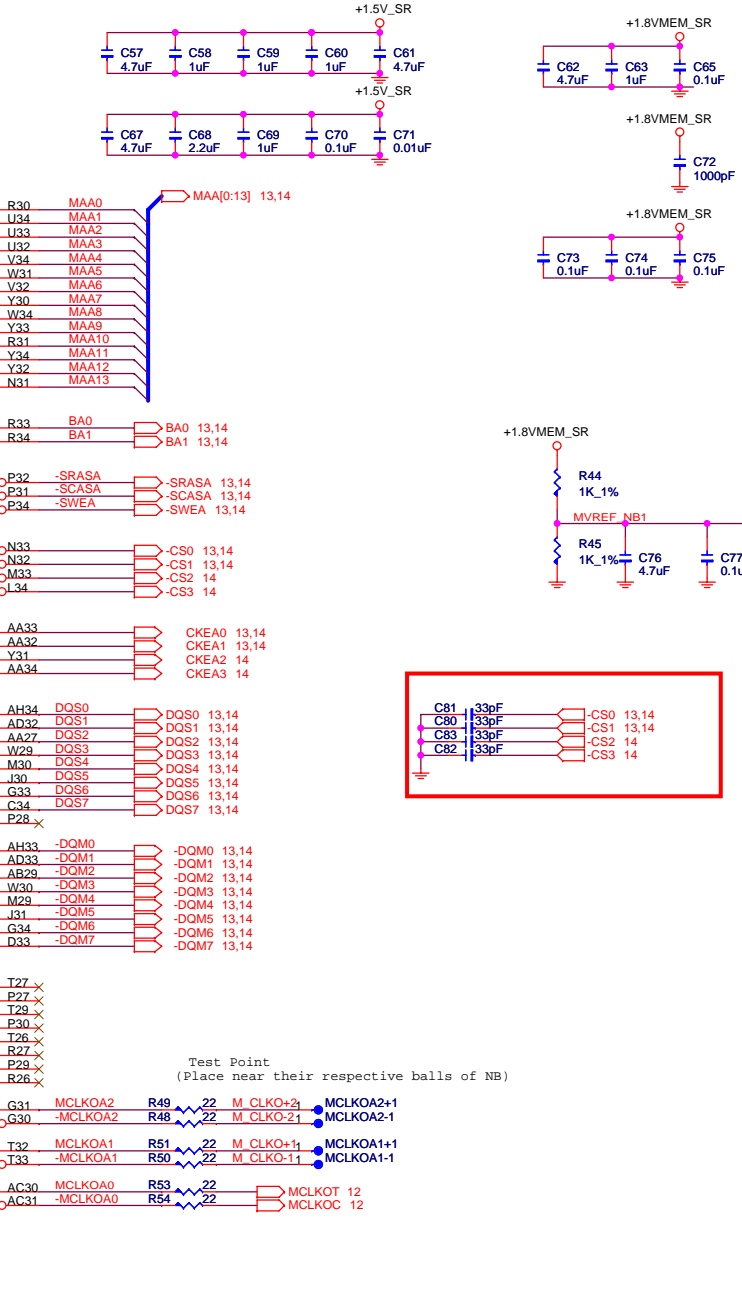
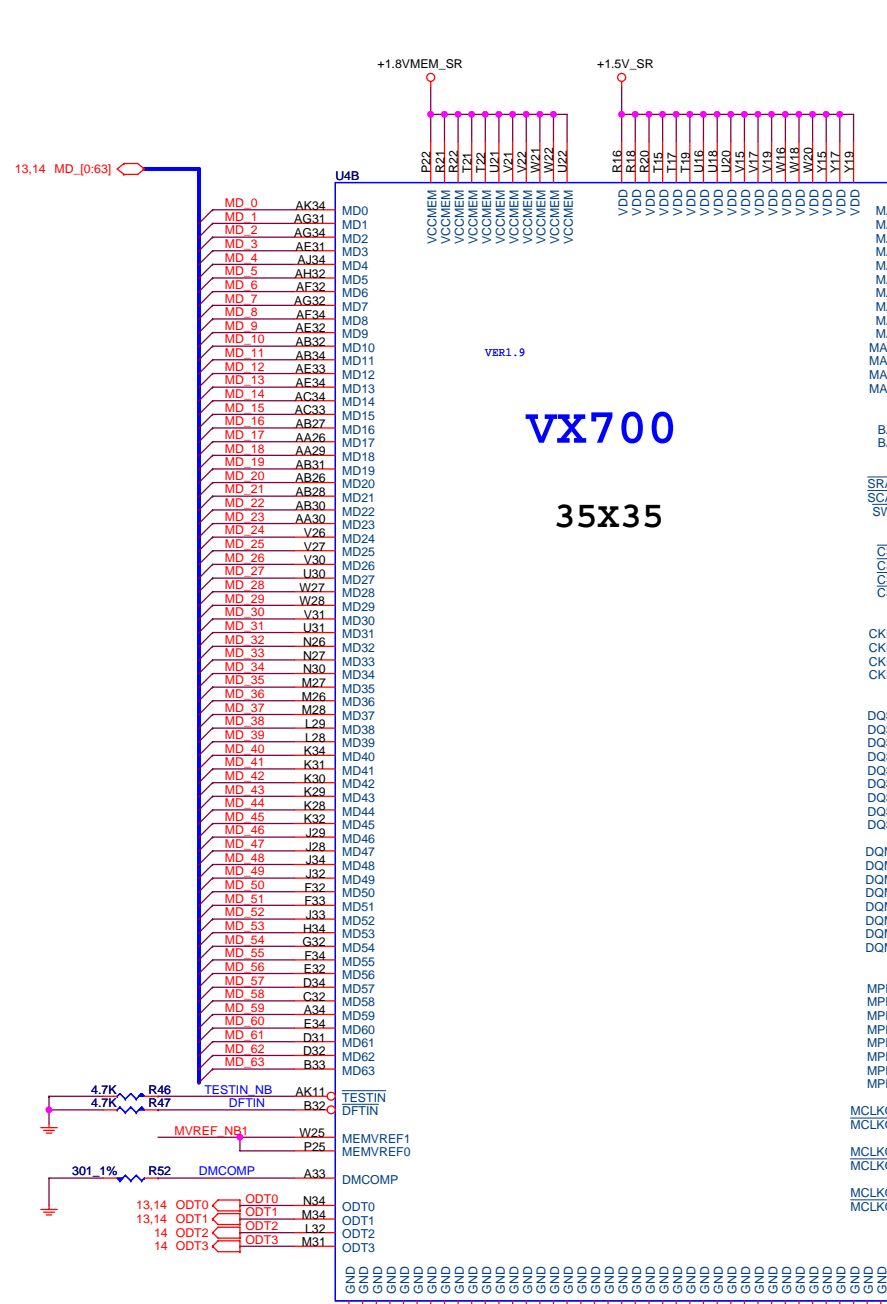


VX700
35x35

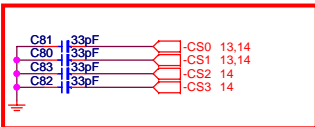
VER 1.9



VIA			VIA TECHNOLOGIES INC.		
Title VX700 HOST BUS					
Size	Document Number				Rev
Custom	VT6304A3				3.1
Date:	Wednesday, August 02, 2006		Sheet	6	of 53



VX700
35X35



VIA VIA TECHNOLOGIES INC.

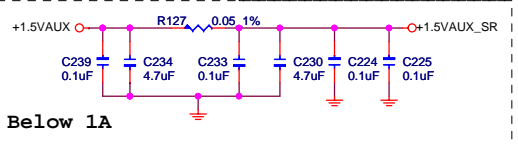
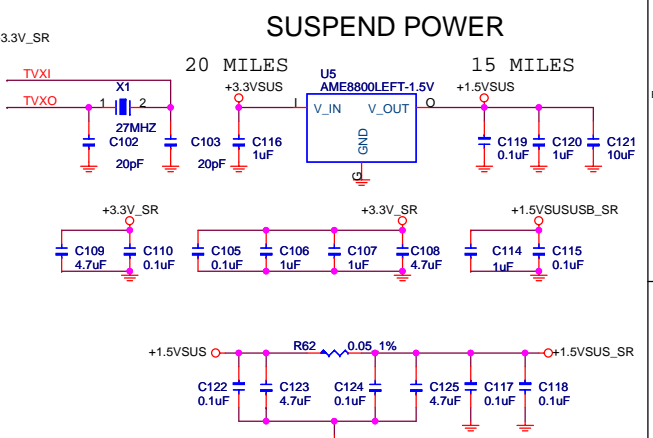
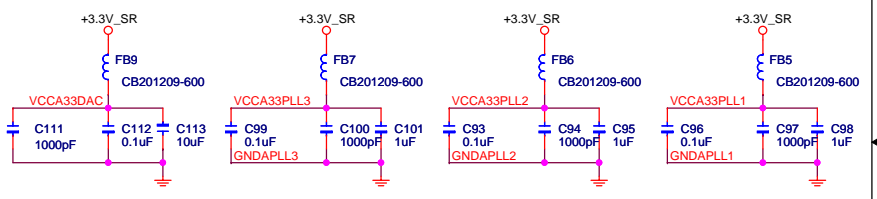
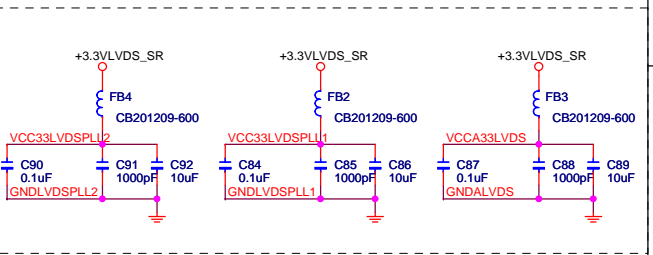
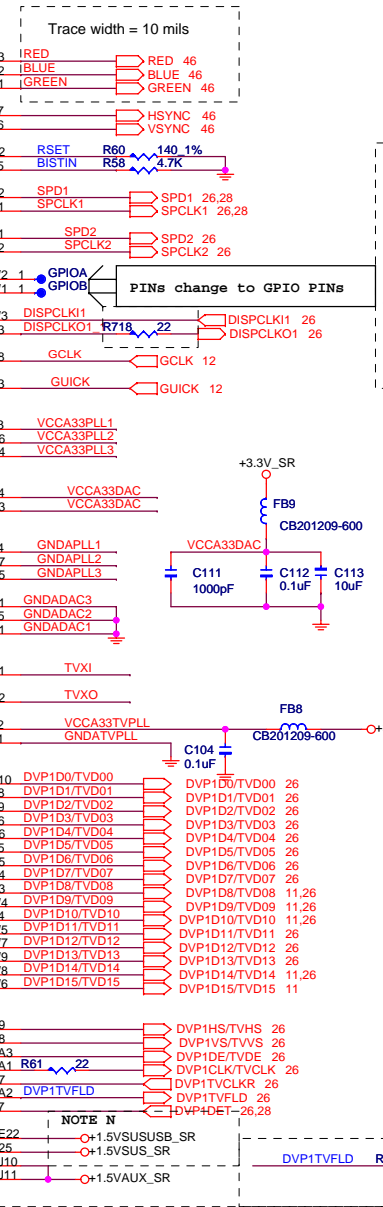
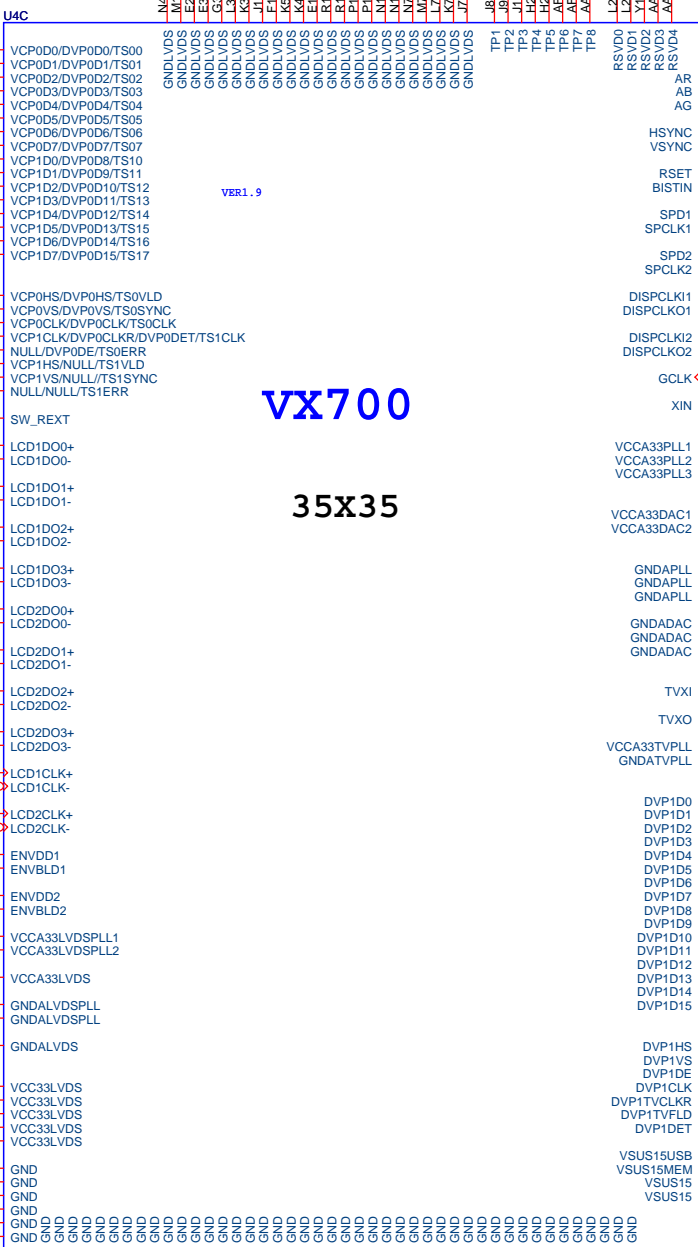
Title: **VX700 Memory BUS**

Size: Custom Document Number: **VT6304A3** Rev: **3.1**

Date: Wednesday, August 02, 2006 Sheet 7 of 53

5 4 3 2 1

5 4 3 2 1

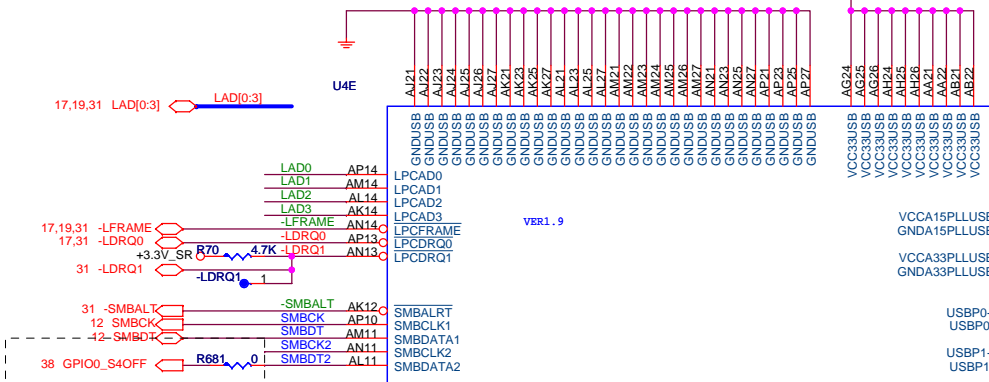
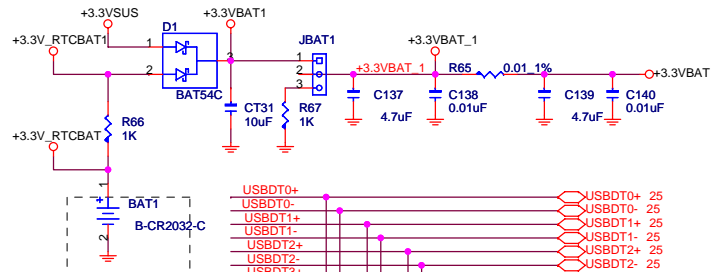
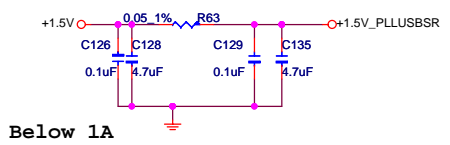
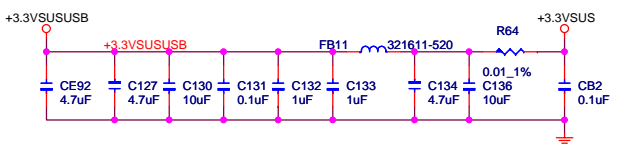


VIA TECHNOLOGIES INC.

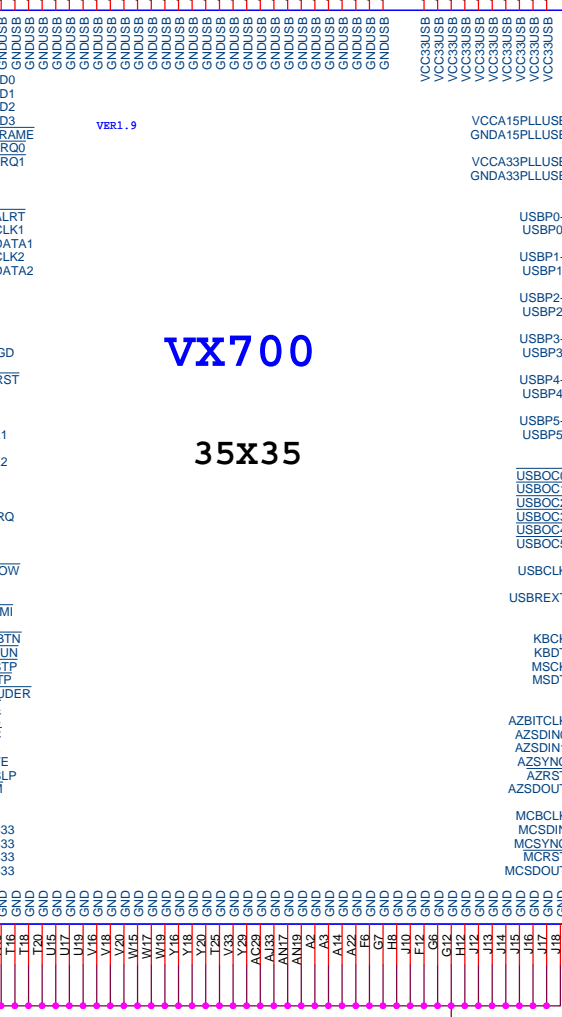
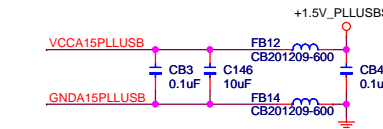
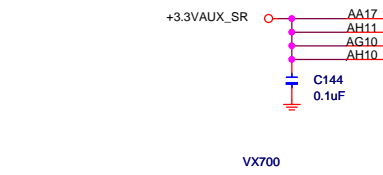
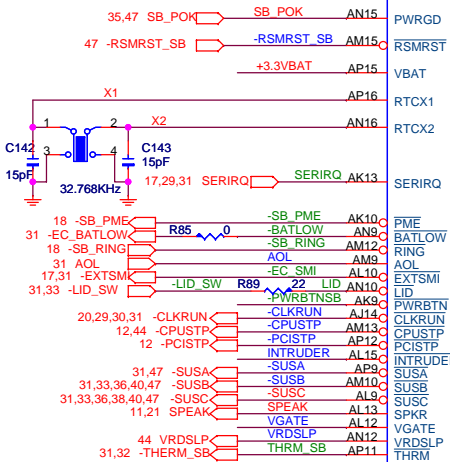
Title: **VX700-VIDEO BUS**

Size: Custom Document Number: **VT6304A3** Rev: **3.1**

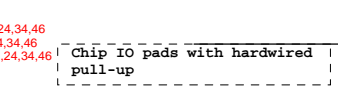
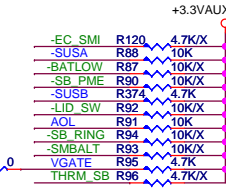
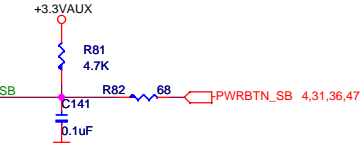
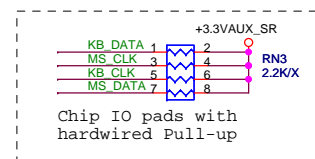
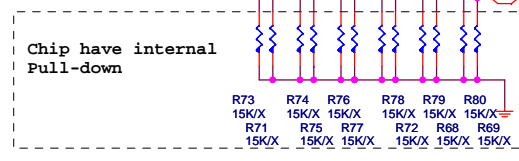
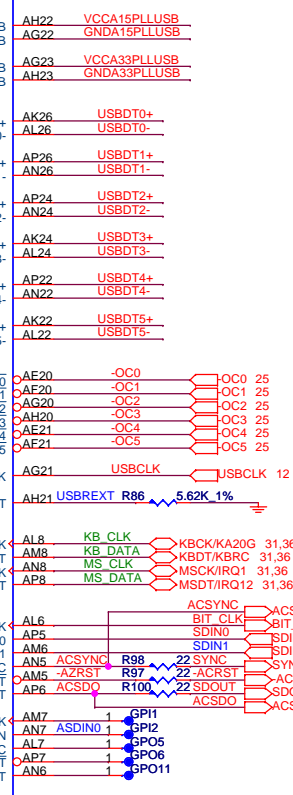
Date: **Wednesday, August 02, 2006** Sheet: **8** of **53**



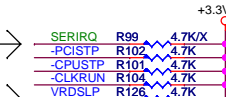
Charles change at 7/27



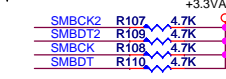
VX700
35X35



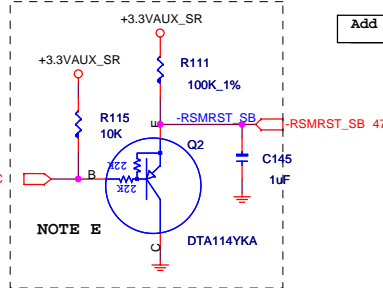
Add pull-up



Change Pull-up Power Plane



Add pull-down



NOTE E

VIA TECHNOLOGIES INC.

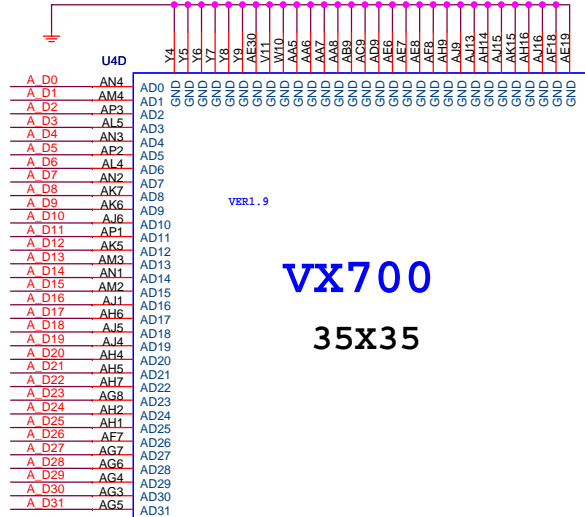
Title: VX700 USB, LPC, AC97, PM

Size: Custom Document Number: VT6304A3 Rev: 3.1

Date: Wednesday, August 02, 2006 Sheet: 9 of 53

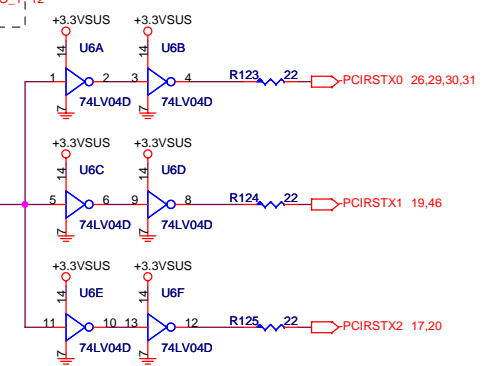
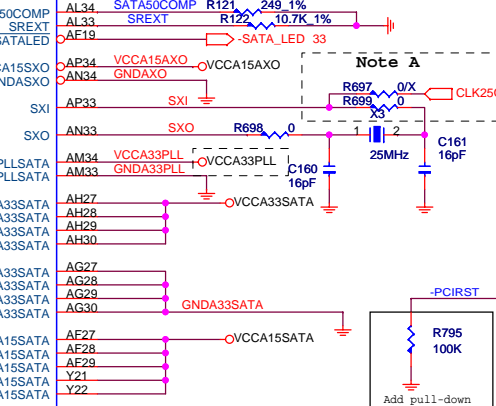
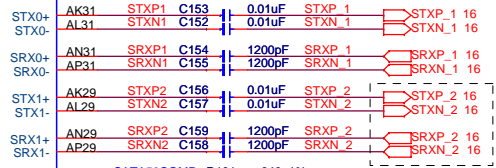
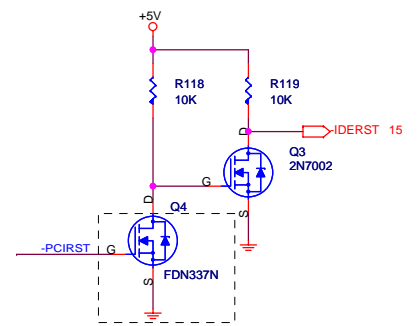
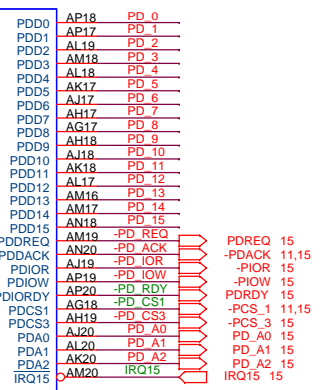
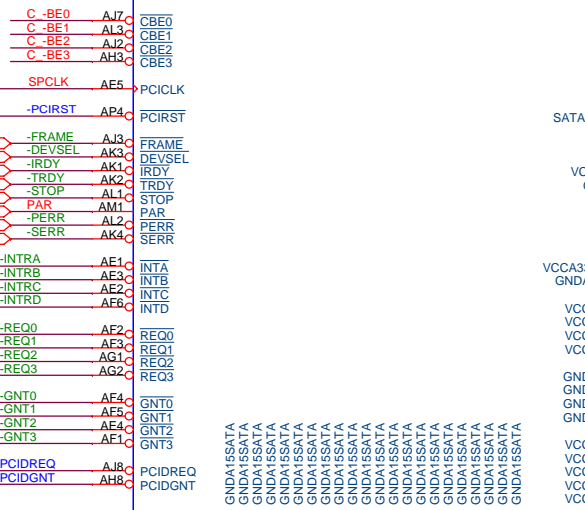
20,29,30 A_D[0:31] A_D[0:31]

PD_[0:15] 15



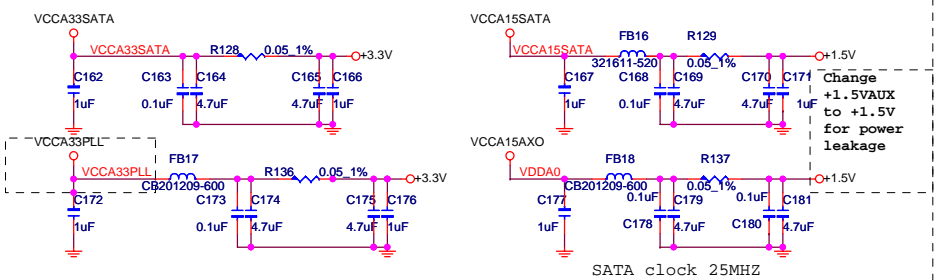
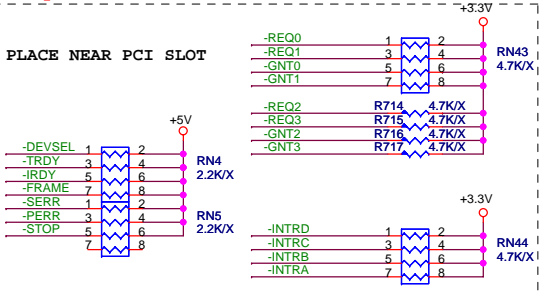
VX700 35X35

20,29,30 C_-BE[0:3] C_-BE[0:3]



46 -DOCK_PRSENT_1 R896 0/X PCIDREQ AJ8
15 -CBLID R700 0/X PCIDGNT AH8

VX700

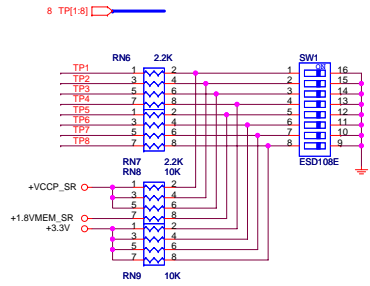


VIA VIA TECHNOLOGIES INC.

Title: VX700 PCI, SATA, PATA BUS

Size: Custom Document Number: VT6304A3 Rev: 3.1

Date: Wednesday, August 02, 2006 Sheet: 10 of 53



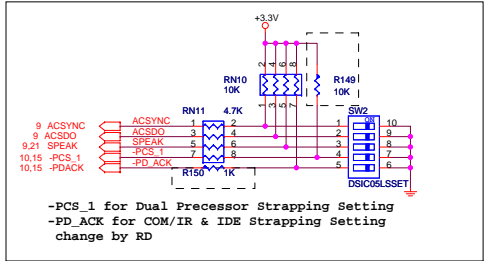
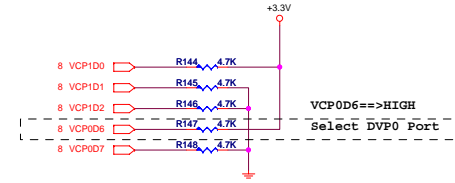
ON : 0
OFF : 1

Table 1

SW1	2	1	DRAM CLK
2'b00	ON	ON	MODE 100
2'b01	ON	OFF	MODE 133
2'b10	OFF	ON	Reserved
2'b11	OFF	OFF	Auto Mode

Table 2

SW1	MODE TYPE	OFF : 1	ON : 0
3	IO QUEUE DEPTH	1 LEVEL	8 LEVEL
4	GTL PULL	NO PULL	PULL
5	RCPU BUS	C3	P4 or V4
6	RCV BUS	V4	P4
7	64/32bit Mode	HD 32 bit	HD 64 bit
8	MEM TYPE	DDR2	DDR1

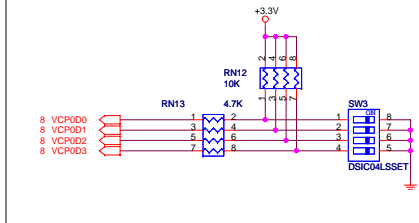


-PCS_1 for Dual Processor Strapping Setting
-PD_ACK for COM/IR & IDE Strapping Setting
change by RD

Table 3

SW2	MODE TYPE	OFF : 1	ON : 0
1	LPC FW Command	Disable	Enable
2	Auto Reboot	Disable	Enable
3	CPU Frequency Strapping	Disable	Enable
4	Dual Processor Configuration	Dual Processor	Single Processor
5	EIDE or COM/IR Port Enable	Enable EIDE Port	Enable COM/IR Port

Option For Panel Type Selection



ON : 0
OFF : 1
X : Don't care

Table 4

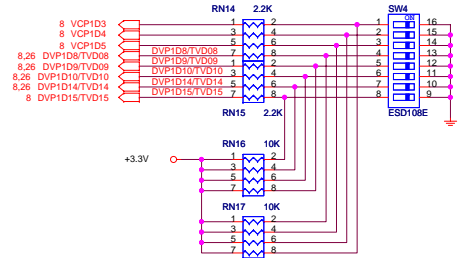
SW4	3	2	1	Description	
	ON	ON	X	DVP-TV output	
		ON	OFF	X	DVP with alpha output
	OFF	ON	ON	DCVI 10-bit data output	
	OFF	ON	OFF	DCVI 8-bit data output	
	OFF	OFF	ON	DCVI 20-bit data output	
	OFF	OFF	OFF	DCVI 16-bit data output	

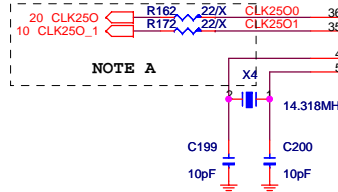
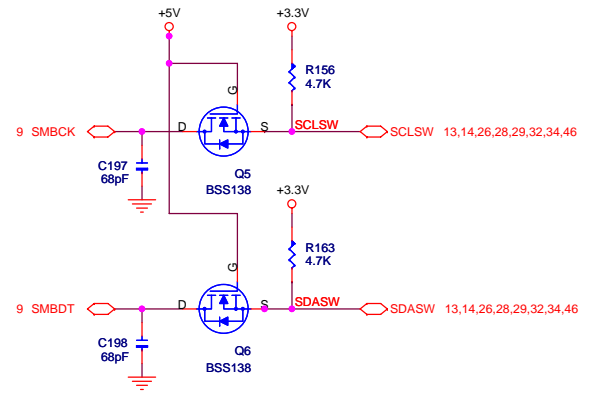
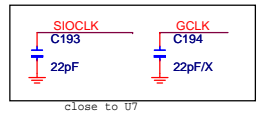
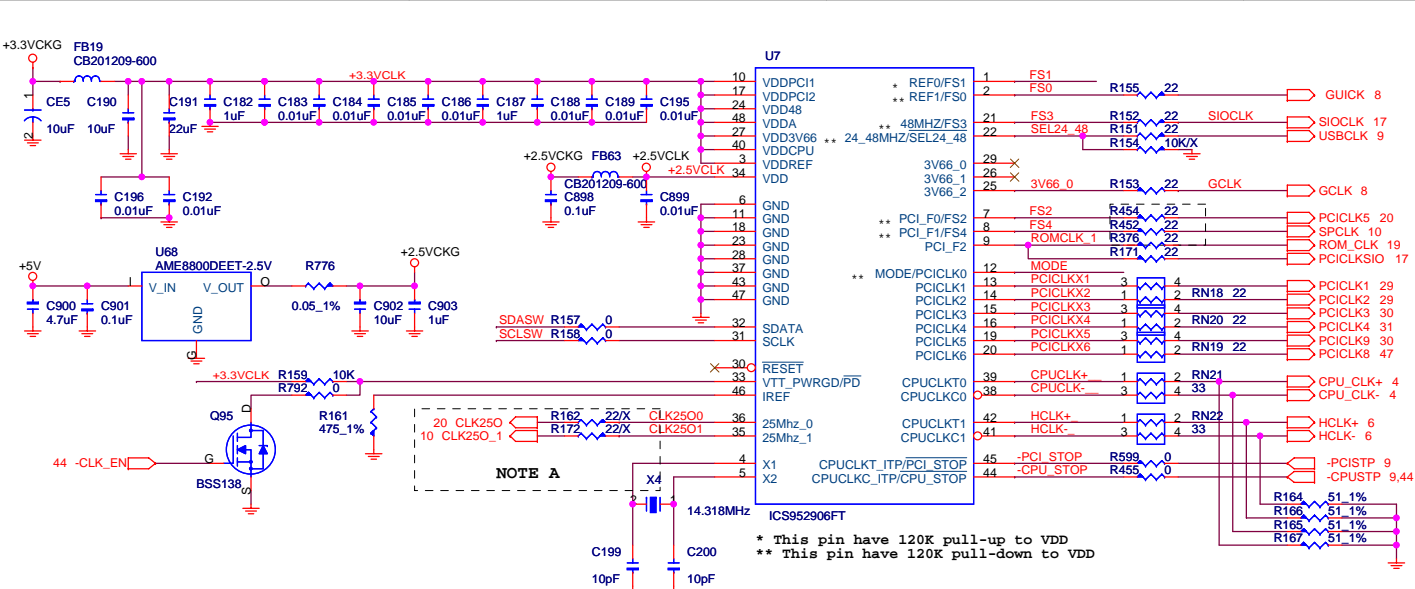
Table 5

SW4	6	5	4	Description
	ON	X	X	DAC A/B/C=R/G/B for CRT
	OFF	ON	ON	DAC A/B/C=C/Y/CVBS for TV
	OFF	ON	OFF	DAC A/B/C=C/Y/Y for TV
	OFF	OFF	ON	DAC A/B/C=R/G/B for TV
	OFF	OFF	OFF	DAC A/B/C=Pr/Y/Pb for TV

Table 6

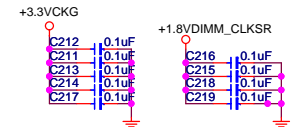
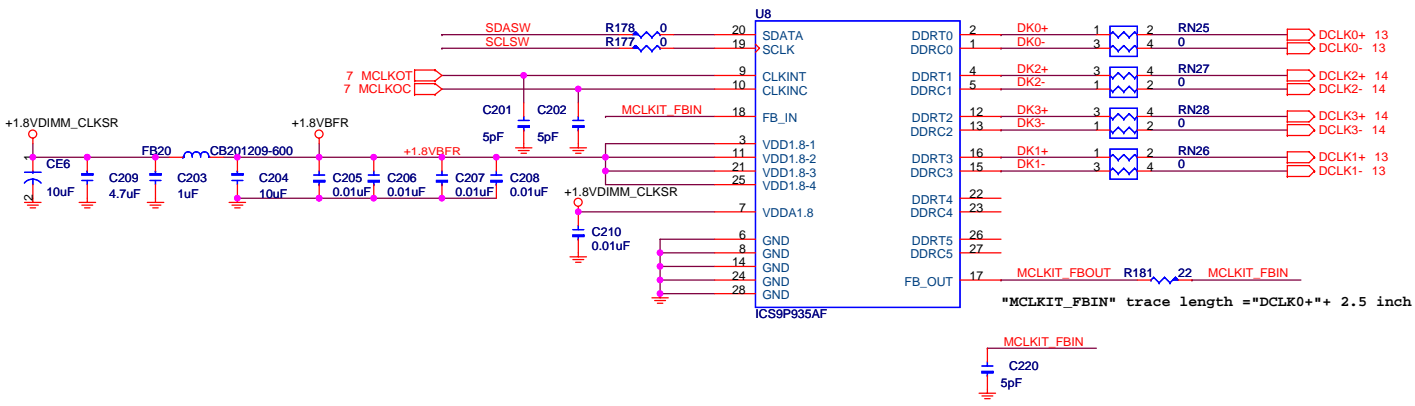
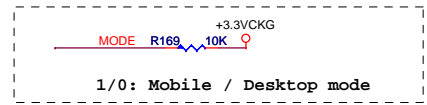
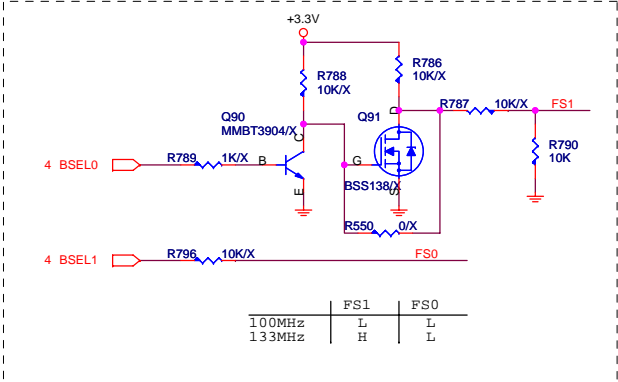
SW4	8	7	Description
	ON	ON	Two Single LVDS Channel : LVDS1 + LVDS2
	ON	OFF	Reserved
	OFF	ON	One Dual LVDS Channel (High resolution panel)
	OFF	OFF	One DVI only





* This pin have 120K pull-up to VDD
 ** This pin have 120K pull-down to VDD

AUTO DETECT CIRCUIT



"MCLKIT_FBIN" trace length = "DCLK0" + 2.5 inch

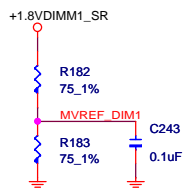
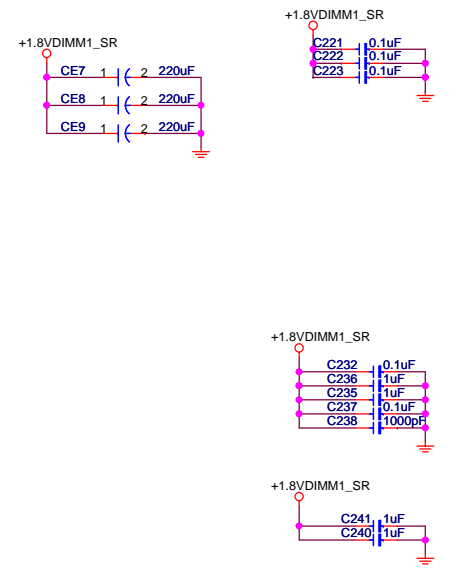
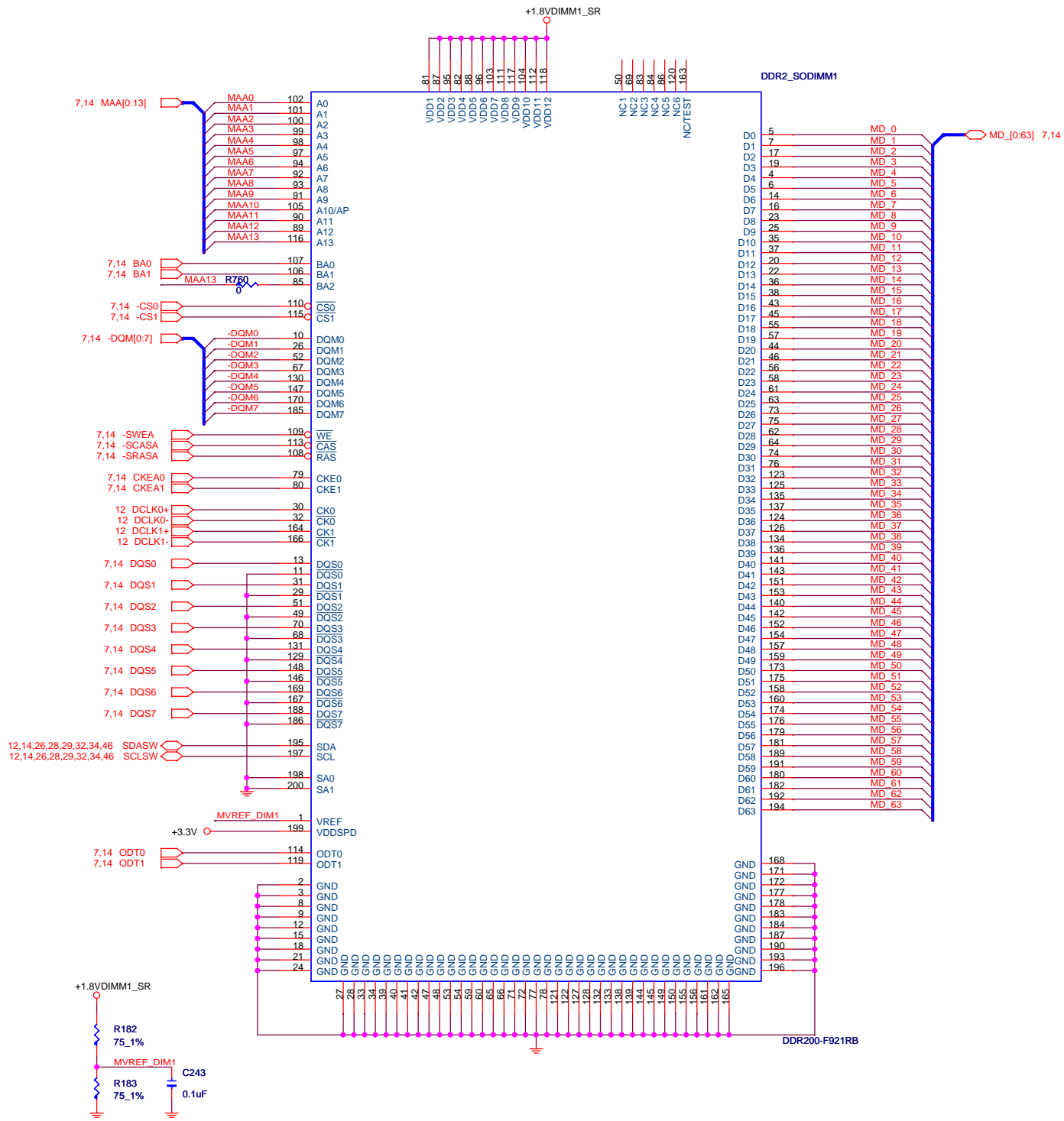
VIA Confidential

VIA TECHNOLOGIES, INC.

File: **CLOCK SYNTHESIZERS**

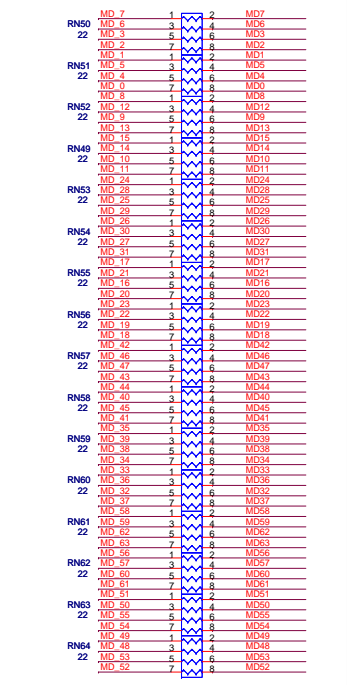
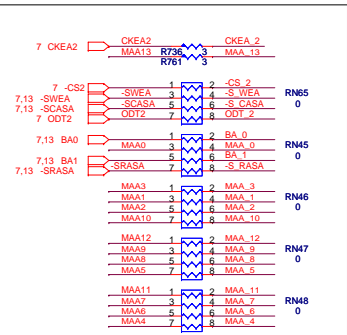
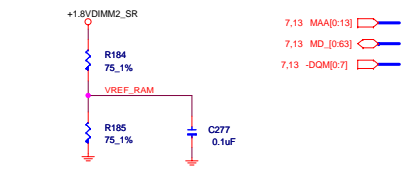
Size C Document Number **VT6304A3** Rev 3.1

Date: Wednesday, August 02, 2006 Sheet 12 of 53

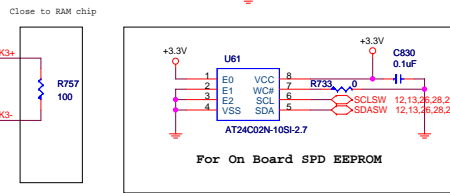
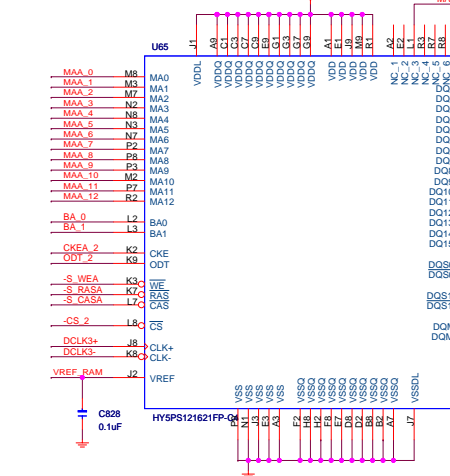
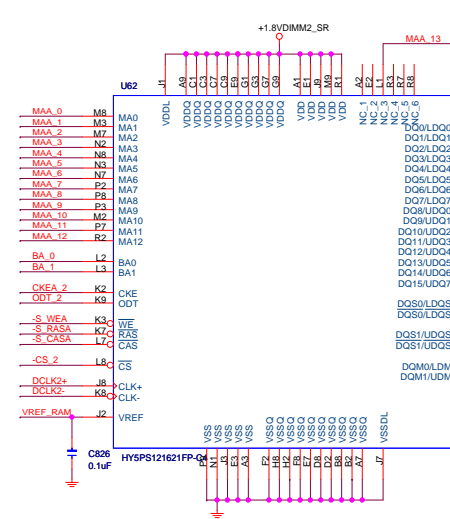


VIA Confidential

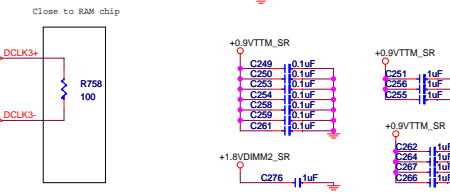
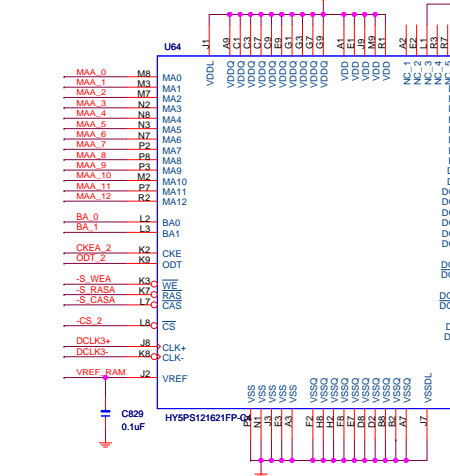
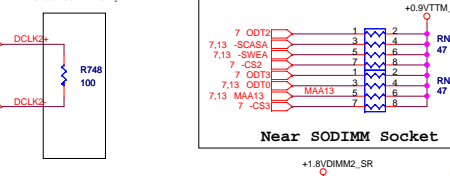
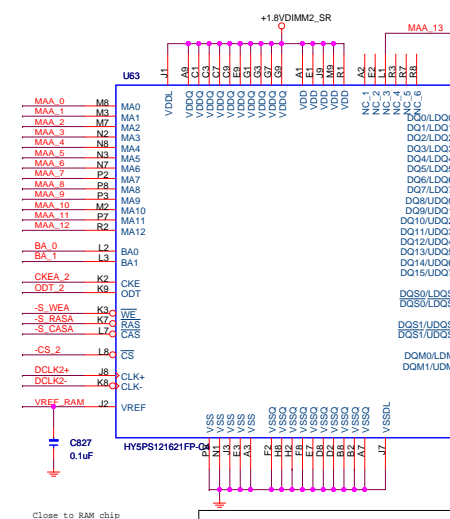
VIA TECHNOLOGIES, INC.		
Title: DDR2 MODULES_DIMM1		
Size: C	Document Number: VT6304A3	Rev: 3.1
Date: Wednesday, August 02, 2006	Sheet: 13	of 53



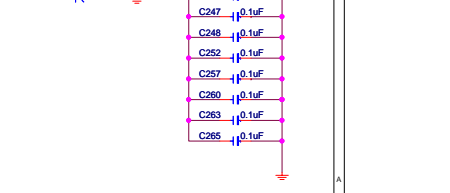
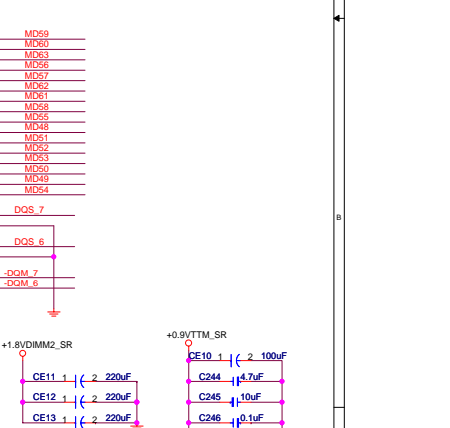
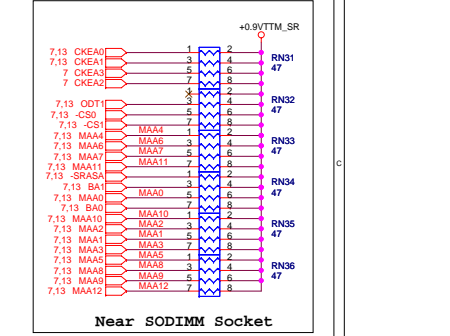
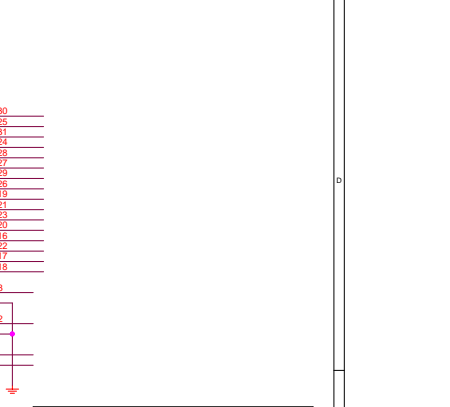
Near SODIMM Socket



For On Board SPD EEPROM



Near SODIMM Socket

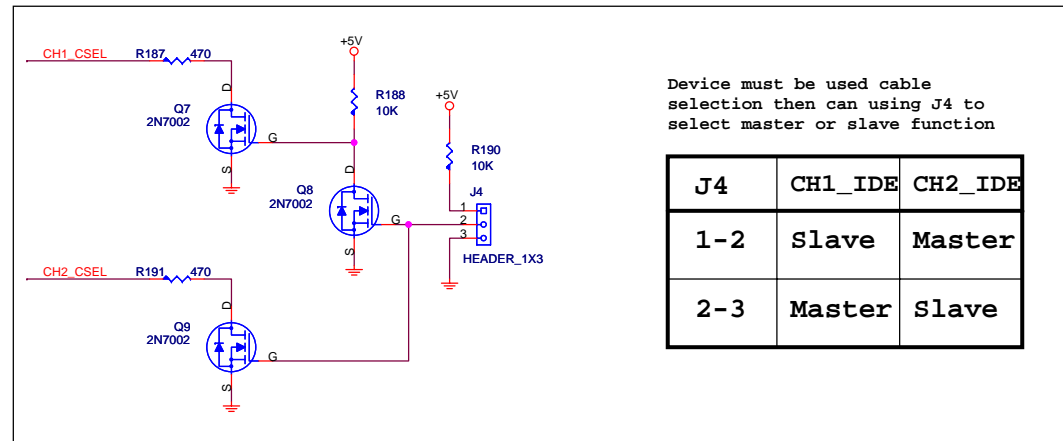
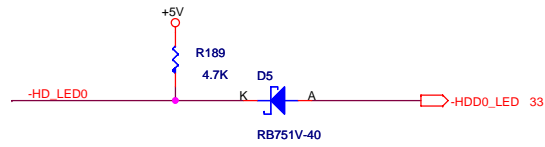
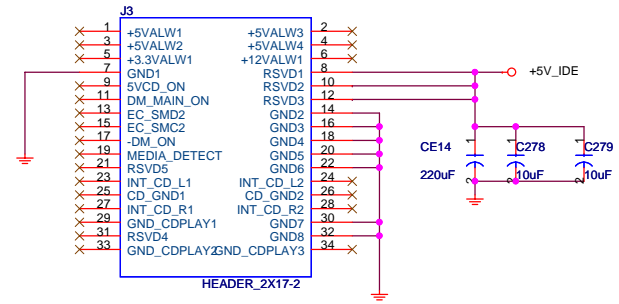
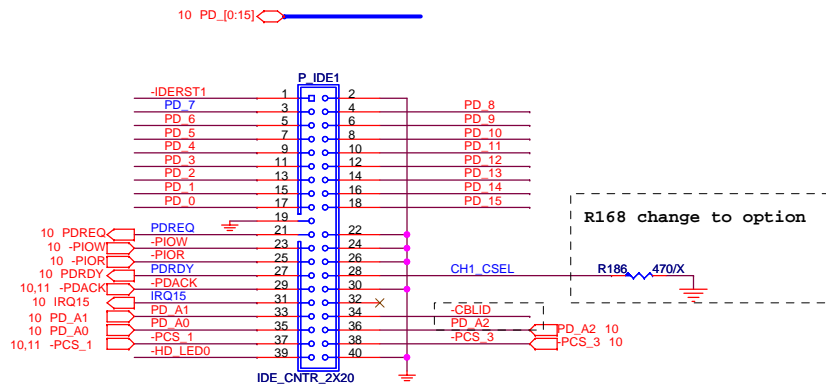


Near SODIMM Socket

VIA Confidential

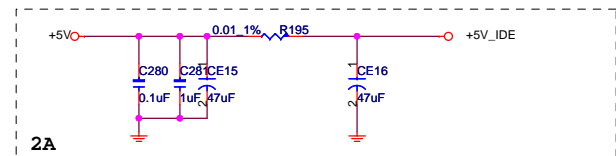
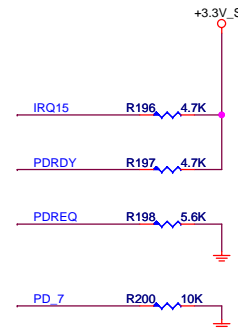
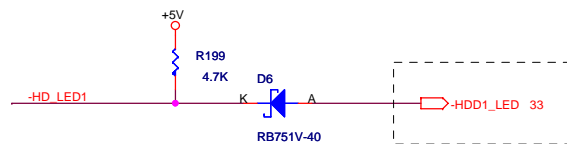
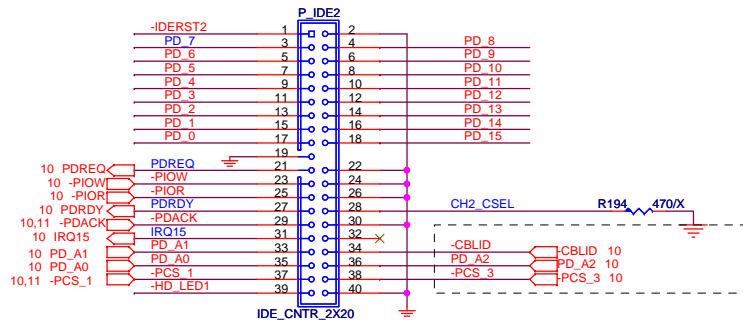
Title			ON Board DDR2 Memory
Size	Document Number	VT6304A3	
Date:	Wednesday, August 02, 2006	Sheet	14 of 53
Rev	3.1		

CH1 IDE



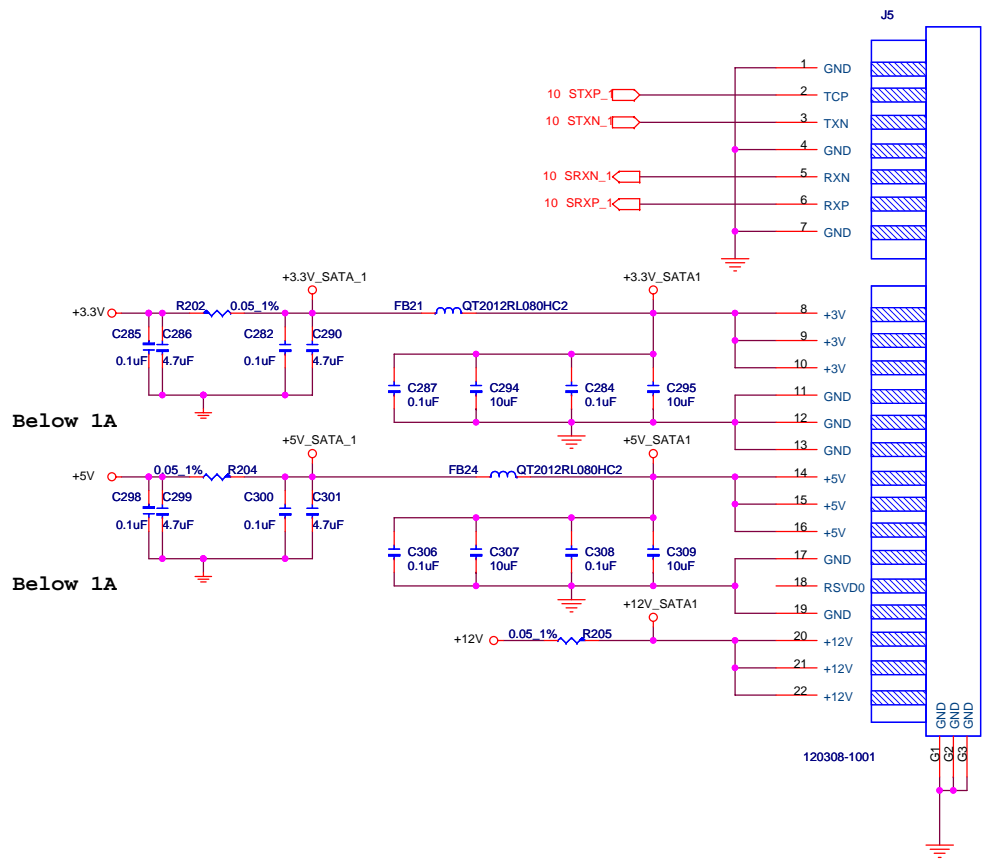
J4	CH1_IDE	CH2_IDE
1-2	Slave	Master
2-3	Master	Slave

CH2 IDE



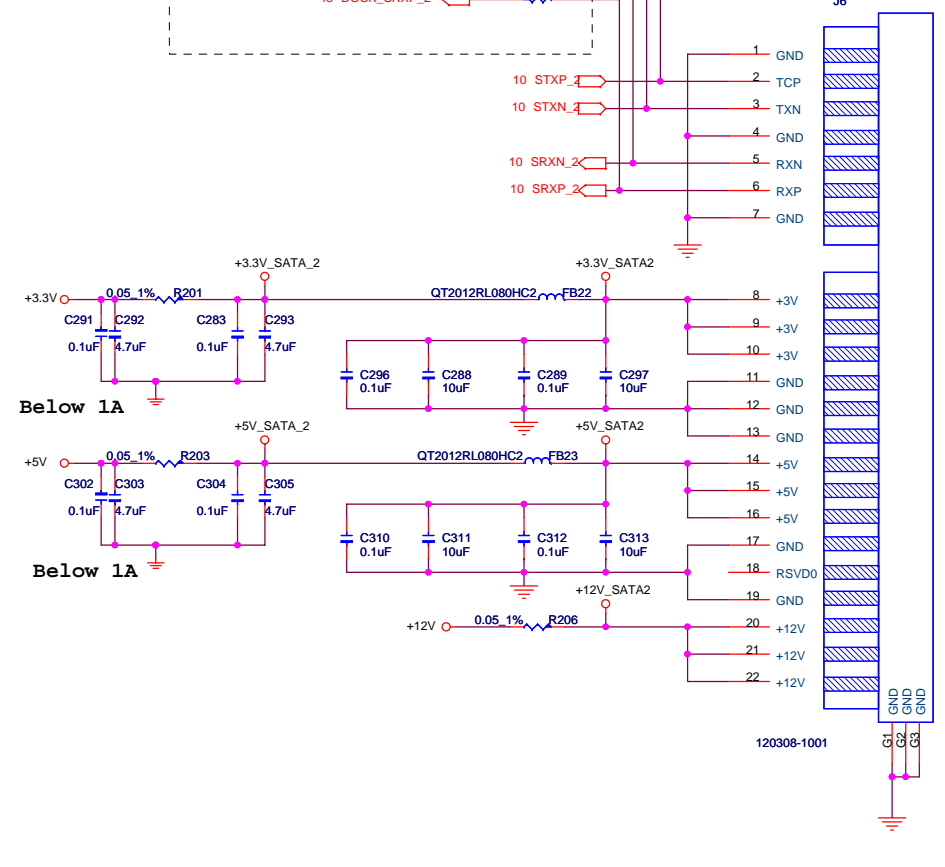
For reserved only by Charles at 7/28

46 DOCK_STXP_2 R702 0/X
 46 DOCK_STXN_2 R703 0/X
 46 DOCK_SRXN_2 R704 0/X
 46 DOCK_SRXP_2 R705 0/X



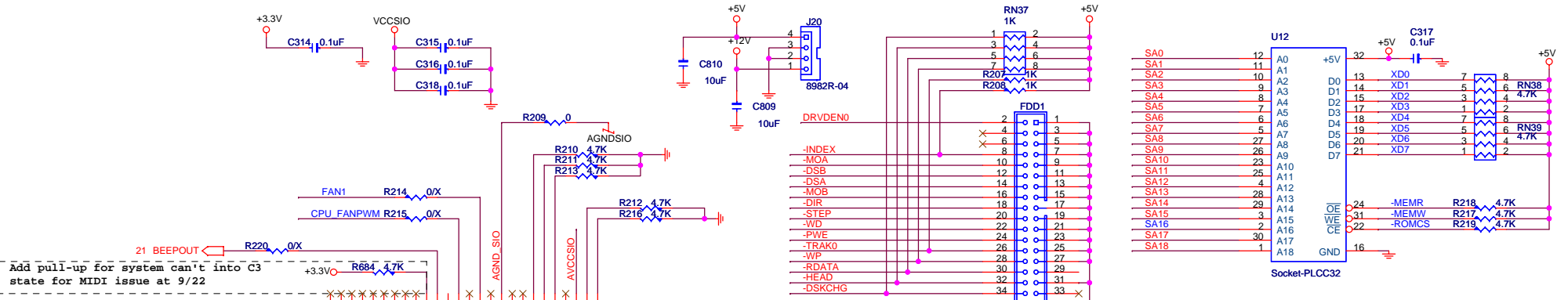
Below 1A

Below 1A

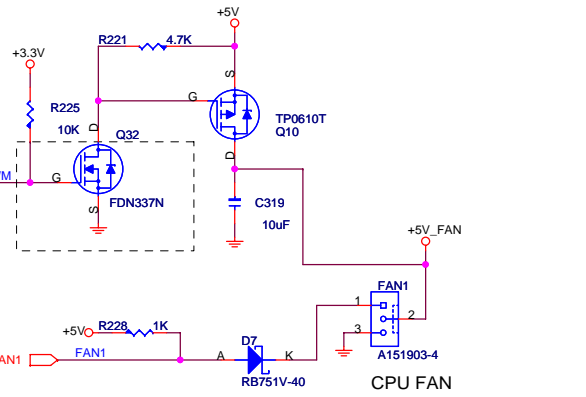
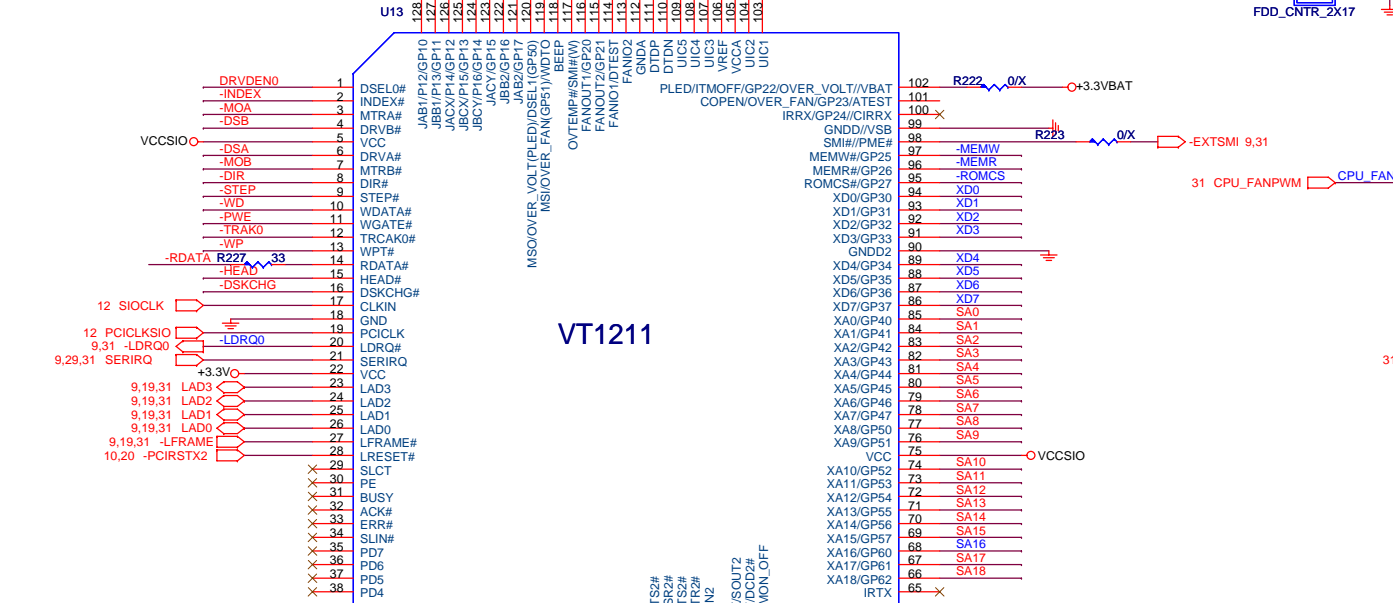


Below 1A

Below 1A



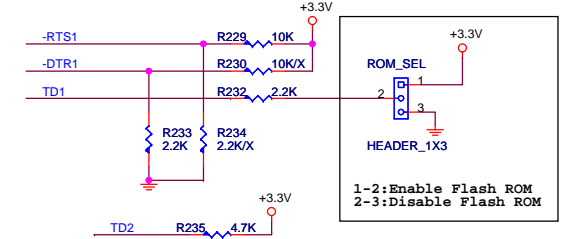
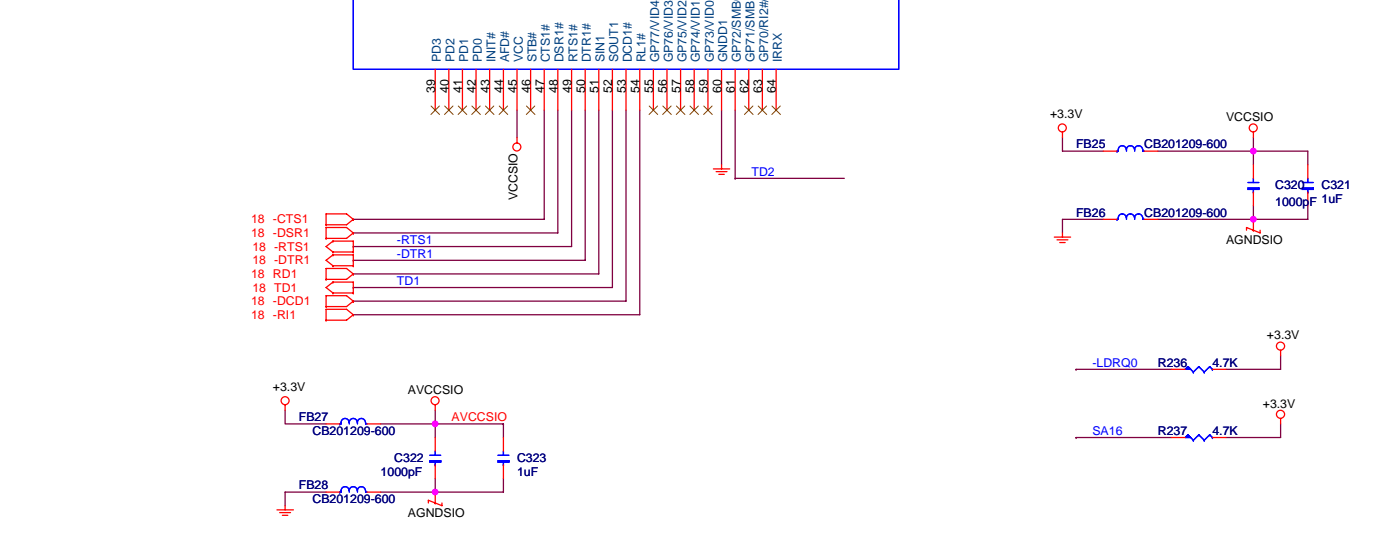
Add pull-up for system can't into C3 state for MIDI issue at 9/22



Super I/O strapping For VT1211

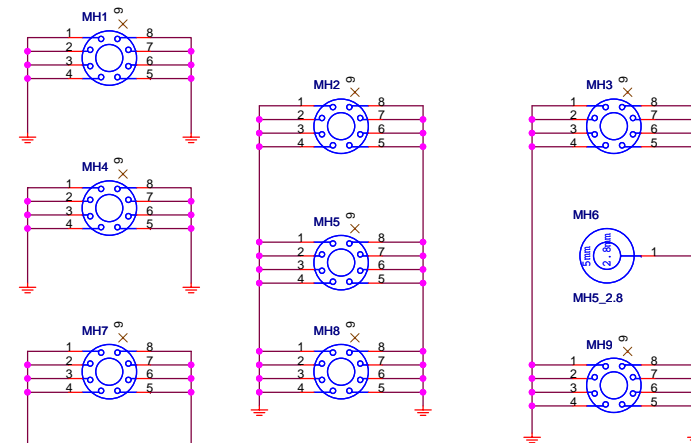
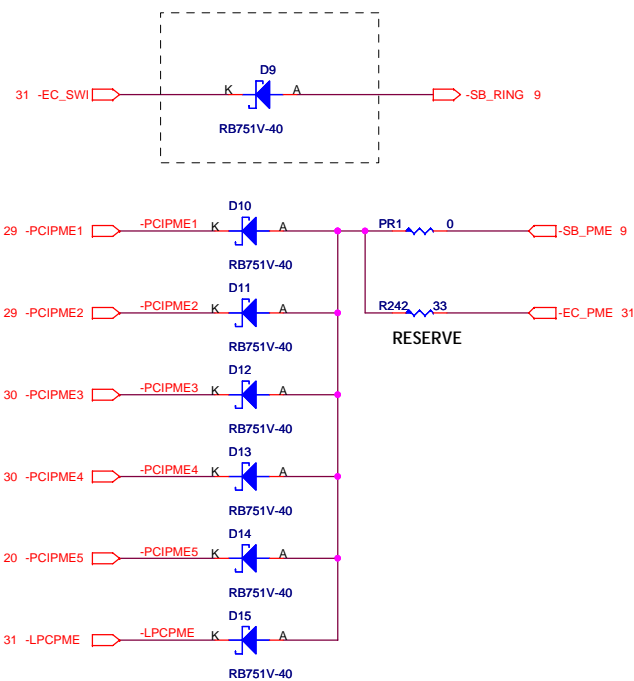
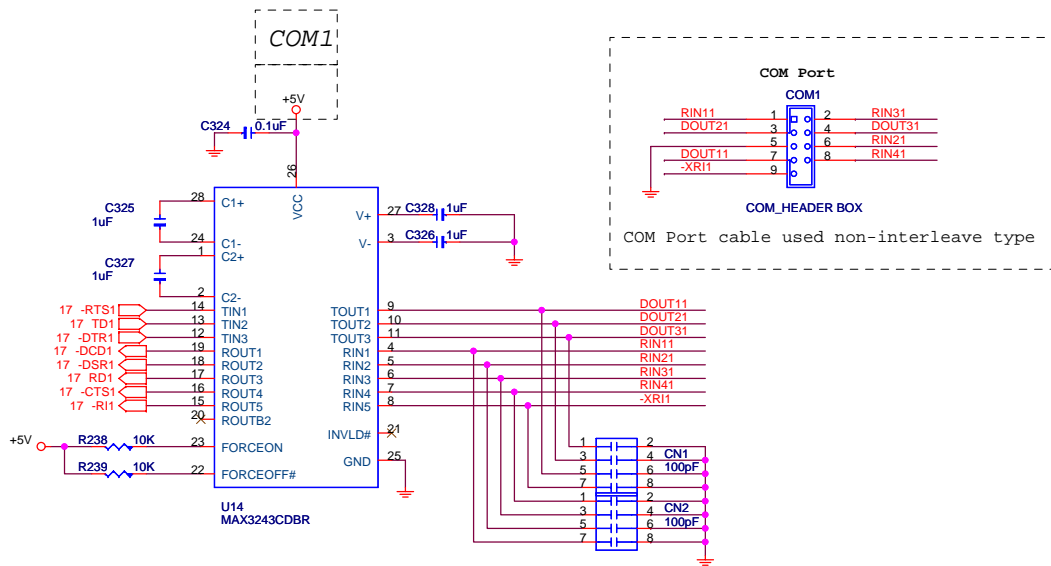
-ETS1 : BASE ADDRESS SELECTION TD1 : ROM I/F SELECTION
 0:4Eh/4Fh 0:Disable Flash Rom
 1:2Eh/2Fh 1:Enable Flash Rom

-DTR1 : TEST MODE SELECTION TD2 : CLOCK INPUT SELECTION
 0:NORMAL MODE 0:24MHz
 1:TEST MODE 1:48MHz



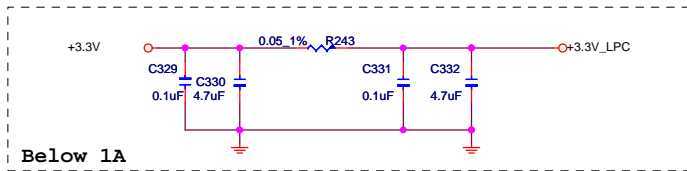
VIA Confidential

VIA		VIA TECHNOLOGIES INC.	
Title LPC SUPER IO, ISA ROM & FAN			
Size C	Document Number VT6304A3	Rev 3.1	
Date: Wednesday, August 02, 2006 Sheet 17 of 53			

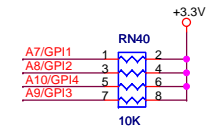
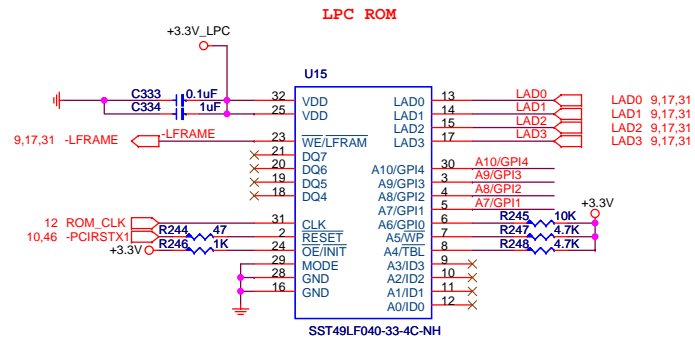


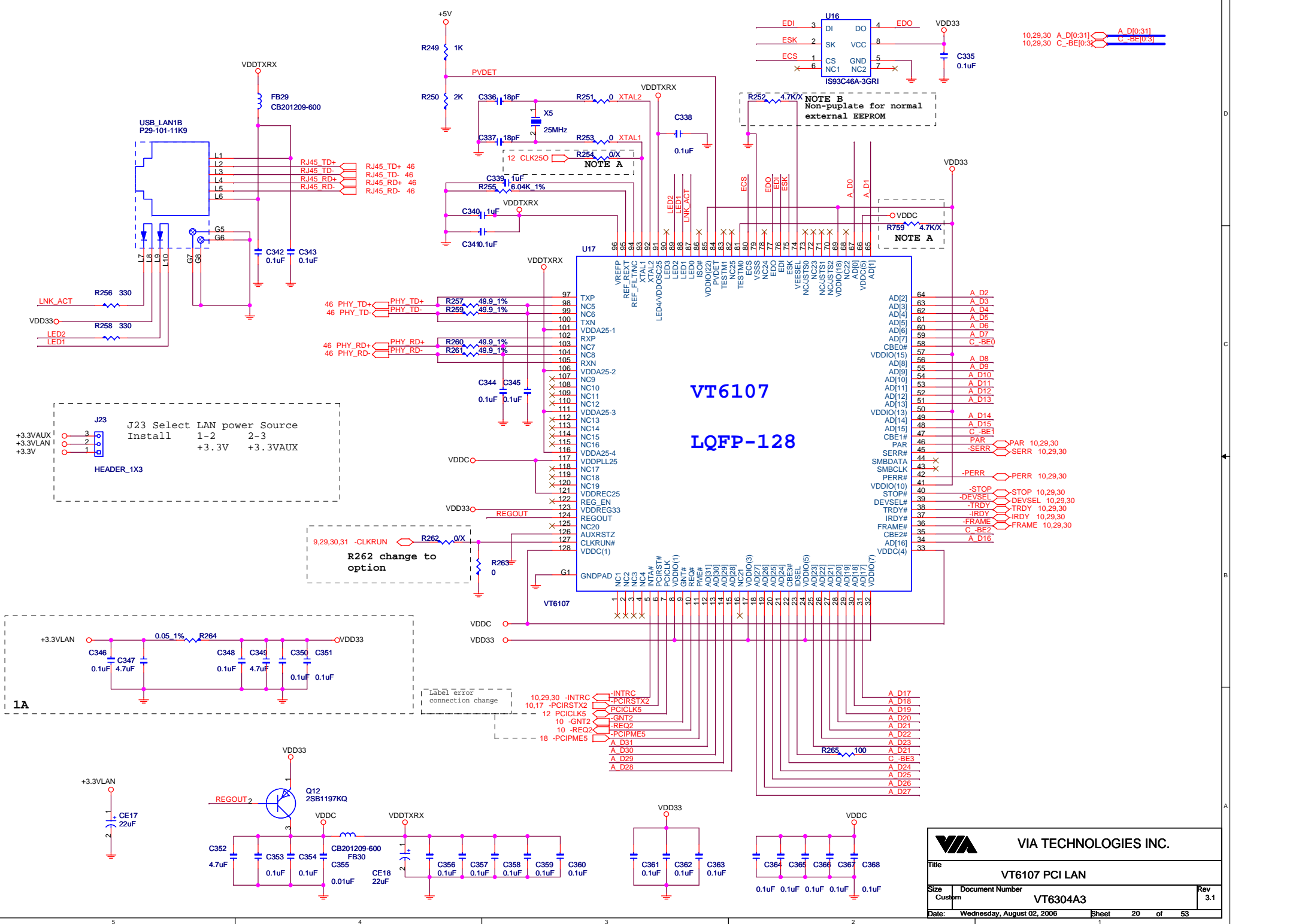
VIA Confidential

VIA		VIA TECHNOLOGIES INC.	
Title			
PME,RI, COM PORT			
Size	Document Number		Rev
C	VT6304A3		3.1
Date:	Wednesday, August 02, 2006	Sheet	18 of 53



Below 1A





VT6107
LQFP-128

10,29,30 A_D[0:3] A_D[0:3]
10,29,30 C_BE[0:3] C_BE[0:3]

NOTE B
Non-puplate for normal external EEPROM

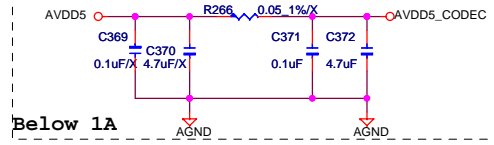
NOTE A

R262 change to option

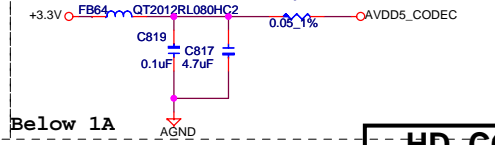
1A

Label error connection change

VIA VIA TECHNOLOGIES INC.		
Title VT6107 PCI LAN		
Size Custom	Document Number VT6304A3	Rev 3.1
Date: Wednesday, August 02, 2006	Sheet 20	of 53



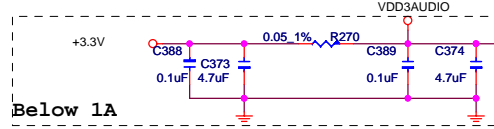
Below 1A



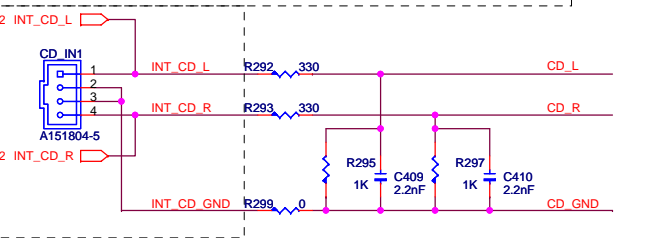
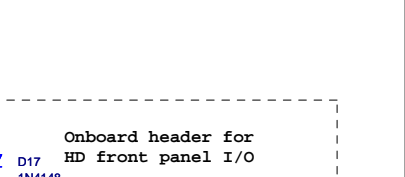
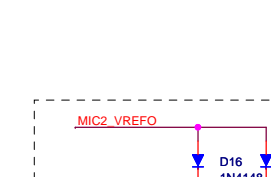
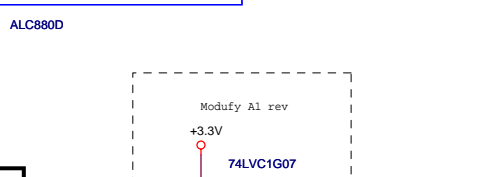
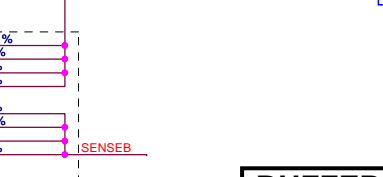
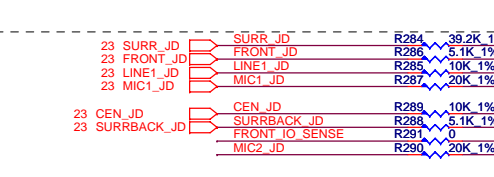
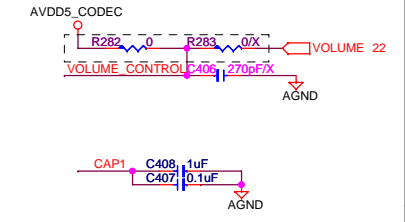
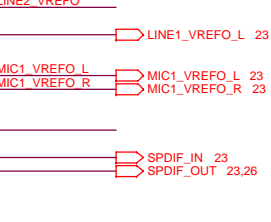
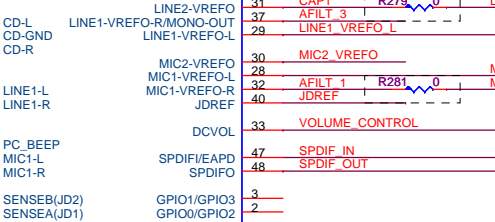
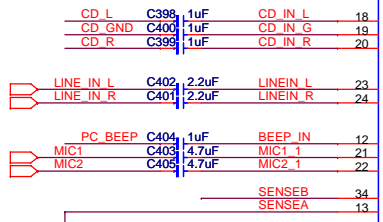
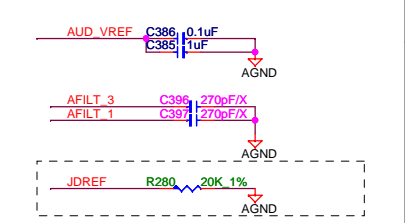
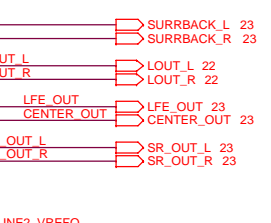
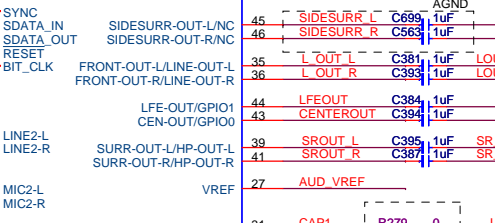
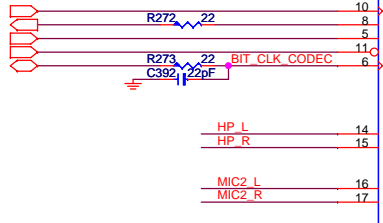
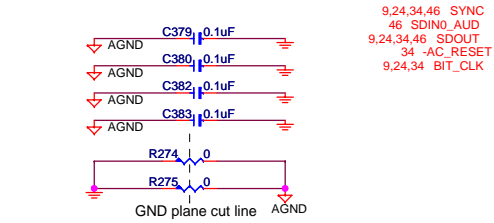
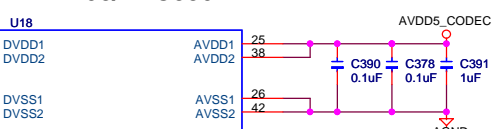
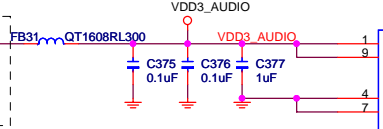
Below 1A

HD CODEC

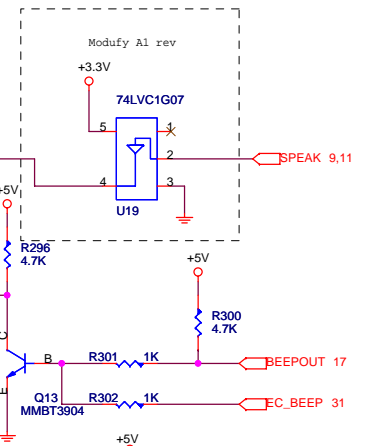
VT1708/ALC880



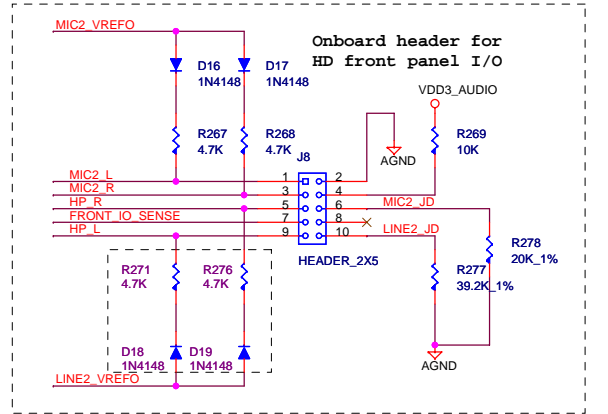
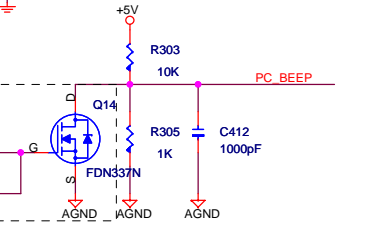
Below 1A



BUZZER



SPEAK_IN

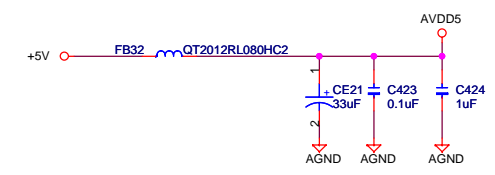
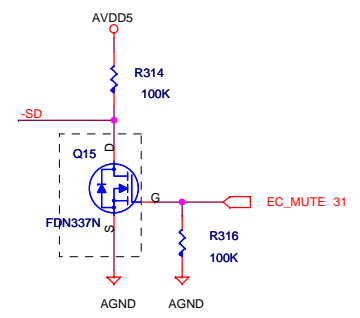
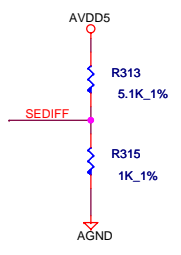
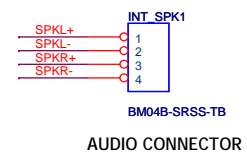
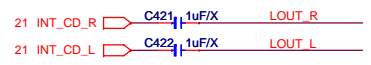
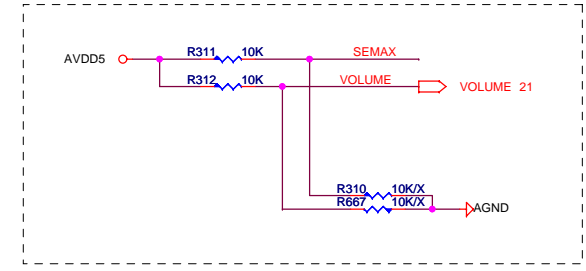
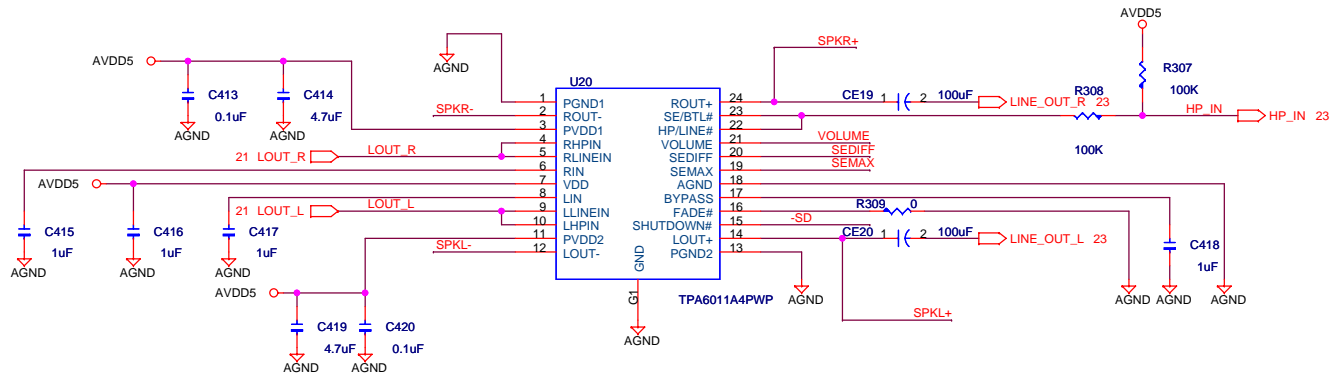


VT1708	ALC880
UN-MOUNT	UN-MOUNT
D18, R271, D19, R276, R283, R279, R281, R282, R332, R334	C406, C396, C397
R280=5.1K_1%	R280=20K_1%


VIA Confidential

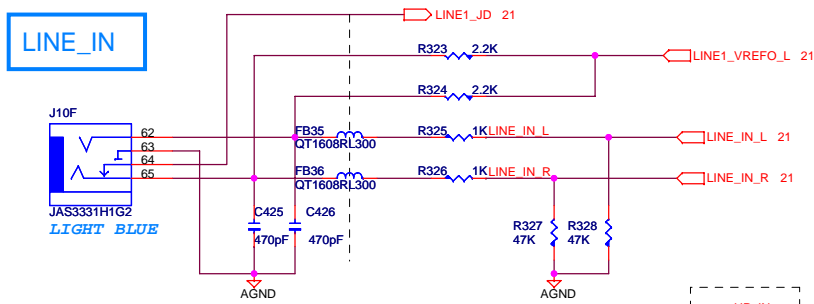
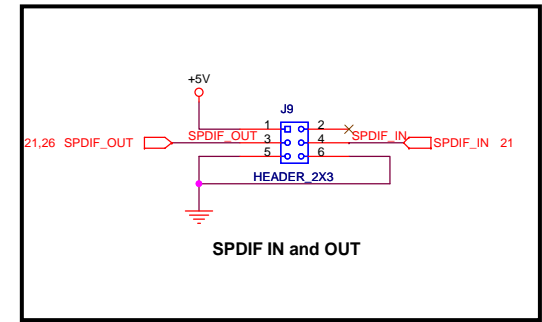
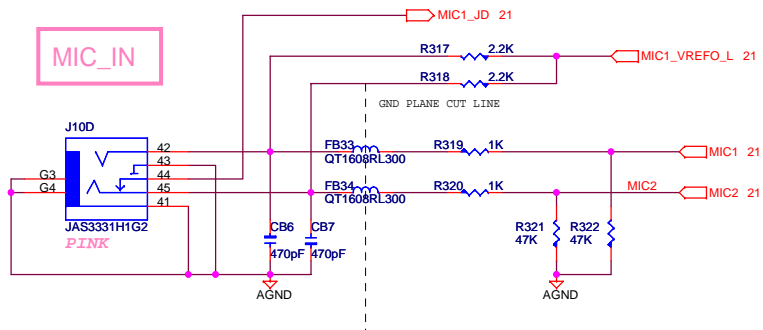
VIA TECHNOLOGIES INC.	
Title: HD CODEC	
Size: C	Document Number: VT6304A3
Date: Wednesday, August 02, 2006	Rev: 3.1
Sheet: 21	of 53

AUDIO_AMP

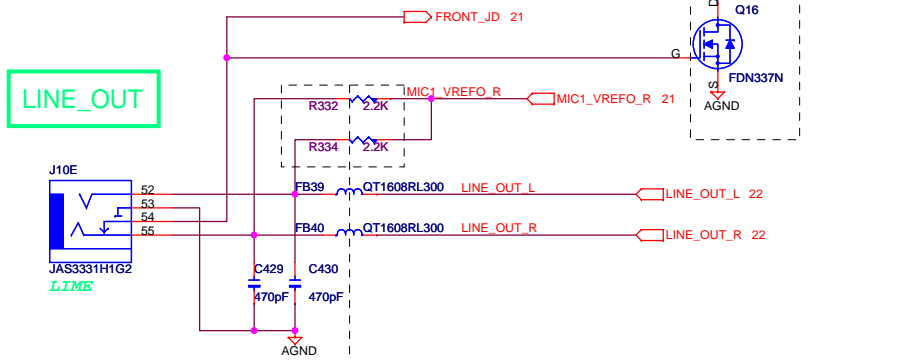
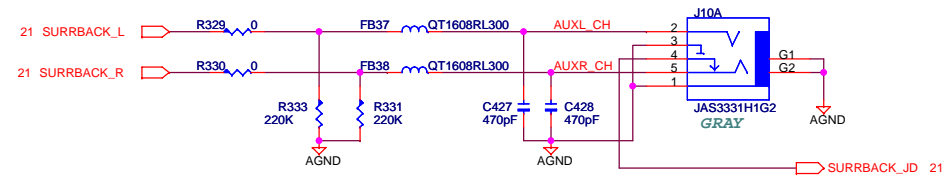


VIA Confidential

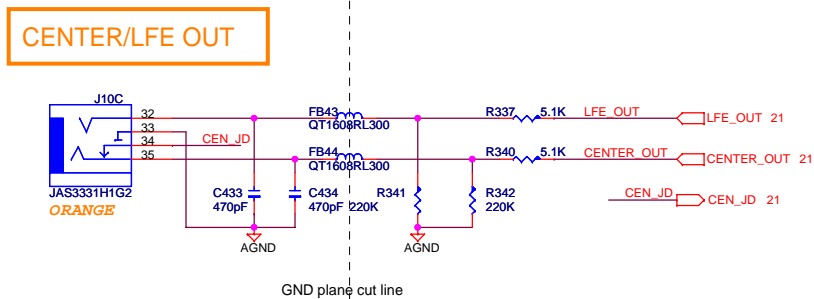
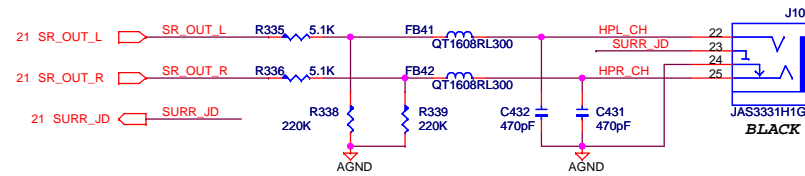
 VIA TECHNOLOGIES, INC.		
Title		
MOBILE AMP.		
Size	Document Number	Rev
C	VT6304A3	3.1
Date: Wednesday, August 02, 2006		
Sheet		of
1		53



SIDESURROUT(1708)

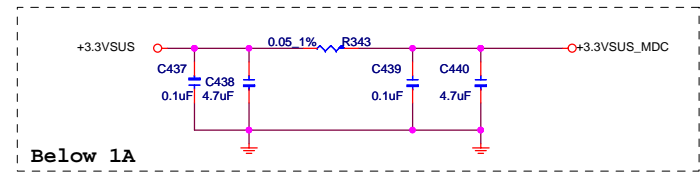
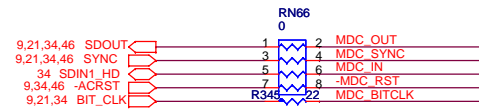
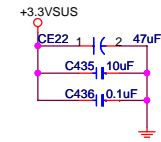
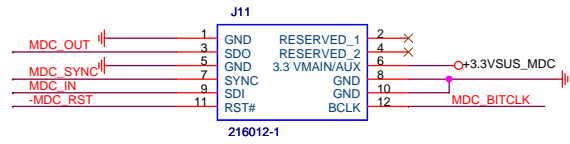


SR CHANNEL (R/L OUT)

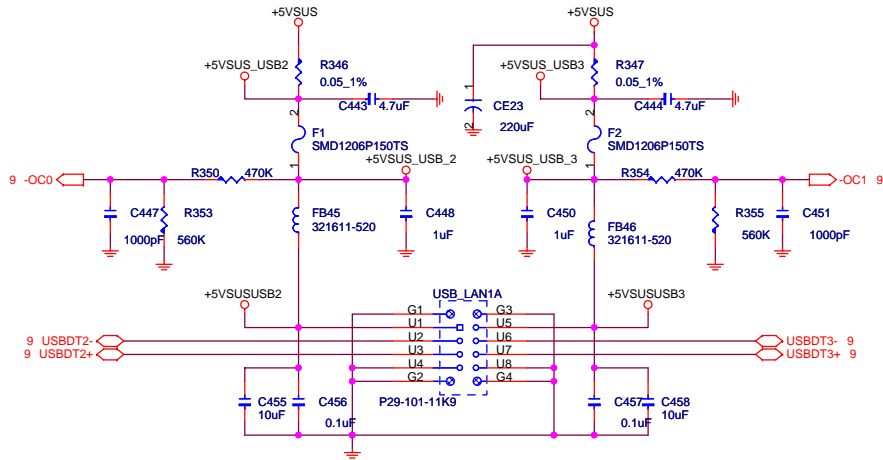


VIA Confidential

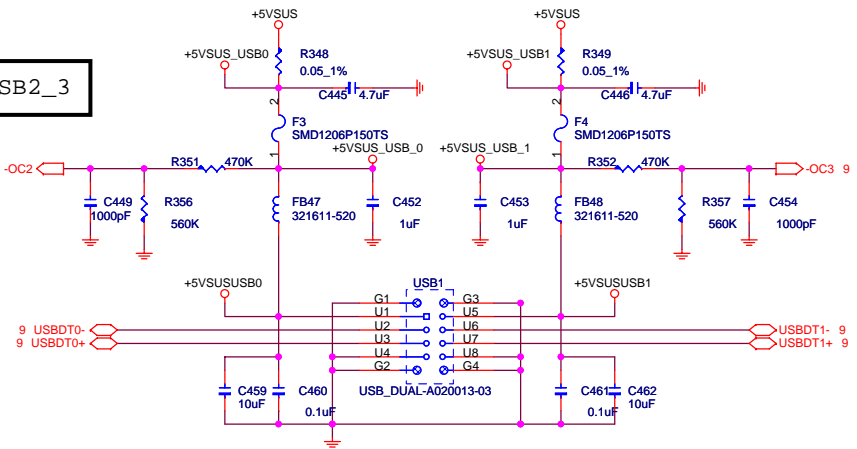
		VIA TECHNOLOGIES INC.	
Title		AUDIO JACK	
Size	Document Number	Rev	
C	VT6304A3	3.1	
Date:	Wednesday, August 02, 2006	Sheet	23 of 53



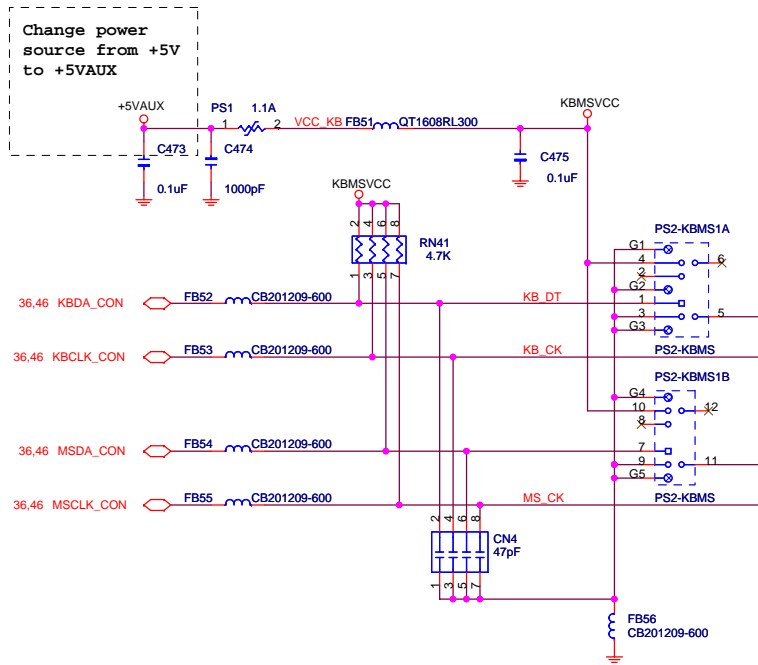
USB0_1



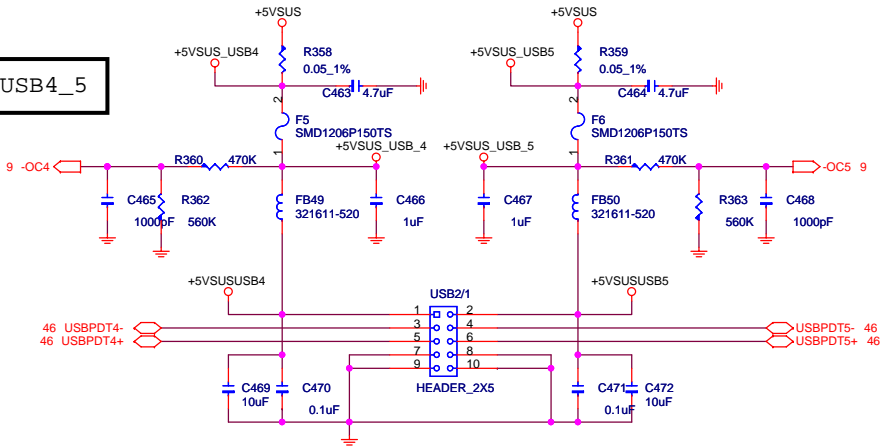
USB2_3



PS2

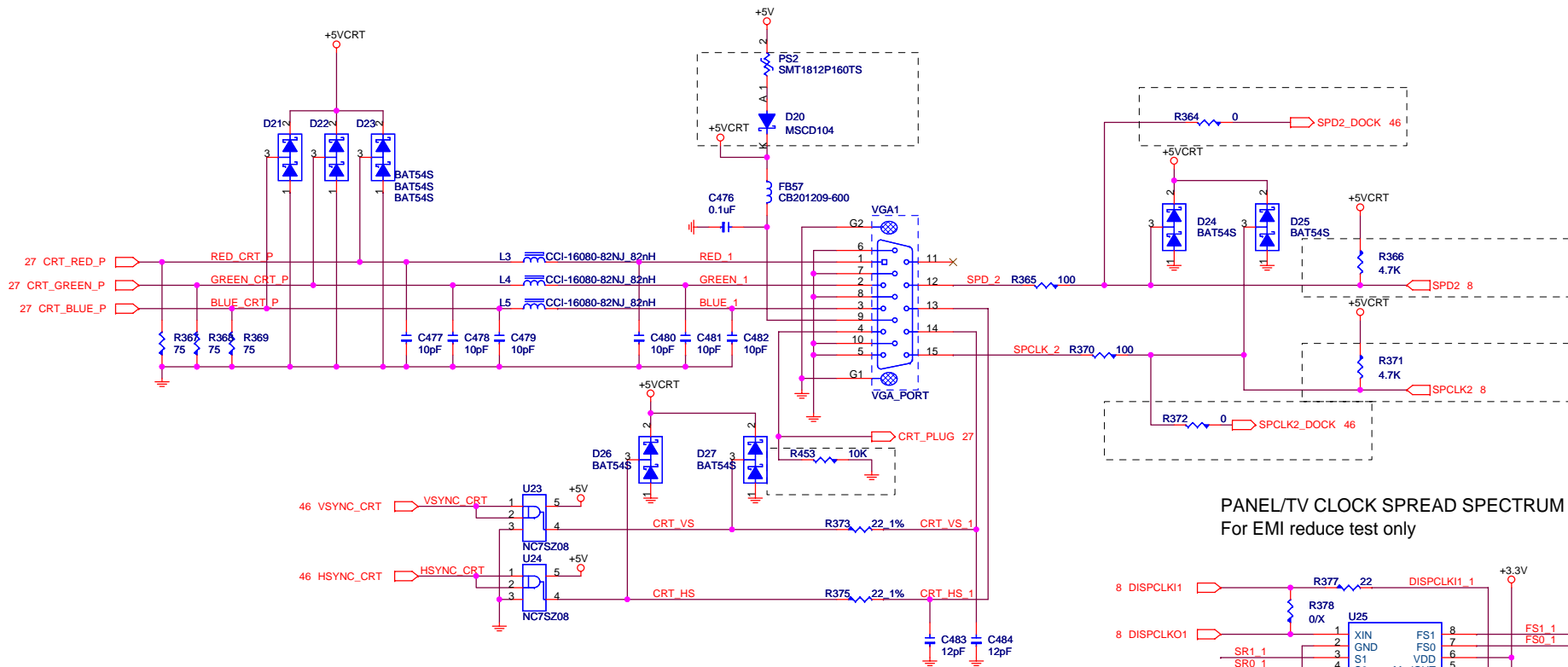


USB4_5

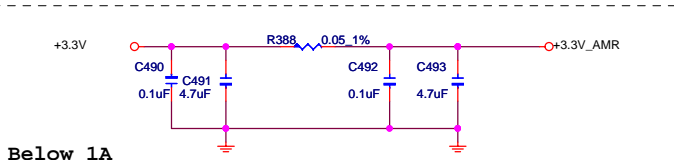
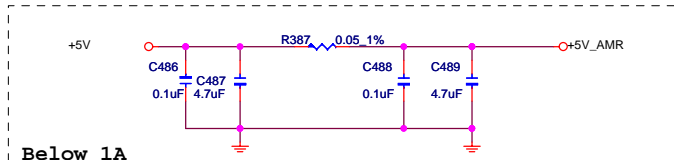
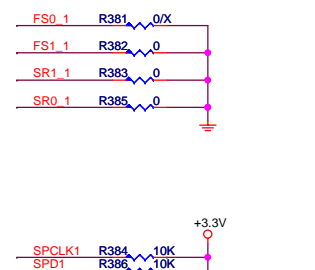
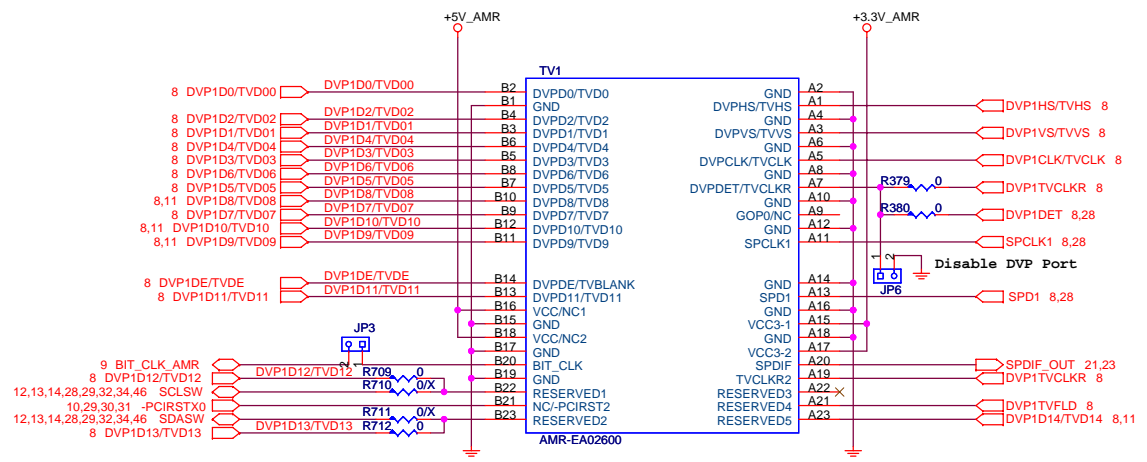
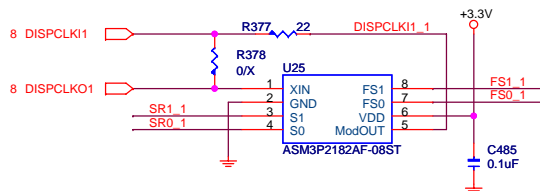


VIA Confidential

		VIA TECHNOLOGIES INC.	
Title KB/MOUSE & USB CONNECTOR			
Size Custom	Document Number VT6304A3	Rev 3.1	
Date: Wednesday, August 02, 2006	Sheet 25	of 53	

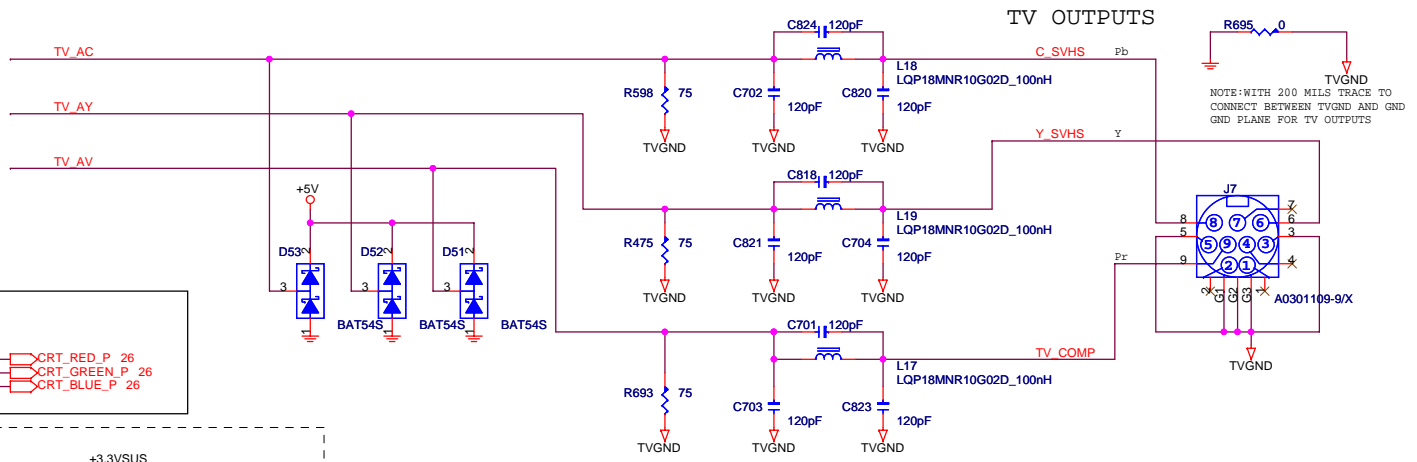
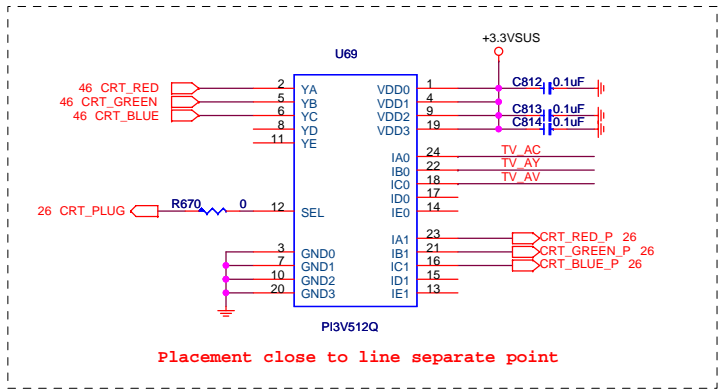
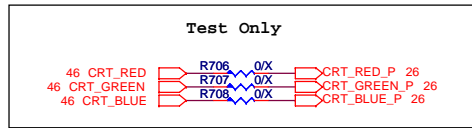


PANEL/TV CLOCK SPREAD SPECTRUM
For EMI reduce test only



VIA Confidential

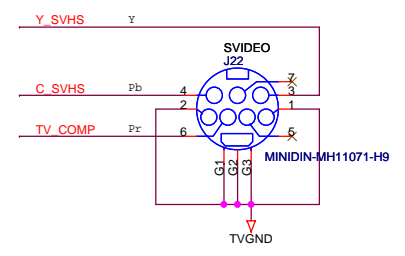
VIA TECHNOLOGIES INC.		
Title VGA CONN & AMR SLOT		
Size C	Document Number VT6304A3	Rev 3.1
Date: Wednesday, August 02, 2006	Sheet 26	of 53

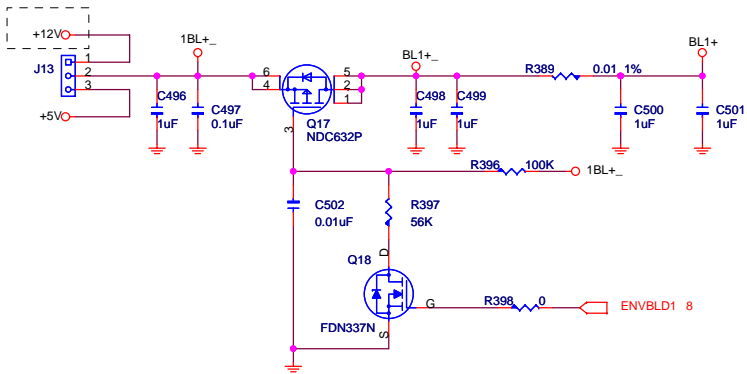


TV OUTPUTS

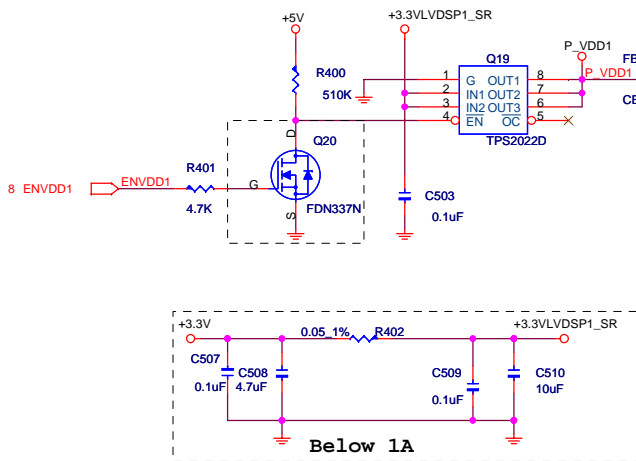
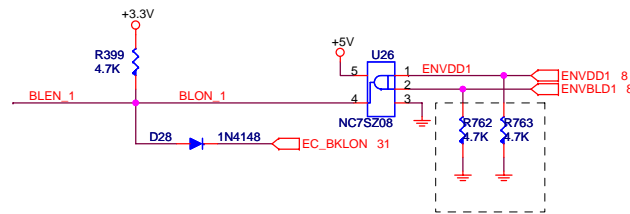
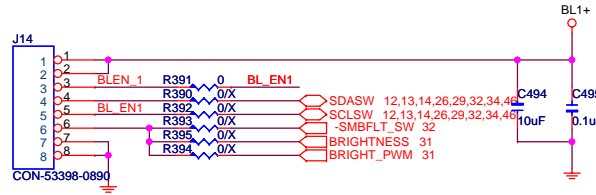
DAC OUTPUT MODE

C	Y	CVBS
R	G	B
Pr	Y	Pb
C	Y	Y1

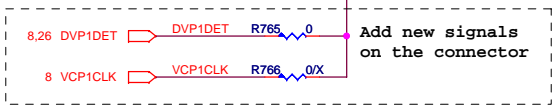
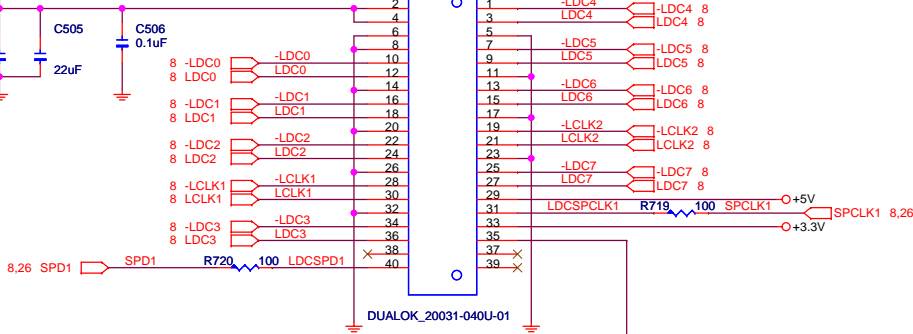




Inverter 1 CONN

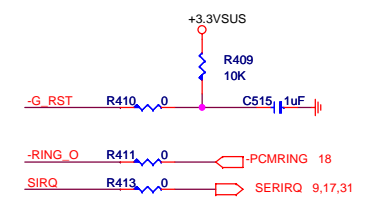
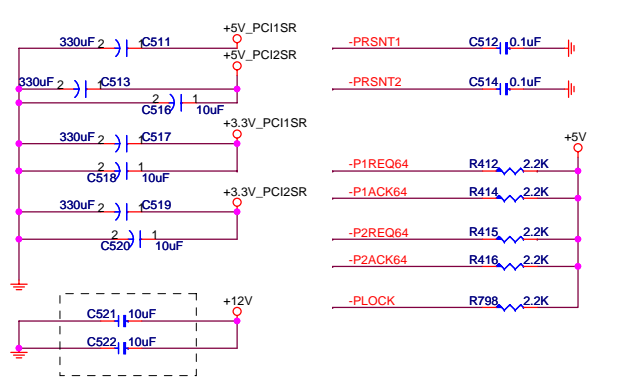
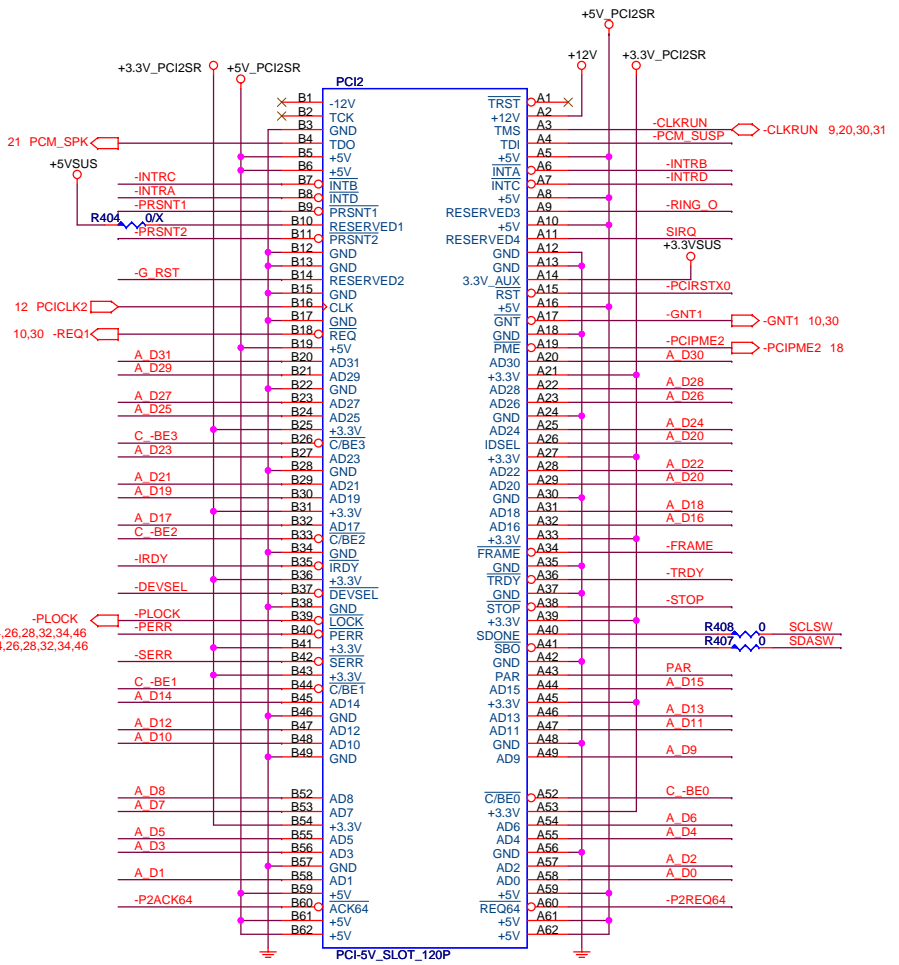
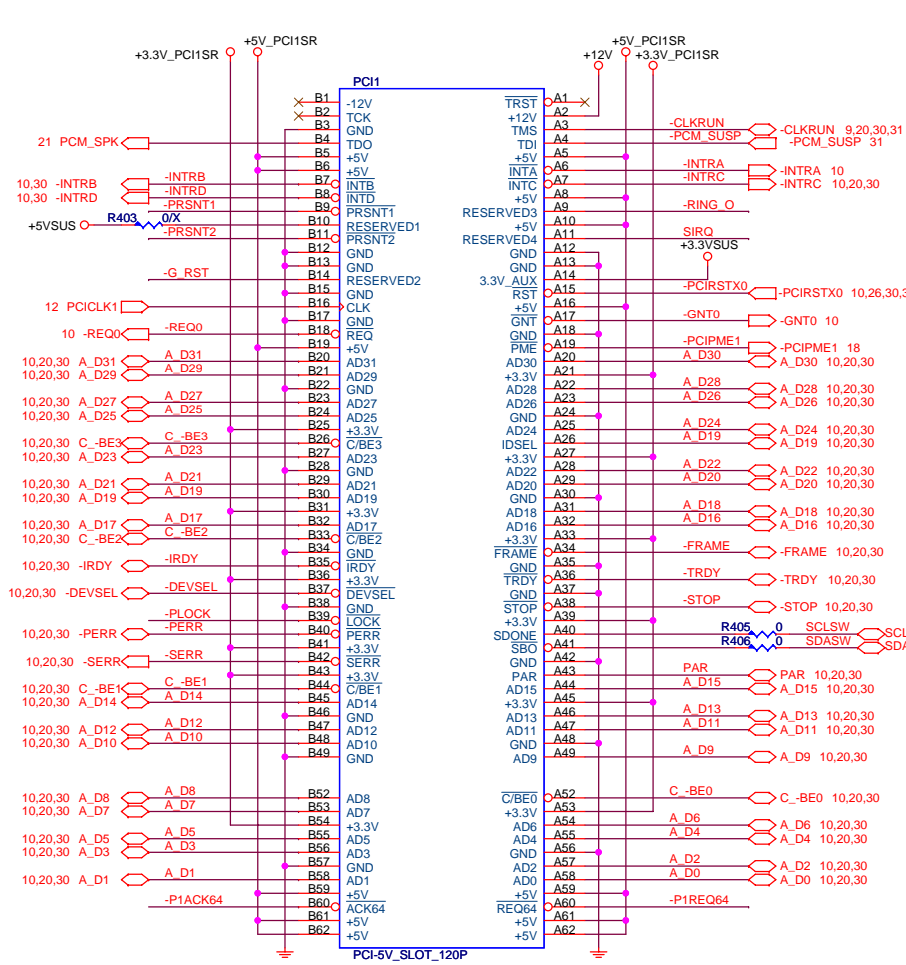


NEAR CONNECTOR

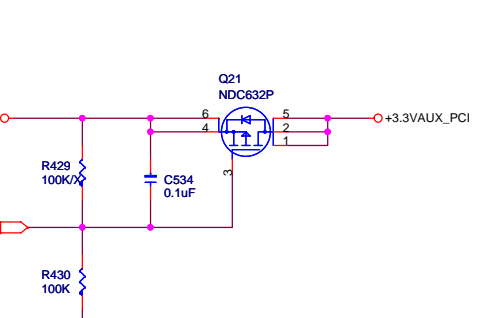
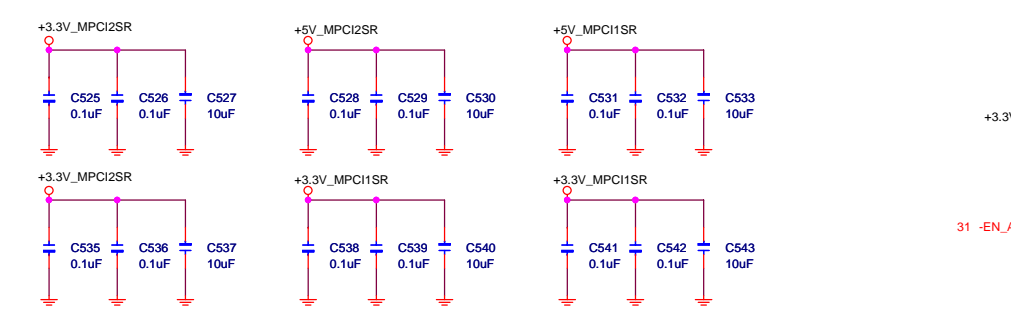
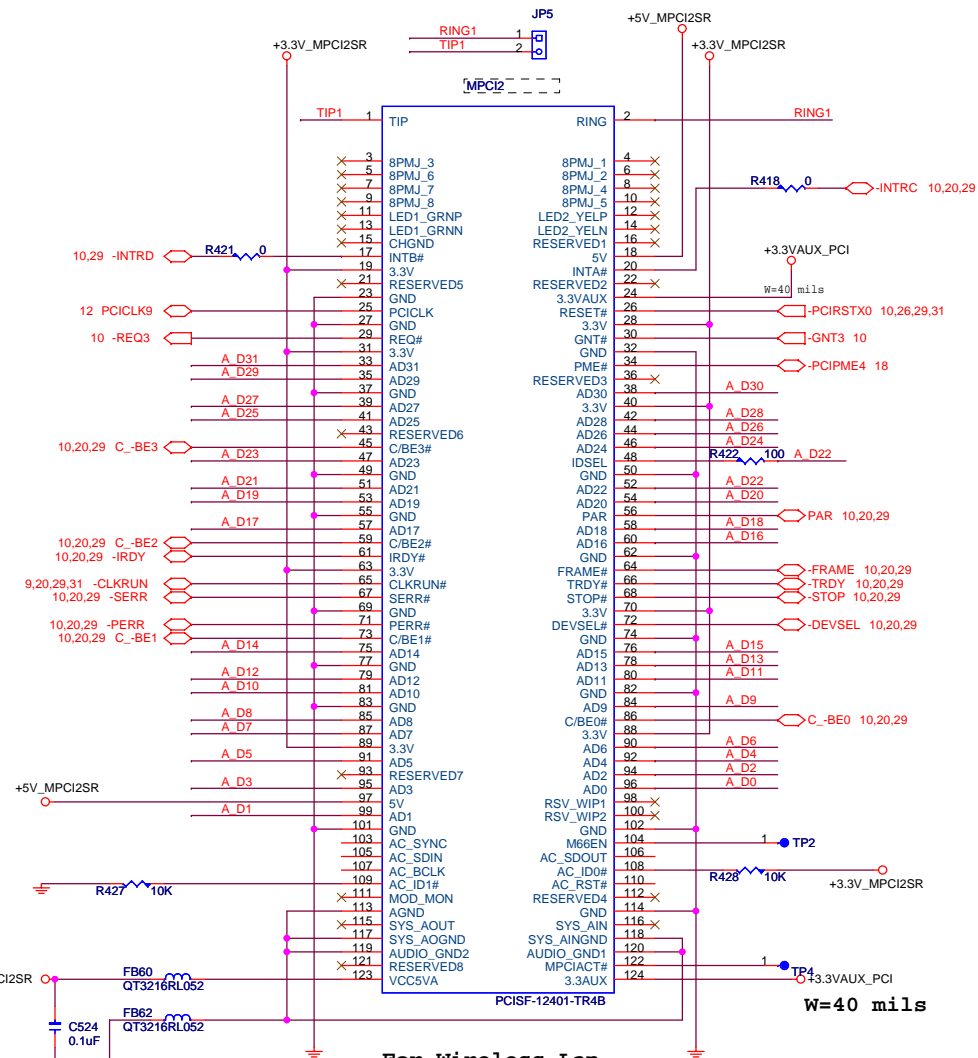
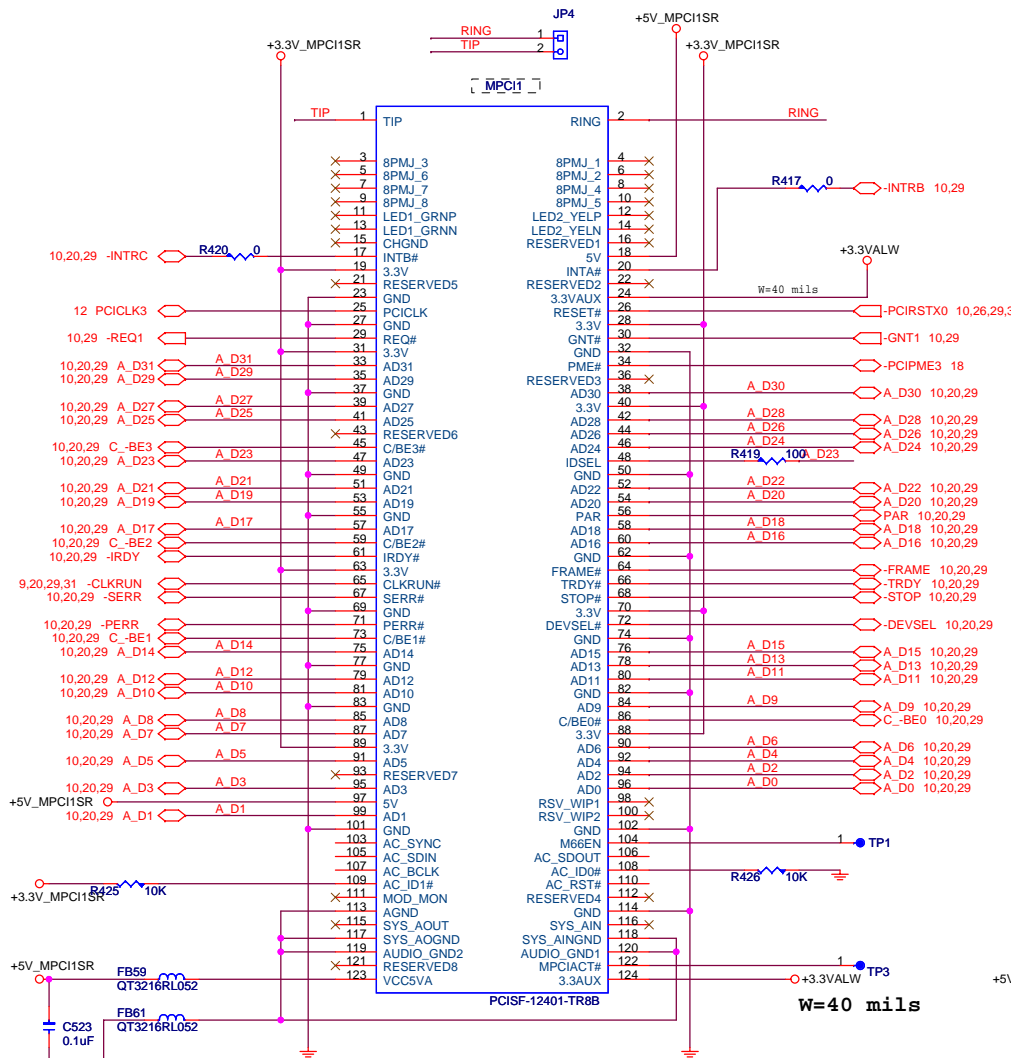


VIA Confidential

VIA VIA TECHNOLOGIES INC.	
Title: LVDS CONN. & B_LEN	
Size: C	Document Number: VT6304A3
Date: Wednesday, August 02, 2006	Rev: 3.1
Page: 28 of 53	

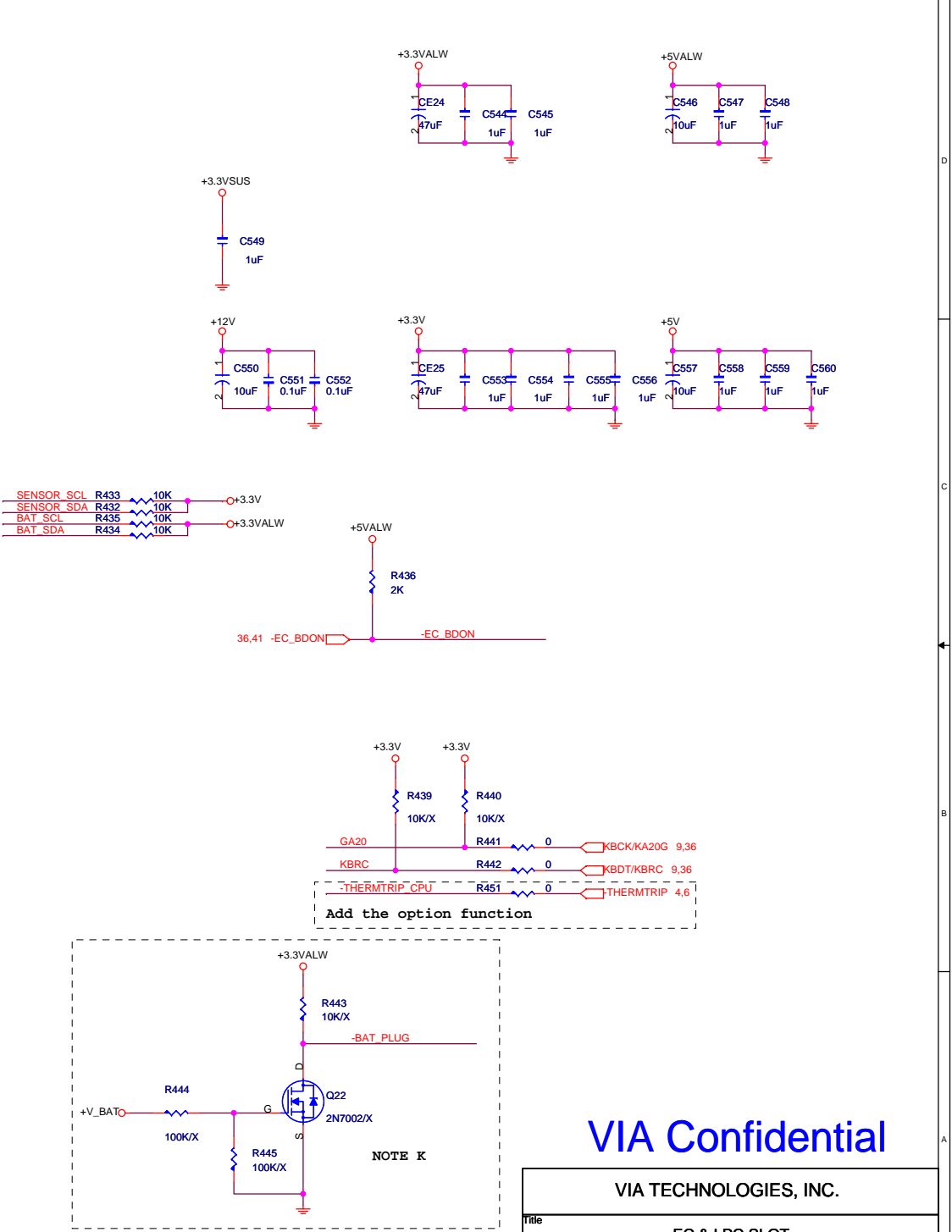
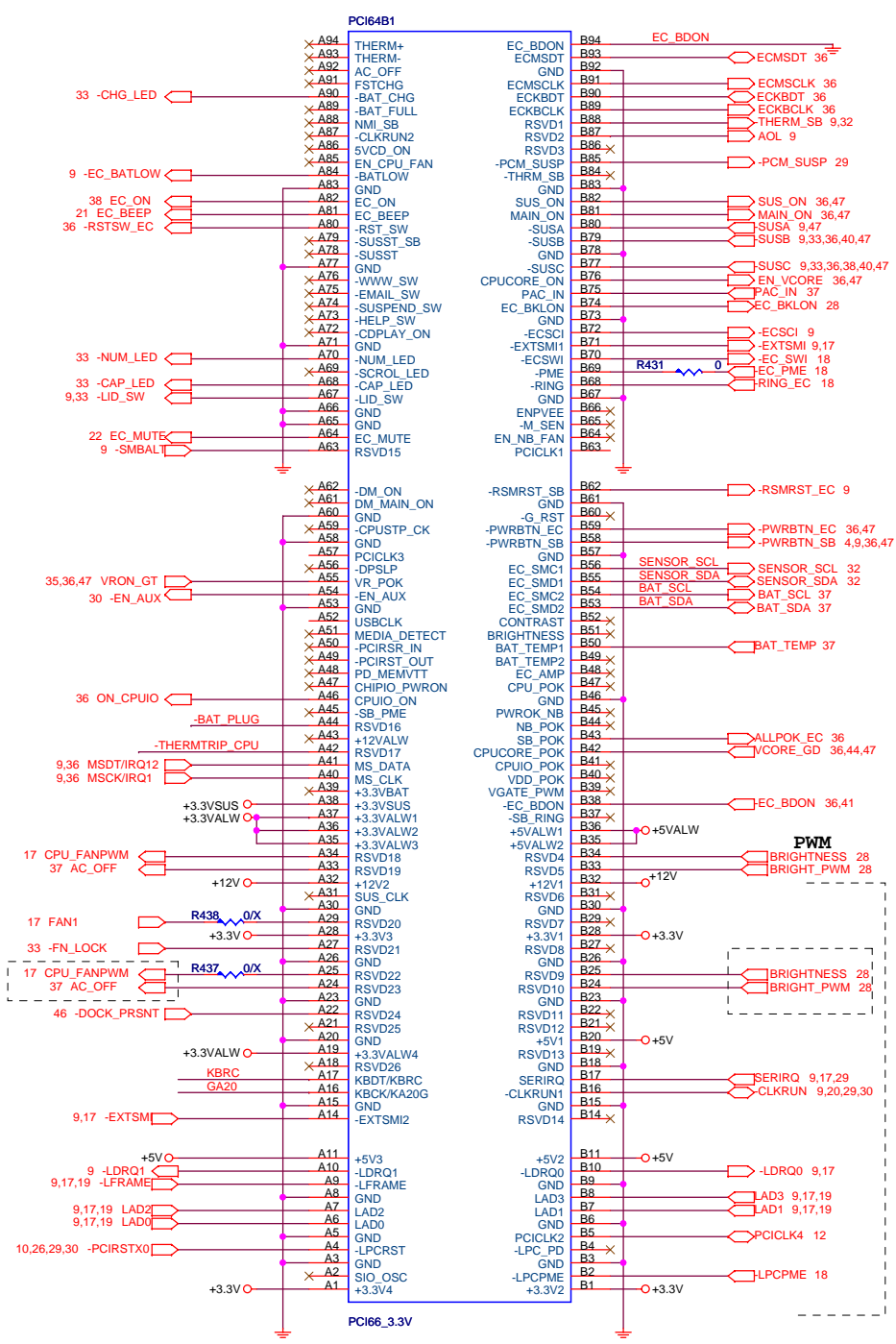


VIA TECHNOLOGIES, INC.		
Title PCI SLOTS 1 & 2		
Size C	Document Number VT6304A3	Rev 3.1
Date: Wednesday, August 02, 2006	Sheet 29	of 53



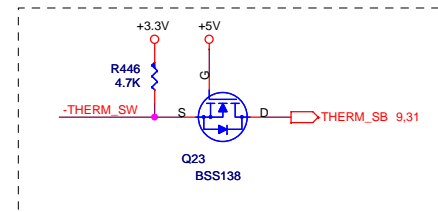
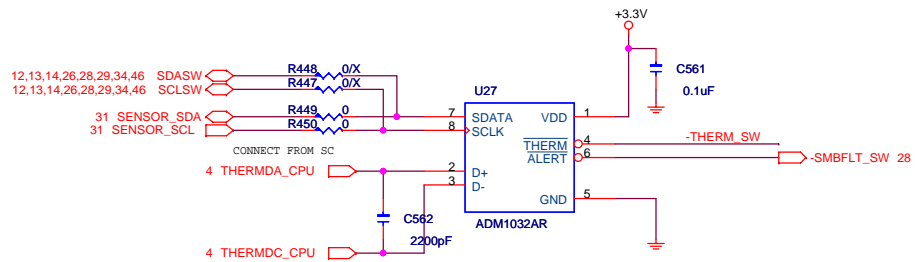
VIA Confidential

		VIA TECHNOLOGIES INC.	
		Title MINIPCI 1 & 2	
Size C	Document Number VT6304A3	Rev 3.1	
Date: Wednesday, August 02, 2006	Sheet 30	of 53	




VIA Confidential

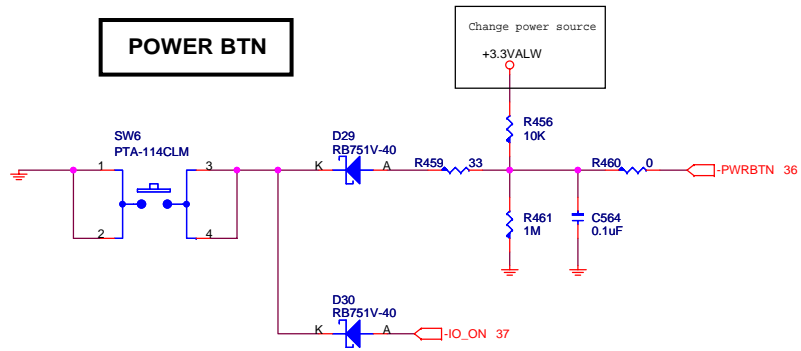
VIA TECHNOLOGIES, INC.		
Title EC & LPC SLOT		
Size	Document Number	Rev
	VT6304A3	3.1
Date:	Wednesday, August 02, 2006	Sheet 31 of 53



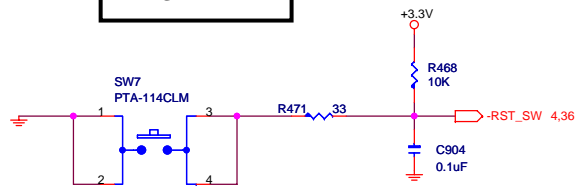
VIA Confidential

		VIA TECHNOLOGIES INC.	
Title			
THERMAL SENSOR			
Size	Document Number	Rev	
C	VT6304A3	3.1	
Date:	Wednesday, August 02, 2006	Sheet	32 of 53

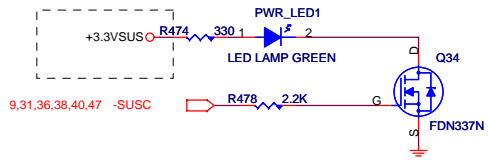
POWER BTN



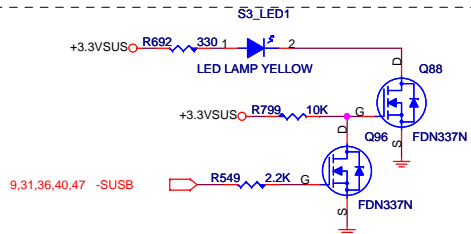
RESET BTN



PWR_LED1



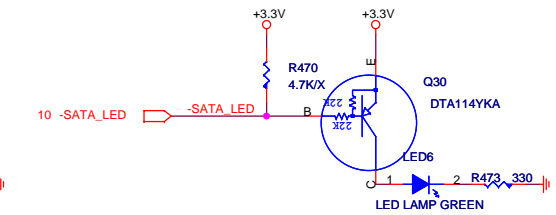
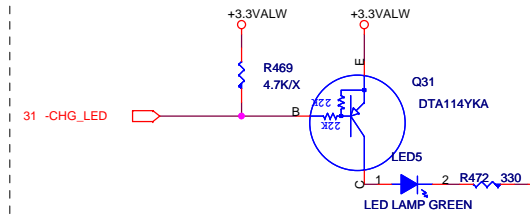
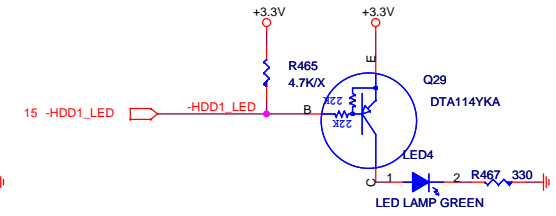
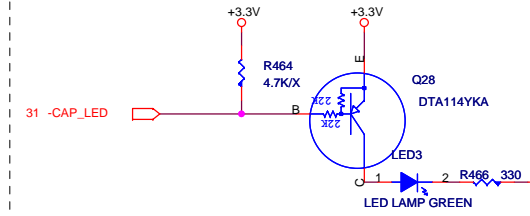
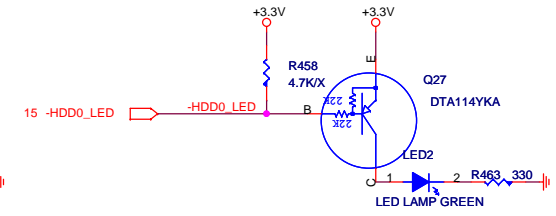
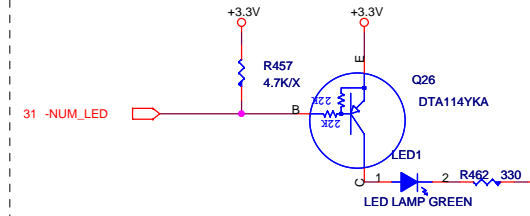
S3_LED1



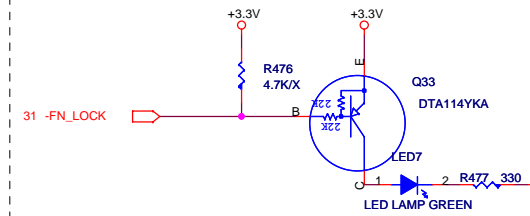
Board add S3 status LED

POWER MANAGEMENT STATUS LED

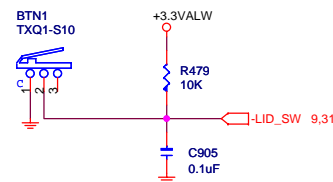
R457, R458, R464, R465, R469, R470, R476 change to Reserved



Hard-Disk Active LED



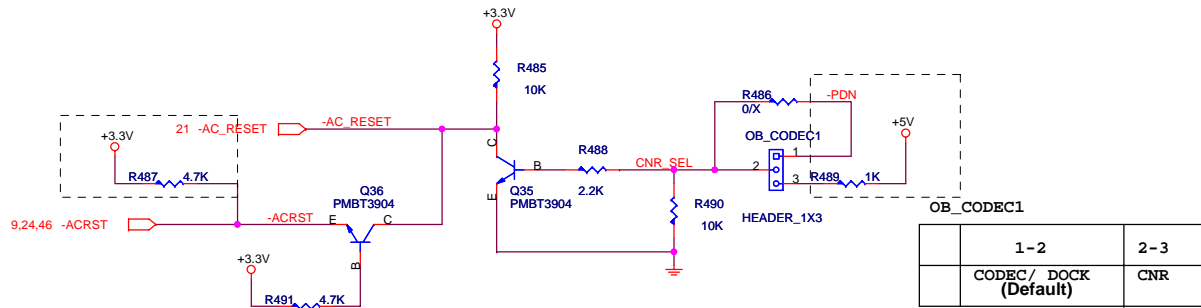
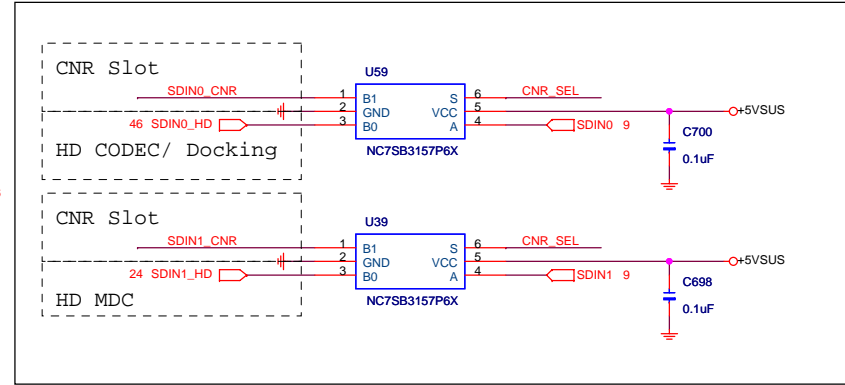
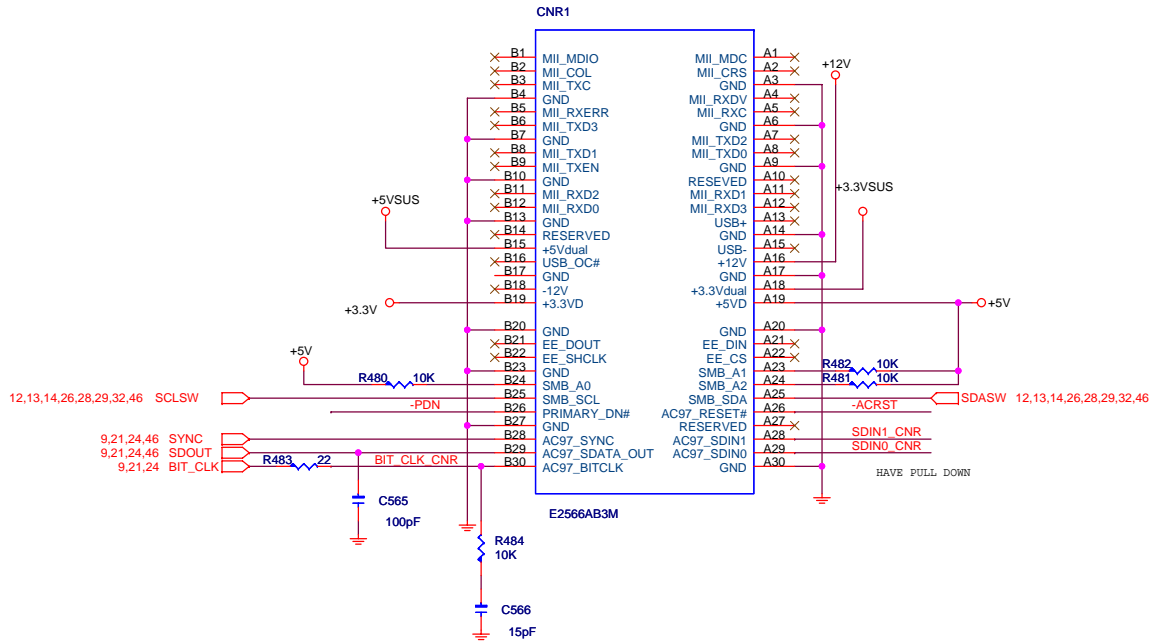
LID



VIA Confidential

VIA TECHNOLOGIES, INC.

Title			SYSTEM BOTTOM & LED
Size	Document Number	Rev	
Custom	VT6304A3	3.1	
Date:	Wednesday, August 02, 2006	Sheet	33 of 53



1-2	2-3
CODEC/ DOCK (Default)	CNR

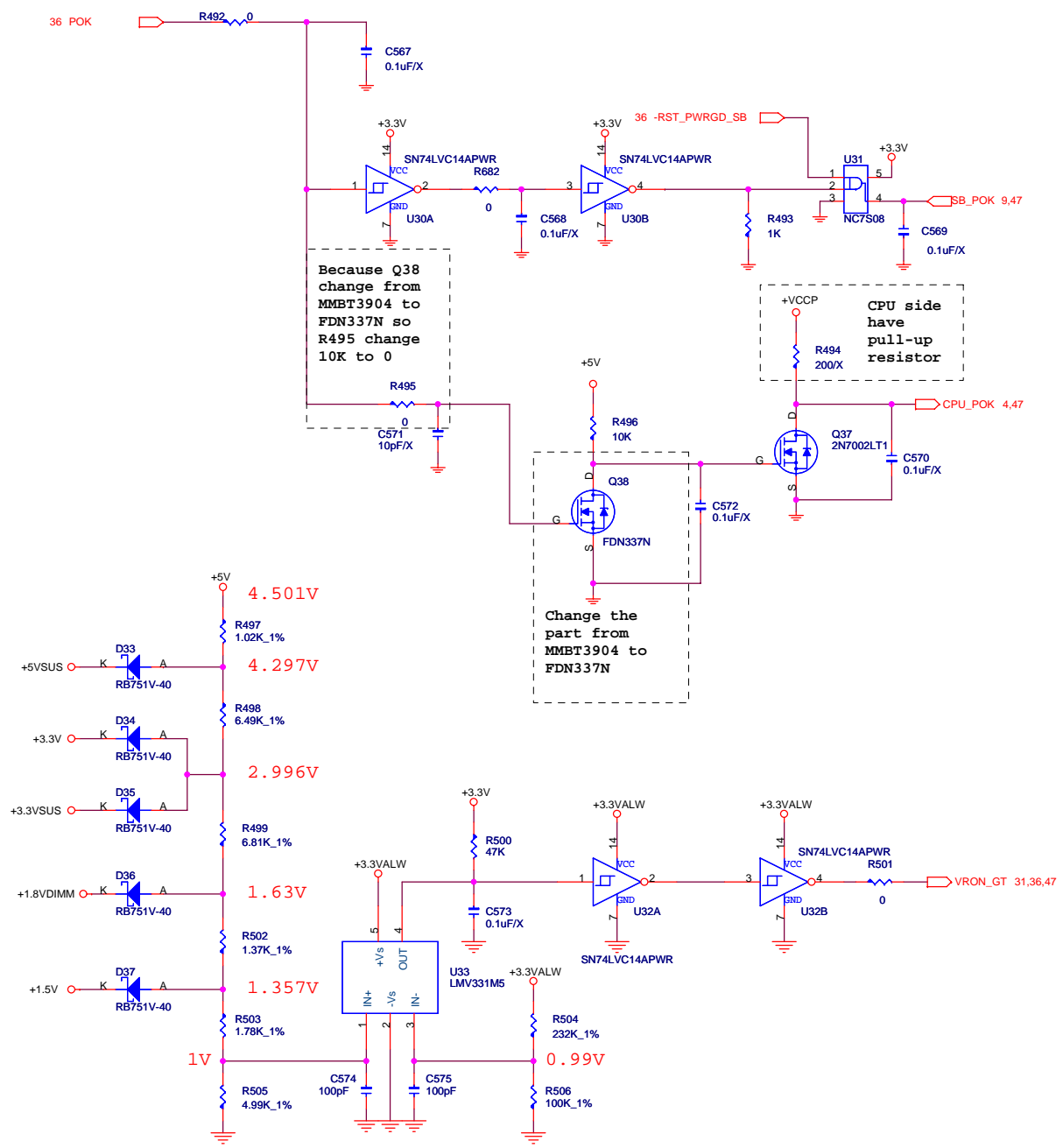
VIA Confidential

VIA TECHNOLOGIES, INC.


Title: CNR SLOT

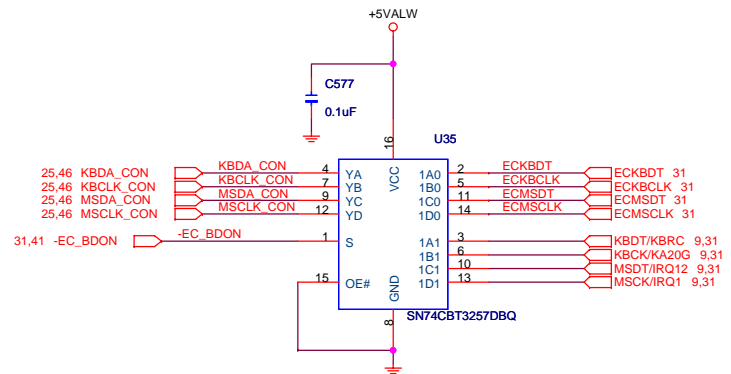
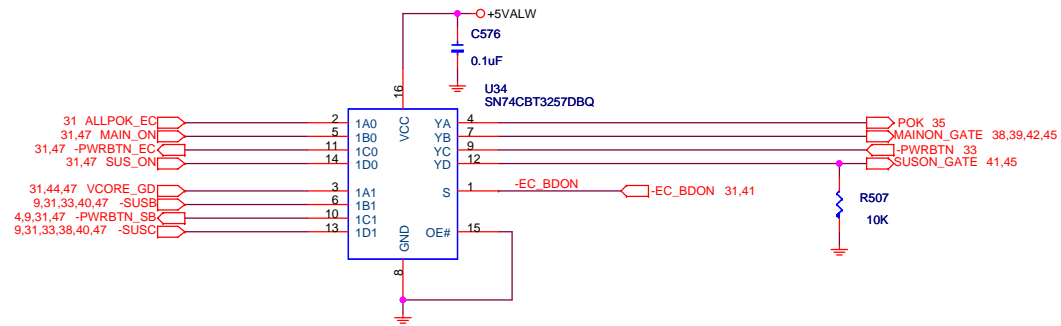
Size C Document Number: VT6304A3 Rev 3.1

Date: Wednesday, August 02, 2006 Sheet 34 of 53

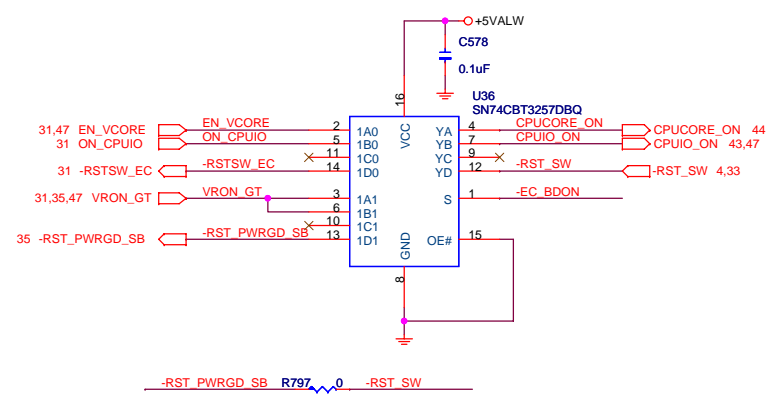


VIA Confidential


		VIA TECHNOLOGIES INC.	
Title		POWER CONTROL CIRCUIT	
Size	Document Number	VT6304A3	
C		Rev 3.1	
Date:	Wednesday, August 02, 2006	Sheet	35 of 53

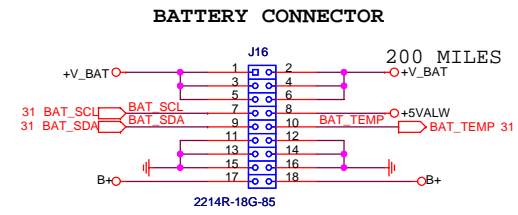
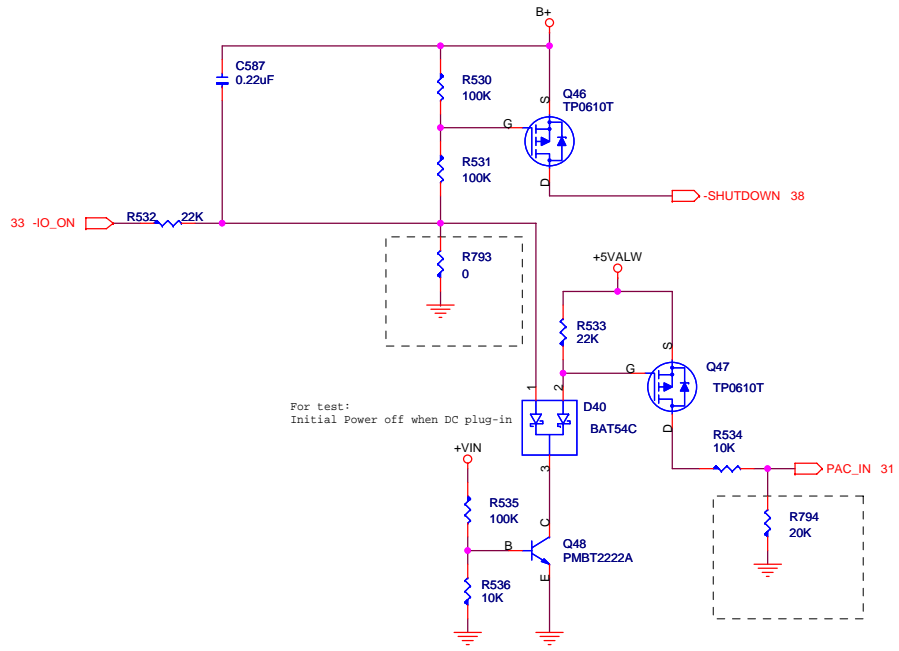
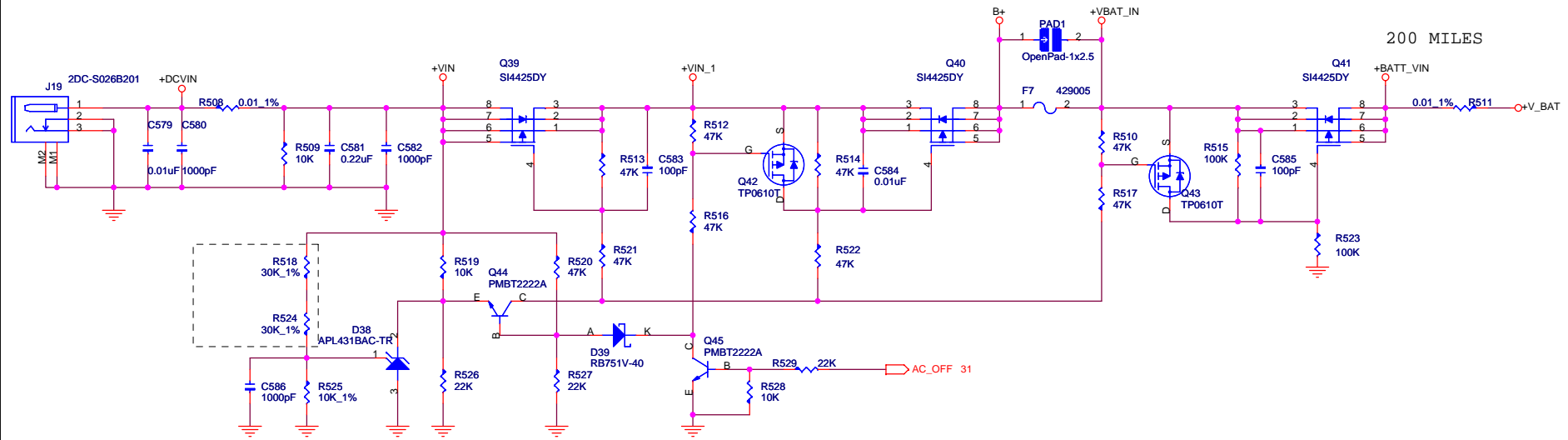


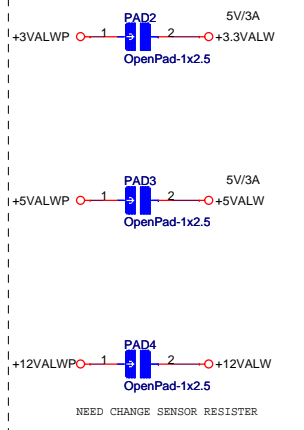
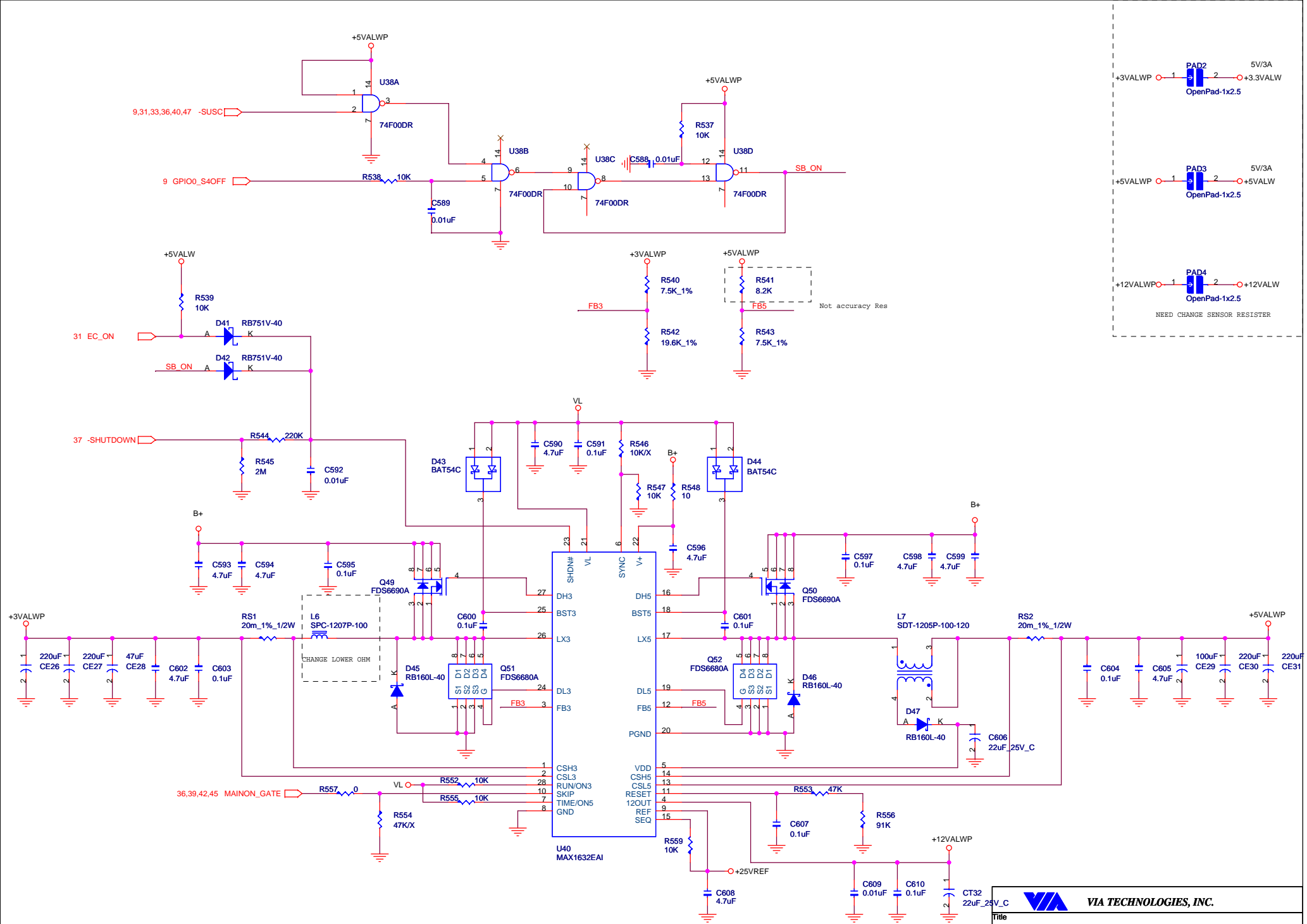
PS2 SIGNAL
SWITCH PS/2 SIGNAL WHILE W/ OR W/O EC



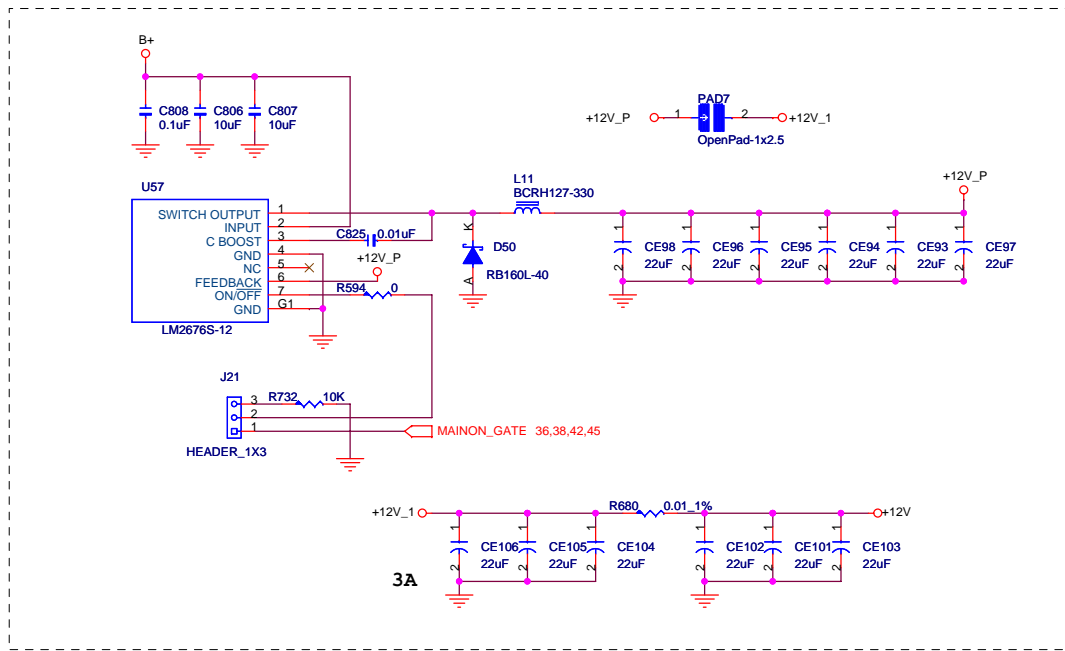
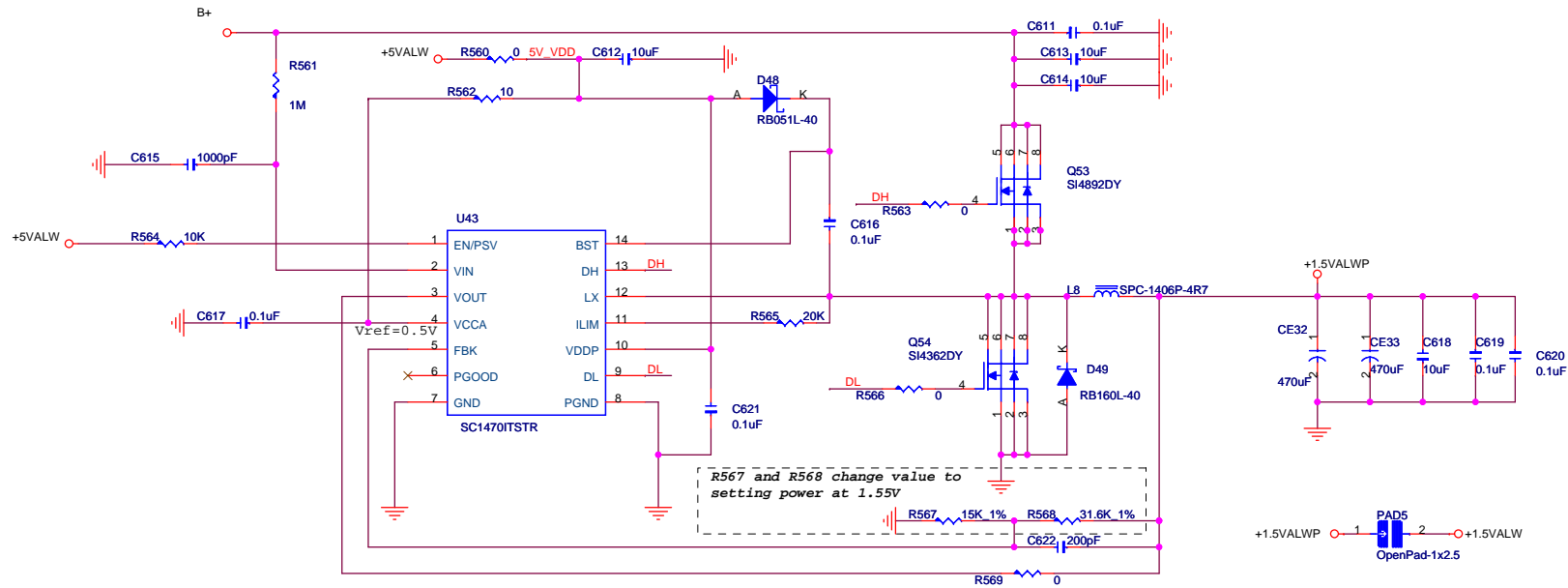
VIA Confidential

		VIA TECHNOLOGIES INC.	
Title: SWITCH PS/2 SIGNAL WHILE W/ OR W/O EC			
Size: C	Document Number: VT6304A3		Rev: 3.1
Date: Wednesday, August 02, 2006	Sheet: 36	of 53	




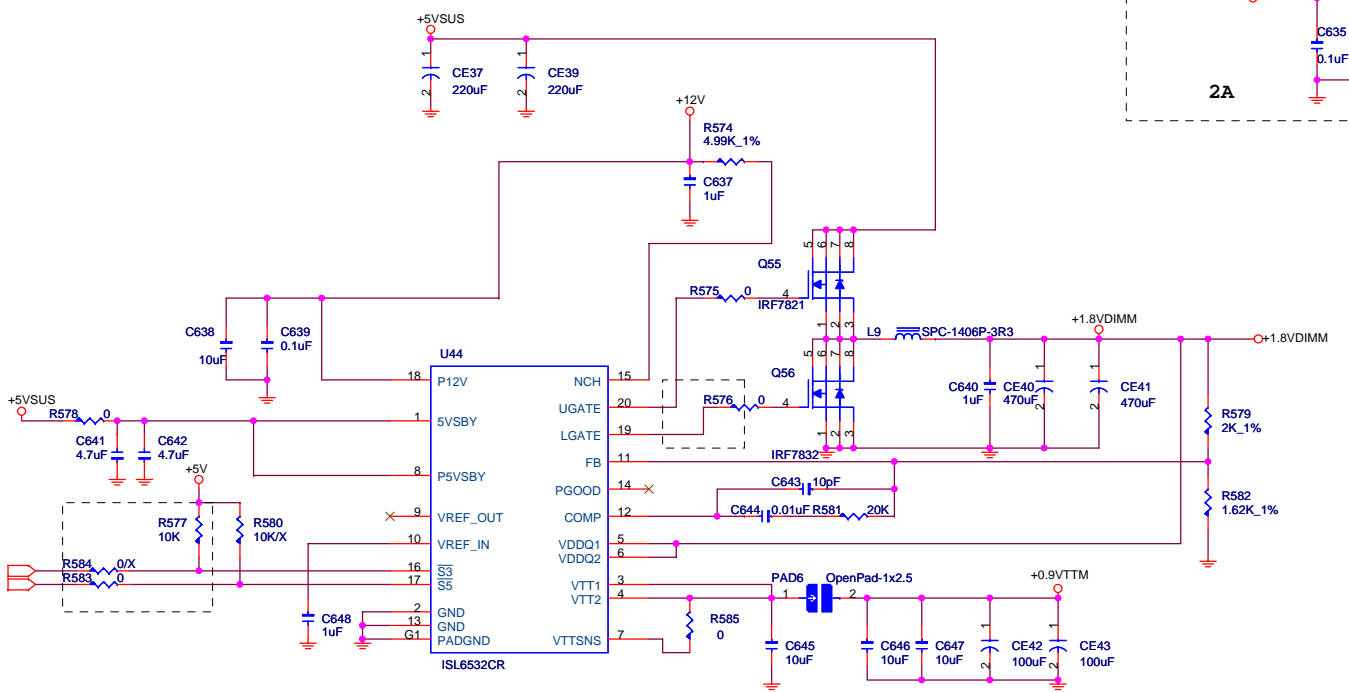
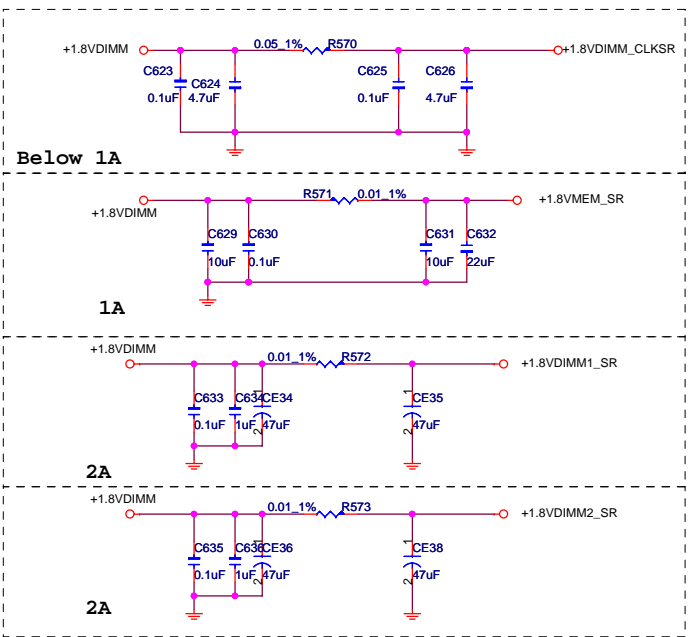
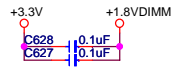


VIA TECHNOLOGIES, INC.		
Title 3V/5V/12V		
Size	Document Number VT6304A3	Rev 3.1
Date: Wednesday, August 02, 2006	Sheet 38	of 53



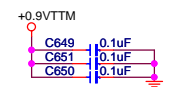
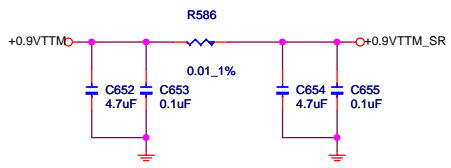
VIA Confidential

		VIA TECHNOLOGIES INC.	
Title			
1.5V/ 12V POWER SOURCE			
Size	Document Number	Rev	
C	VT6304A3	3.1	
Date:	Wednesday, August 02, 2006	Sheet	39 of 53



9.31,33,36,47 -SUSB
9.31,33,36,38,47 -SUSC

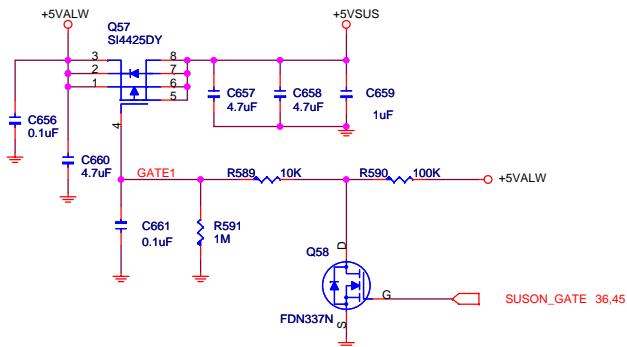
Power for DDR2
Suspend Power for DDR SLOT



VIA Confidential

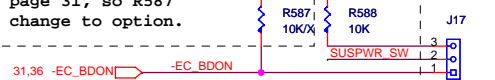
VIA TECHNOLOGIES, INC.	
Title: DDR2 POWER	
Size C	Document Number: VT6304A3
Date: Wednesday, August 02, 2006	Rev: 3.1
Sheet: 40	of 53

+5VALW Transfer to +5VSUS



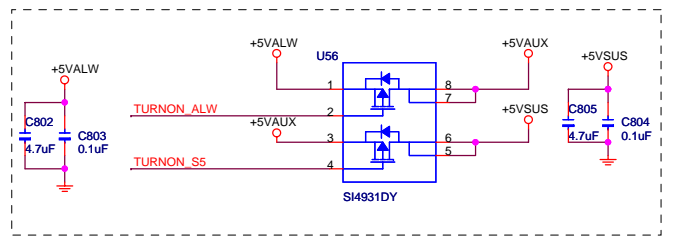
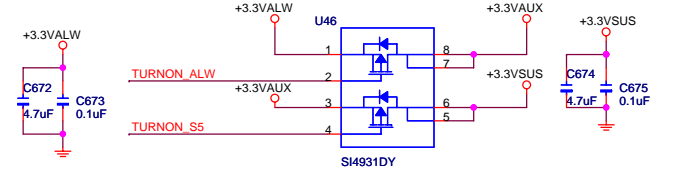
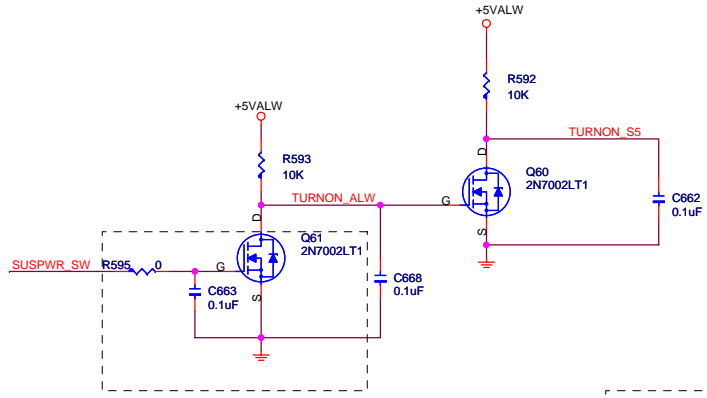
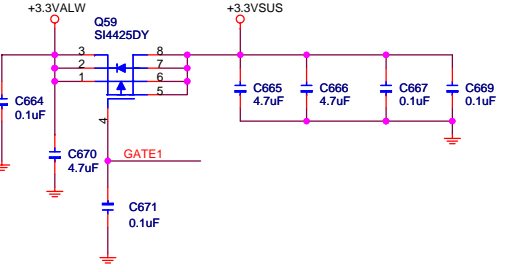
Because "-EC_BDON" have pull-up +5VALW in page 31, so R587 change to option.

Because Q61 change MMBT3904 to 2N7002LT1, so the power source change from +3.3ALWS to +5VALWS

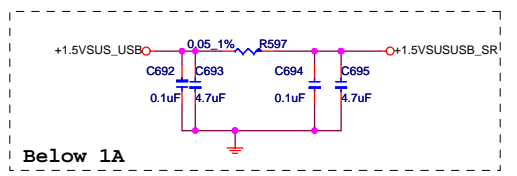
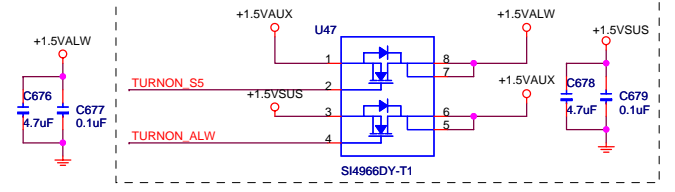
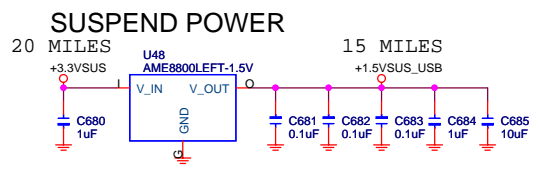


J17 Select SB suspend voltage
Install EC 1-2 2-3
SUS ALW
Remove EC 1-2 2-3
ALW ALW

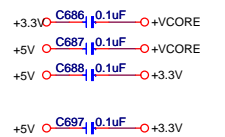
+3.3VALW Transfer to +3.3VSUS



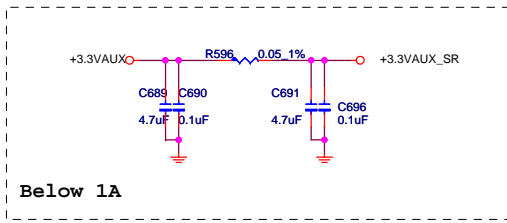
+3.3VSUS Transfer to +1.5VSUS



Below 1A



Place on Between Power Plane

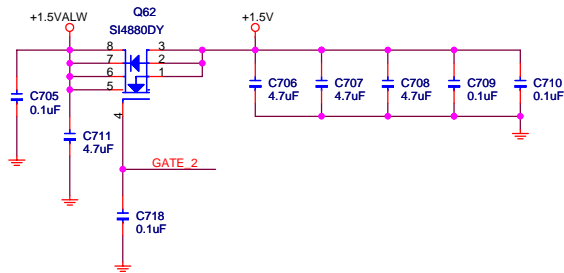


Below 1A

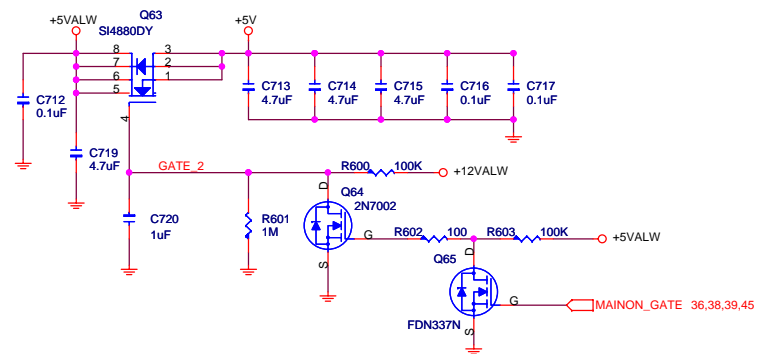
VIA Confidential

VIA TECHNOLOGIES, INC.	
Title DC/DC SUSPEND INTERFACE1	
Size	Document Number VT6304A3
Date: Wednesday, August 02, 2006	Rev 3.1
Sheet 41	of 53

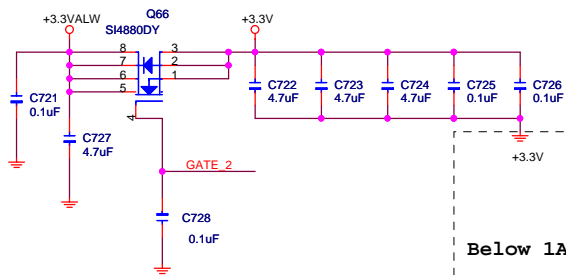
+1.5VALW Transfer to +1.5V



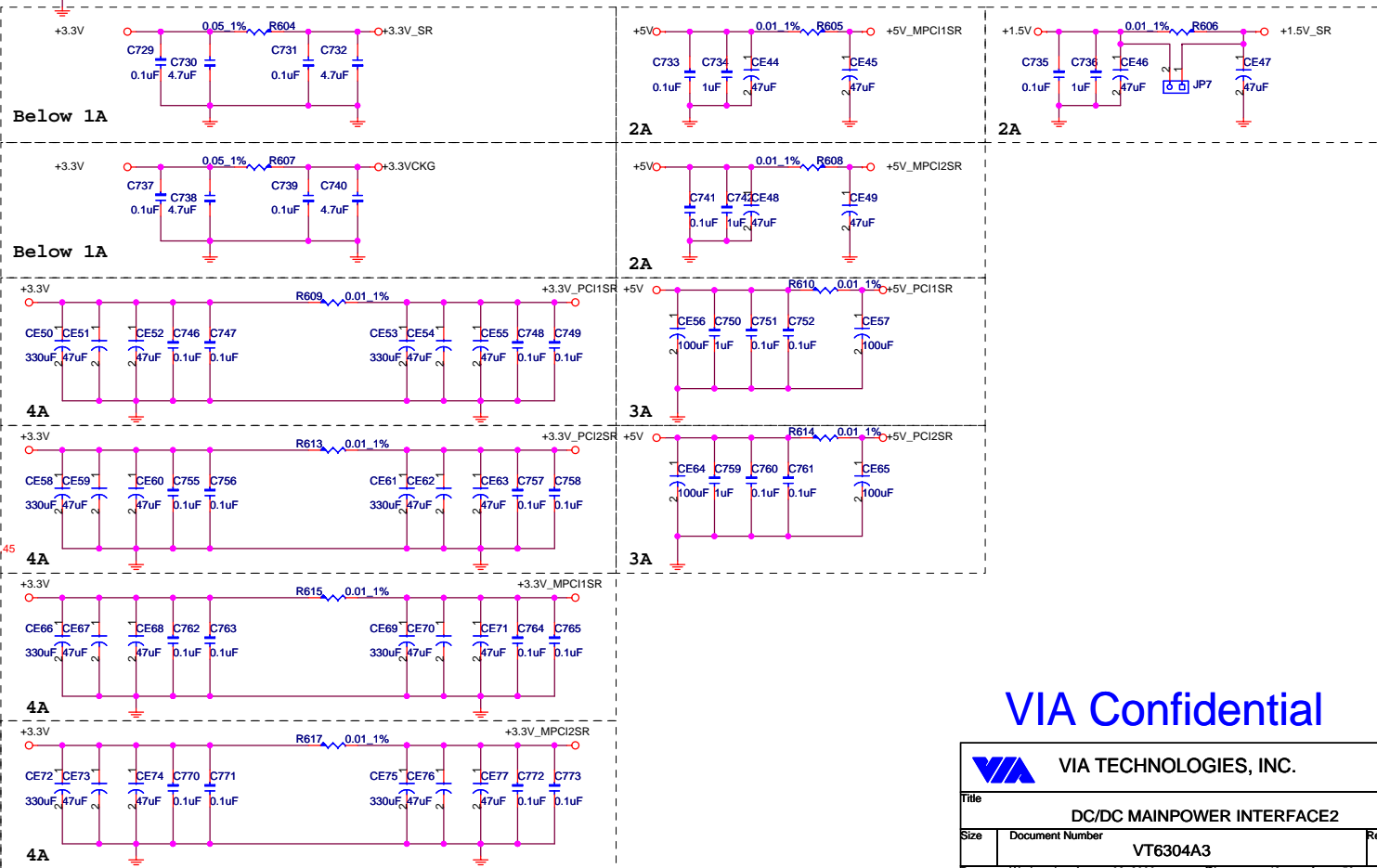
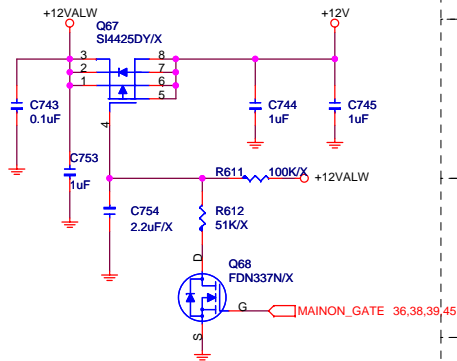
+5VALW Transfer to +5V




+3VALW Transfer to +3V



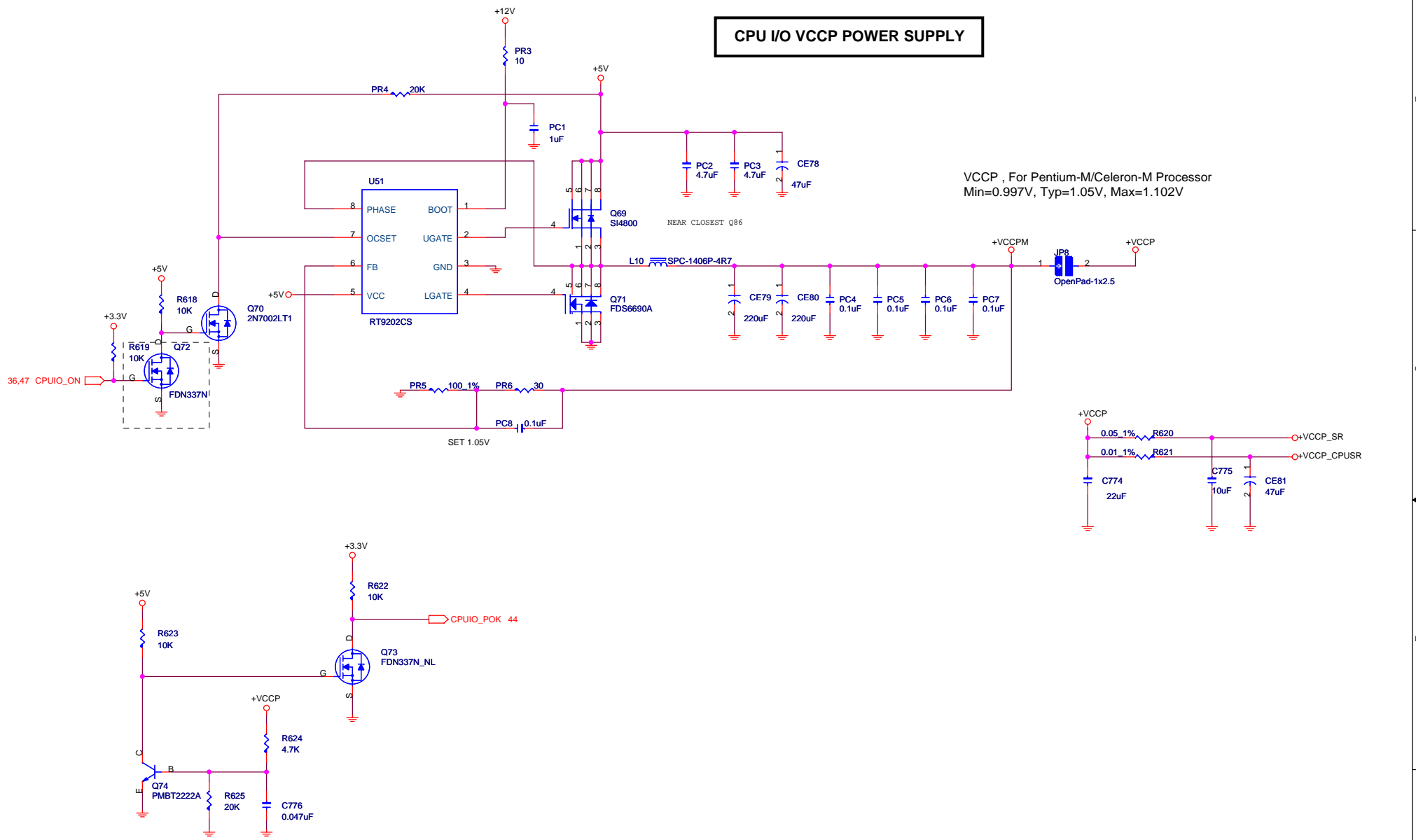
+12VALW TO +12V Transfer



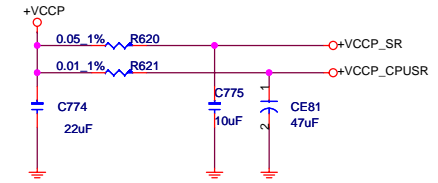
VIA Confidential

 VIA TECHNOLOGIES, INC.	
Title: DC/DC MAINPOWER INTERFACE2	
Size: Document Number	Rev: 3.1
VT6304A3	
Date: Wednesday, August 02, 2006	Sheet 42 of 53

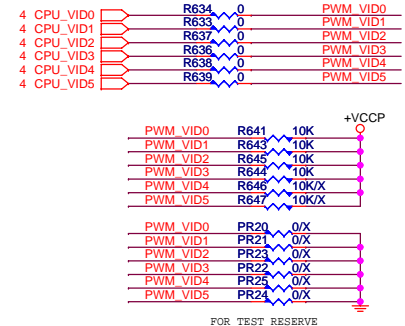
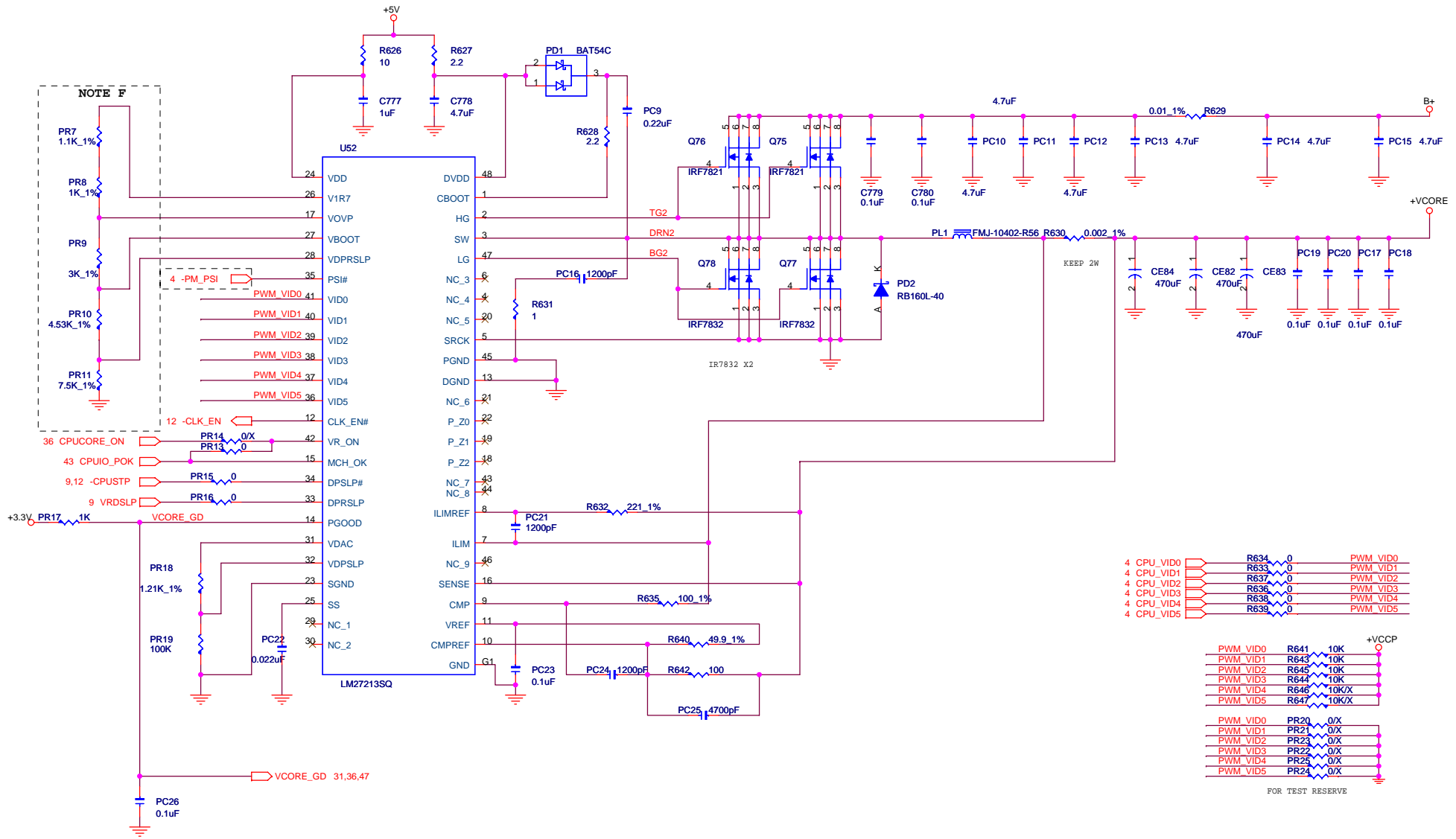
CPU I/O VCCP POWER SUPPLY

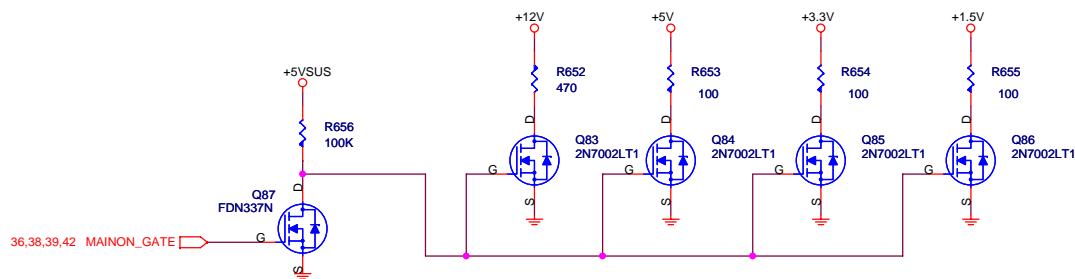
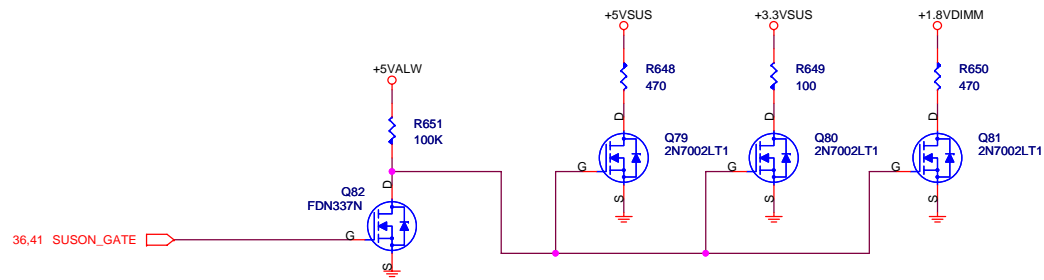


VCCP , For Pentium-M/Celeron-M Processor
Min=0.997V, Typ=1.05V, Max=1.102V




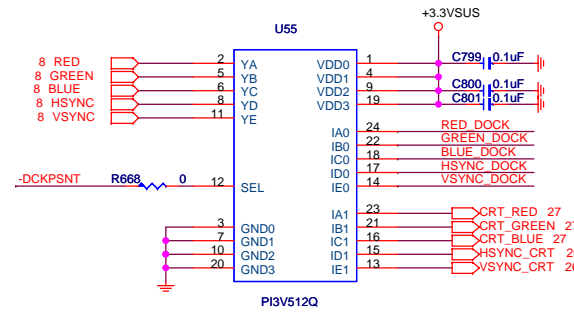
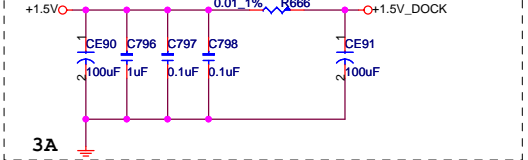
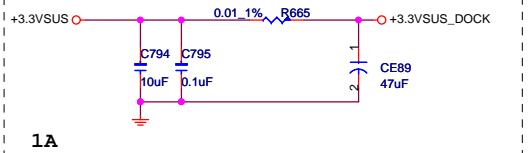
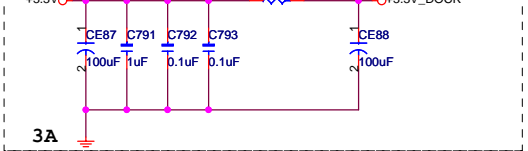
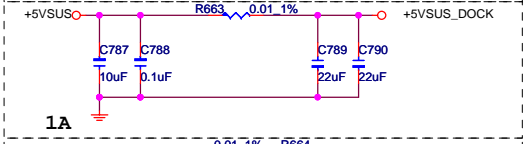
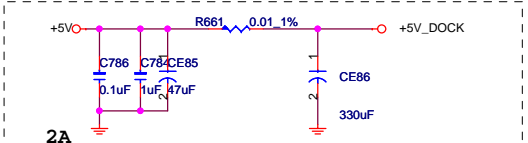
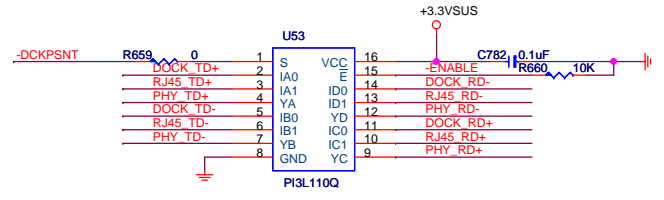
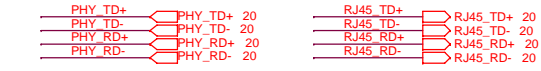
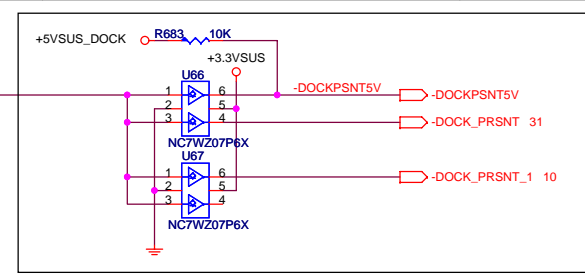
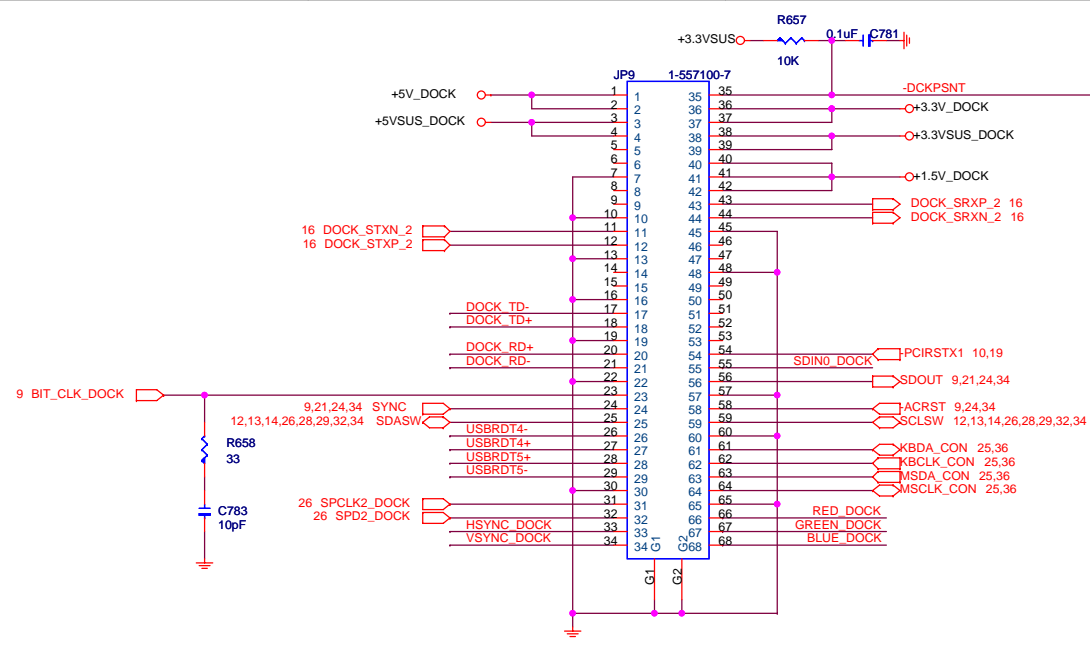
VIA VIA TECHNOLOGIES INC.			
Title		VCCP POWER	
Size	Document Number	Rev	
Custom	VT6304A3	3.1	
Date:	Wednesday, August 02, 2006	Sheet	43 of 53



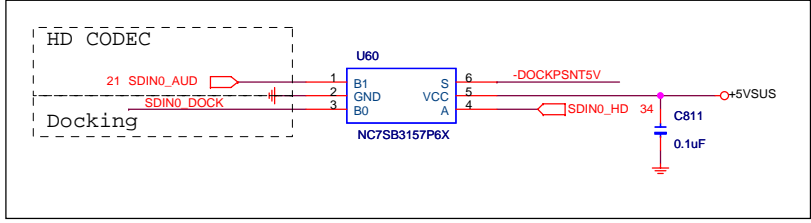
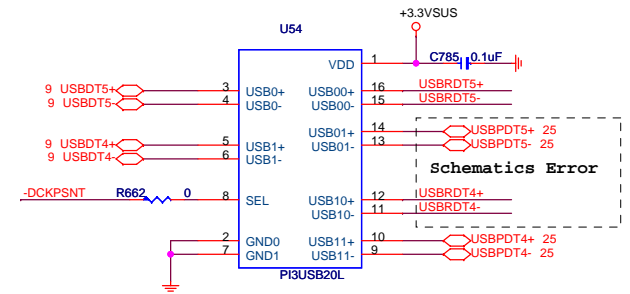


VIA Confidential

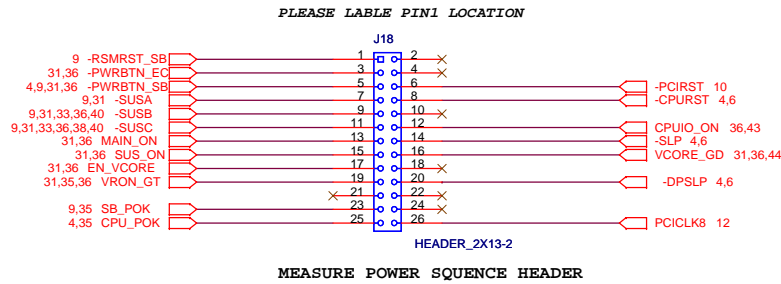
		VIA TECHNOLOGIES INC.	
Title			
DISCHARGE CIRCUIT			
Size	Document Number	Rev	
C	VT6304A3	3.1	
Date:	Wednesday, August 02, 2006	Sheet	45 of 53



Change name to connect TV switch



- 1: -RSMRST_SB
- 2: NC
- 3: -PWRBTN_EC
- 4: -SUSST
- 5: -PWRBTN_SB
- 6: -PCIRSTX
- 7: -SUSA
- 8: -CPURST
- 9: -SUSB
- 10: NC
- 11: -SUSC
- 12: CPUIO_ON
- 13: MAIN_ON
- 14: -SLP
- 15: SUS_ON
- 16: VCORE_GD
- 17: EN_VCORE
- 18: NC
- 19: VRON_GT
- 20: -DPSLP
- 21: NC
- 22: -AGPBZ
- 23: SB_POK
- 24: NC
- 25: CPU_POK
- 26: PCICKL8

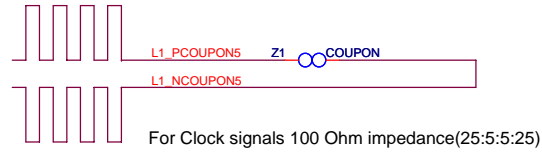


VIA Confidential

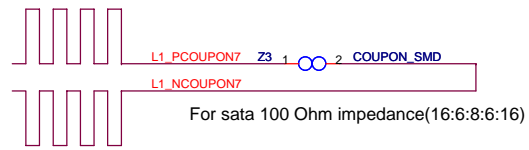
VIA TECHNOLOGIES, INC.		
Title MEASURE PORT		
Size	Document Number VT6304A3	Rev 3.1
Date: Wednesday, August 02, 2006 Sheet 47 of 53		

IMPEDANCE TEST COUPON

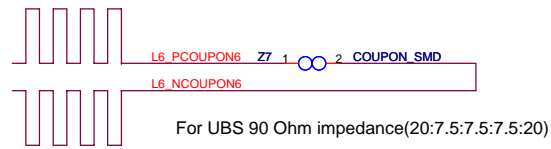
DIFFERENTIAL CLOCC SIGNALS



SATA

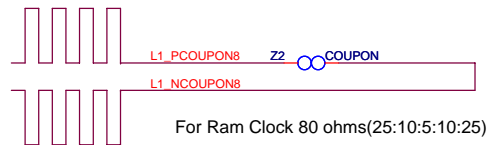


USB



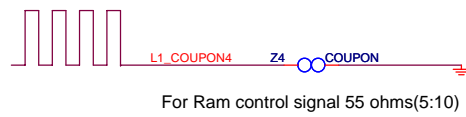
DDR Please close to DIMM

Clock DIFFERENTIAL TRACE SIGNALS

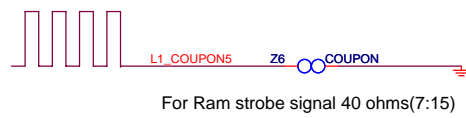


SINGLE END TRACE SIGNALS FOR DRAM


Ctrl signal

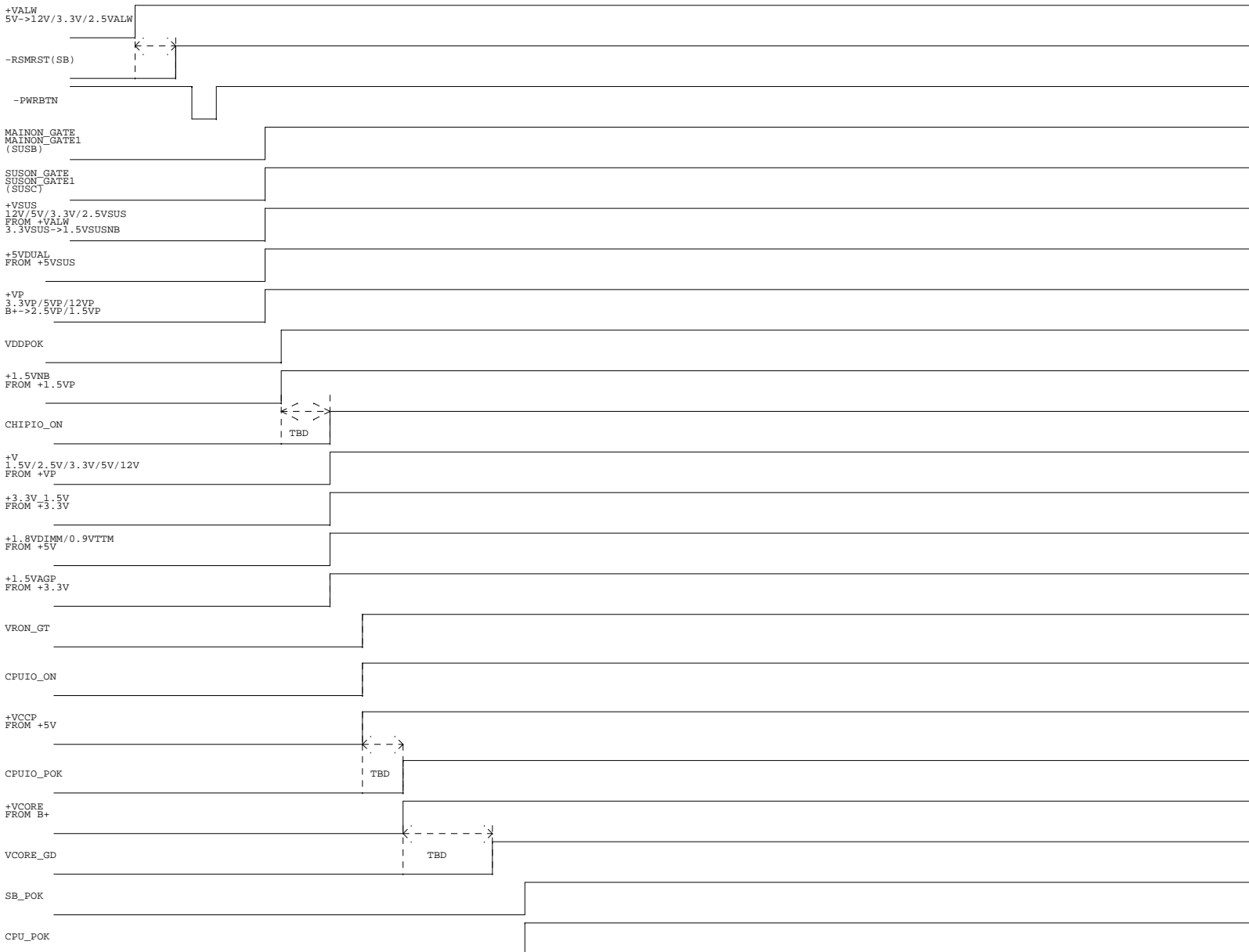


Ram strobe and DATA

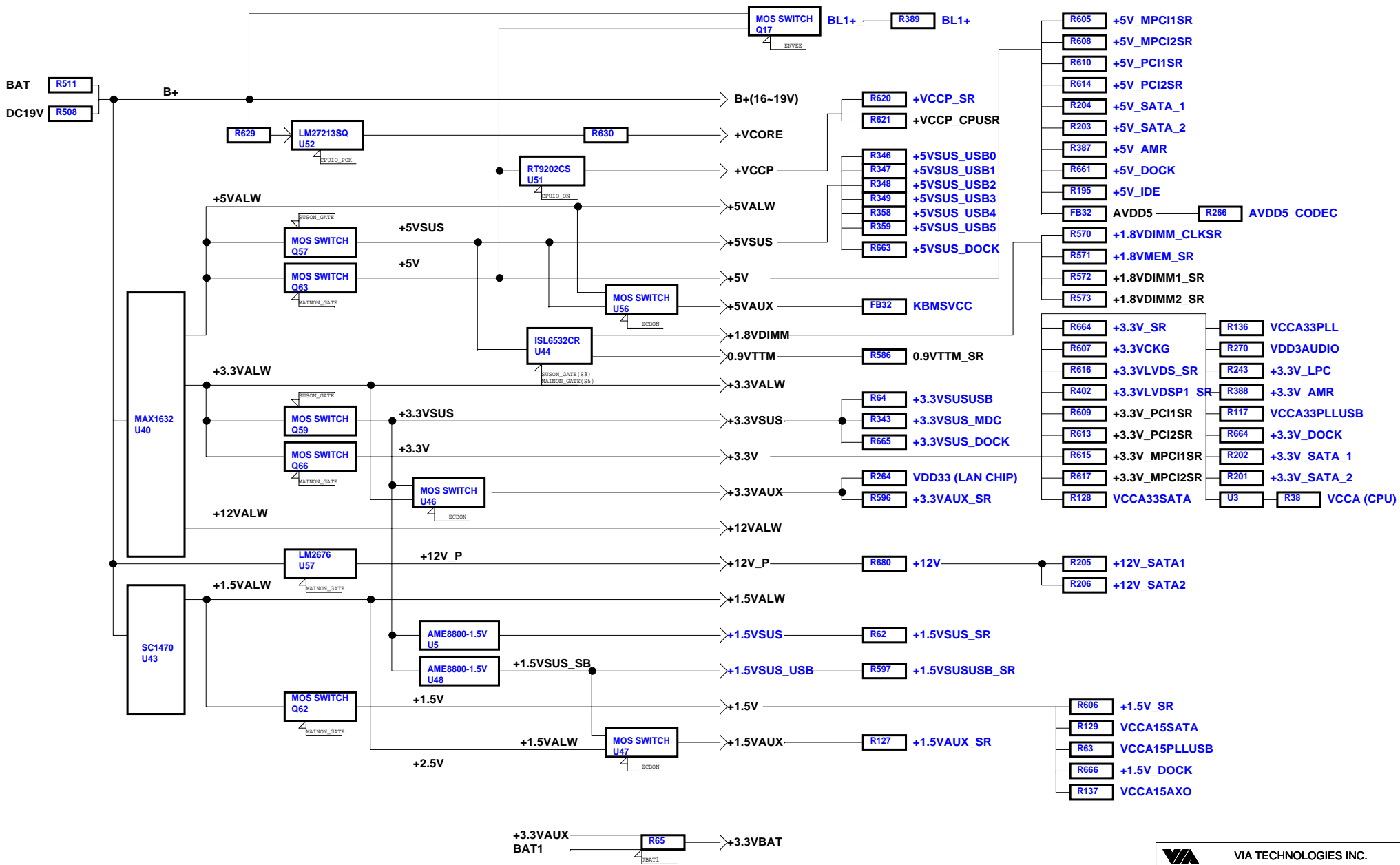


IMPEDANCE TESTING COUPON TRACE LENGTH 6000Mils

		VIA TECHNOLOGIES INC.	
Title			
IMPEDANCE TEST COUPON			
Size	Document Number		Rev
C	VT6304A3		3.1
Date:	Wednesday, August 02, 2006	Sheet	48 of 53



VIA Confidential



NOTICE:

NOTE A. CLK250 (+/-30ppm):Option resister for displace CRYSTAL of SATA and LAN for furture! (LAN can't support wake-up from S3)

NOTE B. Non-puplate for normal external EEPROM


NOTE E:-RSMRST_SB for AN252

NOTE F:PR34,PR35 need to change when enable OVP

NOTE K: For detect battery


NOTE L: Replace resistor pack RN1 and RN2 with individual resistors for compatibility with future processors. The resistors are for strapping options and need to be individually controlled.

NOTE N: If VSUS15USB (AE22) connect S3 power (+1.5VSUSUSB_SR) then regisister need to setting (B0D16F4 Rx61:20, Rx62:01)

		VIA TECHNOLOGIES INC.	
Title		NOTE	
Size C	Document Number VT6304A3	Rev 3.1	
Date:	Wednesday, August 02, 2006	Sheet 1	51 of 53


Version	Date	Revcode	Page	Description		
A	7/25	0.2	9	Modify Srrapping Table (Table 1, 2) R149 1K change to reserved R99 4.7K change to reserved		
			11	RN3 2.2K change power source and option the part		
			25	RN41 4.7K change to reserved KBMSVCC change power source from +5V to +3.3VAUX		
			30	Schematics add EC to control thermtrip signal		
			31	Schematics delete hardware thermaltrip circuit		
			34	Q38 change part from MMBT3904 to 2N7002LT1 R495 change value from 10K to 0		
			40	C663 0.1uF change to reserved Q61 change part from MMBT3904 to 2N7002LT1 R595 Change value from 1K to 0 R585 10K change power source from +3.3VALW to +5VALW R587 10K change to reserved		
			7/27	0.3	5	L2 error connect to VCCA, so the part change connection to CPUVCCA1
			8	Power name error name change from "+3.3V_LVDSSR" to "+3.3VLVDS_SR"		
			10	C156 change signal from "STXP_1" to "STXP_2" C157 change signal from "STXN_1" to "STXN_2" C159 change signal from "SRXP_1" to "SRXP_2" C158 change signal from "SRXN_1" to "SRXN_2" VCCA33PLL no connect to VCCA33 change power to VCCA33PLL		
			12	Add R376 22 for LPC ROM clock		
			15	R168 470 change to reserved		
			20	"PCICLK5" error connect to "PCICLK1" change label to "PCICLK5" "-PCIPME5" error connect to "-PME" change label to "-PME5"		
25	Layout swap USB0,1 and USB2,3 ports					
28	PCI bus Delete double pull-up resistor (RN42, RN43, RN44, RN45)					
32	R457, R458, R464, R465, R469, R470, R476 change to reserved Board add S3 LED circuit (S3 LED1 and R692)					
40	Delete double circuit (R598, C701, C702, C703, C704)					
41	Delete double circuit (JP6, R599)					
8/04	0.9	4, 44	"-PM_PSI" connect to CPU_CORE PWM			
8/17	0.93	4	J1 connector change one "BEVO3" signal add R723 0 connector to ground Change R30 value from 54.9 1% to 0			
		8	"DVP1TVFLD" signal add R713 4.7K pulldown resistor			
		12	Chip PCI clock change to free run clock and add R452 22			
		16	SATA2 connect to Dock connector using R702,R703,R704,R705 for reserved.			

Version	Date	Revcode	Page	Description
A	8/17	0.93	25	KB connector power source change from +3vAUX to +5VAUX
			34	Add HD bus selection circuit for CNR R489 change value from 4.7K to 1K and change power source from +3.3V to +5V
			39	Add +12V power circuit
			41	Add +5VAUX switch power circuit U47 circuit error change +1.5VALW power from pin 1 to pin 7,8 U47 circuit error change +1.5VAUX power from pin 3,7,8 to pin 1,5,6 U47 circuit error change +1.5VSUS power from pin 5,6 to pin 3
			46	Add HD bus selection circuit for DOCK
A	9/22	0.95	4	R25 change to non-populate R26 change value from 100 to 27.4 1% R31 change value from 61.9 1% to 27.4 1%
			8	Add "RSET" signal switch circuit to select different resistor for CRT or TV
			9	Add R126 4.7K for "VRDSLP" signal pull-up
			17	Add R684 4.7K for disable MIDI function
			18	COM port change to using non-interleave type cable
			26	Add R685 4.7K for detect CRT plug-in
			28	Add R761 4.7K pull-down for "ENVDD1" signal Add R760 4.7K pull-down for "ENVBLD1" signal
			34	Circuit ERROR modify switch AC97/HD bus circuit
			46	Modify "-DCKPSNT" signal level shift circuit
			A	10/11

		VIA TECHNOLOGIES INC.	
Title		P.I.R. (1)	
Size	Document Number	Rev	
Custom	VT6304A3	3.1	
Date:	Wednesday, August 02, 2006	Sheet	52 of 53

Version	Date	Revcode	Page	Description
A1	11/11	1.1	5	Delete J2
			8	U4 VSUS15 pin AJ10 and AJ11 change power plant from +1.5VSUS_SR to +1.5VAUX_SR Add measurement +1.5VAUX_SR power current circuit (C239, C233, C224, C225, C230, C234, R127)
			9	BAT1 change package from BH-12T to B7566BP5L
			11	Table 3 have modification
			12	SW5 table have modification R169 non-populate and R168 populate for selection mobile mode
			14	RN65 replace to R734, R735, R737, R738
			15	P_IDE1 pin 34 connect to P_IDE2 pin 34 (-CBLID) Add R700 pin 1 connect "-CBLID" signal, pin 2 connect to U4 pin AH8
			20	U17 pin 16, 68, 72, 78, 82 change signals from power to NC
			21	R299 change ground to INT_CD_GND U18 pin 45, 46 add two capacitor C699, C563 Add CD_IN1 connector
			22	C421, C422 non-populate
			23	J10B and J10C change signals
			27	R706, R707, R708 non-populate for test only
			28	J13 pin 1 change power source from B+ to +12V
			29	C521, C522 change package
			31	PC164B1 modify pin definition, pin A33, A34, B33, B34 change signal to A24, A25, B24, B25
			33	Add R599 (4.7K), Q88 (DTA114YKA) for S3 LED circuit
			40	Separate R575, R576, U44 pin20, 19 signal (circuit error)
			44	U54 pin 13, 14 and pin 11, 12 change signals (circuit error)

Version Date Revcode

		VIA TECHNOLOGIES INC.	
Title		P.I.R. (2)	
Size	Document Number	Rev	
Custom	VT6304A3	3.1	
Date:	Wednesday, August 02, 2006	Sheet	53 of 53