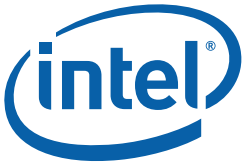

Intel® Core™2 Duo Mobile Processor, Mobile Intel® 965 Express Chipset Family and ICH8M I/O Controller Hub

Schematics

December 2006

Revision 1.5

Intel Confidential

Document Number: 481353

Matanzas

Intel® Core™2 Duo Mobile Processor, Mobile Intel® 965 Express Chipset Family and ICH8M

Customer Reference Board

Rev 1.5

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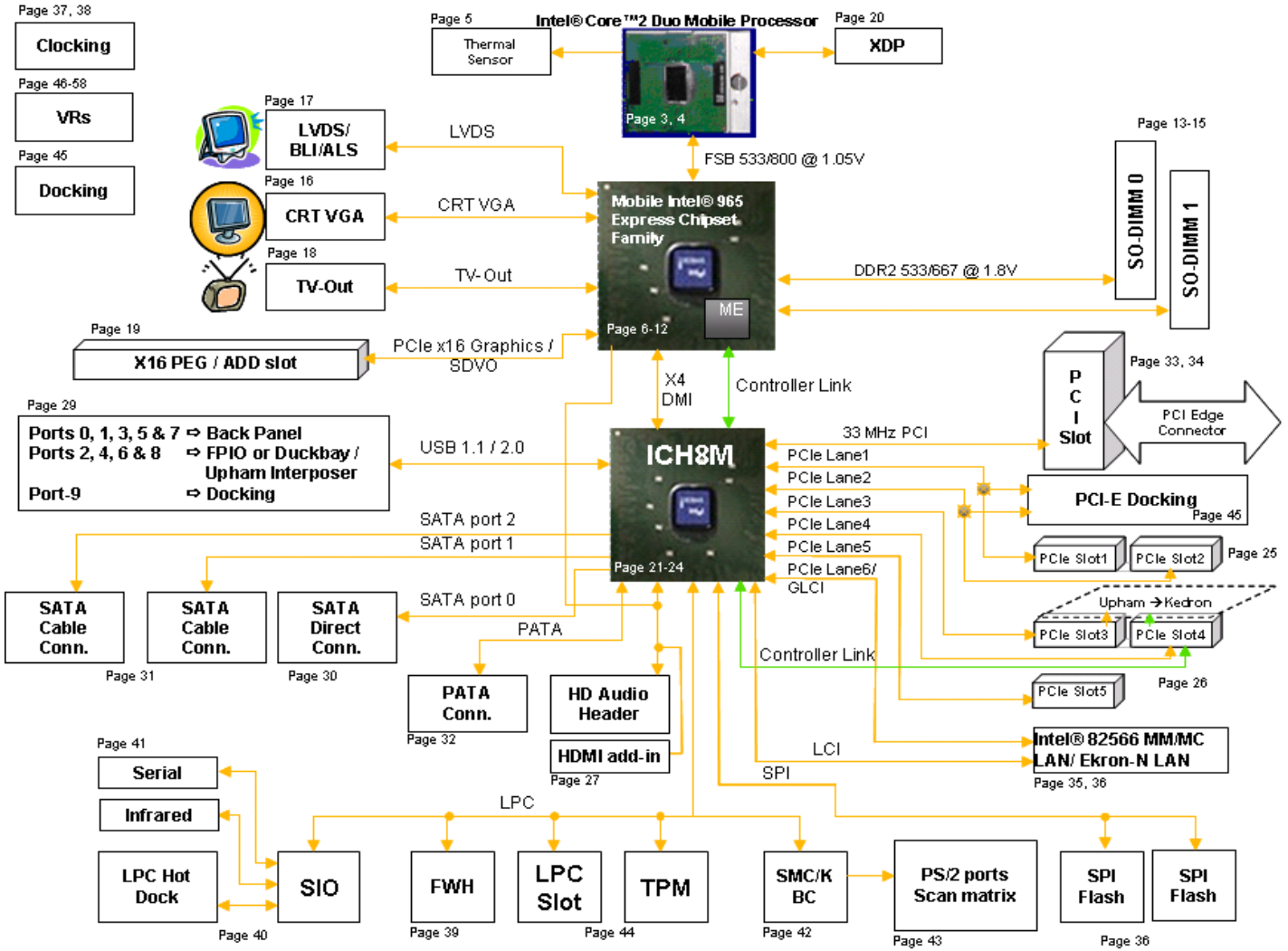

Matanzas		Intel Confidential
Title: TITLE PAGE		
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Rev 1.5 (Changes from Rev 1.301)

Note: Revision 1.5 of the CRB Schematics is based on Fab 3 of Matanzas boards.

Page:3
-The PROCHOT signal pull up value changed from 75 Ohms to 1K Ohms,1%. This fixes the PROCHOT# failure when driven by thermal sensor on the CRB.
Page:7
-Updated Crestline symbol to indicate LVDSB_DATA_3 and LVDSB_DATA#3 pins to support Dual Channel 24-bit LVDS Support.
Page:10
-Crestline CRT/TV QDAC Filter Change (Refer to WW44 Santa Rosa MOW)
-Changed FB5T1 to R5U20 Resistor 100 ohms, 5%,1/16W
-Changed no-stuff R5T5 with C5T20 1.0uF,20%
Page:13
-Corrected net name RSVD-M_A_A14 to M_A_A14
Page:14
-Corrected net name RSVD-M_B_A14 to M_B_A14
Page:17
-LVDS Connector updated to indicate LVDSB_DATA_3 and LVDSB_DATA#3 pins
Page:21
-Added a note that ICH8M Internal VR should not be disabled.
Page:22
-Added strapping configuration information for PCIe x2
Page:23
-Removed the pull-up to +V3.3S circuit on CRB_SV_DET. Customer platforms should pull-up CRB_SV_DET (if used) to +V3.3A via 10k Ohm resistor.
Page 31:
-Clarified SATA Port 1 impact with J7J2 No Shunt
Page:36
-Auto Connect Battery Saver Energy Detect Circuit Update: R5A3 changed from 3.92KOhms to 1.87KOhms. This is an update to the recommendation in the WW44 Santa Rosa MOW.
Page:41
If SPI Descriptor Lock is removed, a 1k Ohms resistor is required between pins 9 and 7 of J8F1 to avoid damage to I/Os.
Page:44
-ME_SMC_ALERT# should be pulled-up to +V3.3A instead of +V3.3M. On the CRB,R6G17 is made no-stuff & the internal pull up on the H8 is enabled. Customer platforms need to pull this signal to +V3.3A.
-Added note on ME_SMC_ALERT# assertion/de-assertion indication
Page:48
-499 Ohms value of R5G10 causes +V1.05S to be +V1.09S. R5G10 changed from 499Ohms to 0Ohms.
Page:49
-R3G13, R3G12, R3G11, R3G9, R3G10 stuff with 20K resistors
-R3G14 stuff with 30K resistor
-R2G16 value changed to 100K resistor
-J2G1 – Removed jumper shunts. No shunts to be installed.
-The pull up on GVR_VID3 (R3G10) and GVR_VR_EN (R3G14) should be connected to +V3.3S instead of +V3.3
-Modified sheet Graphics Controller symbol
Page:52 & 53
-Modified sheet IMVP Controller and FET Symbols
Page:55
-J3G1 Pin1 and 2 should be shorted for ME support in G3 state.
-Corrected net name XDP_DBRESET#_R to XDP_DBRESET#

Title: Revision History		
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SANTA ROSA CUSTOMER REFERENCE PLATFORM

SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

Voltage Rails

POWER PLANE	VOLTAGE	ACTIVE IN	DESCRIPTION
+VBATA	9V-12.5V	S0/M0, (S3-S5)/M1, (S3-S5)/M-off	Battery Rail in Mobile Power Mode
+VBAT	9V-12.5V	S0/M0, (S3-S5)/M1, (S3-S5)/M-off	Battery Rail in Mobile Power Mode
+VBATS	9V-12.5V	S0/M0	Battery Rail in Mobile Power Mode
+V12S	12V	S0/M0	Only on in DT Power Mode
-V12A	-12V	S0/M0, (S3-S5)/M1, (S3-S5)/M-off	Only on in DT Power Mode
-V12S	-12V	S0/M0	Only on in DT Power Mode
+V5A	5V	S0/M0, (S3-S5)/M1, (S3-S5)/M-off	
+V5	5V	S0/M0,* 3/M1, S3/M-off	
+V5S	5V	S0/M0	
+V3.3A	3.3V	S0/M0, (S3-S5)/M1, (S3-S5)/M-off	
+V3.3M	3.3V	S0/M0, (S3-S5)/M1, S3/(M-off w/WOL_EN)	LAN
+V3.3M_CK505	3.3V	S0/M0, (S3-S5)/M1	Clock, MCH
+V3.3	3.3V	S0/M0, S3/M1, S3/M-off	
+V3.3S	3.3V	S0/M0	
+V1.8	1.8V	S0/M0, (S3-S5)/M1, S3/M-off	DDR core
+V1.5S	1.5V	S0/M0	
+V1.25M	1.25V	S0/M0, (S3-S5)/M1	
+V1.25S	1.25V	S0/M0	
+V1.05M	1.05V	S0/M0, (S3-S5)/M1	
+V1.05S	1.05V	S0/M0	GMCH, ICH core, and FSB rail
+V0.9	0.9V	S0/M0, (S3-S5)/M1, S3/M-off	DDR command & control pull up.
+VCC_CORE	0.700V-1.77V	S0/M0	CPU core rail
+VCC_GFXCORE	0.7V-1.25V	S0/M0	GMCH Graphics core rail

I 2 C / SMB Addresses

Device	Address	Hex	Bus
Clock Generator	1101 001x	D2	SMB_ICH_M3
DB800 Clock Buffer	1101 110x	DC	SMB_ICH_M3
SO-DIMM0	1010 000x	A0	SMB_ICH_M2
SO-DIMM1	1010 010x	A4	SMB_ICH_M2
SO-DIMM0 Thermal Sensor	0011 000x	30	SMB_ICH_M2
SO-DIMM1 Thermal Sensor	0011 010x	34	SMB_ICH_M2
DDR Thermal Sensor	0100 110x	4C	SMB_ICH_M2
I2C Bus Expander	0011 xxxx	3x	SMB_ICH
Ambient Lighr Sensor	0111 001x	72	ALS
EMA Display	0011 110x	3C	EMA
CPU Thermal Sensor	1001 100x	98	SMB_THRM
IMVP6 Amb. Temp. Sensor	1001 101x	9A	SMB_THRM
Battery A	0001 011x	16	SMB_BS
Battery B	0001 111x	1E	SMB_BS
Board ID Port Expander	0011 000x	30	SMB_BS
Docking Port Expander	0011 001x	32	SMB_BS
Skin Temperature Sensor	1001 100x	98	SMB_BS
H8	TBD	TBD	SMB_ME
PCI-Slot3	TBD	TBD	SMB_ICH_A1
PCI-Gold Finger	TBD	TBD	SMB_ICH_A1
PCI-Express Slot1-5	TBD	TBD	SMB_ICH_A1
Docking	TBD	TBD	SMB_ICH_A1
PCIe x16 Slot (PEG)	TBD	TBD	SMB_ICH_S4
TPM Header	TBD	TBD	SMB_ICH_S4
ITP-XDP	TBD	TBD	SMB_ICH_S4

Buses labeled SMB_ICH_xx come out of ICH, via an I2C expander.
The rest come out of EC.

Jumper / Switch Settings

Jumper	Default	Description	Page
J1G2	1-2	BSEL0	37
J1G5	1-2	BSEL1	37
J1G8	1-2	BSEL2	37
J2G1	1-2	GFX CORE	49
J2G1	3-4	GFX CORE	49
J2G1	5-6	GFX CORE	49
J2G1	7-8	GFX CORE	49
J2G1	11-12	GFX CORE	49
J2H1	1-X	Force Shutdown	55
J3B2	1-2, 3-4	CPU thermal sensor	5
J3G1	1-X	Power ON Latch	55
J4H1	1-X	ME G3 to M1	55
J5H2	1-X	CMOS Clear	21
J6H2	1-2	CRB/SV Detect	23
J7D1	1-2	SIO Reset	40
J7J2	1-2	SATA Power Enable	31
J8B1	1-2	In-circuit SMC Programming	41
J8B2	1-2	In-circuit SMC Programming	41
J8E2	1-X	Boot BIOS Strap	22
J8F2	1-X	BIOS recovery	23
J9F1	1-2	KSC Enable	42
J9G2	1-2	Boot Block Programming	43
J9H1	1-X	Virtual Docking	42
J9H2	1-X	NMI	43
J9H3	1-X	KBC disable	42
J9H4	1-2	SMC MD0	42
J9H5	1-2	SATA device detect	31
J9H6	1-X	SMC MD2	42
J9H7	1-2	SMC MD1	42
J9H8	1-X	LID Position	42
J9H9	1-X	Virtual Battery	42

Switch	Default	Description	Page
SW9H1	1 - 2	Virtual Docking	42
SW9H2	1 - 2	Virtual Battery	42
SW9J1	1 - 2	LID Switch	42

Changes for Matanzas with PM GMCH SKU

SL No	NO_STUFF	STUFF
1	U6E2, U6E3, U6E4	
2	L5F1	
3	R5E5, R5F9, R5T16, R5U3, R5U11, R5U14, R5U21, R6V1	R5E4, R5T5, R5T8, R5T9, R5T10, R5T12, R5T17
4	C5E8, C5E9, C5E11, C5E12, C5E13, C5E14, C5E15, C5T12, C5T13, C5U1, C5U2, C5U3	C5E8,C5E9,C5T13,C5U3 with 0 Ohm 0402 size res IPN A93549-001
5	FB5F1, FB5F2, FB5T1	
6	J2G1(3 4), J2G1(5 6),	J2G1(1 2), J2G1(13 14)

PCI Devices

Device	IDSEL #	REQ/GNT #	Interrupts
Slot 3	AD18	2 2	D, C, A, B
LAN	(AD24 internal)		

Net Naming Conventions

Suffix
= Active Low Signal

Prefix
H = Host
M = DDR Memory
TP = Test Point (does not connect anywhere else)

LEDs and Switches

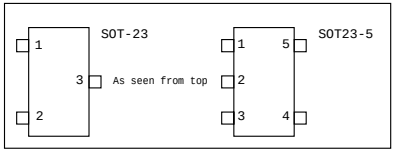
LED	Page	Reference
xTA Activity	21	CR6J1
VID0	41	CR1B1
VID1	41	CR1B2
VID2	41	CR1B3
VID3	41	CR1B4
VID4	41	CR1B5
VID5	41	CR1B6
VID6	41	CR1B7
Num Lock	42	CR9G1
Scroll Lock	42	CR9G2
Caps Lock	42	CR9G3
S3	57	CR3G2
M0/M1	57	CR4H1
S4	57	CR5H3
S5	57	CR5H4
S0	57	CR5H5
System Power Good	57	CR5J1

Switch	Page	Reference
Power Button	55	SW1C1
Reset Button	55	SW1C2
Net Detect	55	SW8E1
Virtual Docking	42	SW9H1
Virtual Battery	42	SW9H2
LID Switch	42	SW9J1

Wake Events

Wake Events	State Supported
RI# from serial port	S3
PME# from PCI, mini PCI slot/device, LPC slot/device	S3
PCI Express, mini PCI Express, Express-card wake event	S3
Wake on LAN	S3/M1
LID switch attached to SMC	S3
USB	S3
HDA wake on ring	S3
SmLink for AOLII	S3
Hot Key from Scan matrix keyboard	S3
PS/2 Keyboard/mouse	S3
PWRBTN#	S3
Netdetect	S3, S4, S5 / M1

PCB Footprints



Power States	SLP_S3#	S4_STATE#	SLP_S4#	SLP_S5#	SLP_M#	+V*A	+V3.3M	+V1.25M/ +V1.05M	+V3.3M_CK505	+V1.8/+V0.9	+V5/+V3.3	+V*S	Clocks
S0 (Full on)/M0	HIGH	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON	ON	ON	ON
S3 (Suspend to RAM)/M1	LOW	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON	ON	OFF	only MCH BCLK
S3 (Suspend to RAM)/Moff	LOW	HIGH	HIGH	HIGH	LOW	ON	OFF	OFF	OFF	ON	ON	OFF	OFF
S3 (Susp to RAM)/Moff w/WOL_EN	LOW	HIGH	HIGH	HIGH	LOW	ON	ON	OFF	OFF	ON	ON	OFF	OFF
S4 (Suspend to Disk)/M1	LOW	LOW	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON	OFF	OFF	only MCH BCLK
S5 (Soft Off)/M1	LOW	LOW	HIGH	LOW	HIGH	ON	ON	ON	ON	ON	OFF	OFF	only MCH BCLK
S4 (Suspend to Disk)/Moff	LOW	LOW	LOW	HIGH	LOW	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF
S5 (Soft Off)/Moff	LOW	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF

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Title: NOTES

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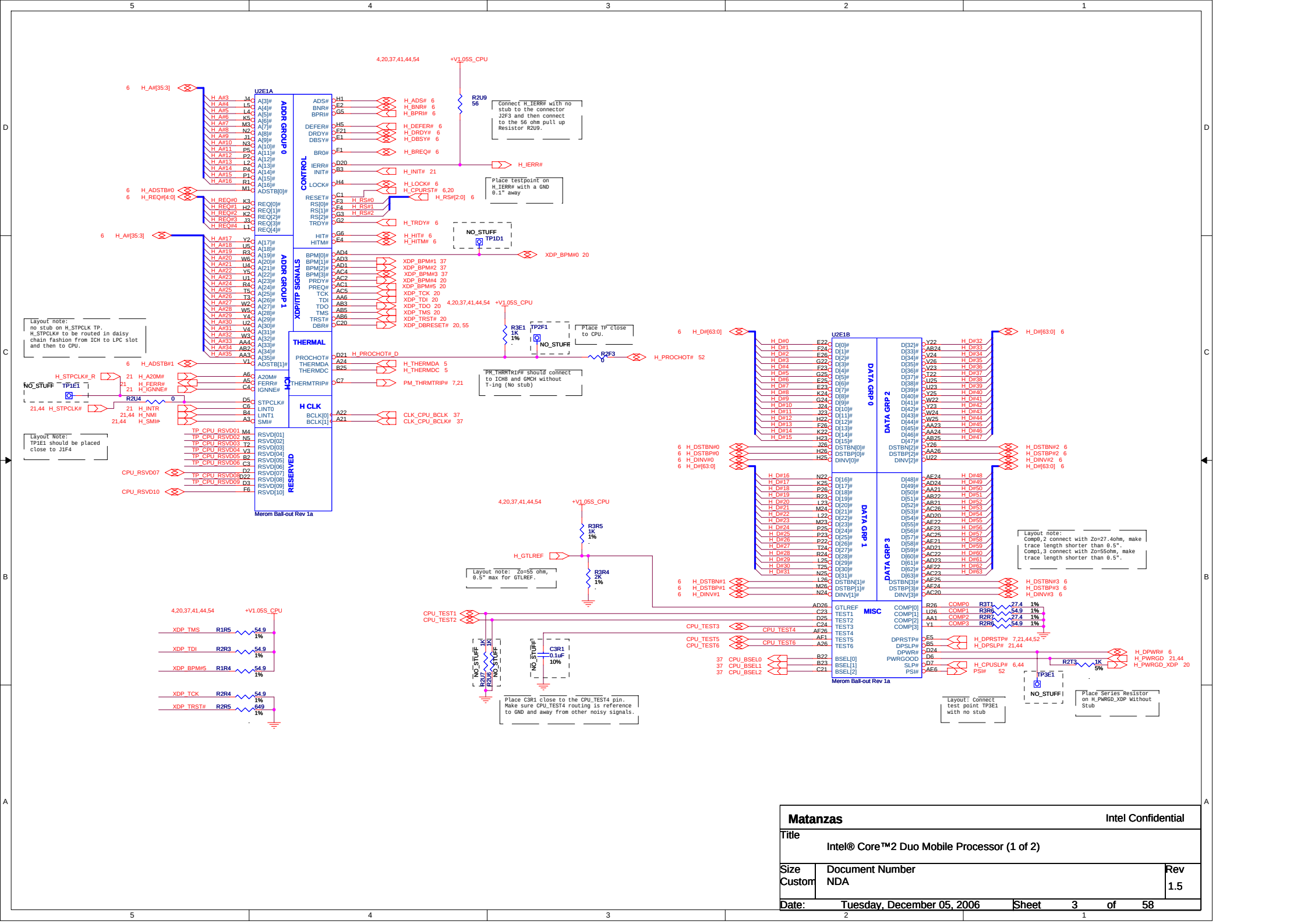
U2E1A
ADDR GROUP 0
ADDR GROUP 1
CONTROL
XDP/ITP SIGNALS
THERMAL
H CLK
RESERVED
Merom Ball-out Rev 1a
U2E1B
DATA GRP 0
DATA GRP 1
DATA GRP 2
DATA GRP 3
MISC
Merom Ball-out Rev 1a
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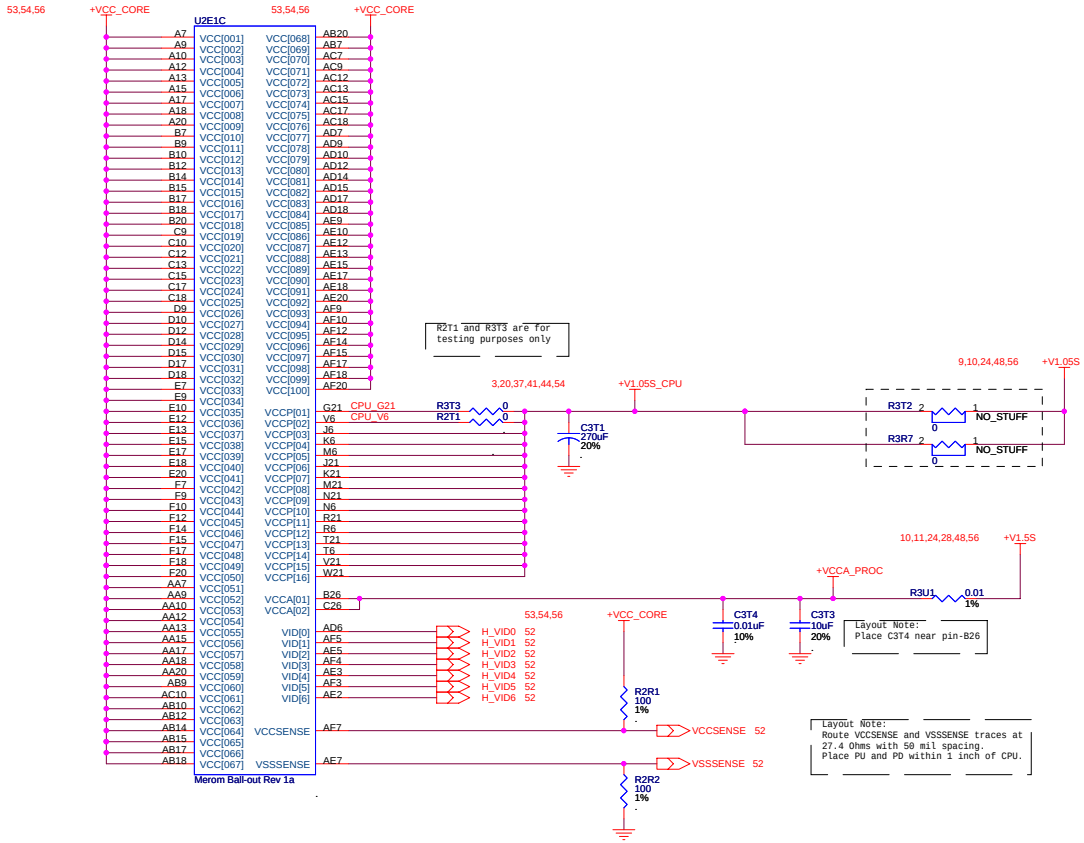

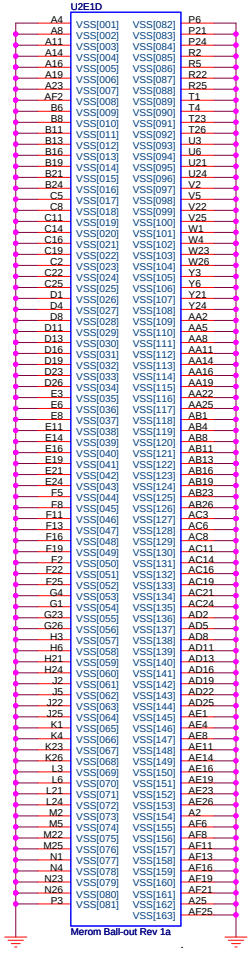

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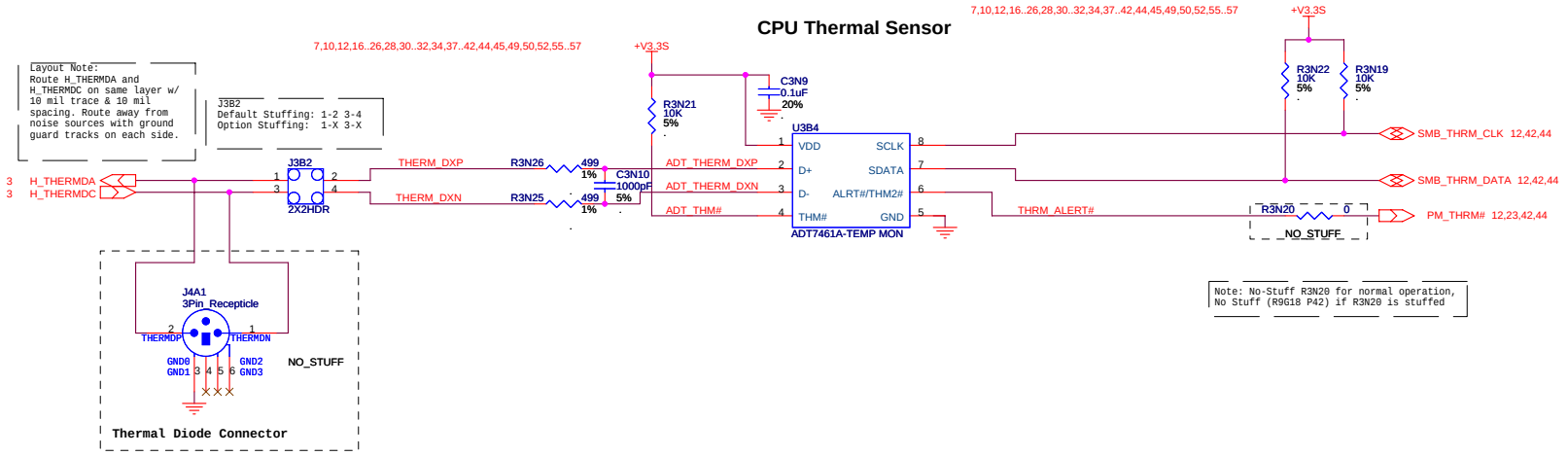
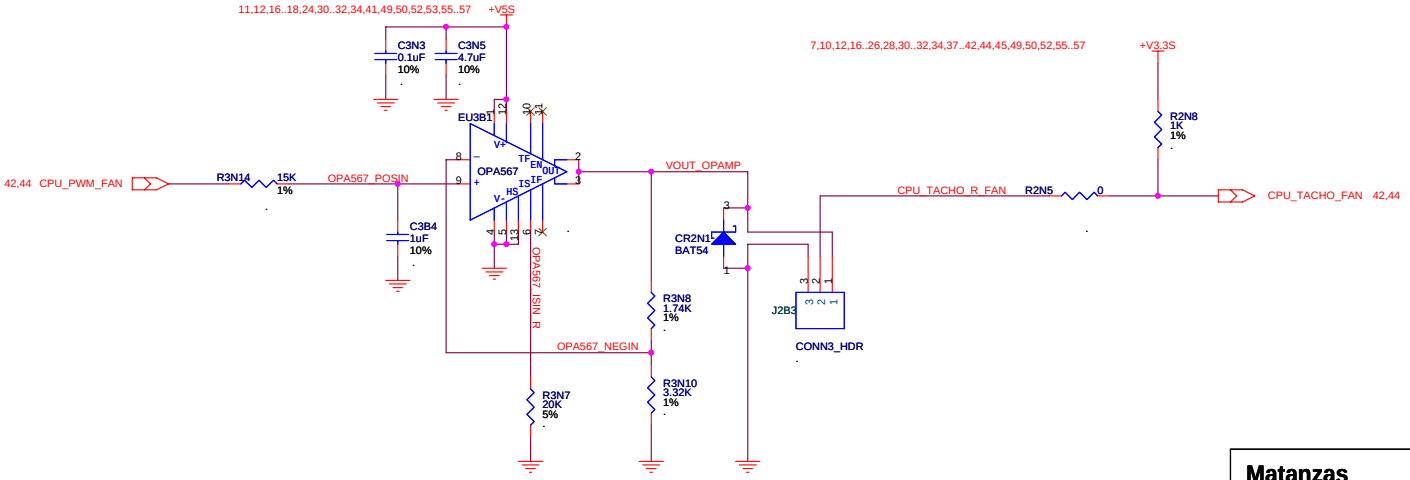
CPU Thermal Sensor



CPU Fan Power Control



Matanzas		Intel Confidential
Title: CPU Thermal Sensor & Fan		
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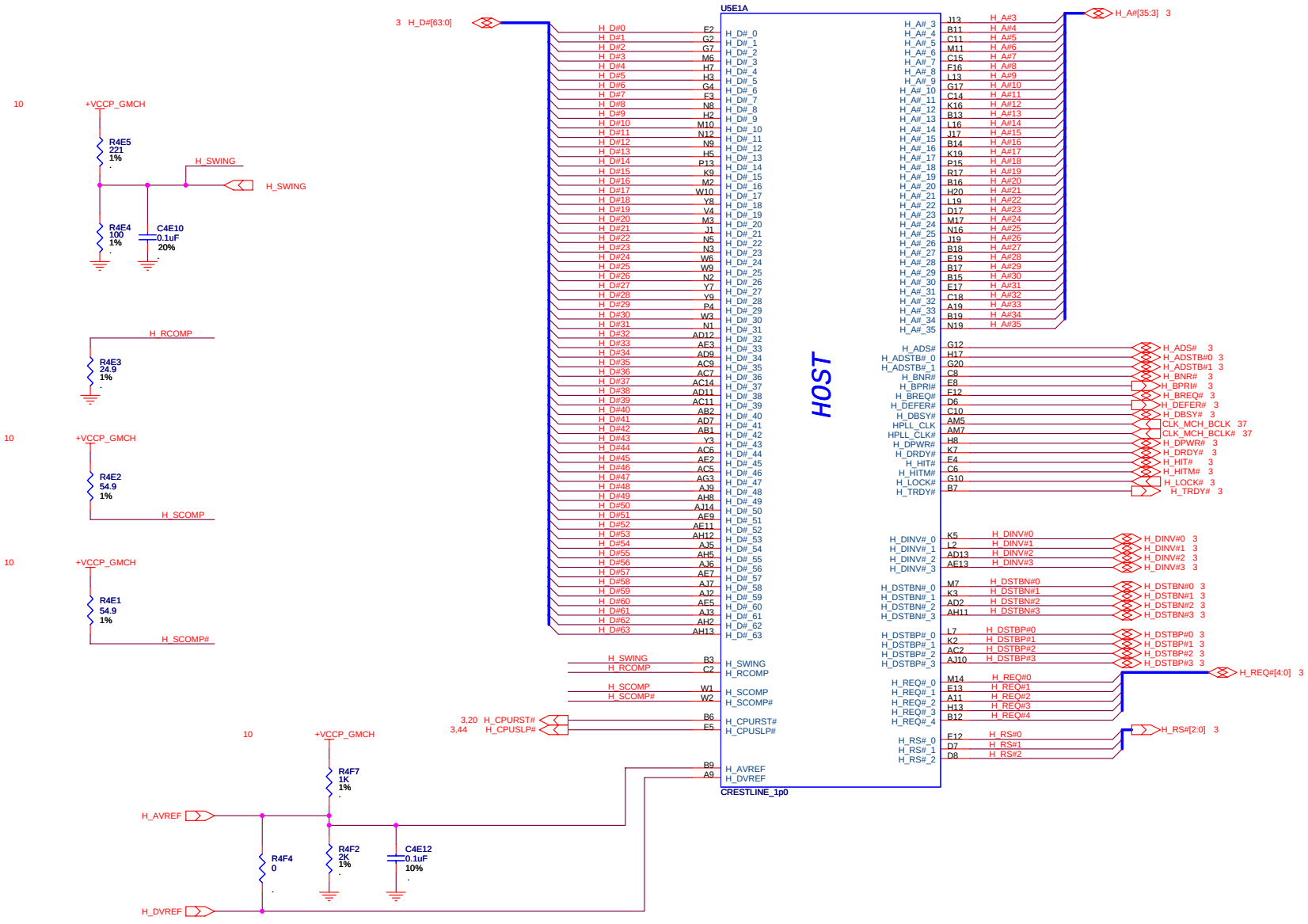

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Title	Mobile Intel® 965 Express Chipset Family (1 OF 6)	
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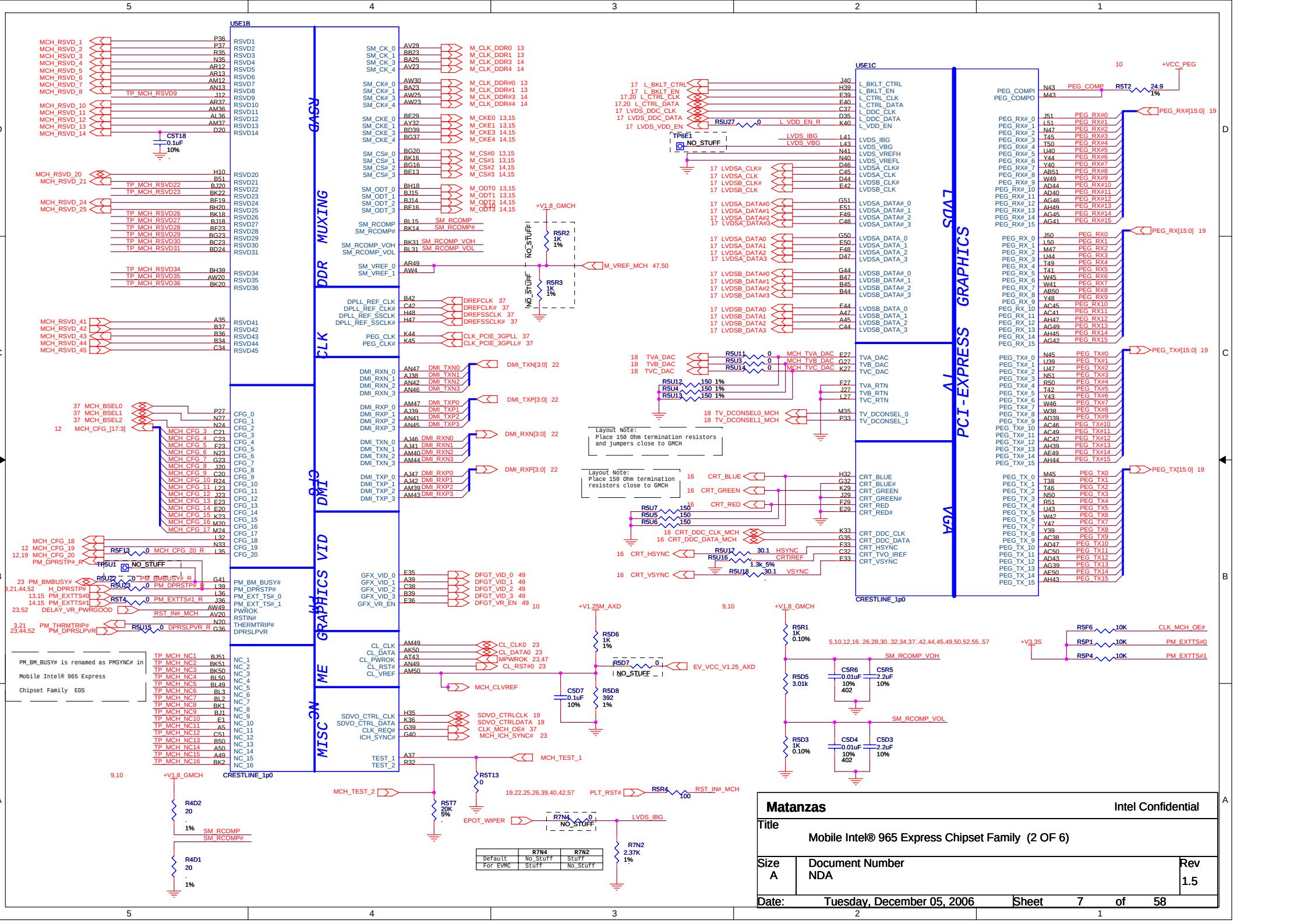
U5E1B
MCH_RSVD_1
MCH_RSVD_2
MCH_RSVD_3
MCH_RSVD_4
MCH_RSVD_5
MCH_RSVD_6
MCH_RSVD_7
MCH_RSVD_8
TP_MCH_RSVD9
MCH_RSVD_10
MCH_RSVD_11
MCH_RSVD_12
MCH_RSVD_13
MCH_RSVD_14
C5T18 0.1uF 10%
MCH_RSVD_20
MCH_RSVD_21
TP_MCH_RSVD22
TP_MCH_RSVD23
MCH_RSVD_24
MCH_RSVD_25
TP_MCH_RSVD26
TP_MCH_RSVD27
TP_MCH_RSVD28
TP_MCH_RSVD29
TP_MCH_RSVD30
TP_MCH_RSVD31
TP_MCH_RSVD34
TP_MCH_RSVD35
TP_MCH_RSVD36
MCH_RSVD_41
MCH_RSVD_42
MCH_RSVD_43
MCH_RSVD_44
MCH_RSVD_45
EASY
DDR MUXING
CLK
DMI
GRAPHICS VID
MISC
ME
SM_CK_0
SM_CK_1
SM_CK_3
SM_CK_4
SM_CK#_0
SM_CK#_1
SM_CK#_3
SM_CK#_4
SM_CKE_0
SM_CKE_1
SM_CKE_3
SM_CKE_4
SM_CS#_0
SM_CS#_1
SM_CS#_2
SM_CS#_3
SM_ODT_0
SM_ODT_1
SM_ODT_2
SM_ODT_3
SM_RCOMP
SM_RCOMP#
SM_RCOMP_VOH
SM_RCOMP_VOL
SM_VREF_0
SM_VREF_1
M_CLK_DDR0 13
M_CLK_DDR1 13
M_CLK_DDR3 14
M_CLK_DDR4 14
M_CLK_DDR#0 13
M_CLK_DDR#1 13
M_CLK_DDR#3 14
M_CLK_DDR#4 14
M_CKE0 13,15
M_CKE1 13,15
M_CKE3 14,15
M_CKE4 14,15
M_CS#0 13,15
M_CS#1 13,15
M_CS#2 14,15
M_CS#3 14,15
M_ODT0 13,15
M_ODT1 13,15
M_ODT2 14,15
M_ODT3 14,15
+V1.8_GMCH
R5R2 1K 1%
R5R3 1K 1%
NO_STUFF
M_VREF_MCH 47,50
DPLL_REF_CLK
DPLL_REF_CLK#
DPLL_REF_SSCLK
DPLL_REF_SSCLK#
DREFCLK 37
DREFCLK# 37
DREFSSCLK 37
DREFSSCLK# 37
PEG_CLK
PEG_CLK#
CLK_PCIE_3GPLL 37
CLK_PCIE_3GPLL# 37
DMI_RXN_0
DMI_RXN_1
DMI_RXN_2
DMI_RXN_3
DMI_RXP_0
DMI_RXP_1
DMI_RXP_2
DMI_RXP_3
DMI_TXN_0
DMI_TXN_1
DMI_TXN_2
DMI_TXN_3
DMI_TXP_0
DMI_TXP_1
DMI_TXP_2
DMI_TXP_3
DMI_TXN[3:0] 22
DMI_TXP[3:0] 22
DMI_RXN[3:0] 22
DMI_RXP[3:0] 22
GFX_VID_0
GFX_VID_1
GFX_VID_2
GFX_VID_3
GFX_VR_EN
DFGT_VID_0 49
DFGT_VID_1 49
DFGT_VID_2 49
DFGT_VID_3 49
DFGT_VR_EN 49
CL_CLK
CL_DATA
CL_PWROK
CL_RST#
CL_VREF
CL_CLK0 23
CL_DATA0 23
MPWROK 23,47
CL_RST#0 23
MCH_CLVREF
SDVO_CTRL_CLK
SDVO_CTRL_DATA
CLK_REQ#
ICH_SYNC#
SDVO_CTRLCLK 19
SDVO_CTRLDATA 19
CLK_MCH_OE# 37
MCH_ICH_SYNC# 23
TEST_1
TEST_2
MCH_TEST_1
MCH_TEST_2
R5T13 0
R5T7 20K 5%
EPOT_WIPER
R7N4 0 NO_STUFF
R7N2 2.37K 1%
LVDS_IBG
R4D2 20 1%
R4D1 20 1%
SM_RCOMP
SM_RCOMP#
CFG_0
CFG_1
CFG_2
CFG_3
CFG_4
CFG_5
CFG_6
CFG_7
CFG_8
CFG_9
CFG_10
CFG_11
CFG_12
CFG_13
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CFG_15
CFG_16
CFG_17
CFG_18
CFG_19
CFG_20
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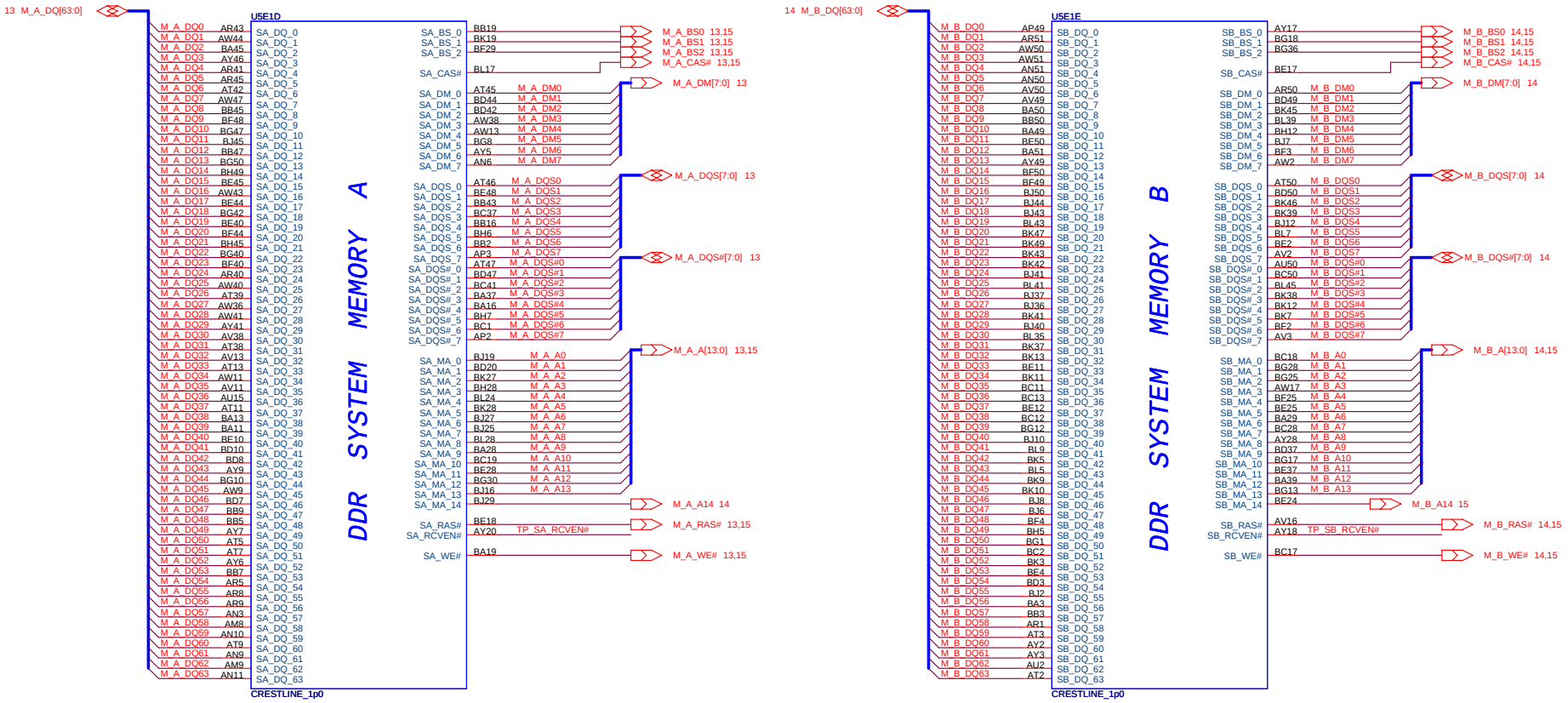
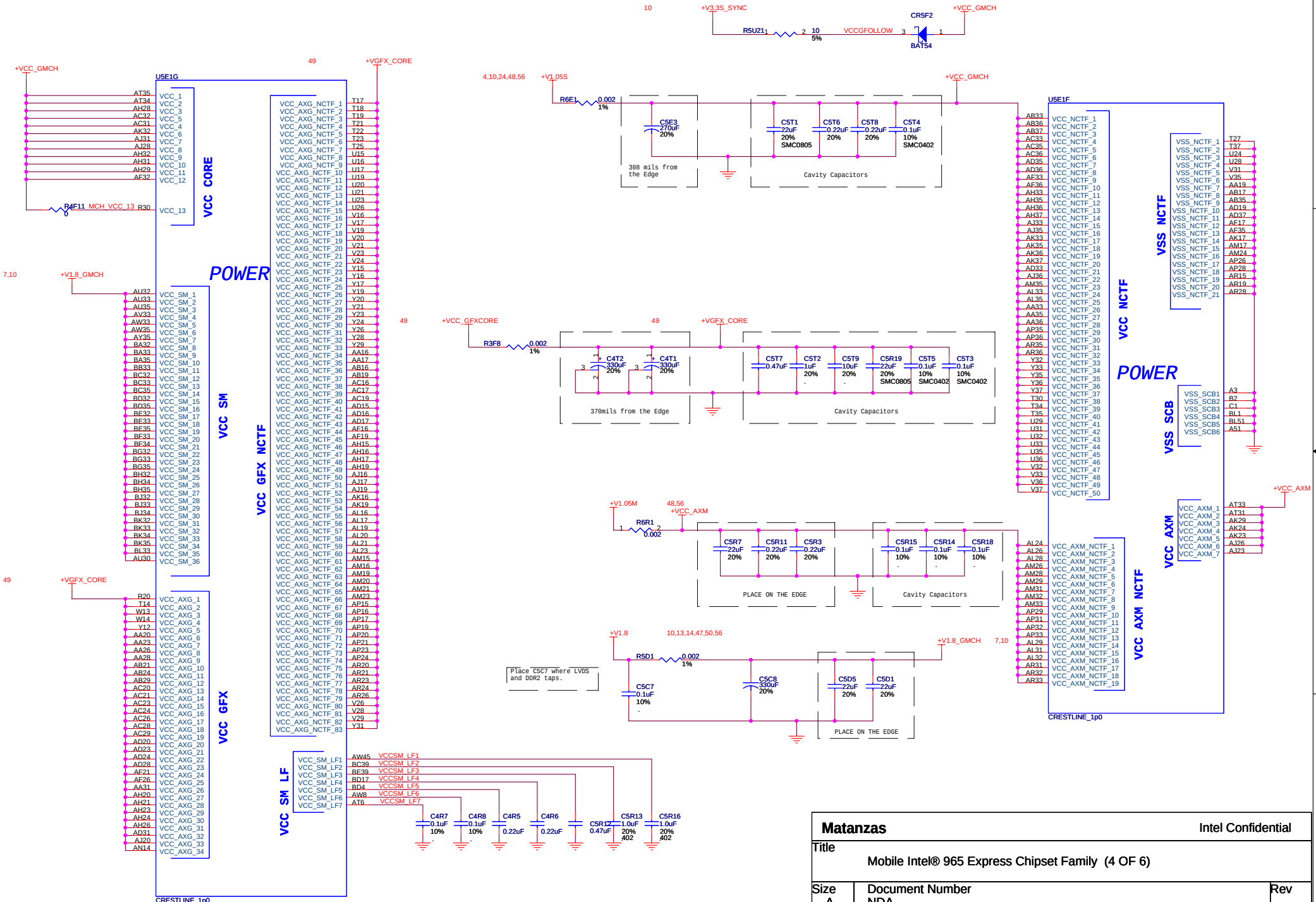
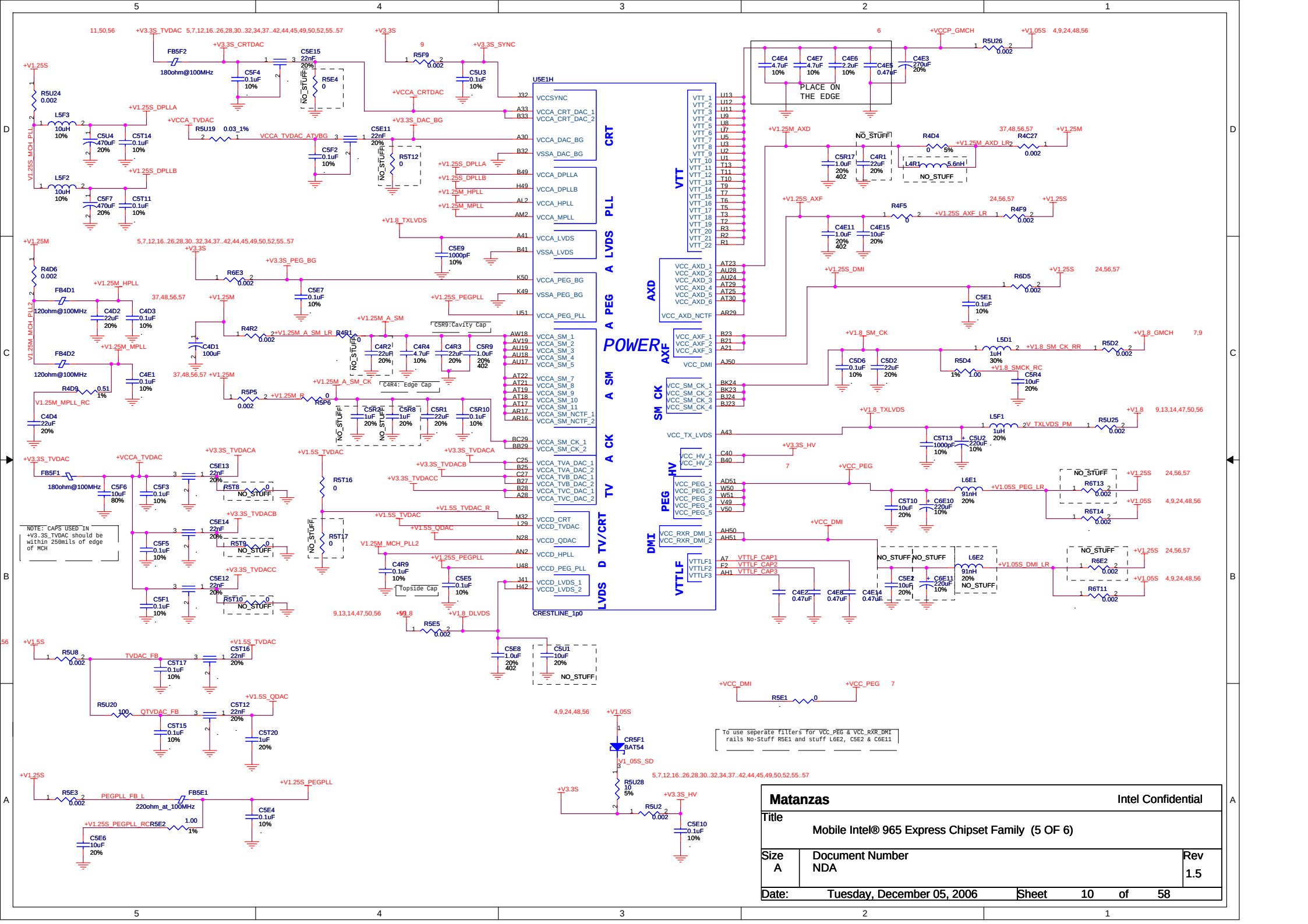
MCH_BSEL1
MCH_BSEL2
MCH_CFG_[17:3]
MCH_CFG_18
MCH_CFG_19
MCH_CFG_20
PM_DPRSTP#_R
R5F13 0 MCH_CFG_20_R
TP5U1 NO_STUFF
R5U22 0 PM_BMBUSY#_R
R5U23 0 PM_DPRSTP#_R
R5T4 0 PM_EXTTS#1_R
RST_IN#_MCH
R5U15 0 DPRSLPVR_R
PM_BMBUSY#
H_DPRSTP#
PM_EXTTS#0
PM_EXTTS#1
DELAY_VR_PWRGOOD
PM_THRMTRIP#
PM_DPRSLPVR
PM_BM_BUSY#
PM_DPRSTP#
PM_EXT_TS#_0
PM_EXT_TS#_1
PWROK
RSTIN#
THERMTRIP#
DPRSLPVR
PM_BM_BUSY# is renamed as PMSYNC# in Mobile Intel® 965 Express Chipset Family EDS
TP_MCH_NC1
TP_MCH_NC2
TP_MCH_NC3
TP_MCH_NC4
TP_MCH_NC5
TP_MCH_NC6
TP_MCH_NC7
TP_MCH_NC8
TP_MCH_NC9
TP_MCH_NC10
TP_MCH_NC11
TP_MCH_NC12
TP_MCH_NC13
TP_MCH_NC14
TP_MCH_NC15
TP_MCH_NC16
NC_1
NC_2
NC_3
NC_4
NC_5
NC_6
NC_7
NC_8
NC_9
NC_10
NC_11
NC_12
NC_13
NC_14
NC_15
NC_16
CRESTLINE_1p0
9,10
+V1.8_GMCH
U5E1C
L_BKLT_CTRL
L_BKLT_EN
L_CTRL_CLK
L_CTRL_DATA
L_DDC_CLK
L_DDC_DATA
L_VDD_EN
R5U27 0 L_VDD_EN_R
TP6E1 NO_STUFF
LVDS_IBG
LVDS_VBG
LVDS_VREFH
LVDS_VREFL
LVDSA_CLK#
LVDSA_CLK
LVDSB_CLK#
LVDSB_CLK
LVDSA_DATA#_0
LVDSA_DATA#_1
LVDSA_DATA#_2
LVDSA_DATA#_3
LVDSA_DATA_0
LVDSA_DATA_1
LVDSA_DATA_2
LVDSA_DATA_3
LVDSB_DATA#_0
LVDSB_DATA#_1
LVDSB_DATA#_2
LVDSB_DATA#_3
LVDSB_DATA_0
LVDSB_DATA_1
LVDSB_DATA_2
LVDSB_DATA_3
LVDS
PCI-EXPRESS GRAPHICS
TVA
VGA
TVA_DAC
TVB_DAC
TVC_DAC
TVA_RTN
TVB_RTN
TVC_RTN
TV_DCONSEL_0
TV_DCONSEL_1
R5U11 0 MCH_TVA_DAC
R5U3 0 MCH_TVB_DAC
R5U14 0 MCH_TVC_DAC
R5U12 150 1%
R5U4 150 1%
R5U13 150 1%
TV_DCONSEL0_MCH
TV_DCONSEL1_MCH
Layout Note: Place 150 Ohm termination resistors and jumpers close to GMCH
CRT_BLUE
CRT_BLUE#
CRT_GREEN
CRT_GREEN#
CRT_RED
CRT_RED#
CRT_DDC_CLK
CRT_DDC_DATA
CRT_HSYNC
CRT_TVO_IREF
CRT_VSYNC
R5U7 150
R5U5 150
R5U6 150
CRT_DDC_CLK_MCH
CRT_DDC_DATA_MCH
R5U17 30.1 HSYNC
R5U16 CRTIREF 1.3K_5%
R5U18 30.1 VSYNC
Layout Note: Place 150 Ohm termination resistors close to GMCH
CRESTLINE_1p0
PEG_COMPI
PEG_COMPO
PEG_COMP
R5T2 24.9 1%
+VCC_PEG
PEG_RX#_0
PEG_RX#_1
PEG_RX#_2
PEG_RX#_3
PEG_RX#_4
PEG_RX#_5
PEG_RX#_6
PEG_RX#_7
PEG_RX#_8
PEG_RX#_9
PEG_RX#_10
PEG_RX#_11
PEG_RX#_12
PEG_RX#_13
PEG_RX#_14
PEG_RX#_15
PEG_RX#[15:0] 19
PEG_RX_0
PEG_RX_1
PEG_RX_2
PEG_RX_3
PEG_RX_4
PEG_RX_5
PEG_RX_6
PEG_RX_7
PEG_RX_8
PEG_RX_9
PEG_RX_10
PEG_RX_11
PEG_RX_12
PEG_RX_13
PEG_RX_14
PEG_RX_15
PEG_RX[15:0] 19
PEG_TX#_0
PEG_TX#_1
PEG_TX#_2
PEG_TX#_3
PEG_TX#_4
PEG_TX#_5
PEG_TX#_6
PEG_TX#_7
PEG_TX#_8
PEG_TX#_9
PEG_TX#_10
PEG_TX#_11
PEG_TX#_12
PEG_TX#_13
PEG_TX#_14
PEG_TX#_15
PEG_TX#[15:0] 19
PEG_TX_0
PEG_TX_1
PEG_TX_2
PEG_TX_3
PEG_TX_4
PEG_TX_5
PEG_TX_6
PEG_TX_7
PEG_TX_8
PEG_TX_9
PEG_TX_10
PEG_TX_11
PEG_TX_12
PEG_TX_13
PEG_TX_14
PEG_TX_15
PEG_TX[15:0] 19
9,10
+V1.25M_AXD
R5D6 1K 1%
R5D7 0 NO_STUFF
EV_VCC_V1.25_AXD
R5D8 392 1%
C5D7 0.1uF 10%
5,10,12,16..26,28,30..32,34,37..42,44,45,49,50,52,55..57
SM_RCOMP_VOH
SM_RCOMP_VOL
R5D5 3.01k
R5D3 1K 0.10%
C5R6 0.01uF 10% 402
C5R5 2.2uF 10%
C5D4 0.01uF 10% 402
C5D3 2.2uF 10%
R5R1 1K 0.10%
+V3.3S
R5F6 10K CLK_MCH_OE#
R5P1 10K PM_EXTTS#0
R5P4 10K PM_EXTTS#1
19,22,25,26,39,40,42,57
PLT_RST#
R5R4 100 RST_IN#_MCH
R7N4 R7N2
Default No_Stuff Stuff
For EVMC Stuff No_Stuff
Matanzas
Intel Confidential
Title
Mobile Intel® 965 Express Chipset Family (2 OF 6)
Size A
Document Number NDA
Rev 1.5
Date: Tuesday, December 05, 2006
Sheet 7 of 58



Matanzas		Intel Confidential
Title	Mobile Intel® 965 Express Chipset Family (3 OF 6)	
Size A	Document Number NDA	Rev 1.5
Date: Tuesday, December 05, 2006	Sheet 8 of 58	



Matanzas		Intel Confidential
Title	Mobile Intel® 965 Express Chipset Family (4 OF 6)	
Size A	Document Number NDA	Rev 1.5
Date: Tuesday, December 05, 2006	Sheet 9 of 58	


U5E1H
CRESTLINE_1p0
CRT
PLL
LVDS
A LVDS
A PEG
A SM
A CK
TV
D TV/CRT
LVDS
VTT
AXD
POWER
AXF
SM CK
VCC_HV
PEG HV
DMI
VTTLF
PLACE ON THE EDGE
NOTE: CAPS USED IN +V3.3S_TVDAC should be within 250mils of edge of MCH
To use seperate filters for VCC_PEG & VCC_RXR_DMI rails No-Stuff R5E1 and stuff L6E2, C5E2 & C6E11
Matanzas
Intel Confidential
Title
Mobile Intel® 965 Express Chipset Family (5 OF 6)
Size A
Document Number NDA
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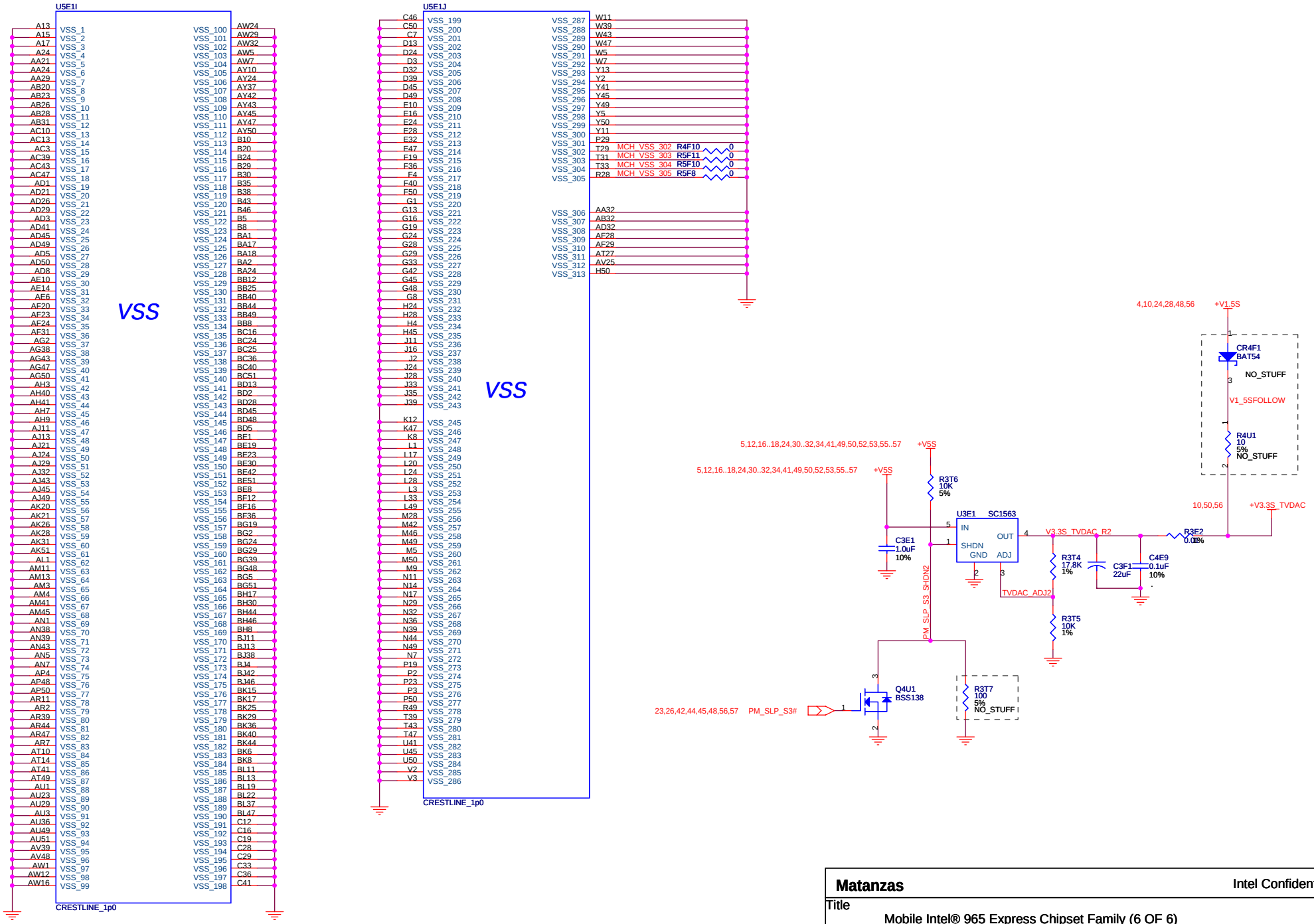
Date: Tuesday, December 05, 2006
Sheet 10 of 58



Matanzas		Intel Confidential
Title	Mobile Intel® 965 Express Chipset Family (6 OF 6)	
Size A	Document Number NDA	Rev 1.5
Date: Tuesday, December 05, 2006	Sheet 11 of 58	

Layout Note:
Location of all MCH_CFG strap resistors
needs to be close to trace to minimize stub

7 MCH_CFG_5

DMI X2 Select	
MCH_CFG_5	Low = DMIx2 High = DMIx4 (default)

R1D4 4.02K 1% NO_STUFF

5,7,10,16..26,28,30..32,34,37..42,44,45,49,50,52,55..57 +V3.3S

SDVO/PCIE Concurrent Operation	
MCH_CFG_20	Low = Only SDVO or PCIE x1 is operational (default) High = SDVO and PCIE x1 are operating simultaneously via the PEG port

R6P3 4.02K 1% NO_STUFF

7,19 MCH_CFG_20

GMCH Fan Power Control

5,11,16..18,24,30..32,34,41,49,50,52,53,55..57 +V5S

C3P3 0.1uF 10%
C3C8 4.7uF 10%

EU4C1 OPA567

42,44 MCH_PWM_FAN
R4P2 15K 1%
OPA567_POSIN_R
C4C18 1uF 10%

MCH_TACHO_OP_FAN
CR3P1 BAT54
MCH_TACHO_R_FAN
R3P3 0
MCH_TACHO_FAN 42,44

5,7,10,16..26,28,30..32,34,37..42,44,45,49,50,52,55..57 +V3.3S
R3P2 1K 1%

R3P1 1.74K 1%
R4C26 3.32K 1%
R4P1 20K 5%
OPA567_NEGIN_R
OPA567_ISIN_MCH_R

J3C1 CONN3_HDR

7 MCH_CFG_16

FSB Dynamic ODT	
MCH_CFG_16	Low = Dynamic ODT Disabled High = Dynamic ODT Enabled (default)

R1E1 4.02K 1% NO_STUFF

7 MCH_CFG_9

PCI Express Graphics Lane	
MCH_CFG_9	Low = Reverse Lane (default) High = Normal operation

R1E7 4.02K 1%

5,7,10,16..26,28,30..32,34,37..42,44,45,49,50,52,55..57 +V3.3S

DMI Lane Reversal	
MCH_CFG_19	Low = Normal (default) High = Lanes Reversed

R5F15 4.02K 1% NO_STUFF

7 MCH_CFG_19

IMVP6 & Amb Thermal sensors

5,7,10,16..26,28,30..32,34,37..42,44,45,49,50,52,55..57 +V3.3S

R3B23 10K 1%
C3B6 0.1uF 20%
R3B24 10K 1%

Q3C6 2N3904
7481_D1P_Q R3B20 0
7481_D1N_Q R3B22 0
C3N8 1000pF 10%
Place in IMVP_6 Hot Spot

U3B3 ADT7481ARMZ-1 TEMP MON
VDD D1+ D1- THM# GND
SCLK SDATA ALRT#/THM2# D2+ D2-
7481_D1P 7481_D1N

SMB_THRM_CLK 5,42,44
SMB_THRM_DATA 5,42,44

7481_D2P R3B19 0 7481_D2P_Q
7481_D2N R3B21 0 7481_D2N_Q
C3N7 1000pF 10%
Q3B1 2N3904
Spare sensor, For Amb. temp sensor

7481_THRM2# R3N24 0 NO_STUFF
PM_THRM# 5,23,42,44
7481_THRM# R3N23 0 NO_STUFF

Place ADT7481 near Air inlet not under SODIMM

7 MCH_CFG_12
7 MCH_CFG_13

XOR / ALLZ / Clock Un-gating		
MCH_CFG_12	MCH_CFG_13	Configuration
0	0	Clock Gating Disabled
0	1	XOR Mode Enabled
1	0	All-Z Mode Enabled
1	1	Normal Operation (Default)

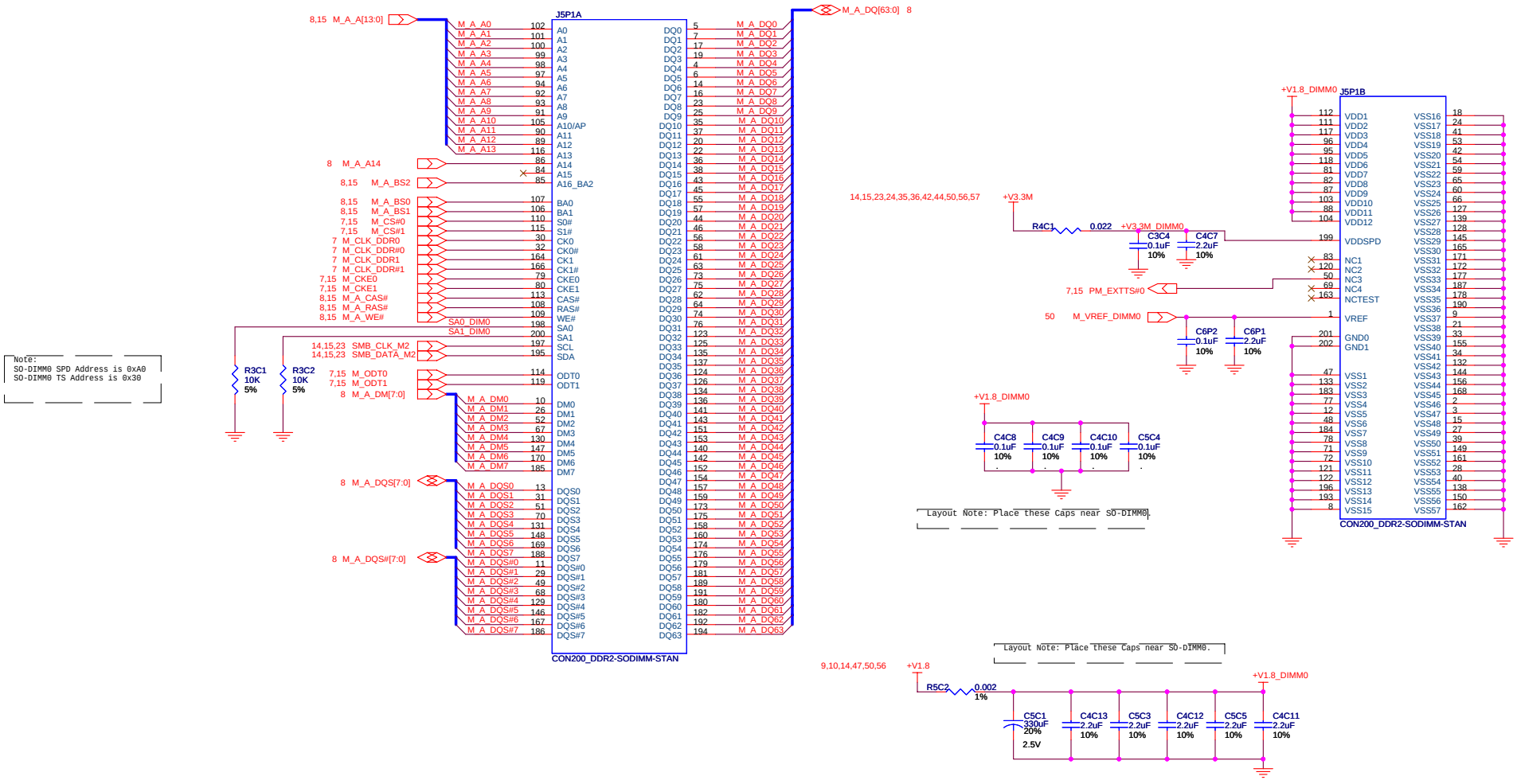
R1E11 4.02K 1% NO_STUFF
R1E10 4.02K 1% NO_STUFF

Matanzas Intel Confidential

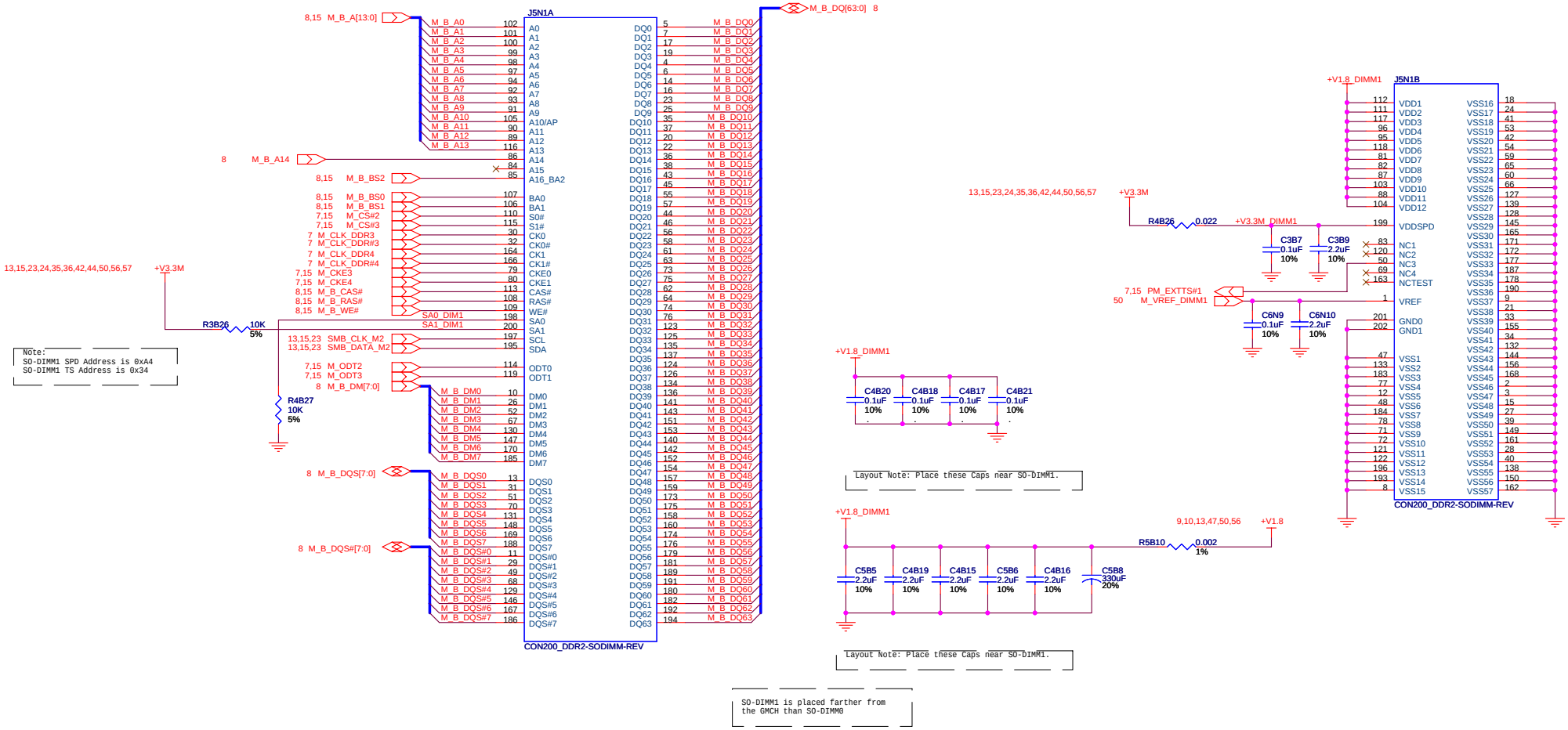
Title: Mobile Intel® 965 Express Chipset Family STRAPPING

Size	Document Number	Rev
A	NDA	1.5

Date: Tuesday, November 21, 2006 Sheet 12 of 58



Matanzas		Intel Confidential
Title: DDR2 SODIMM 0		
Size: A	Document Number: NDA	Rev: 1.5
Date: Tuesday, December 05, 2006	Sheet 13 of 58	



Matanzas		Intel Confidential
Title: DDR2 SODIMM 1		
Size: A	Document Number: NDA	Rev: 1.5
Date: Tuesday, December 05, 2006	Sheet 14 of 58	

On Board DDR2 Thermal Sensor

Layout Note:
Place Q5N2
under DIMM0

DDR_THERM1
DDR_THERM2
Q5N2
2N3904
+V3.3M
13,14,23,24,35,36,42,44,50,56,57
U5P1
VDD
D+
D-
THERM#
SCLK
SDATA
ALERT#
GND
ADM1032AR
SMB_CLK_M2 13,14,23
SMB_DATA_M2 13,14,23
PM_EXTTS#0_D
R5P2
0
PM_EXTTS#0 7,13
7,14 PM_EXTTS#1
R5P3
0
PM_EXTTS#1_D

Layout Note:
Place U5P1
under DIMM1

Layout note: Place one cap close to every 2 pullup resistors terminated to +V0.9

+V0.9
14,47,56

C4C3 0.1uF 10%
C4C15 0.1uF 10%
C4C1 0.1uF 10%
C4C5 0.1uF 10%
C4B24 0.1uF 10%
C4B14 0.1uF 10%
C4B9 0.1uF 10%
C4B25 0.1uF 10%
C4B26 0.1uF 10%
C4B10 0.1uF 10%
C4C6 0.1uF 10%
C4C4 0.1uF 10%
C4B8 0.1uF 10%
C5C6 0.1uF 10%
C5B7 0.1uF 10%
C4B23 0.1uF 10%
C4B12 0.1uF 10%
C4B22 0.1uF 10%
C4C17 0.1uF 10%
C4C14 0.1uF 10%
C4C16 0.1uF 10%
C5B4 0.1uF 10%
C4C2 0.1uF 10%
C5C2 0.1uF 10%
C4B11 0.1uF 10%
C4B13 0.1uF 10%

+V0.9
14,47,56

R5C1	56		M_CKE0 7,13
R5C3	56		M_CKE1 7,13
R5B8	56		M_CKE3 7,14
R5B11	56		M_CKE4 7,14
R4C24	56		M_ODT0 7,13
R4C13	56		M_ODT1 7,13
R4B37	56		M_ODT2 7,14
R4B25	56		M_ODT3 7,14
R4C14	56		M_A_BS0 8,13
R4C21	56		M_A_BS1 8,13
R4C2	56		M_A_BS2 8,13
R4C10	56		M_A_WE# 8,13
R4C11	56		M_A_CAS# 8,13
R4C22	56		M_A_RAS# 8,13
R4B21	56		M_B_BS0 8,14
R4B34	56		M_B_BS1 8,14
R5B9	56		M_B_BS2 8,14
R4B22	56		M_B_WE# 8,14
R4B23	56		M_B_CAS# 8,14
R4B35	56		M_B_RAS# 8,14
R4C23	56		M_CS#0 7,13
R4C12	56		M_CS#1 7,13
R4B36	56		M_CS#2 7,14
R4B24	56		M_CS#3 7,14
R4C20	56	M_A_A0	M_A_A[13:0] 8,13
R4C8	56	M_A_A1	
R4C19	56	M_A_A2	
R4C7	56	M_A_A3	
R4C18	56	M_A_A4	
R4C6	56	M_A_A5	
R4C16	56	M_A_A6	
R4C17	56	M_A_A7	
R4C5	56	M_A_A8	
R4C4	56	M_A_A9	
R4C9	56	M_A_A10	
R5C4	56	M_A_A11	
R4C3	56	M_A_A12	
R4C25	56	M_A_A13	
R4B33	56	M_B_A0	M_B_A[13:0] 8,14
R4B18	56	M_B_A1	
R4B32	56	M_B_A2	
R4B19	56	M_B_A3	
R4B31	56	M_B_A4	
R4B17	56	M_B_A5	
R4B28	56	M_B_A6	
R4B30	56	M_B_A7	
R4B16	56	M_B_A8	
R4B15	56	M_B_A9	
R4B20	56	M_B_A10	
R5B12	56	M_B_A11	
R4B14	56	M_B_A12	
R4B38	56	M_B_A13	

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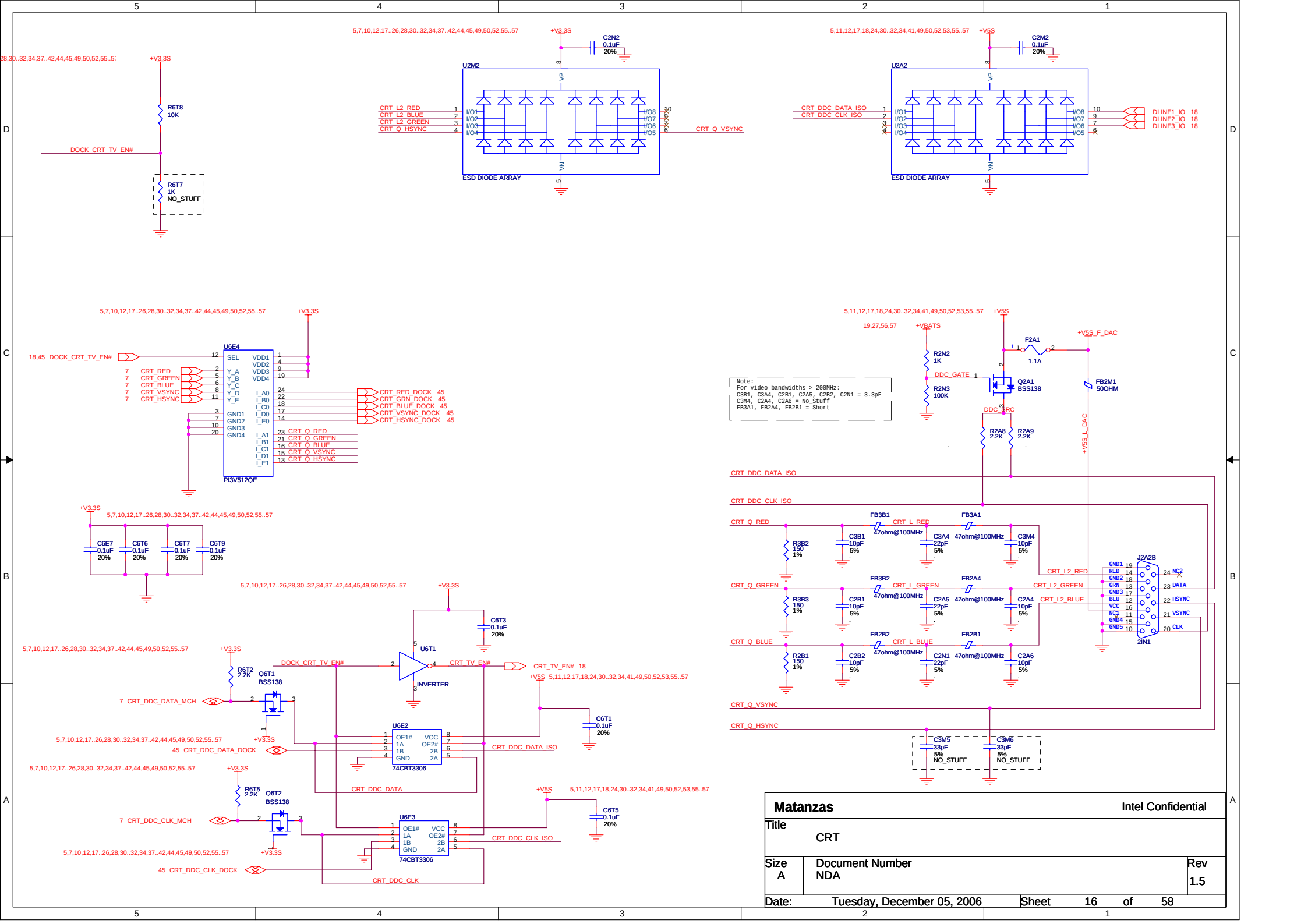
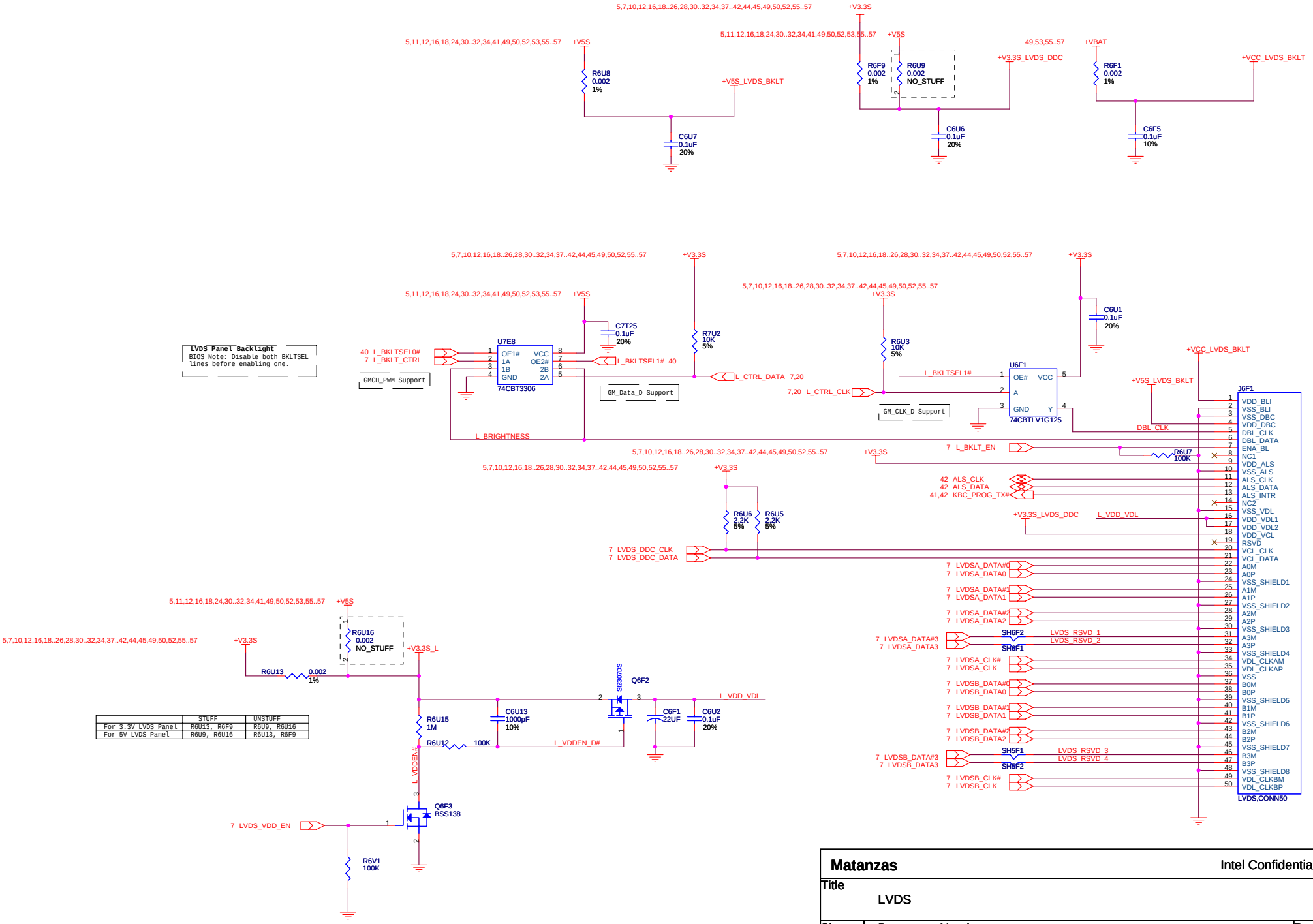
Title: DDR2 TERMINATION AND THERMAL SENSOR

Size	Document Number	Rev
A	NDA	1.5

Date: Tuesday, December 05, 2006 Sheet 15 of 58



Matanzas		Intel Confidential
Title	CRT	
Size A	Document Number NDA	Rev 1.5
Date: Tuesday, December 05, 2006	Sheet 16 of 58	



Matanzas	Intel Confidential
Title: LVDS	
Size: A	Document Number: NDA — Rev: 1.5
Date: Tuesday, December 05, 2006	Sheet 17 of 58

Port Value					Voltage		
IO2	IO1	IO0	Format	Aspect Ratio	Line1	Line2	Line3
0	0	0b	525i (480)	4:3	0V	0V	0V
0	0	1b	525i (480)	16:9	0V	0V	5V
0	0	Xb	525i (480)	4:3 Letterbox	0V	0V	2.2V
0	1	0b	525p (480)	4:3	0V	5V	0V
0	1	1b	525p (480)	16:9	0V	5V	5V
0	1	Xb	525p (480)	4:3 Letterbox	0V	5V	2.2V
X	1	0b	750p (720)	4:3	2.2V	5V	0V
X	1	1b	750p (720)	16:9	2.2V	5V	5V
1	0	0b	1125i (1080)	4:3	5V	0V	0V
1	0	1b	1125i (1080)	16:9	5V	0V	5V
1	1	0b	1125p (1080)	4:3	5V	5V	0V
1	1	1b	1125p (1080)	16:9	5V	5V	5V

Layout Note:
Place 150 Ohm termination resistors, ferrite beads and capicators close to connector

Note:
ESD Diode Array for the TV DAC A, DAC B, DAC C signals located on CRT page.

Note:
Pins 12 & 14 are shorted inside D-Connector plug.

TV-OUT DAC Channel Definition

	Composite Video	S-Video	Component Video
Channel A (DACA)	CVBS Signal	X	Chrominance (Pb)
Channel B(DACB)	X	Luminance (Y)	Luminance (Y)
Channel C (DACC)	X	Chrominance (C)	Chrominance (Pr)

Matanzas		Intel Confidential
Title: TV		
Size: A	Document Number: NDA	Rev: 1.5
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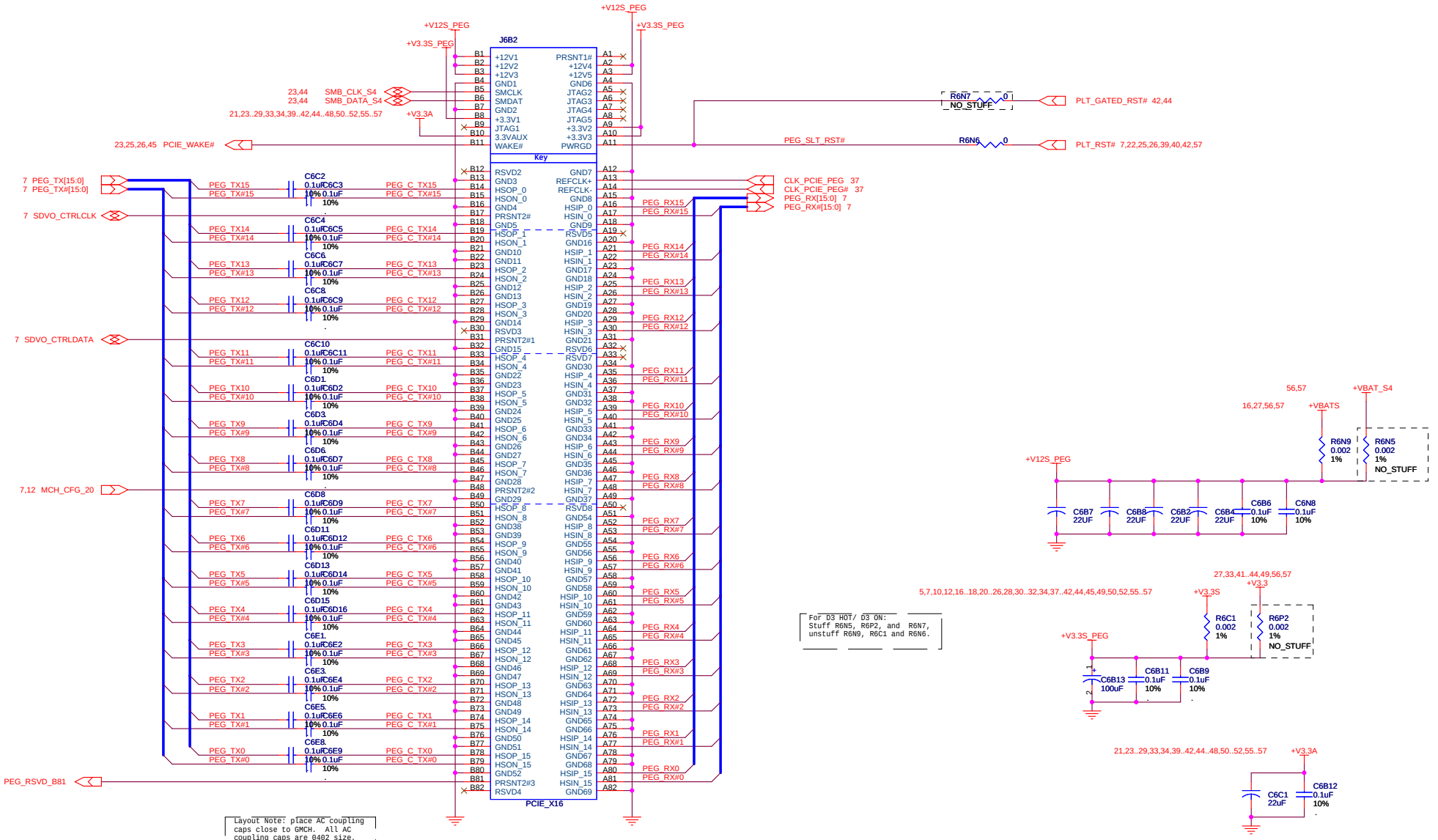
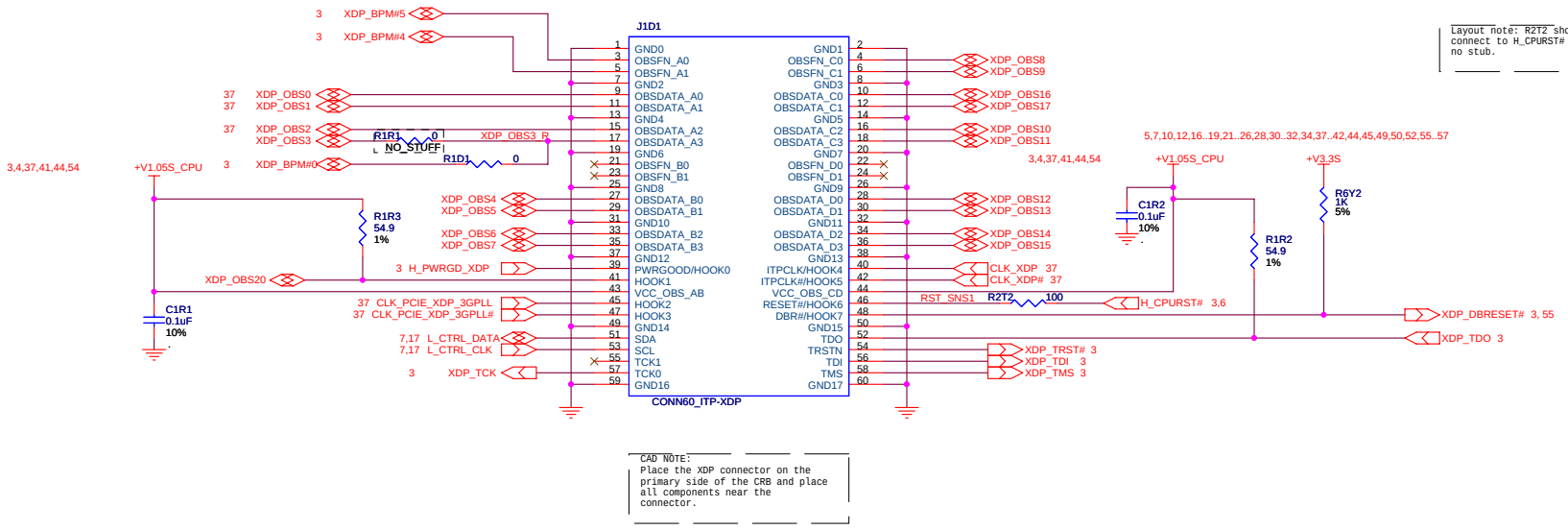
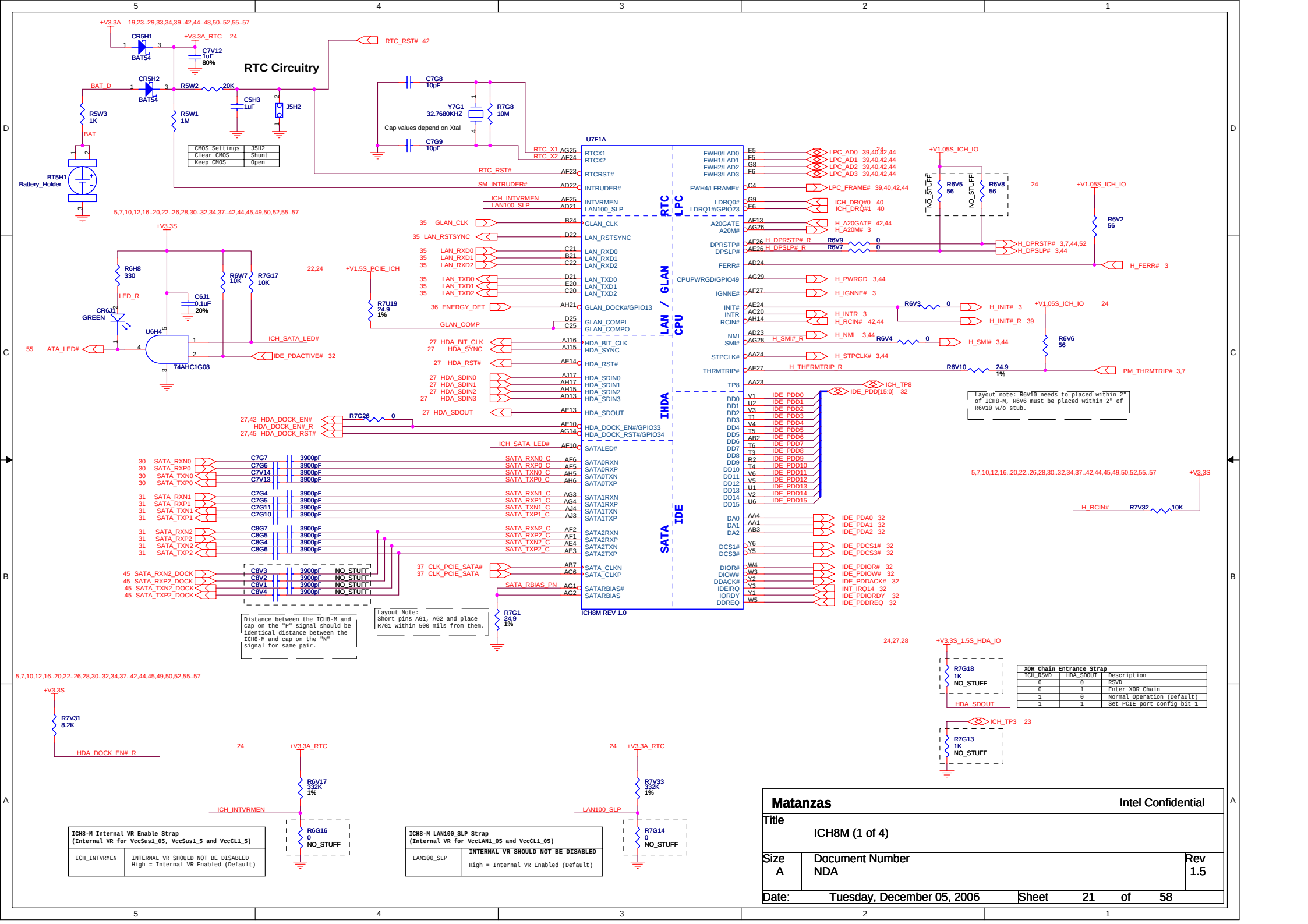


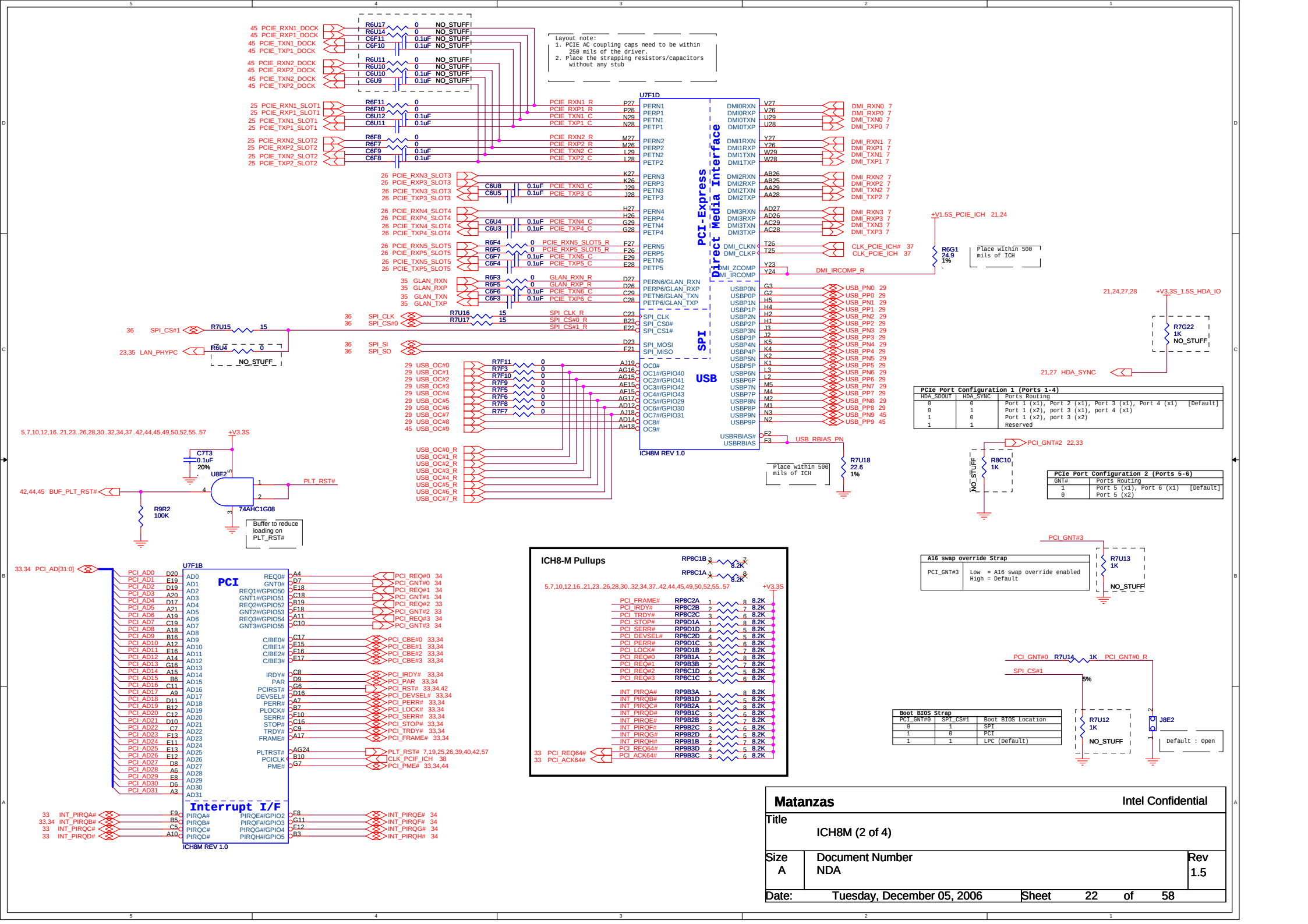
Matanzas		Intel Confidential
Title: PCIE GRAPHICS		
Size: A	Document Number: NDA	Rev: 1.5
Date: Tuesday, December 05, 2006	Sheet 19 of 58	

XDP



Matanzas		Intel Confidential
Title: XDP		
Size: A	Document Number: NDA	Rev: 1.5
Date: Tuesday, December 05, 2006	Sheet 20 of 58	


RTC Circuitry
U7F1A
ICH8M REV 1.0
RTC
LPC
LAN / GLAN
CPU
IHDA
SATA
IDE
Cap values depend on Xtal
Distance between the ICH8-M and cap on the "P" signal should be identical distance between the ICH8-M and cap on the "N" signal for same pair.
Layout Note: Short pins AG1, AG2 and place R7G1 within 500 mils from them.
Layout note: R6V10 needs to placed within 2" of ICH8-M, R6V6 must be placed within 2" of R6V10 w/o stub.
ICH8-M Internal VR Enable Strap (Internal VR for VccSus1_05, VccSus1_5 and VccCL1_5)
ICH8-M LAN100_SLP Strap (Internal VR for VccLAN1_05 and VccCL1_05)
XOR Chain Entrance Strap
Matanzas
Intel Confidential
Title
ICH8M (1 of 4)
Size A
Document Number NDA
Rev 1.5
Date: Tuesday, December 05, 2006
Sheet 21 of 58


Layout note:
1. PCIE AC coupling caps need to be within 250 mils of the driver.
2. Place the strapping resistors/capacitors without any stub
U7F1D
PCI-Express
Direct Media Interface
SPI
USB
ICH8M REV 1.0
Place within 500 mils of ICH
PCIe Port Configuration 1 (Ports 1-4)
HDA_SDOUT | HDA_SYNC | Ports Routing
0 | 0 | Port 1 (x1), Port 2 (x1), Port 3 (x1), Port 4 (x1) [Default]
0 | 1 | Port 1 (x2), port 3 (x1), port 4 (x1)
1 | 0 | Port 1 (x2), port 3 (x2)
1 | 1 | Reserved
PCIe Port Configuration 2 (Ports 5-6)
GNT# | Ports Routing
1 | Port 5 (x1), Port 6 (x1) [Default]
0 | Port 5 (x2)
Buffer to reduce loading on PLT_RST#
ICH8-M Pullups
A16 swap override Strap
PCI_GNT#3 | Low = A16 swap override enabled
High = Default
Boot BIOS Strap
PCI_GNT#0 | SPI_CS#1 | Boot BIOS Location
0 | 1 | SPI
1 | 0 | PCI
1 | 1 | LPC (Default)
Default : Open
PCI
Interrupt I/F
ICH8M REV 1.0
Matanzas
Intel Confidential
Title
ICH8M (2 of 4)
Size
A
Document Number
NDA
Rev
1.5
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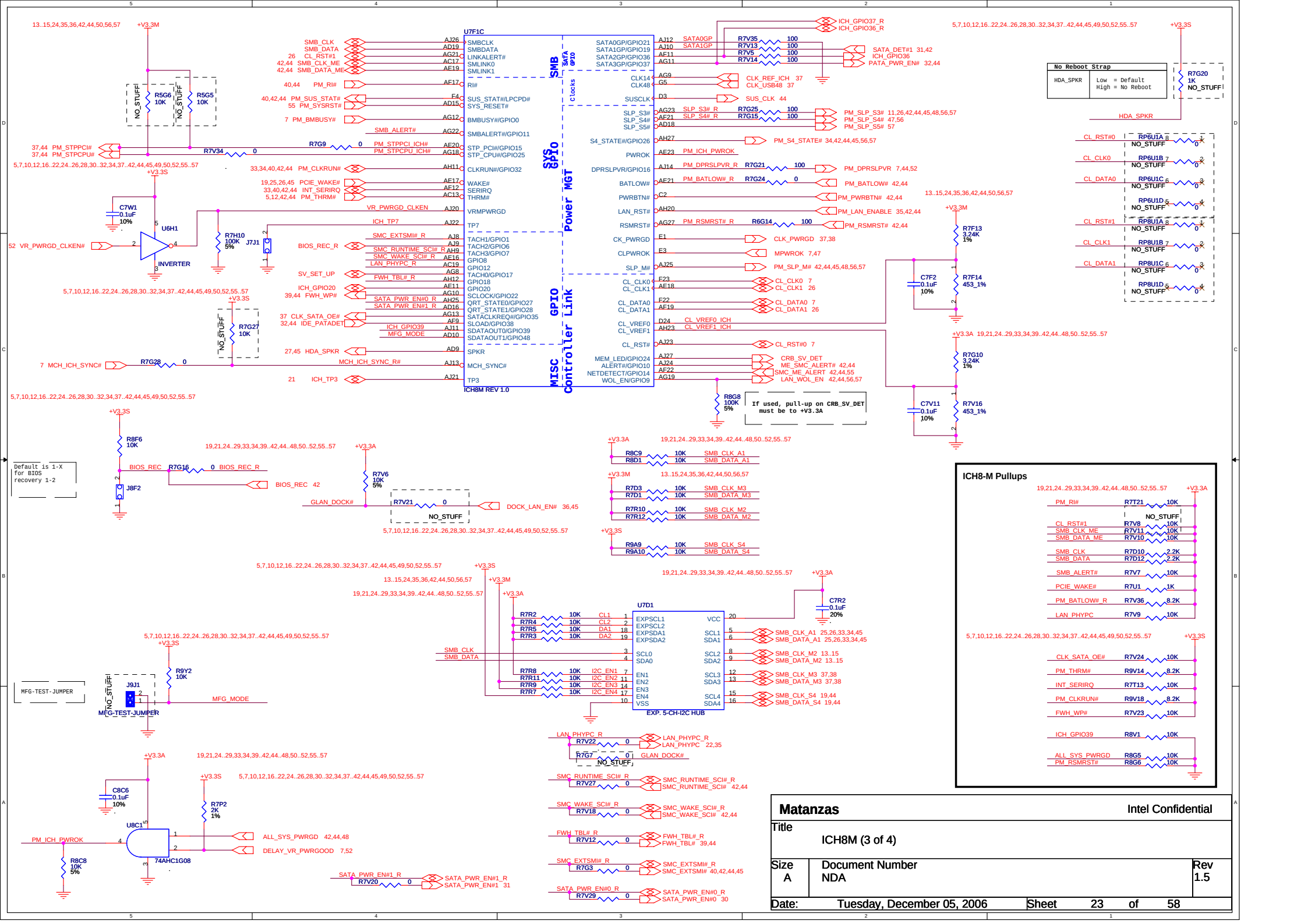
U7F1C
SMB
SATA GPIO
Clocks
SYS GPIO
Power MGT
GPIO
Controller Link
MISC
ICH8M REV 1.0
SMBCLK
SMBDATA
LINKALERT#
SMLINK0
SMLINK1
RI#
SUS_STAT#/LPCPD#
SYS_RESET#
BMBUSY#/GPIO0
SMBALERT#/GPIO11
STP_PCI#/GPIO15
STP_CPU#/GPIO25
CLKRUN#/GPIO32
WAKE#
SERIRQ
THRM#
VRMPWRGD
TP7
TACH1/GPIO1
TACH2/GPIO6
TACH3/GPIO7
GPIO8
GPIO12
TACH0/GPIO17
GPIO18
GPIO20
SCLOCK/GPIO22
QRT_STATE0/GPIO27
QRT_STATE1/GPIO28
SATACLKREQ#/GPIO35
SLOAD/GPIO38
SDATAOUT0/GPIO39
SDATAOUT1/GPIO48
SPKR
MCH_SYNC#
TP3
SATA0GP/GPIO21
SATA1GP/GPIO19
SATA2GP/GPIO36
SATA3GP/GPIO37
CLK14
CLK48
SUSCLK
SLP_S3#
SLP_S4#
SLP_S5#
S4_STATE#/GPIO26
PWROK
DPRSLPVR/GPIO16
BATLOW#
PWRBTN#
LAN_RST#
RSMRST#
CK_PWRGD
CLPWROK
SLP_M#
CL_CLK0
CL_CLK1
CL_DATA0
CL_DATA1
CL_VREF0
CL_VREF1
CL_RST#
MEM_LED/GPIO24
ALERT#/GPIO10
NETDETECT/GPIO14
WOL_EN/GPIO9
SMB_CLK
SMB_DATA
SMB_ALERT#
PM_RI#
PM_STPPCI#
PM_STPCPU#
PM_CLKRUN#
PCIE_WAKE#
INT_SERIRQ
PM_THRM#
VR_PWRGD_CLKEN
ICH_TP7
SMC_EXTSMI#_R
SMC_RUNTIME_SCI#_R
SMC_WAKE_SCI#_R
LAN_PHYPC_R
SV_SET_UP
FWH_TBL#_R
ICH_GPIO20
FWH_WP#
SATA_PWR_EN#0_R
SATA_PWR_EN#1_R
CLK_SATA_OE#
IDE_PATADET
ICH_GPIO39
MFG_MODE
HDA_SPKR
MCH_ICH_SYNC_R#
ICH_TP3
ICH_GPIO37_R
ICH_GPIO36_R
SATA_DET#1 31,42
ICH_GPIO36
PATA_PWR_EN# 32,44
CLK_REF_ICH 37
CLK_USB48 37
SUS_CLK 44
PM_SLP_S3# 11,26,42,44,45,48,56,57
PM_SLP_S4# 47,56
PM_SLP_S5# 57
PM_S4_STATE# 34,42,44,45,56,57
PM_DPRSLPVR 7,44,52
PM_BATLOW# 42,44
PM_PWRBTN# 42,44
PM_LAN_ENABLE 35,42,44
PM_RSMRST# 42,44
CLK_PWRGD 37,38
MPWROK 7,47
PM_SLP_M# 42,44,45,48,56,57
CL_CLK0 7
CL_CLK1 26
CL_DATA0 7
CL_DATA1 26
CL_VREF0_ICH
CL_VREF1_ICH
CL_RST#0 7
CRB_SV_DET
ME_SMC_ALERT# 42,44
SMC_ME_ALERT 42,44,55
LAN_WOL_EN 42,44,56,57
If used, pull-up on CRB_SV_DET must be to +V3.3A
No Reboot Strap
HDA_SPKR
Low = Default
High = No Reboot
R7G20 1K NO_STUFF
ICH8-M Pullups
U6H1
INVERTER
U8C1
74AHC1G08
U7D1
EXP. 5-CH-I2C HUB
EXPSCL1
EXPSCL2
EXPSDA1
EXPSDA2
SCL0
SDA0
EN1
EN2
EN3
EN4
VSS
VCC
SCL1
SDA1
SCL2
SDA2
SCL3
SDA3
SCL4
SDA4
Default is 1-X for BIOS recovery 1-2
MFG-TEST-JUMPER
Matanzas
Intel Confidential
Title
ICH8M (3 of 4)
Size A
Document Number NDA
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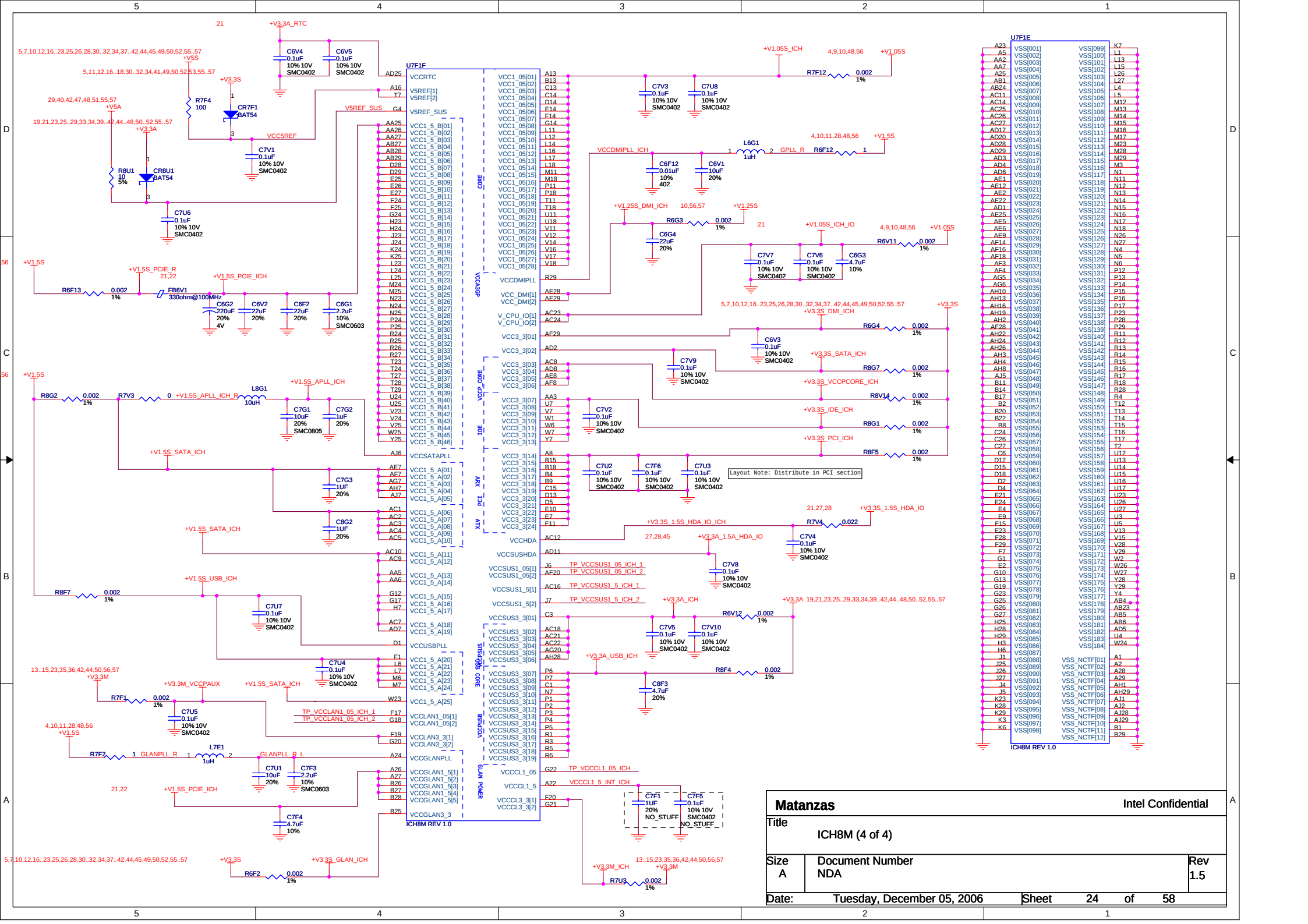
U7F1F
ICH8M REV 1.0
U7F1E
ICH8M REV 1.0
Layout Note: Distribute in PCI section
Matanzas
Intel Confidential
Title
ICH8M (4 of 4)
Size
A
Document Number
NDA
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1.5
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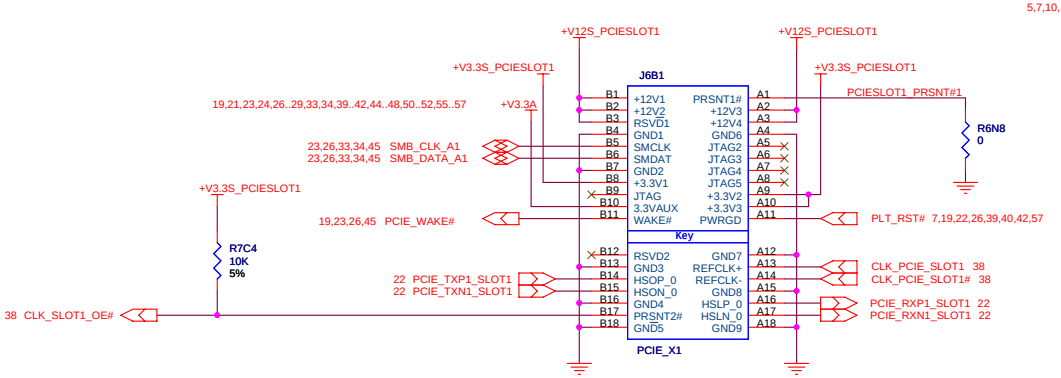
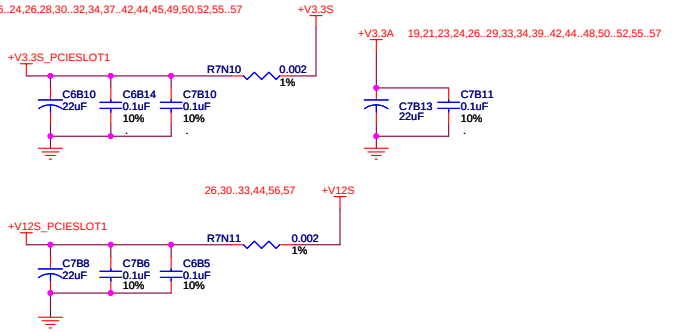
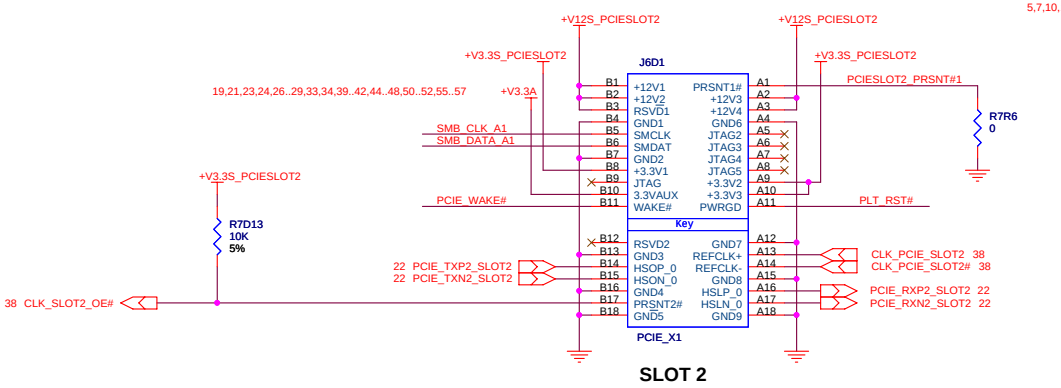


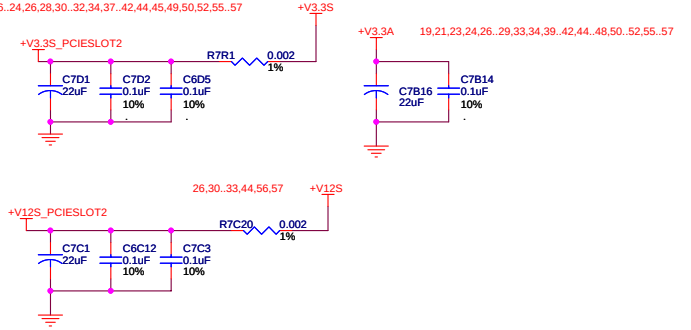
SLOT 1

NOTE: SLOTS 1 AND 2
ARE PHYSICALY IN-LINE

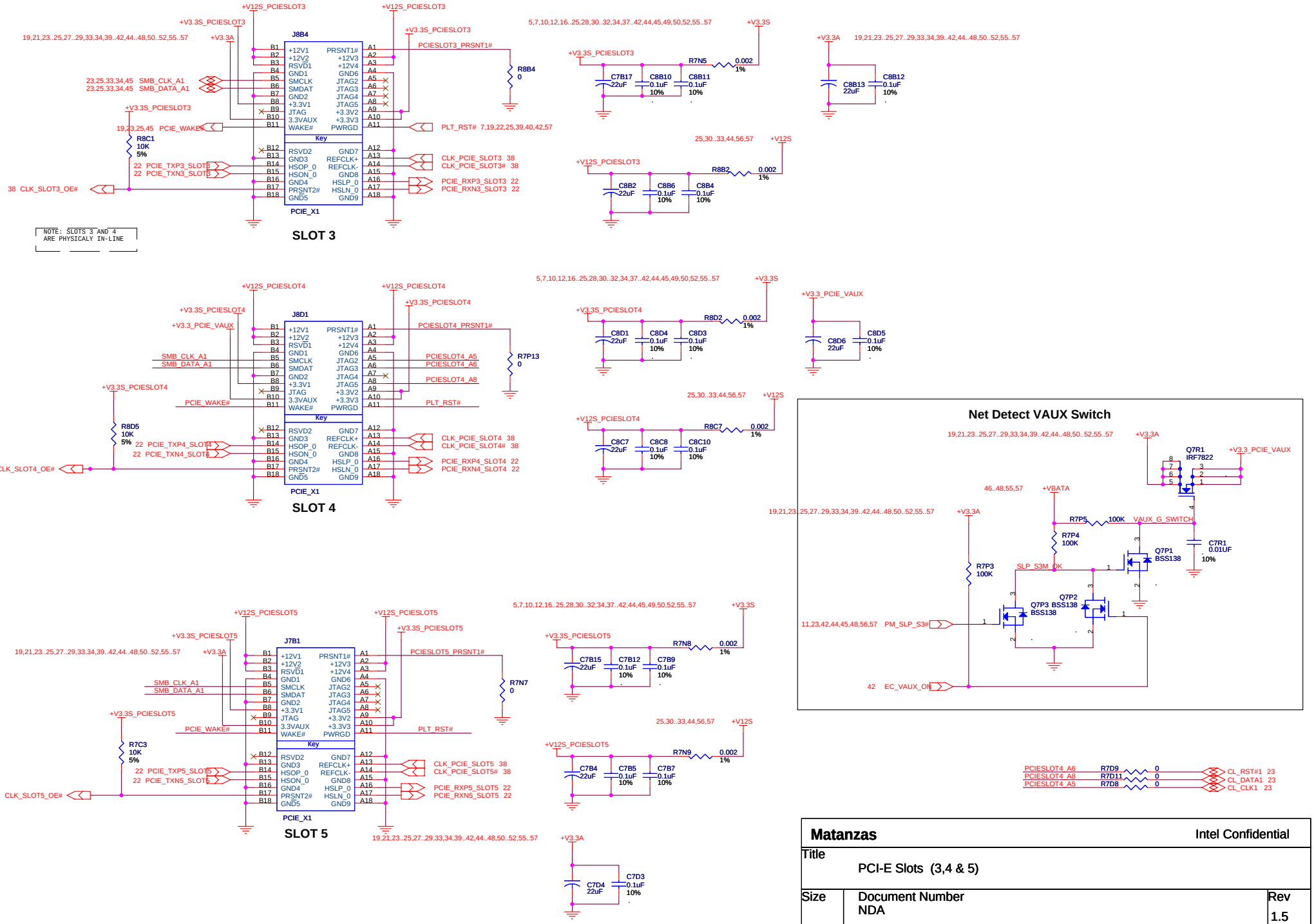




SLOT 2



Matanzas		Intel Confidential
Title	PCI-E Slots (1 & 2)	
Size	Document Number NDA	Rev 1.5
Date: Tuesday, November 21, 2006	Sheet 25 of 58	


SLOT 3
SLOT 4
SLOT 5
J8B4
J8D1
J7B1
PCIE_X1
NOTE: SLOTS 3 AND 4 ARE PHYSICALY IN-LINE
Net Detect VAUX Switch
Matanzas
Intel Confidential
Title
PCI-E Slots (3,4 & 5)
Size
Document Number
NDA
Rev
1.5
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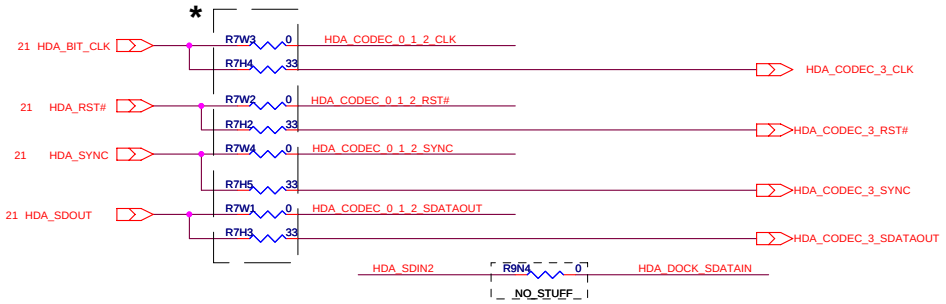
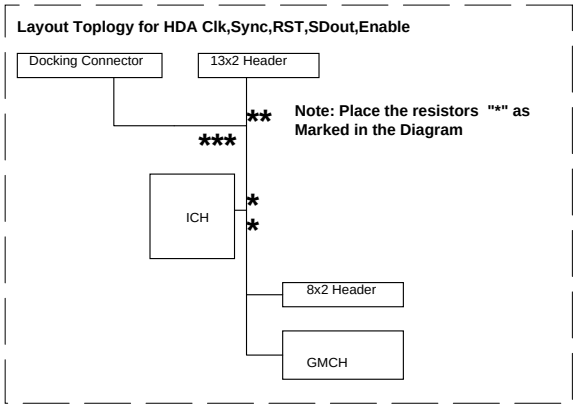
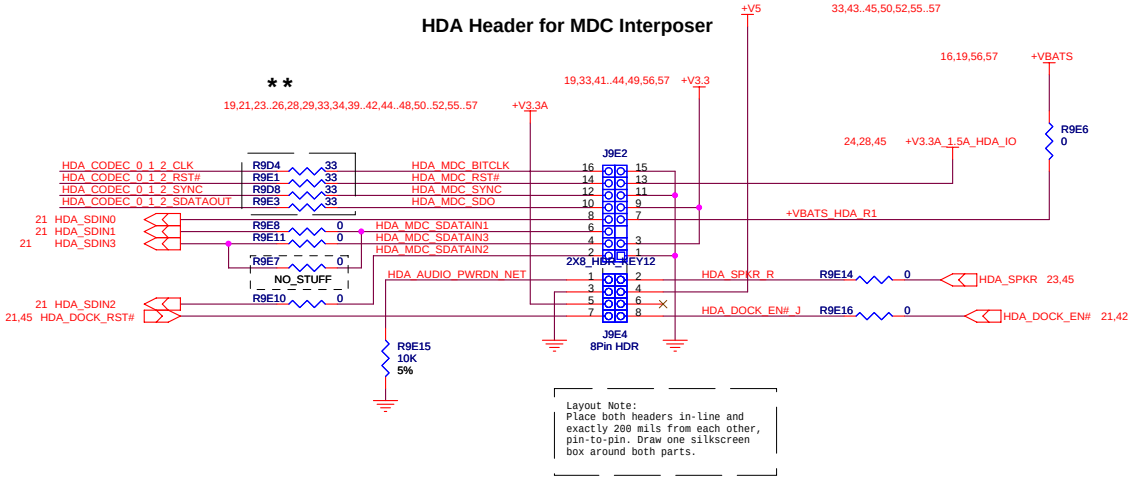


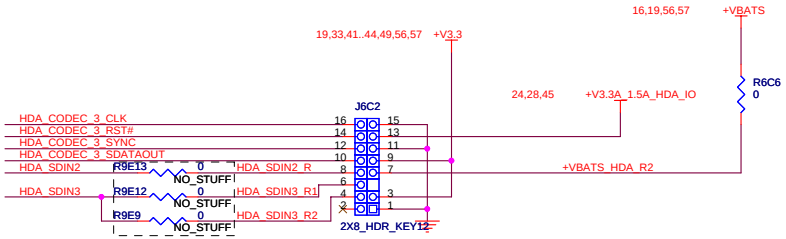


HDA Header for MDC Interposer



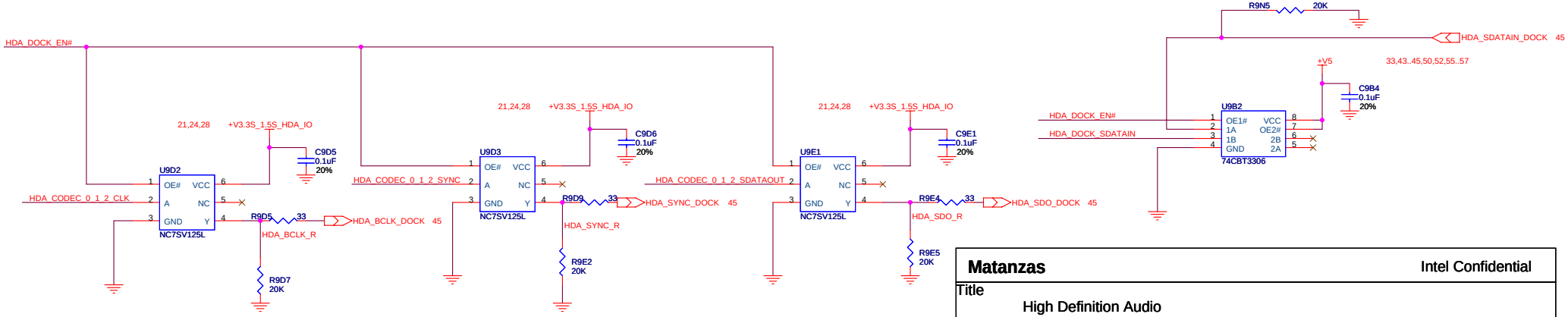
Layout Note:
Place both headers in-line and exactly 200 mils from each other, pin-to-pin. Draw one silkscreen box around both parts.

HDA Header for External HDMI Support



These Resistors need to be Mounted appropriately when SDIN2 & SDIN3 need to get tested using the MDC.

HDA Docking Circuit



Matanzas		Intel Confidential
Title: High Definition Audio		
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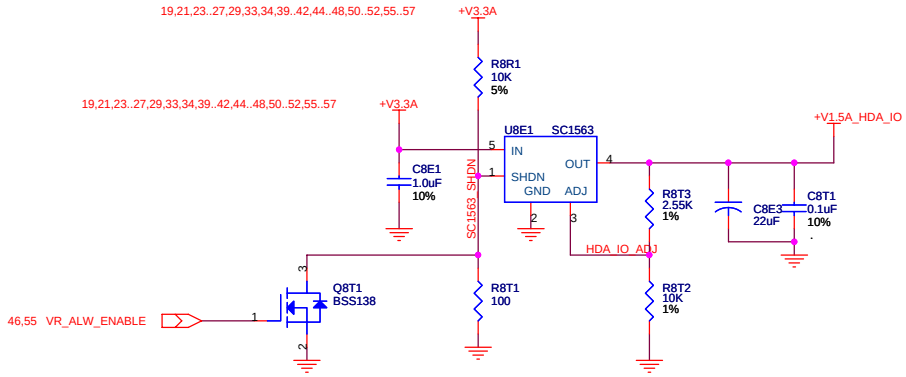
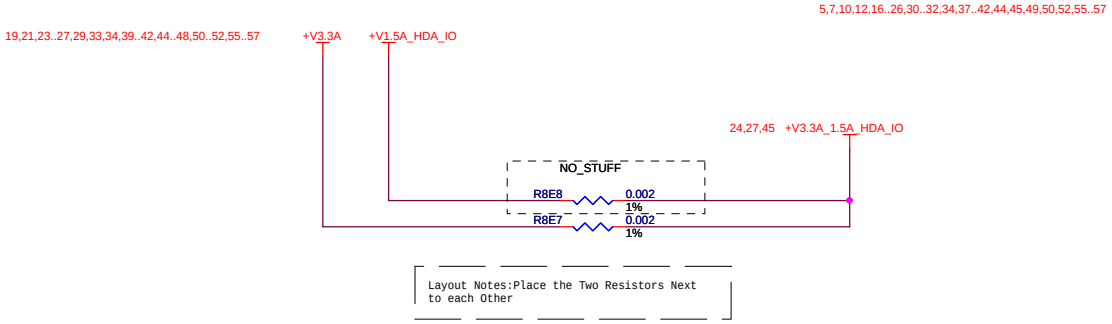
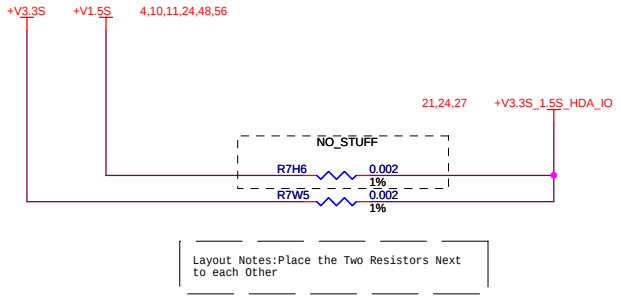
Power Supply for High Definiton Audio



Selection of I/O Voltage for the High Definition Audio





Matanzas		Intel Confidential
Title: HDA Power Supply		
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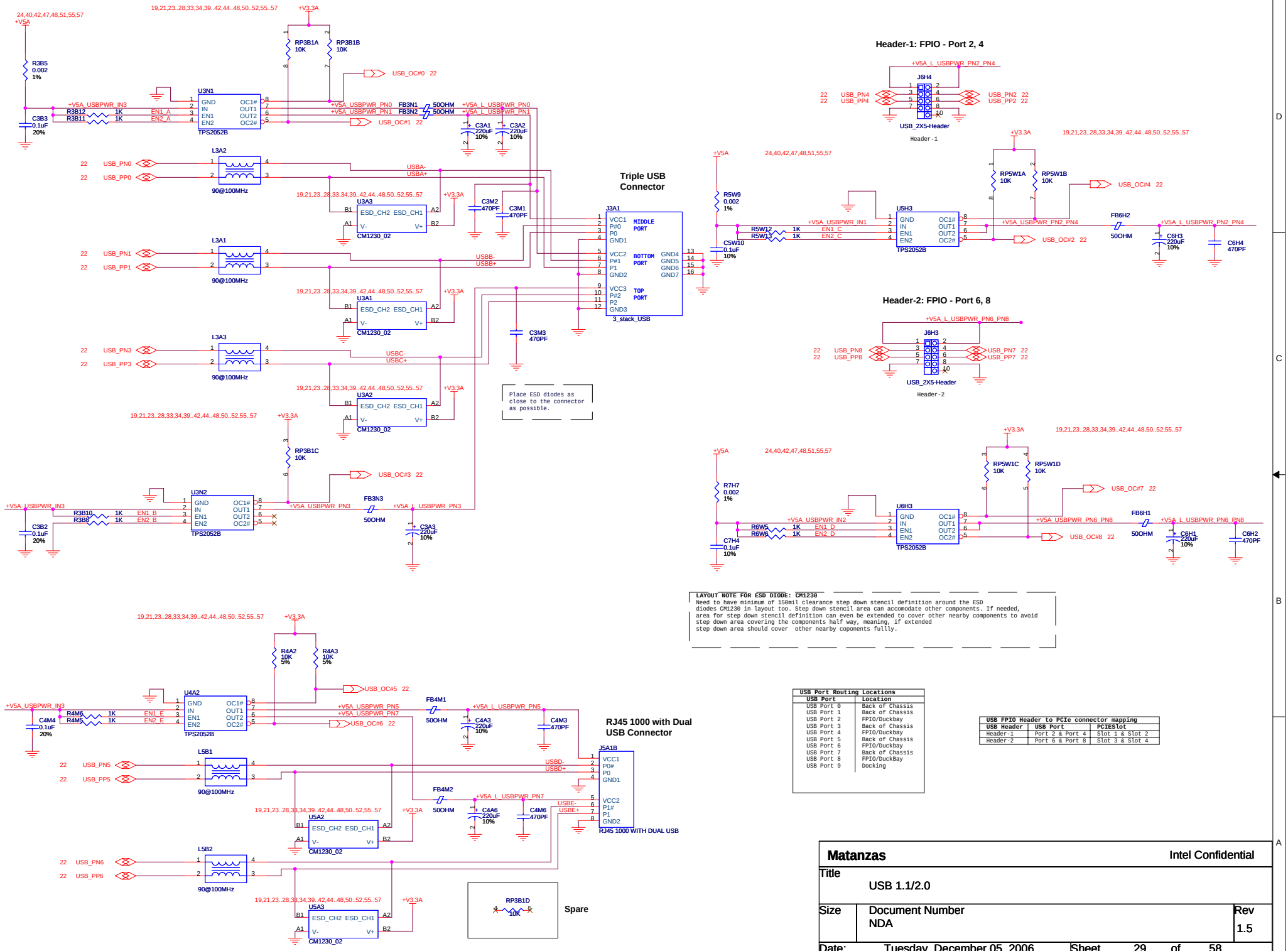
Triple USB Connector
RJ45 1000 with Dual USB Connector
Header-1: FPIO - Port 2, 4
Header-2: FPIO - Port 6, 8
Spare
Place ESD diodes as close to the connector as possible.
LAYOUT NOTE FOR ESD DIODE: CM1230
Need to have minimum of 150mil clearance step down stencil definition around the ESD diodes CM1230 in layout too. Step down stencil area can accomodate other components. If needed, area for step down stencil definition can even be extended to cover other nearby components to avoid step down area covering the components half way, meaning, if extended step down area should cover other nearby coponents fullly.
USB Port Routing Locations
USB Port | Location
USB Port 0 | Back of Chassis
USB Port 1 | Back of Chassis
USB Port 2 | FPIO/Duckbay
USB Port 3 | Back of Chassis
USB Port 4 | FPIO/Duckbay
USB Port 5 | Back of Chassis
USB Port 6 | FPIO/Duckbay
USB Port 7 | Back of Chassis
USB Port 8 | FPIO/DuckBay
USB Port 9 | Docking
USB FPIO Header to PCIe connector mapping
USB Header | USB Port | PCIESlot
Header-1 | Port 2 & Port 4 | Slot 1 & Slot 2
Header-2 | Port 6 & Port 8 | Slot 3 & Slot 4
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Intel Confidential
Title
USB 1.1/2.0
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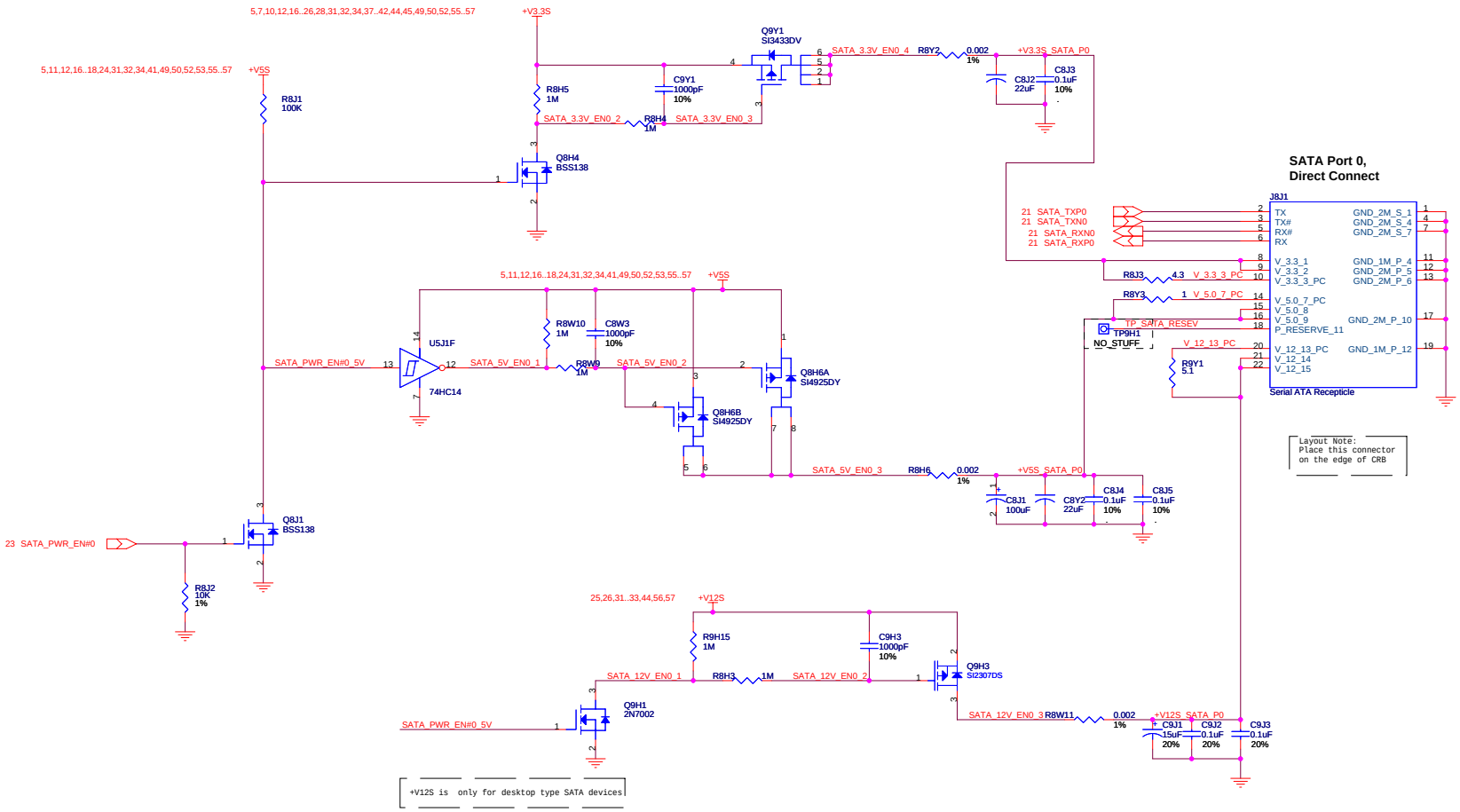
SATA Port-0,Direct Connect



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Title	SATA (1 of 3)	
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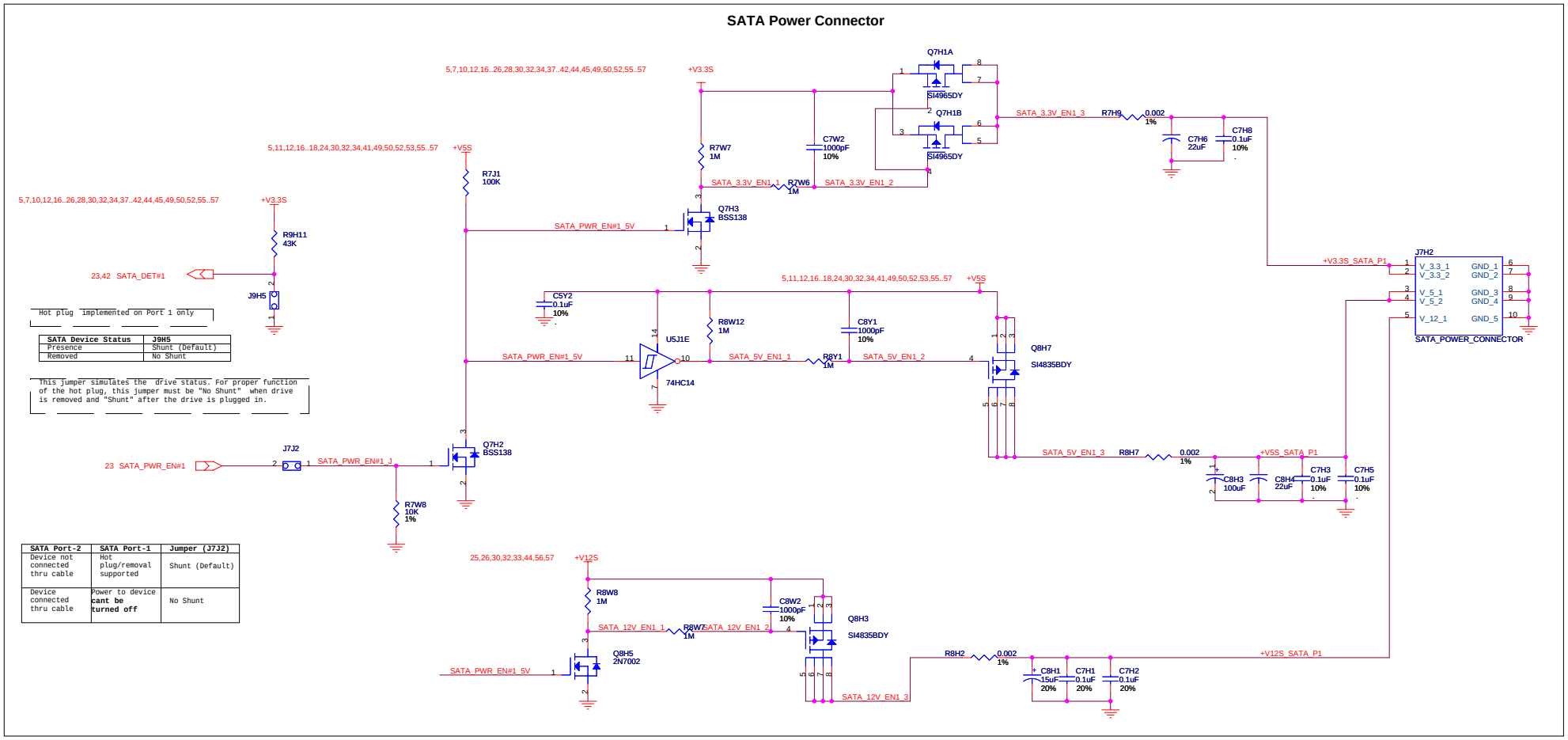
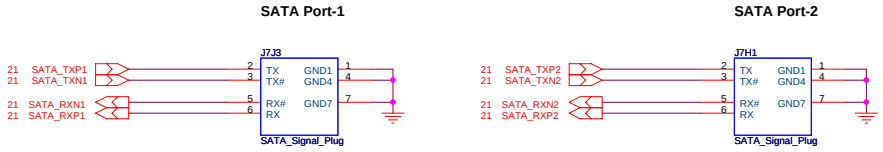
SATA Port-1 and Port-2, Cable Connect

SATA Power Connector



SATA Signal Connectors



Notes:
-- Both SATA Port-1 and SATA Port-2 share the same power connector, J7H2
-- Use Y-Cable available with Kit to feed the power from J7H2 to SATA device on port-1 and SATA device on Port-2.
-- Connect Power cable first before connecting SATA signal cable.

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Title: SATA (2 and 3 of 3)		
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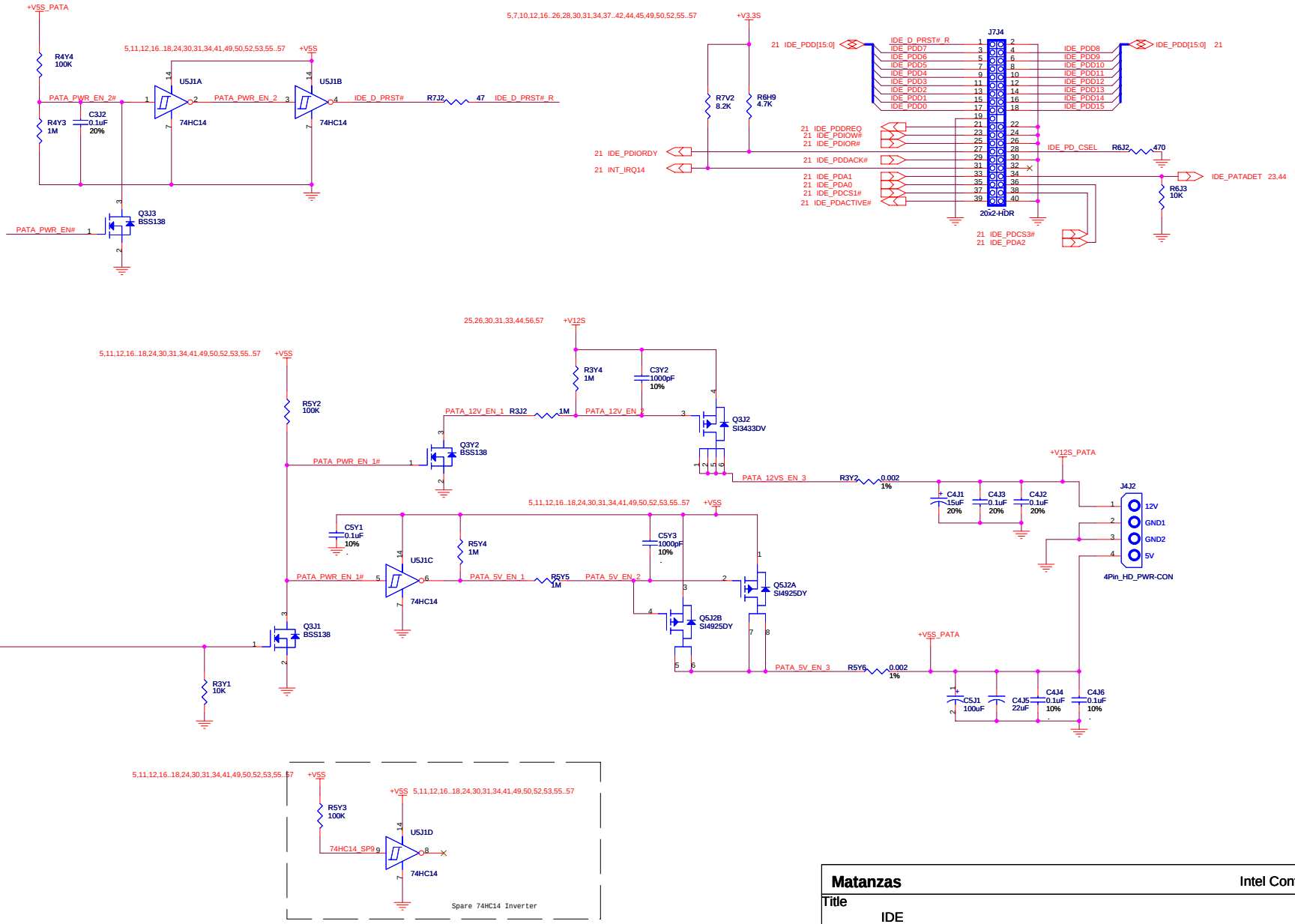

Matanzas		Intel Confidential
Title: IDE		
Size	Document Number: NDA	Rev: 1.5
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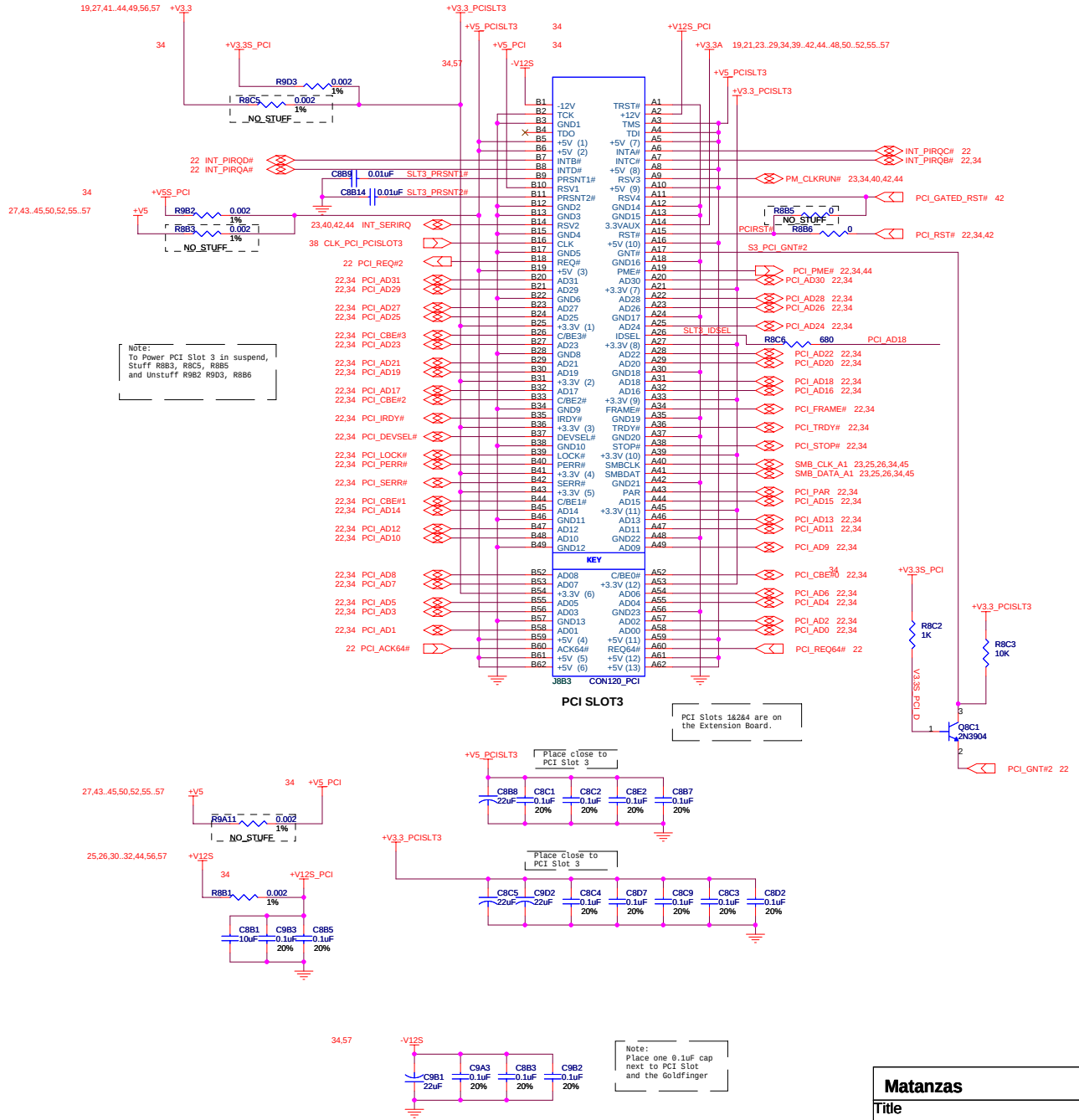
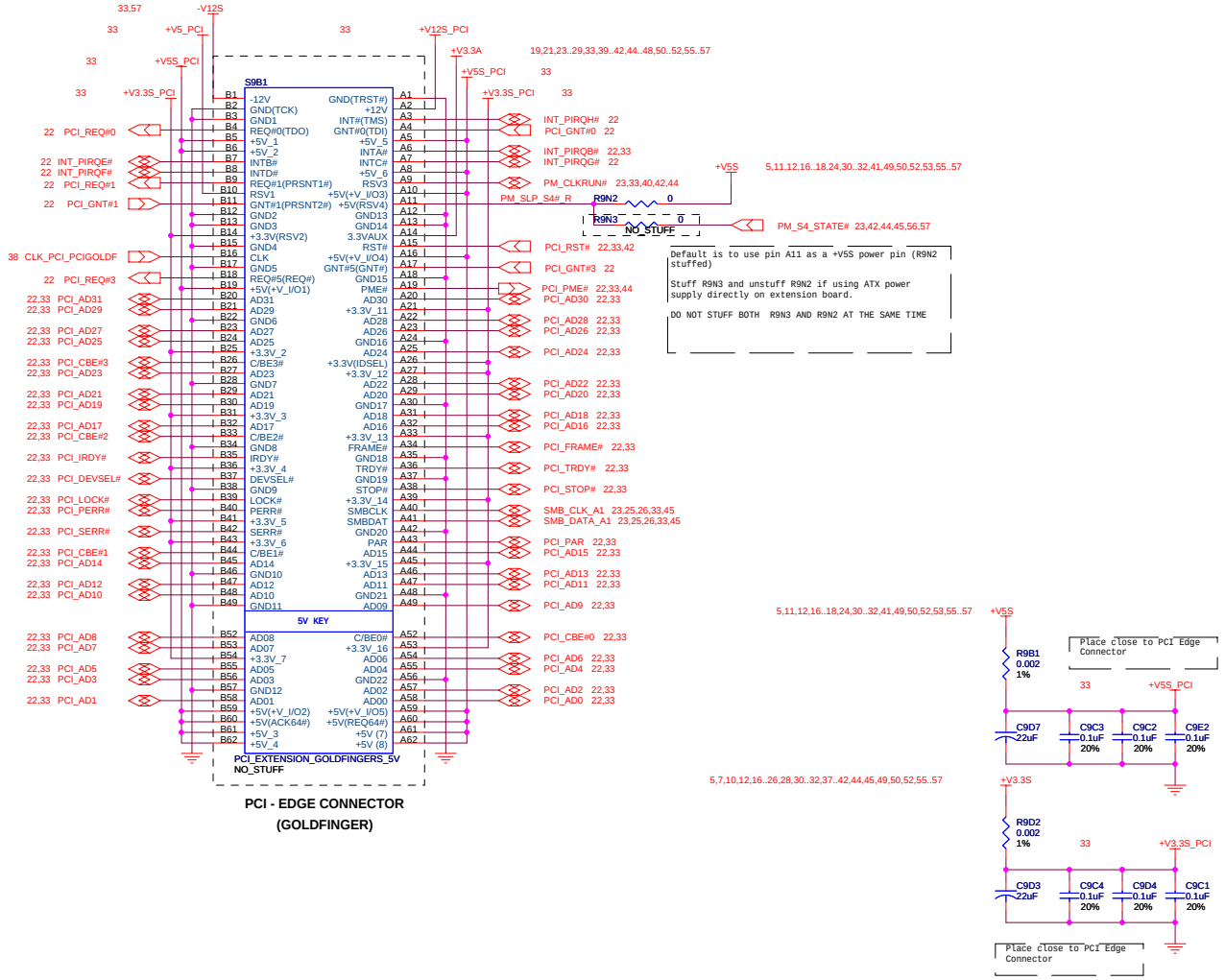


Matanzas		Intel Confidential
Title	PCI Slot 3	
Size	Document Number NDA	Rev 1.5
Date: Tuesday, November 21, 2006	Sheet 33 of 58	



Matanzas		Intel Confidential
Title: PCI Edge Connector (Goldfinger)		
Size	Document Number: NDA	Rev: 1.5
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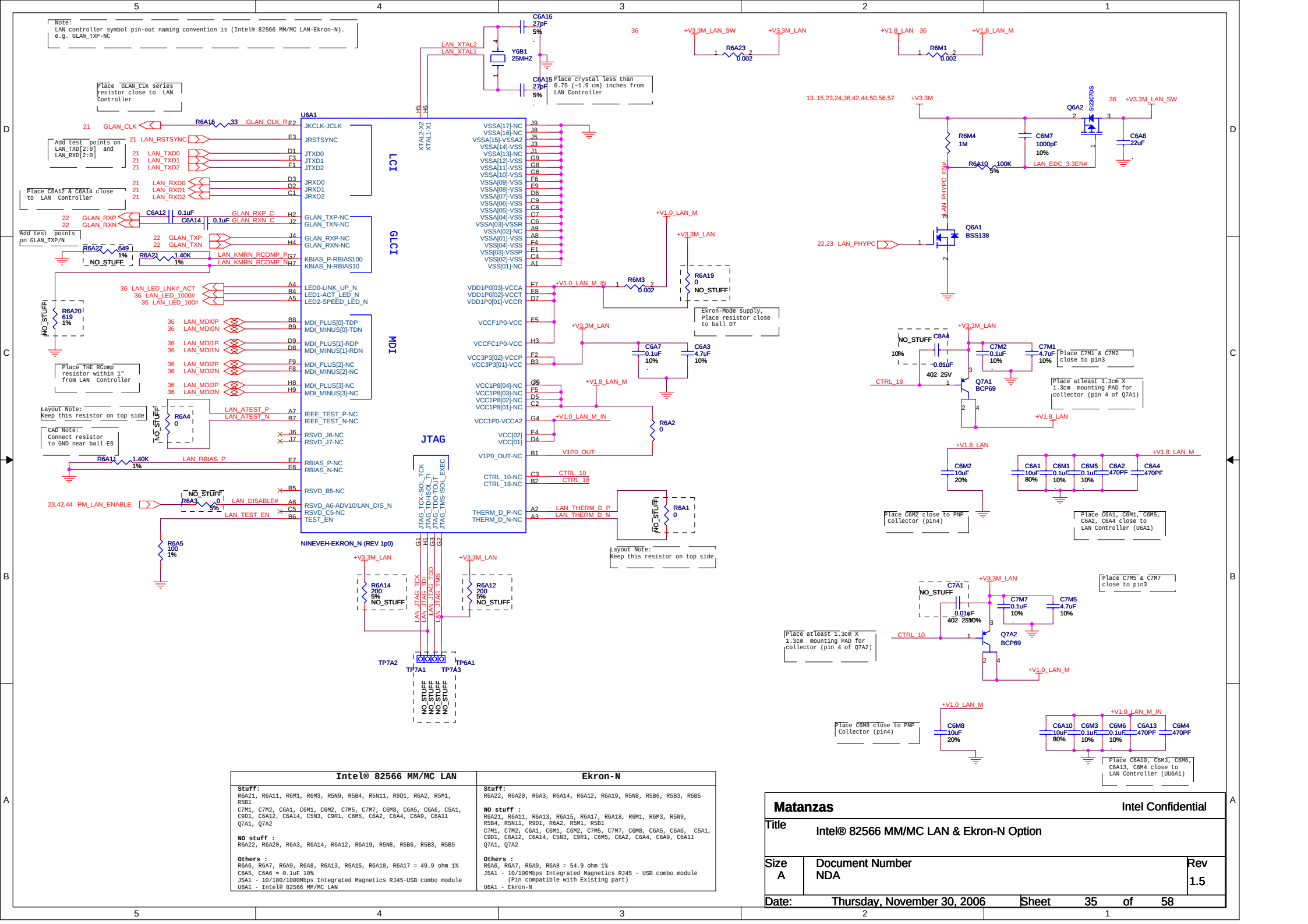

Intel® 82566 MM/MC LAN	Ekron-N
Stuff: R6A21, R6A11, R6M1, R6M3, R5N9, R5B4, R5N11, R9D1, R6A2, R5M1, R5B1 C7M1, C7M2, C6A1, C6M1, C6M2, C7M5, C7M7, C6M8, C6A5, C6A6, C5A1, C9D1, C6A12, C6A14, C5N3, C9R1, C6M5, C6A2, C6A4, C6A9, C6A11 Q7A1, Q7A2 **NO stuff :** R6A22, R6A20, R6A3, R6A14, R6A12, R6A19, R5N8, R5B6, R5B3, R5B5 **Others :** R6A6, R6A7, R6A9, R6A8, R6A13, R6A15, R6A18, R6A17 = 49.9 ohm 1% C6A5, C6A6 = 0.1uF 10% J5A1 - 10/100/1000Mbps Integrated Magnetics RJ45-USB combo module U6A1 - Intel® 82566 MM/MC LAN	**Stuff:** R6A22, R6A20, R6A3, R6A14, R6A12, R6A19, R5N8, R5B6, R5B3, R5B5 **NO stuff :** R6A21, R6A11, R6A13, R6A15, R6A17, R6A18, R6M1, R6M3, R5N9, R5B4, R5N11, R9D1, R6A2, R5M1, R5B1 C7M1, C7M2, C6A1, C6M1, C6M2, C7M5, C7M7, C6M8, C6A5, C6A6, C5A1, C9D1, C6A12, C6A14, C5N3, C9R1, C6M5, C6A2, C6A4, C6A9, C6A11 Q7A1, Q7A2 **Others :** R6A6, R6A7, R6A9, R6A8 = 54.9 ohm 1% J5A1 - 10/100Mbps Integrated Magnetics RJ45 - USB combo module (Pin compatible with Existing part) U6A1 - Ekron-N

Matanzas		Intel Confidential
Title	Intel® 82566 MM/MC LAN & Ekron-N Option	
Size A	Document Number NDA	Rev 1.5
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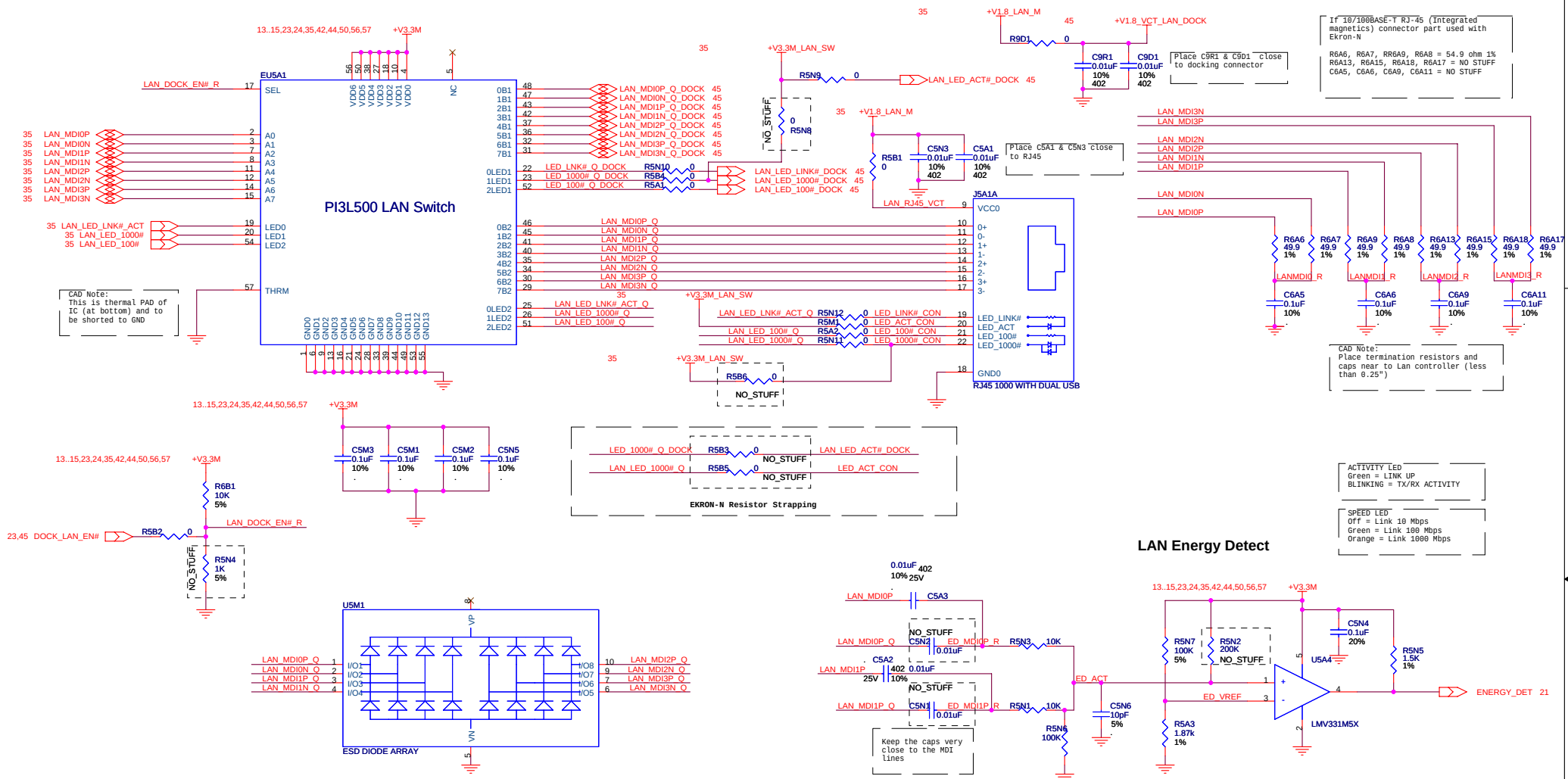

Matanzas		Intel Confidential
Title: LAN Docking and SPI		
Size: A	Document Number: NDA	Rev: 1.5
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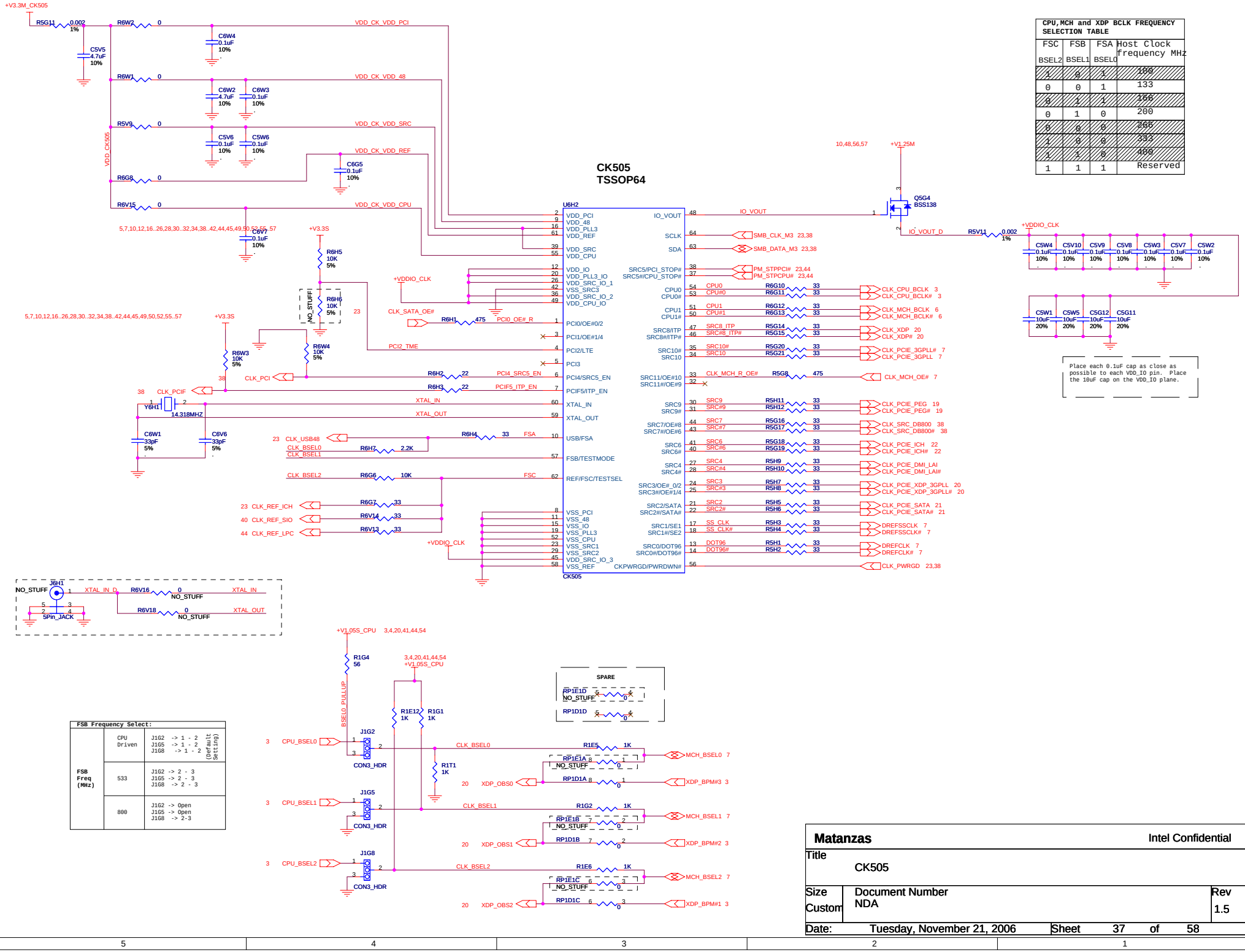
CK505
TSSOP64
U6H2
CK505
+V3.3M_CK505
VDD_CK_VDD_PCI
VDD_CK_VDD_48
VDD_CK_VDD_SRC
VDD_CK_VDD_REF
VDD_CK_VDD_CPU
VDD_CK505
+V3.3S
+VDDIO_CLK
+V1.25M
10,48,56,57
Q5G4
BSS138
IO_VOUT
IO_VOUT_D
R5V11 0.002 1%
SMB_CLK_M3 23,38
SMB_DATA_M3 23,38
PM_STPPCI# 23,44
PM_STPCPU# 23,44
CLK_CPU_BCLK 3
CLK_CPU_BCLK# 3
CLK_MCH_BCLK 6
CLK_MCH_BCLK# 6
CLK_XDP 20
CLK_XDP# 20
CLK_PCIE_3GPLL# 7
CLK_PCIE_3GPLL 7
CLK_MCH_OE# 7
CLK_PCIE_PEG 19
CLK_PCIE_PEG# 19
CLK_SRC_DB800 38
CLK_SRC_DB800# 38
CLK_PCIE_ICH 22
CLK_PCIE_ICH# 22
CLK_PCIE_DMI_LAI
CLK_PCIE_DMI_LAI#
CLK_PCIE_XDP_3GPLL 20
CLK_PCIE_XDP_3GPLL# 20
CLK_PCIE_SATA 21
CLK_PCIE_SATA# 21
DREFSSCLK 7
DREFSSCLK# 7
DREFCLK 7
DREFCLK# 7
CLK_PWRGD 23,38
Place each 0.1uF cap as close as possible to each VDD_IO pin. Place the 10uF cap on the VDD_IO plane.
CPU,MCH and XDP BCLK FREQUENCY SELECTION TABLE
FSC BSEL2 | FSB BSEL1 | FSA BSEL0 | Host Clock frequency MHz
1 0 1 100
0 0 1 133
0 1 1 166
0 1 0 200
0 0 0 266
1 0 0 333
1 1 0 400
1 1 1 Reserved
FSB Frequency Select:
FSB Freq (MHz)
CPU Driven: J1G2 -> 1 - 2, J1G5 -> 1 - 2, J1G8 -> 1 - 2 (Default Setting)
533: J1G2 -> 2 - 3, J1G5 -> 2 - 3, J1G8 -> 2 - 3
800: J1G2 -> Open, J1G5 -> Open, J1G8 -> 2-3
SPARE
Matanzas
Intel Confidential
Title
CK505
Size
Custom
Document Number
NDA
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1.5
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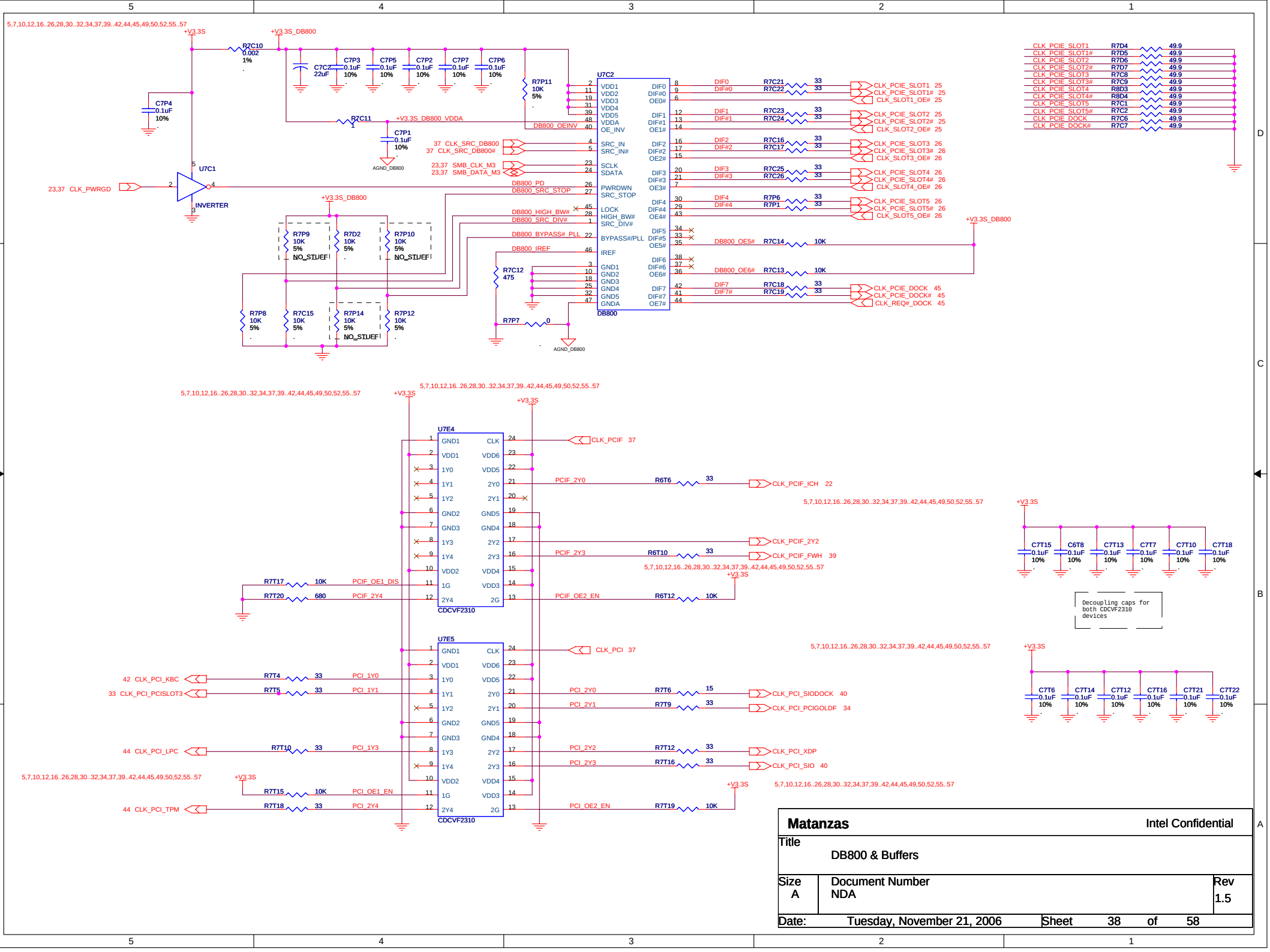

Matanzas		Intel Confidential
Title	DB800 & Buffers	
Size A	Document Number NDA	Rev 1.5
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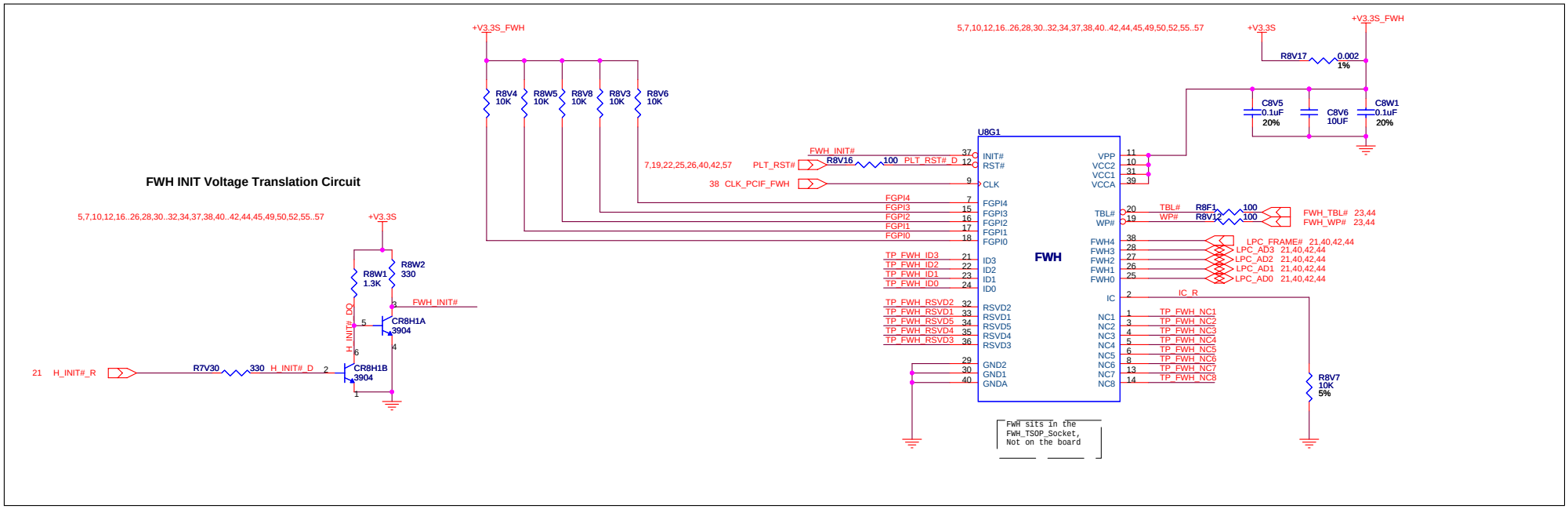
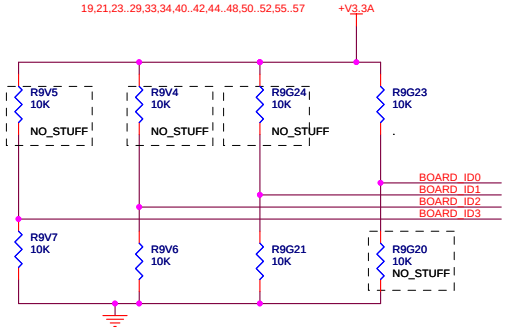
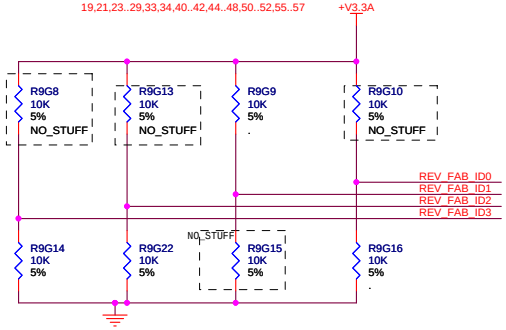
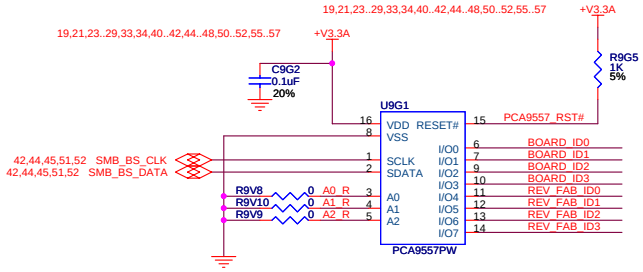


BOARD REVISION

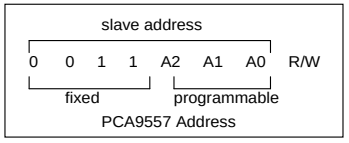


FAB REVISION





8-bit I/O Port Expander



FAB ID Strapping Table

FAB_REV				BOARD FAB
3	2	1	0	
0	0	0	0	1
0	0	0	1	2
0	0	1	0	3
0	0	1	1	4
0	1	0	0	5
0	1	0	1	6
0	1	1	0	7
0	1	1	1	8
1	0	0	0	9
1	0	0	1	10
1	0	1	0	11
1	0	1	1	12
1	1	0	0	13
1	1	0	1	14
1	1	1	0	15
1	1	1	1	16

BOARD REVISION Strapping Table

BOARD_REVISION				BOARD ID
3	2	1	0	
0	0	0	1	Matanzas

Matanzas — Intel Confidential

Title: FWH and I/O Port Expander

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A	NDA	1.5

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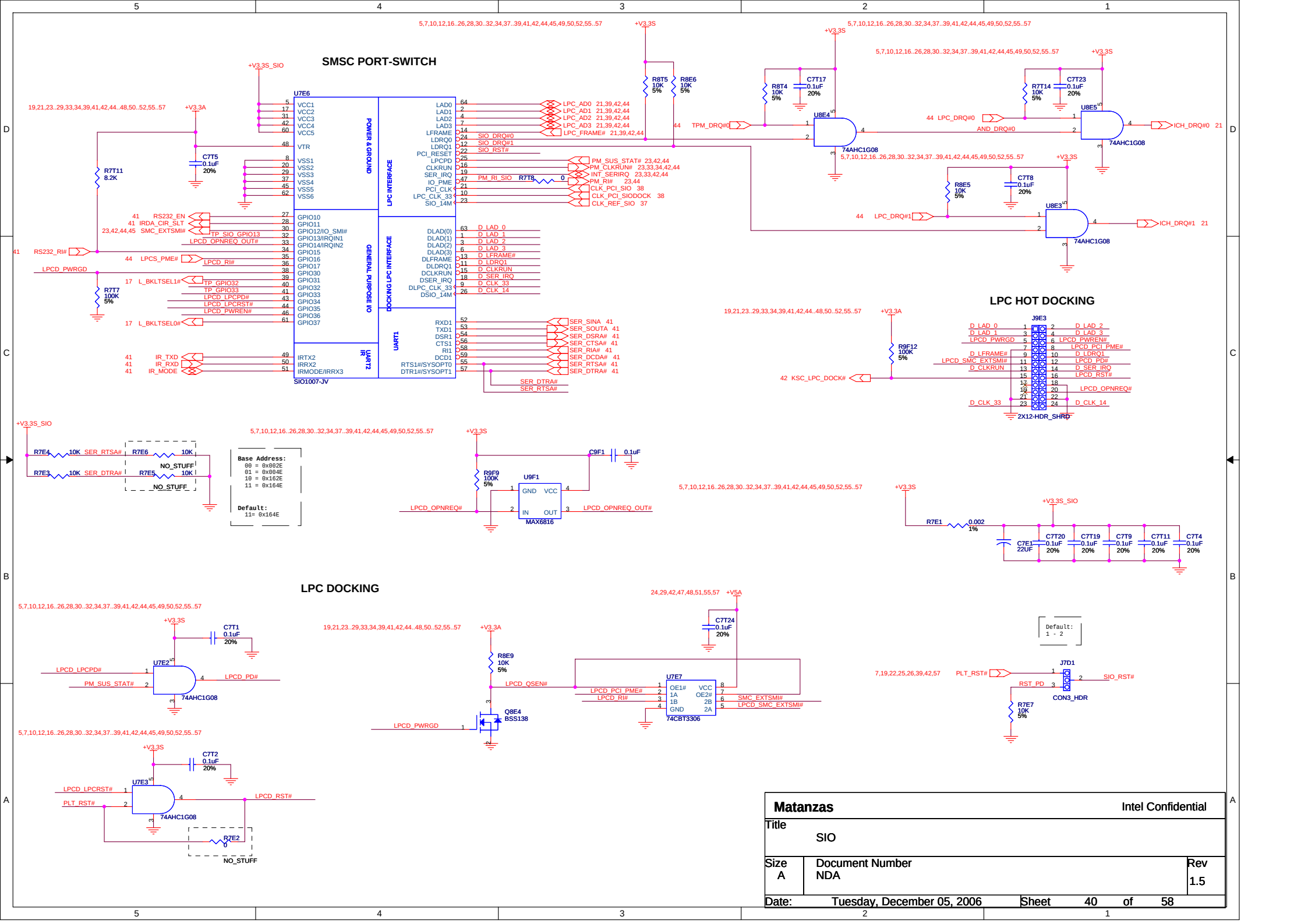
SMSC PORT-SWITCH
U7E6
SIO1007-JV
POWER & GROUND
LPC INTERFACE
GENERAL PURPOSE I/O
DOCKING LPC INTERFACE
UART1
UART2
IR
LPC HOT DOCKING
J9E3
2X12-HDR_SHRD
LPC DOCKING
U9F1
MAX6816
U7E2
U7E3
U7E7
74CBT3306
74AHC1G08
U8E4
U8E5
U8E3
Q8E4
BSS138
J7D1
CON3_HDR
Base Address:
00 = 0x002E
01 = 0x004E
10 = 0x162E
11 = 0x164E
Default:
11= 0x164E
Default:
1 - 2
NO_STUFF
Matanzas
Intel Confidential
Title
SIO
Size
A
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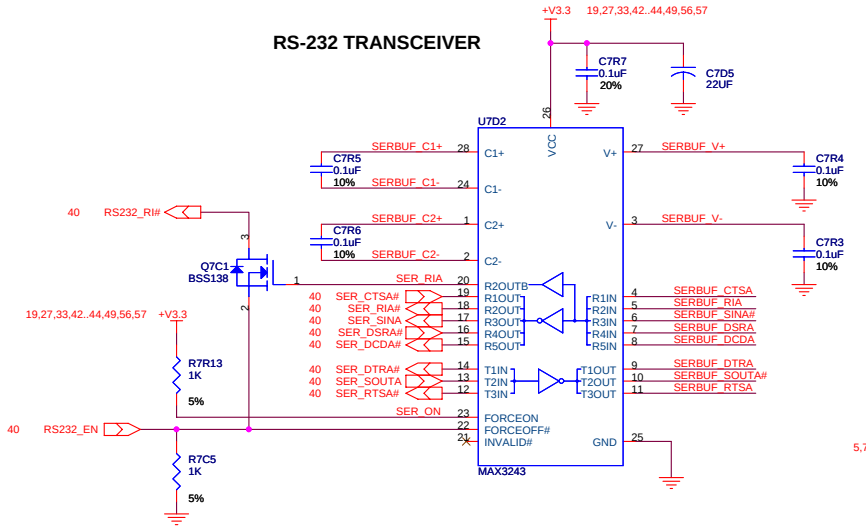
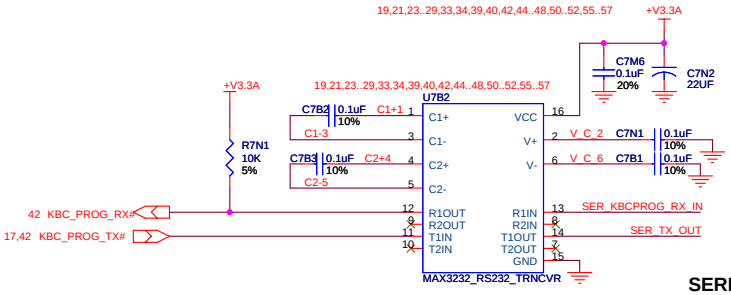
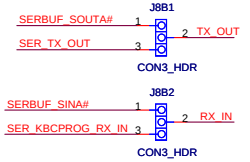
RS-232 TRANSCEIVER

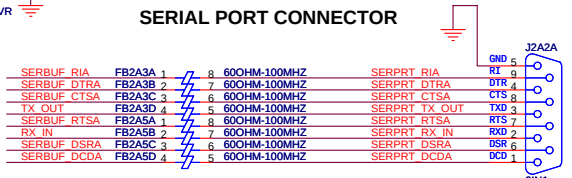




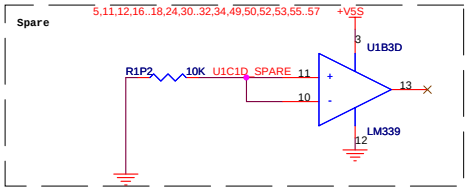
In Ckt H8 Programming	J8B1 and J8B2
Disable	1-2 (Default)
Enable	2-3 (In Ckt Programming)

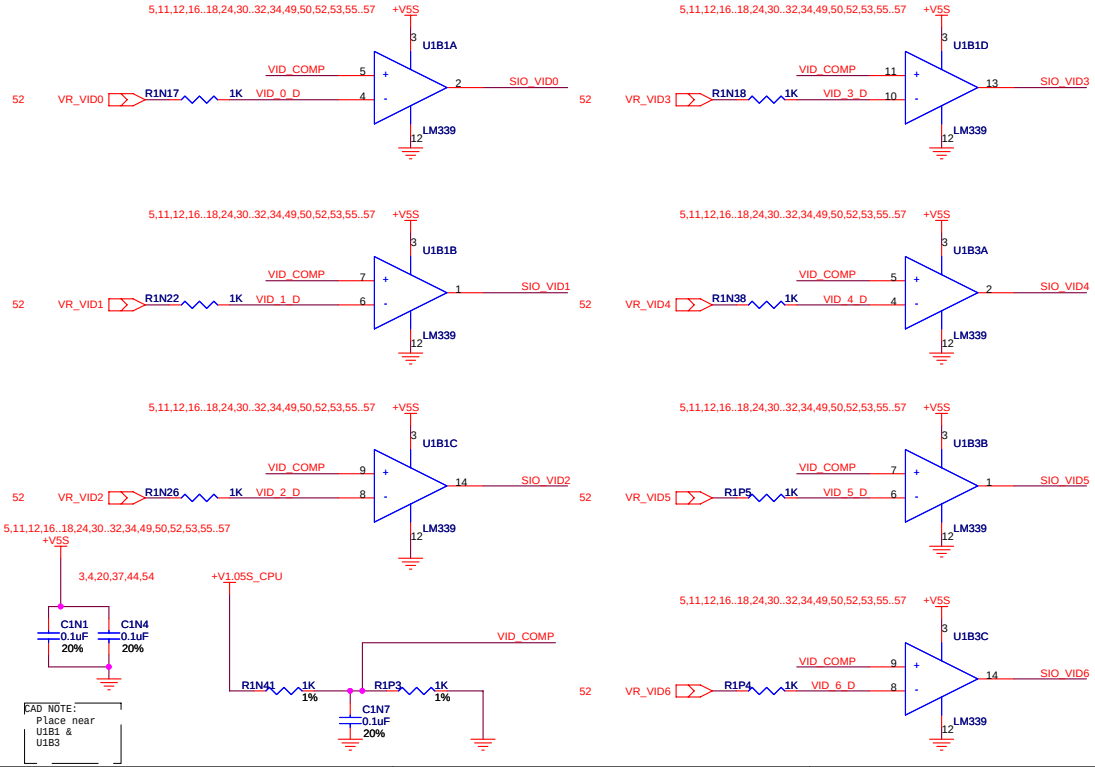


SERIAL PORT CONNECTOR

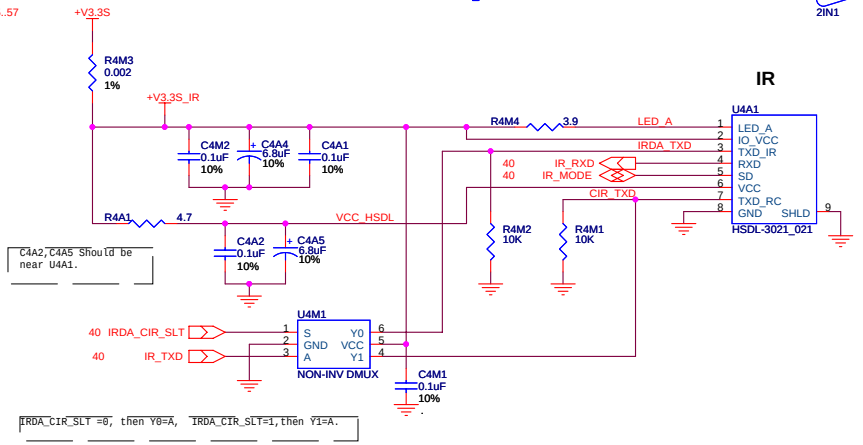


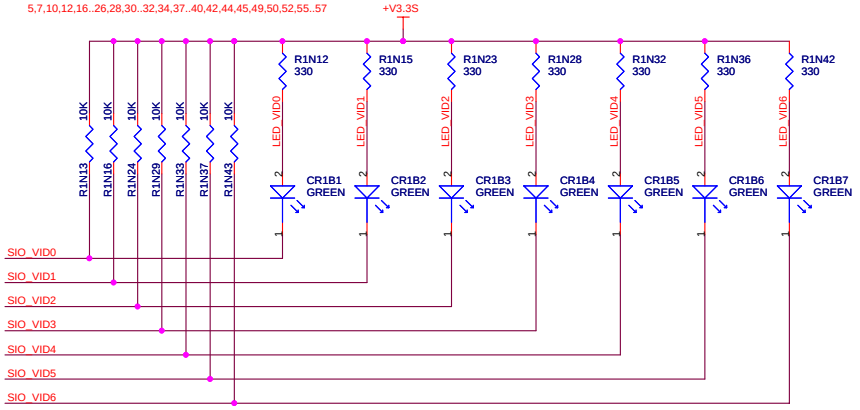
SIO VID VOLTAGE TRANSLATION





IR





Matanzas		Intel Confidential
Title: Legacy Support		
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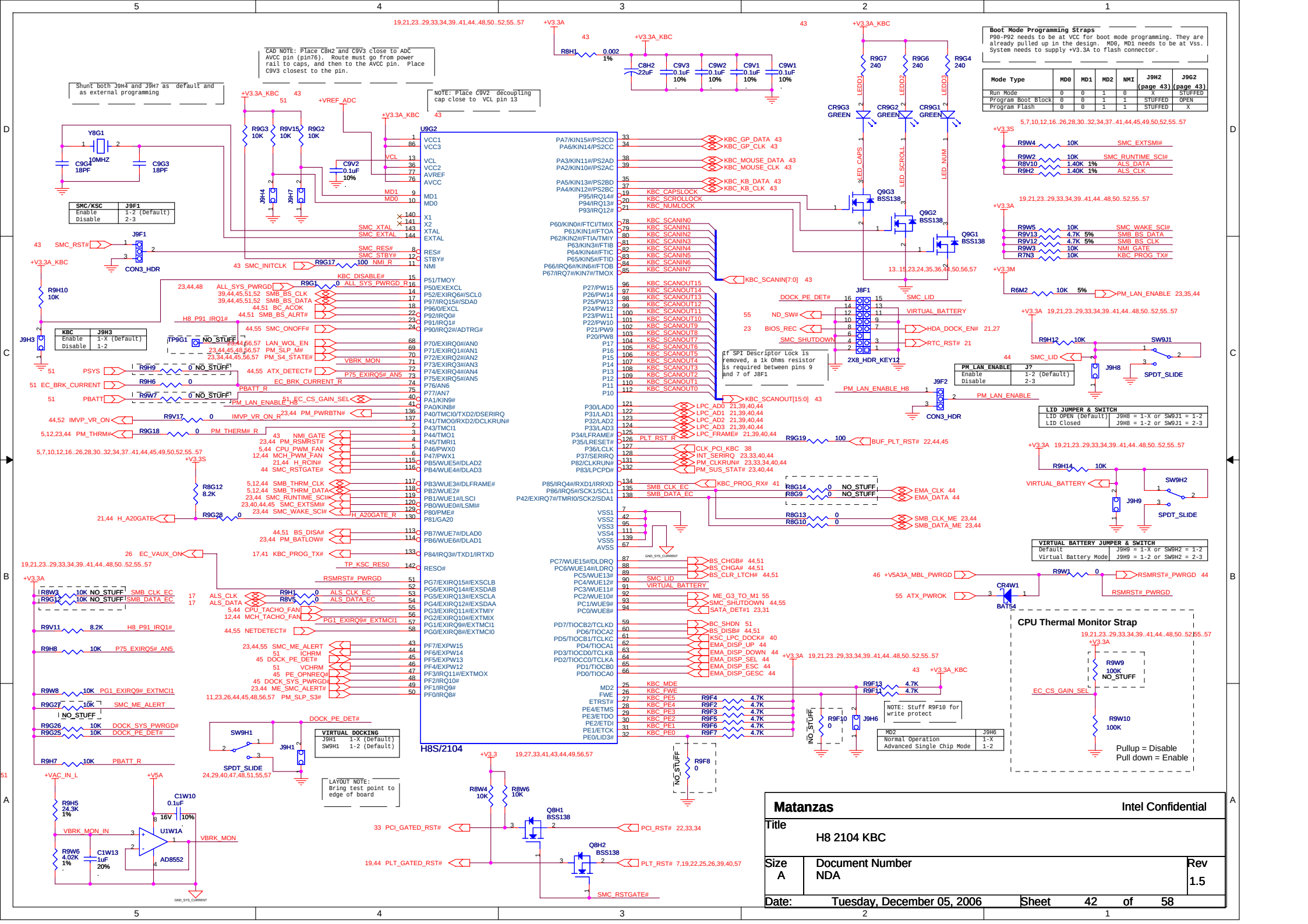
CAD NOTE: Place C8H2 and C9V3 close to ADC AVCC pin (pin76). Route must go from power rail to caps, and then to the AVCC pin. Place C9V3 closest to the pin.
Shunt both J9H4 and J9H7 as default and as external programming
NOTE: Place C9V2 decoupling cap close to VCL pin 13
Boot Mode Programming Straps
P90-P92 needs to be at VCC for boot mode programming. They are already pulled up in the design. MD0, MD1 needs to be at Vss. System needs to supply +V3.3A to flash connector.
Mode Type | MD0 | MD1 | MD2 | NMI | J9H2 (page 43) | J9G2 (page 43)
Run Mode | 0 | 0 | 1 | 0 | X | STUFFED
Program Boot Block | 0 | 0 | 1 | 1 | STUFFED | OPEN
Program Flash | 0 | 0 | 1 | 1 | STUFFED | X
SMC/KSC | J9F1
Enable | 1-2 (Default)
Disable | 2-3
KBC | J9H3
Enable | 1-X (Default)
Disable | 1-2
If SPI Descriptor Lock is removed, a 1k Ohms resistor is required between pins 9 and 7 of J8F1
PM_LAN_ENABLE | J?
Enable | 1-2 (Default)
Disable | 2-3
LID JUMPER & SWITCH
LID OPEN (Default) | J9H8 = 1-X or SW9J1 = 1-2
LID Closed | J9H8 = 1-2 or SW9J1 = 2-3
VIRTUAL BATTERY JUMPER & SWITCH
Default | J9H9 = 1-X or SW9H2 = 1-2
Virtual Battery Mode | J9H9 = 1-2 or SW9H2 = 2-3
VIRTUAL_DOCKING
J9H1 1-X (Default)
SW9H1 1-2 (Default)
MD2 | J9H6
Normal Operation | 1-X
Advanced Single Chip Mode | 1-2
NOTE: Stuff R9F10 for write protect
LAYOUT NOTE: Bring test point to edge of board
CPU Thermal Monitor Strap
Pullup = Disable
Pull down = Enable
H8S/2104
Matanzas
Intel Confidential
Title
H8 2104 KBC
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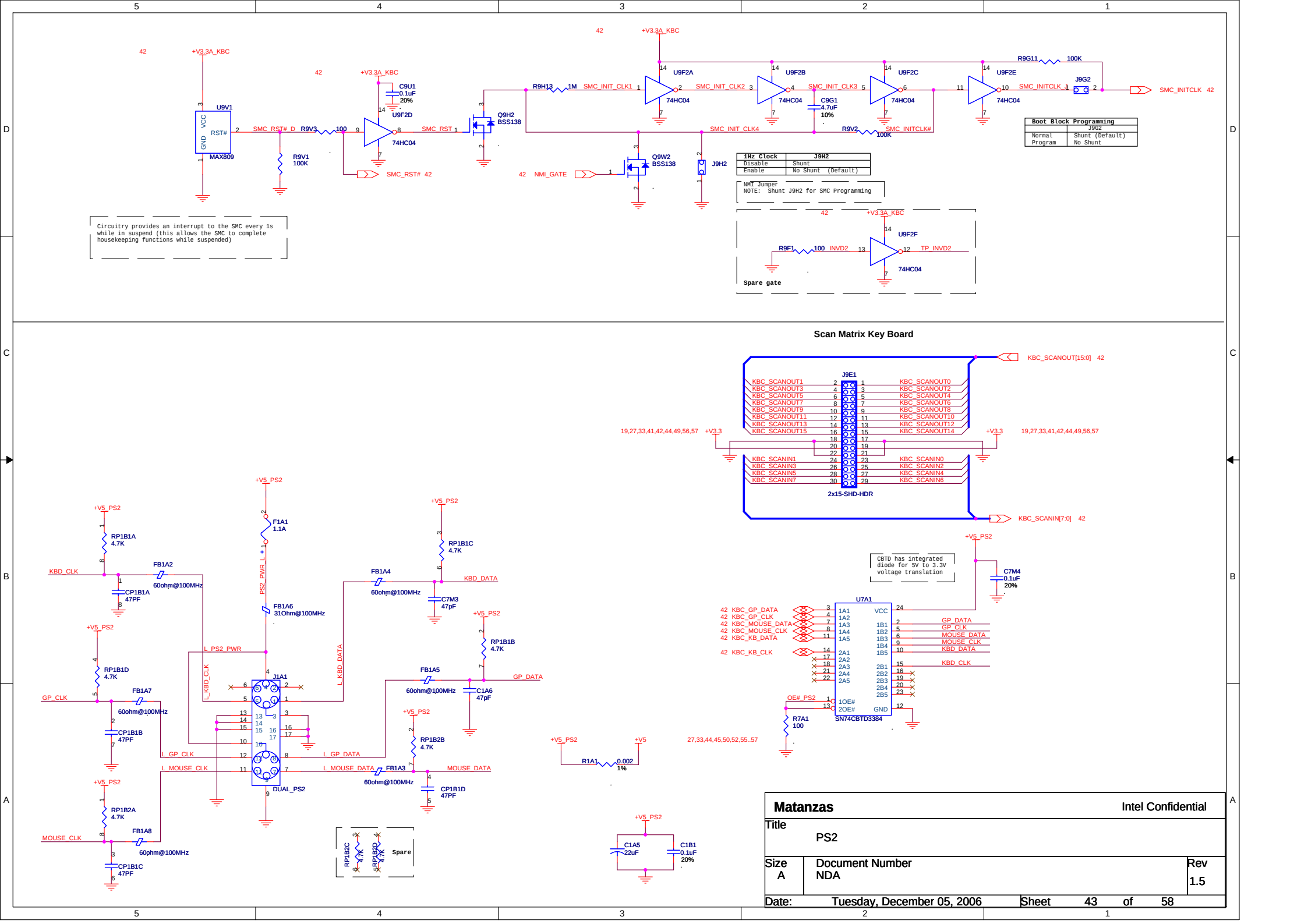
Circuitry provides an interrupt to the SMC every 1s while in suspend (this allows the SMC to complete housekeeping functions while suspended)
MAX809
74HC04
BSS138
SMC_RST#
SMC_INIT_CLK1
SMC_INIT_CLK2
SMC_INIT_CLK3
SMC_INIT_CLK4
SMC_INITCLK#
SMC_INITCLK
NMI_GATE
Boot Block Programming
1Hz Clock
NMI Jumper
NOTE: Shunt J9H2 for SMC Programming
Spare gate
Scan Matrix Key Board
2x15-SHD-HDR
SN74CBTD3384
CBTD has integrated diode for 5V to 3.3V voltage translation
DUAL_PS2
Spare
Matanzas
Intel Confidential
Title
PS2
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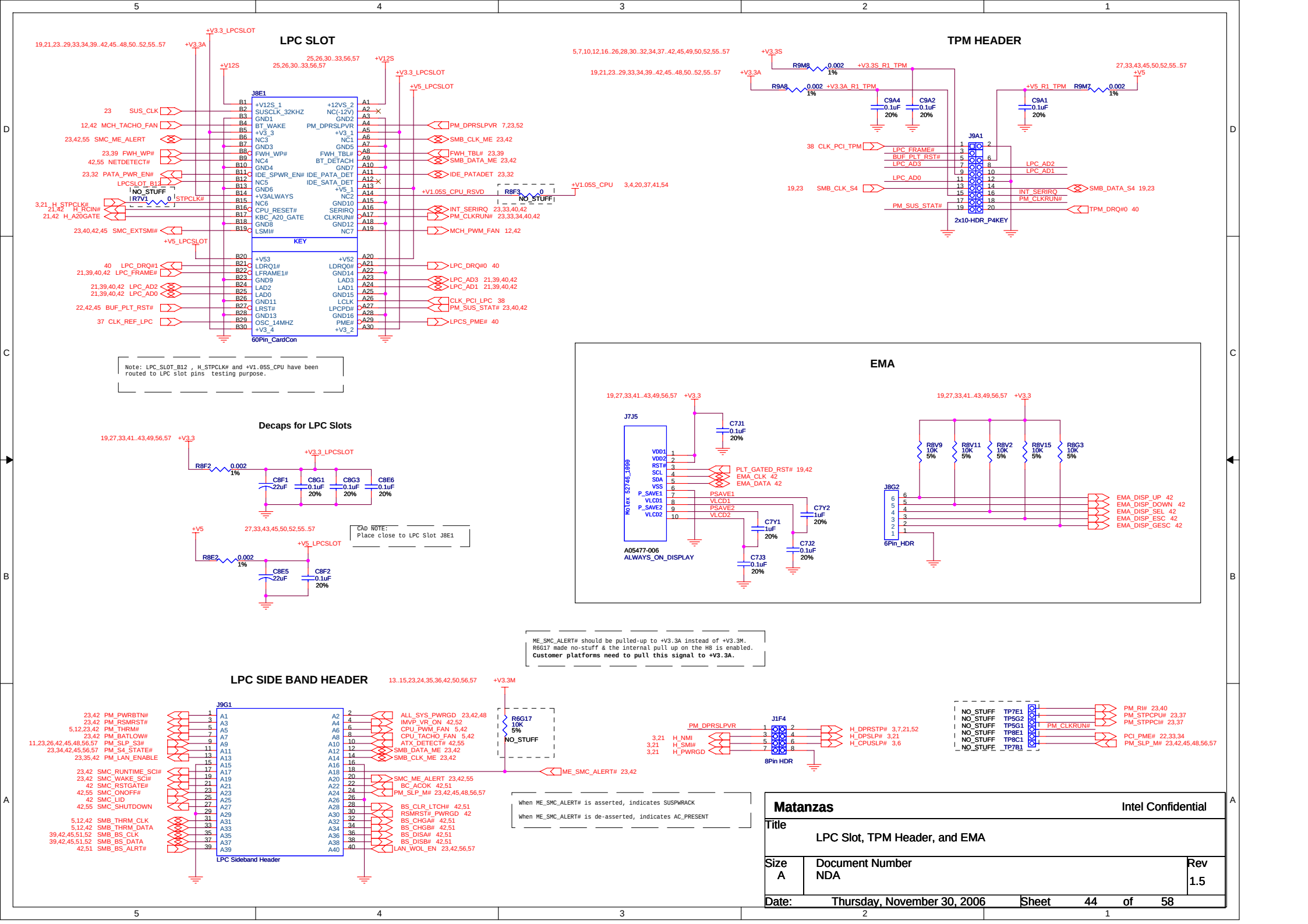
LPC SLOT
TPM HEADER
EMA
Decaps for LPC Slots
LPC SIDE BAND HEADER
J8E1
60Pin_CardCon
J9A1
2x10-HDR_P4KEY
J7J5
A05477-006
ALWAYS_ON_DISPLAY
J8G2
6Pin_HDR
J9G1
LPC Sideband Header
J1F4
8Pin HDR
Note: LPC_SLOT_B12 , H_STPCLK# and +V1.05S_CPU have been routed to LPC slot pins testing purpose.
CAD NOTE: Place close to LPC Slot J8E1
ME_SMC_ALERT# should be pulled-up to +V3.3A instead of +V3.3M. R6G17 made no-stuff & the internal pull up on the H8 is enabled. Customer platforms need to pull this signal to +V3.3A.
When ME_SMC_ALERT# is asserted, indicates SUSPWRACK
When ME_SMC_ALERT# is de-asserted, indicates AC_PRESENT
Matanzas
Intel Confidential
Title
LPC Slot, TPM Header, and EMA
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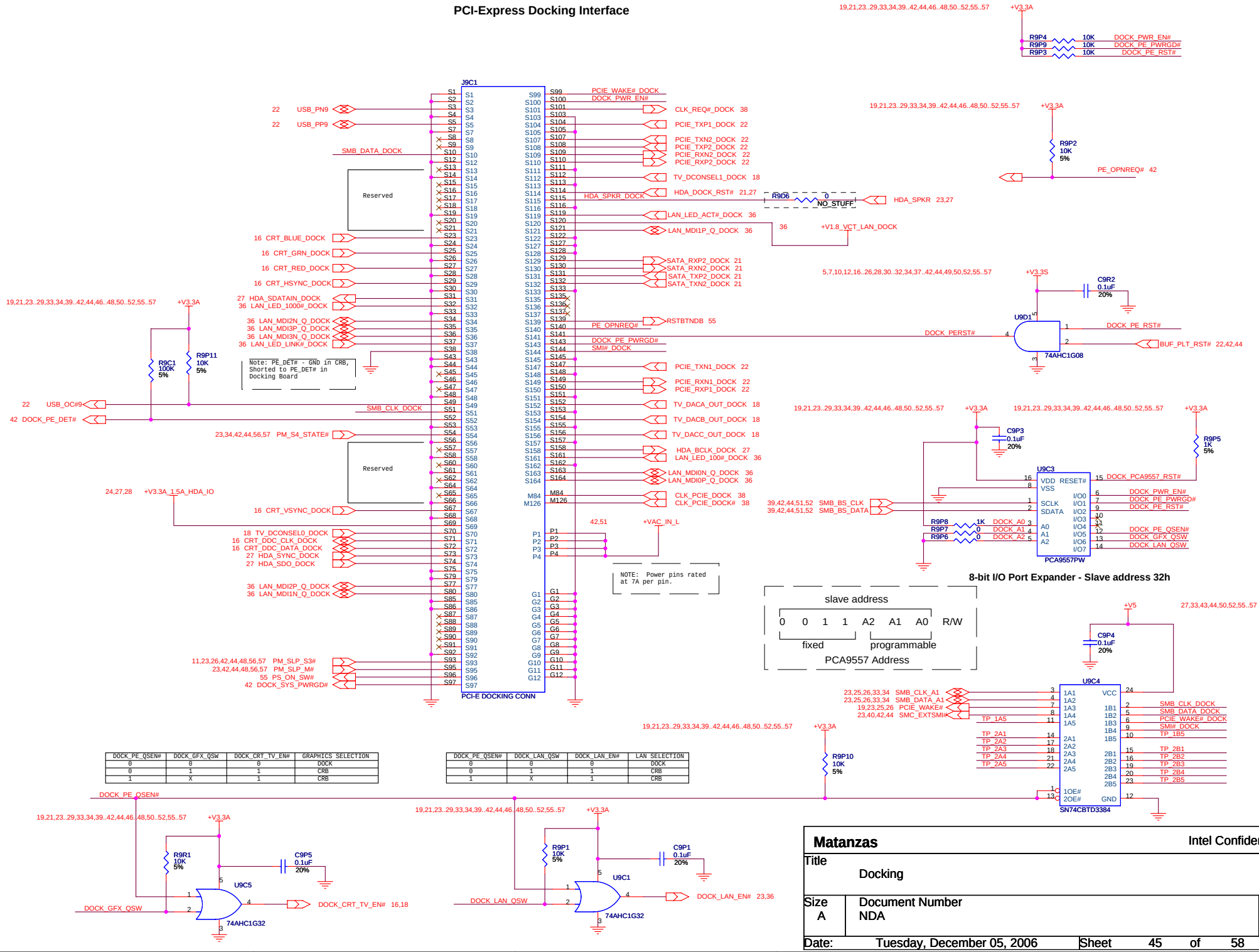
PCI-Express Docking Interface



DOCK_PE_QSEN#	DOCK_GFX_QSW	DOCK_CRT_TV_EN#	GRAPHICS SELECTION
0	0	0	DOCK
0	1	1	CRB
1	X	1	CRB

DOCK_PE_QSEN#	DOCK_LAN_QSW	DOCK_LAN_EN#	LAN SELECTION
0	0	0	DOCK
0	1	1	CRB
1	X	1	CRB

Matanzas			Intel Confidential
Title: Docking			
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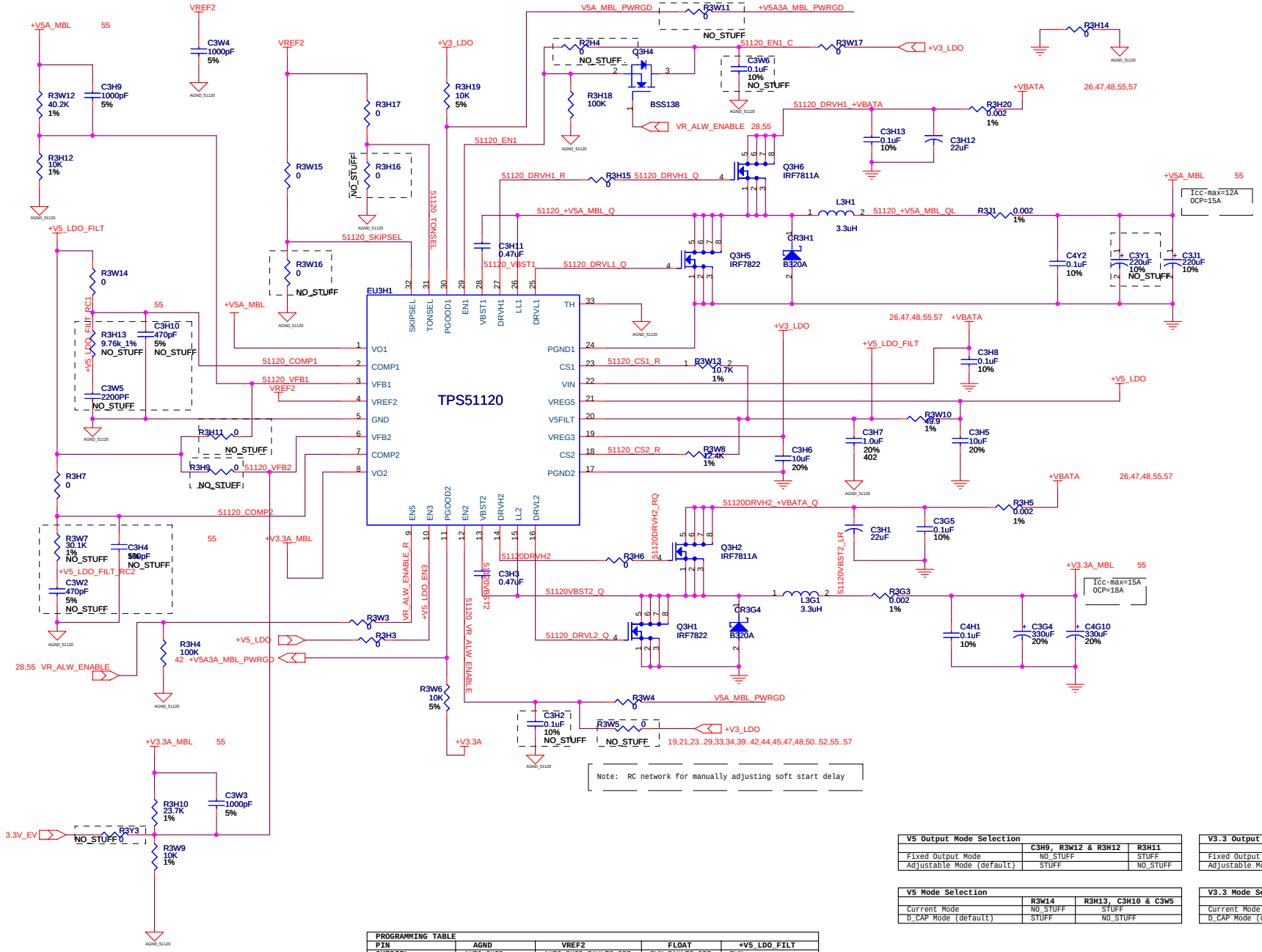

PROGRAMMING TABLE				
PIN	AGND	VREF2	FLOAT	+V5_LDO_FILT
SKIPSEL	AUTO-SKIP	AUTO-SKIP FAULTS OFF	PWM FAULTS OFF	PWM
COMP	N/A	N/A	N/A	D-CAP MODE
TONSEL(CH1/2)	380KHz/590KHz	290KHz/440KHz	220KHz/330KHz	180KHz/280KHz
VFB1	N/A	SHOULD NOT BE USED	N/A	5V FIXED OUTPUT
VFB2	N/A	SHOULD NOT BE USED	N/A	3.3V FIXED OUTPUT
EN1,EN2	SWITCHER OFF	SHOULD NOT BE USED	N/A	SWITCHER ON
EN3,EN5	LDO OFF	SHOULD NOT BE USED	N/A	LDO ON

V5 Output Mode Selection		
	C3H9, R3W12 & R3H12	R3H11
Fixed Output Mode	NO_STUFF	STUFF
Adjustable Mode (default)	STUFF	NO_STUFF

V3.3 Output Mode Selection		
	C3W3, R3H10 & R3W9	R3H9
Fixed Output Mode	NO_STUFF	STUFF
Adjustable Mode (default)	STUFF	NO_STUFF

V5 Mode Selection		
	R3W14	R3H13, C3H10 & C3W5
Current Mode	NO_STUFF	STUFF
D_CAP Mode (default)	STUFF	NO_STUFF

V3.3 Mode Selection		
	R3H7	R3W7, C3H4 & C3W2
Current Mode	NO_STUFF	STUFF
D_CAP Mode (default)	STUFF	NO_STUFF

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Title: TPS51120 System Power

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DDR2 VREG

Discharge Selection	R4B1	R4A6
Tracking Discharge (Default)	STUFF	NO_STUFF
Non-tracking Discharge	NO_STUFF	STUFF

Mode Selection	R4B11	R4B10, C4N5 & C4B4
Current Mode	NO_STUFF	STUFF
D_CAP Mode (default)	STUFF	NO_STUFF

VDDQSET	R4B6	R4B3
VOUT 1.8V (Default)	STUFF	NO_STUFF
VOUT 1.5V	NO_STUFF	STUFF

Layout Note: C4N4, R4N4 & RR4B12 shoud be place close to chipset.

Note: OCP set point at 14A

Vout = 1.8/1.5V
V Iout = 10A

Adds 3.3M to the MPWROK tree. Needed to support G3->M1 and Moff to M1 transitions.

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Title: DDR2 VR		
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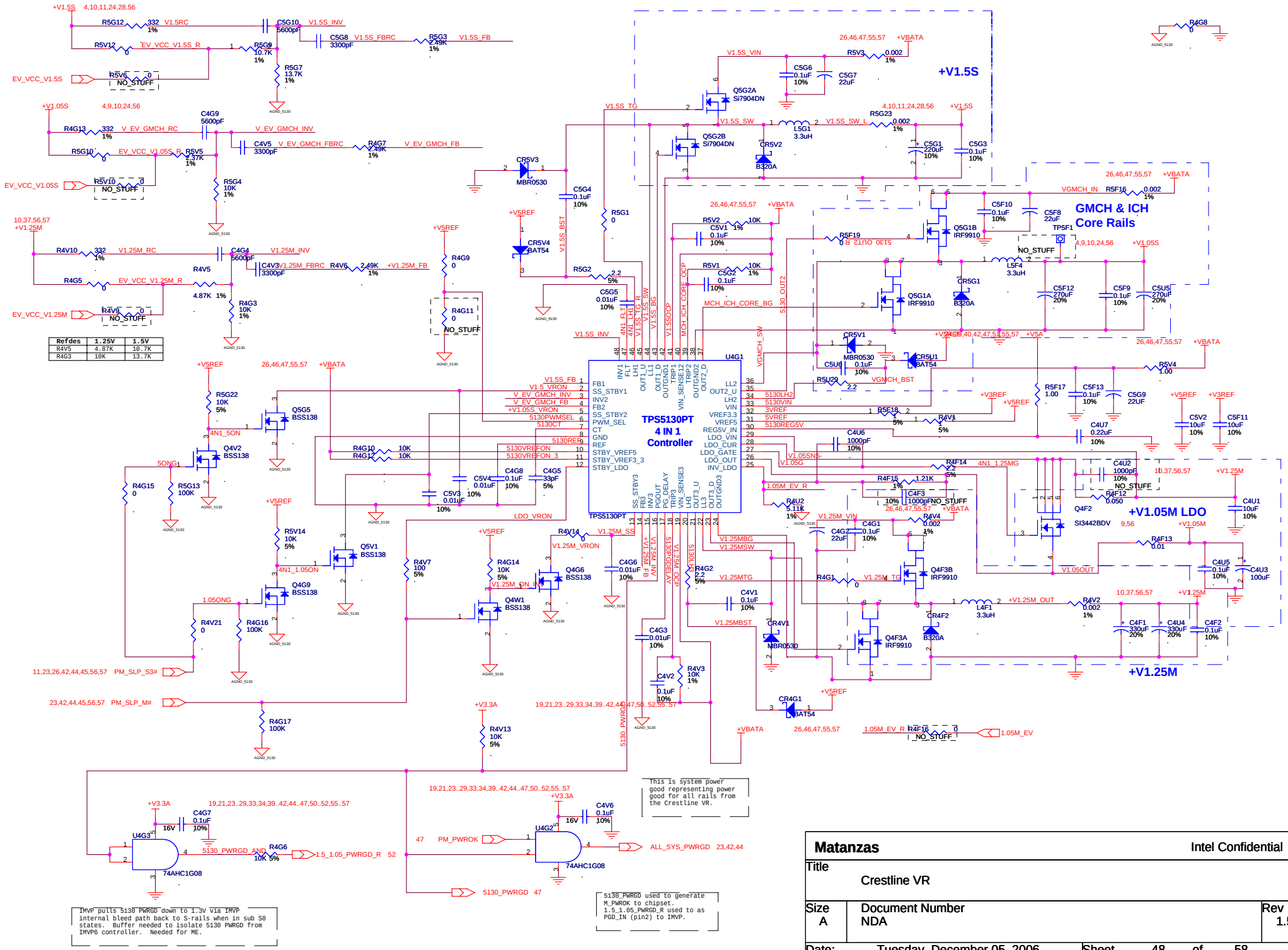
+V1.5S
+V1.05S
+V1.25M
+V1.05M LDO
+V1.25M
GMCH & ICH
Core Rails
TPS5130PT
4 IN 1
Controller
U4G1
TPS5130PT
Refdes 1.25V 1.5V
R4V5 4.87K 10.7K
R4G3 10K 13.7K
Matanzas
Intel Confidential
Title
Crestline VR
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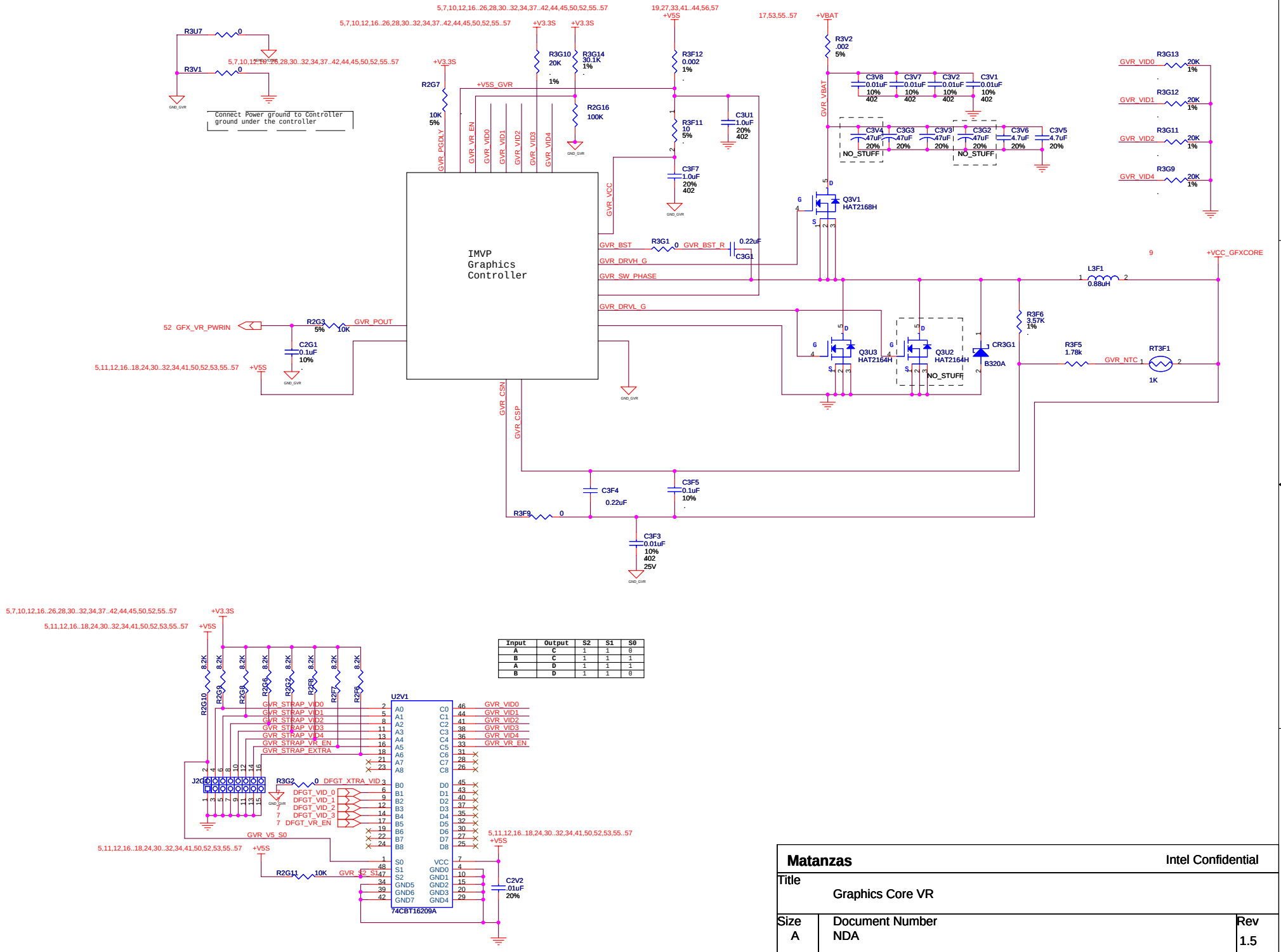
IMVP pulls 5130_PWRGD down to 1.3V via IMVP internal bleed path back to S-rails when in sub S0 states. Buffer needed to isolate 5130_PWRGD from IMVP6 controller. Needed for ME.
This is system power good representing power good for all rails from the Crestline VR.
5130_PWRGD used to generate M_PWROK to chipset. 1.5_1.05_PWRGD_R used to as PGD_IN (pin2) to IMVP.



Input	Output	S2	S1	S0
A	C	1	1	0
B	C	1	1	1
A	D	1	1	1
B	D	1	1	0

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Title	Graphics Core VR	
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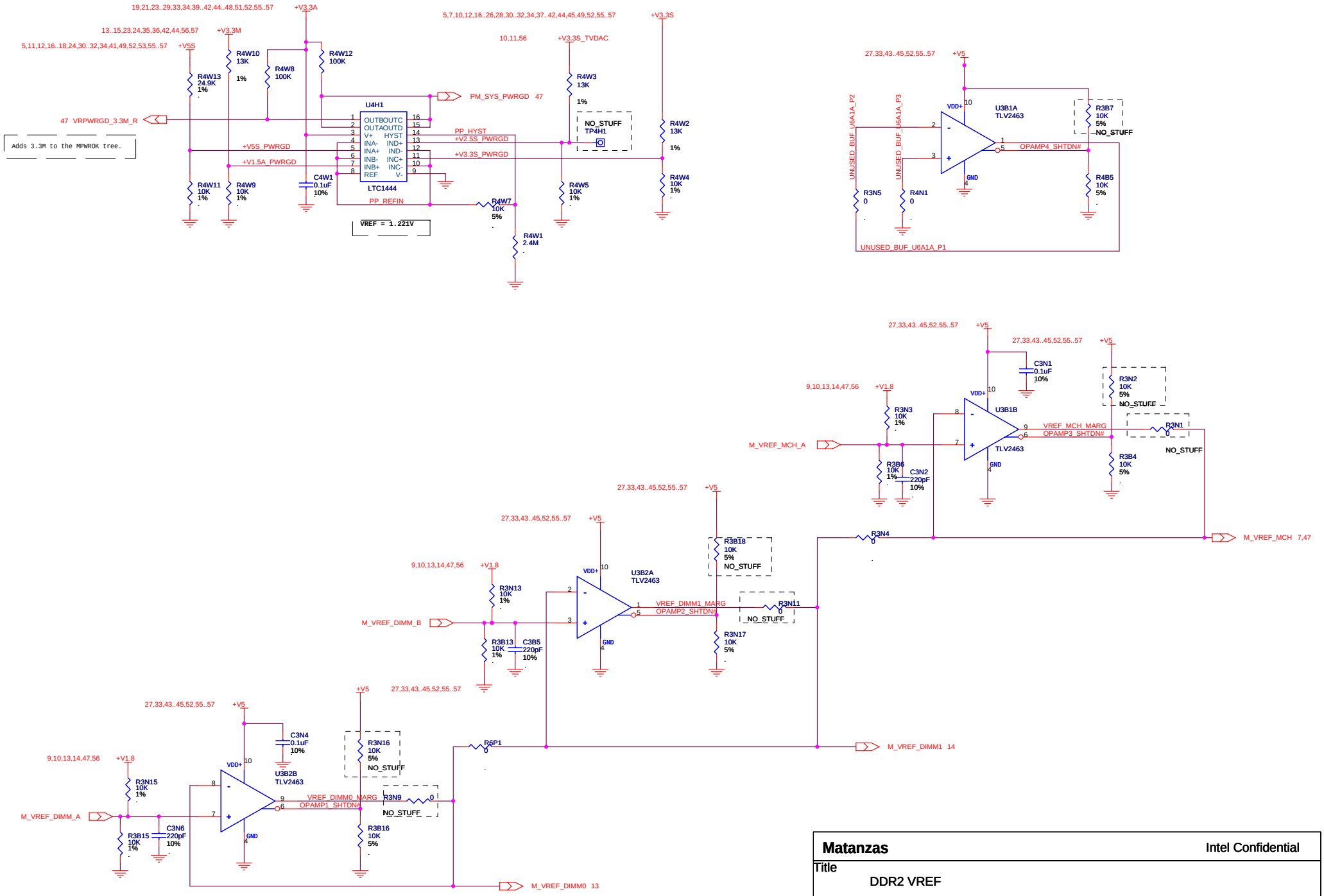
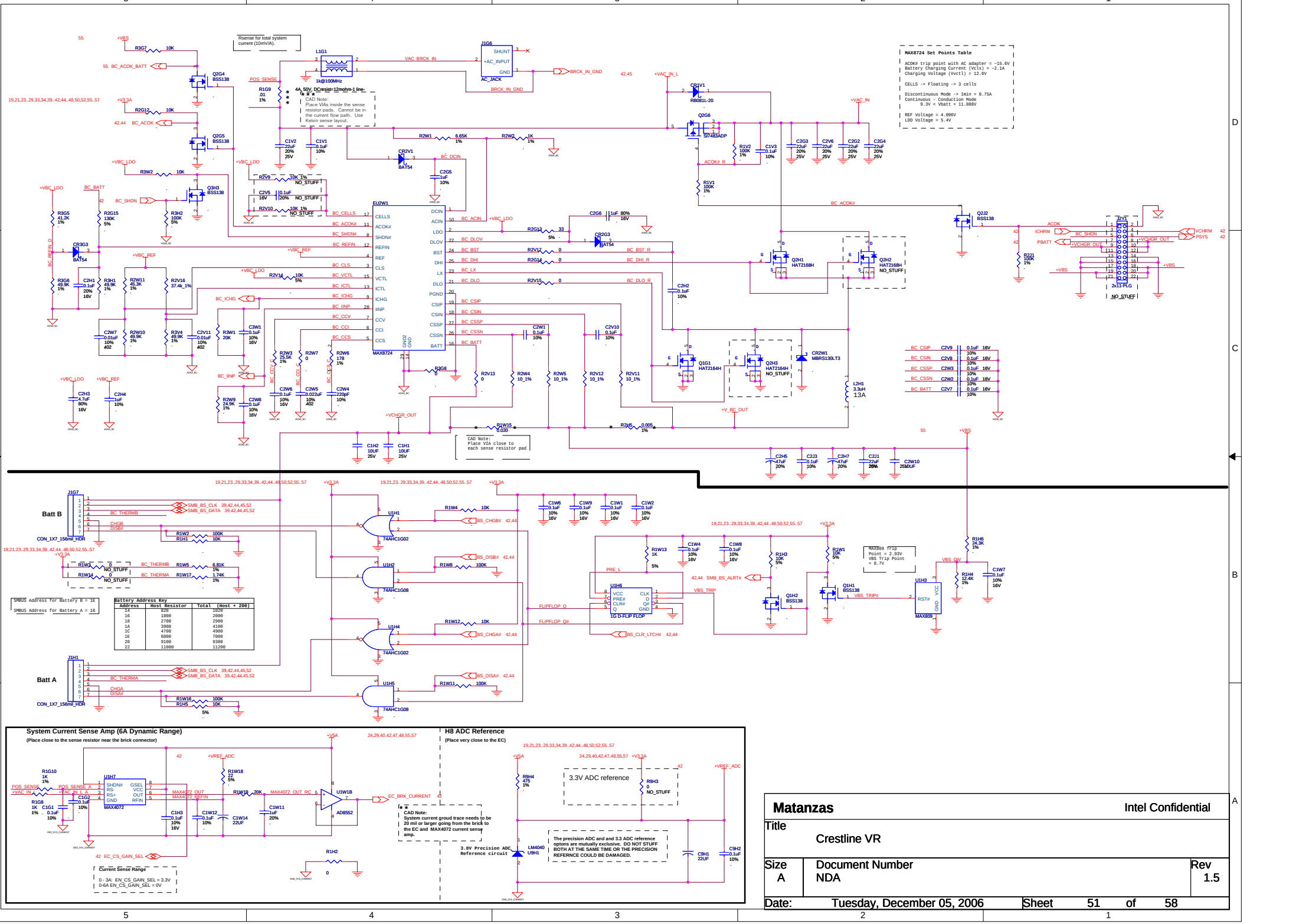


Matanzas		Intel Confidential
Title	DDR2 VREF	
Size A	Document Number NDA	Rev 1.5
Date: Tuesday, December 05, 2006	Sheet 50 of 58	


MAX8724 Set Points Table
ACOK# trip point with AC adapter = -15.6V
Battery Charging Current (Vcls) = -2.1A
Charging Voltage (Vvctl) = 12.6V
CELLS -> Floating -> 3 cells
Discontinuous Mode -> Imin = 0.75A
Continuous - Conduction Mode
9.3V < Vbatt < 11.088V
REF Voltage = 4.096V
LDO Voltage = 5.4V
Batt B
Batt A
CON_1X7_156mil_HDR
Battery Address Key
Address | Host Resistor | Total (Host + 200)
SMBUS Address for Battery B = 1E
SMBUS Address for Battery A = 16
System Current Sense Amp (6A Dynamic Range)
(Place close to the sense resistor near the brick connector)
Current Sense Range
0 - 3A: EN_CS_GAIN_SEL = 3.3V
0-6A EN_CS_GAIN_SEL = 0V
H8 ADC Reference
(Place very close to the EC)
3.3V ADC reference
3.0V Precision ADC Reference circuit
CAD Note: Place VIAs inside the sense resistor pads. Cannot be in the current flow path. Use Kelvin sense layout.
CAD Note: Place VIA close to each sense resistor pad
CAD Note: System current groud trace needs to be 20 mil or larger going from the brick to the EC and MAX4072 current sense amp.
The precision ADC and and 3.3 ADC reference optons are mutually exclusive. DO NOT STUFF BOTH AT THE SAME TIME OR THE PRECISION REFERNCE COULD BE DAMAGED.
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Title
Crestline VR
Size
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Document Number
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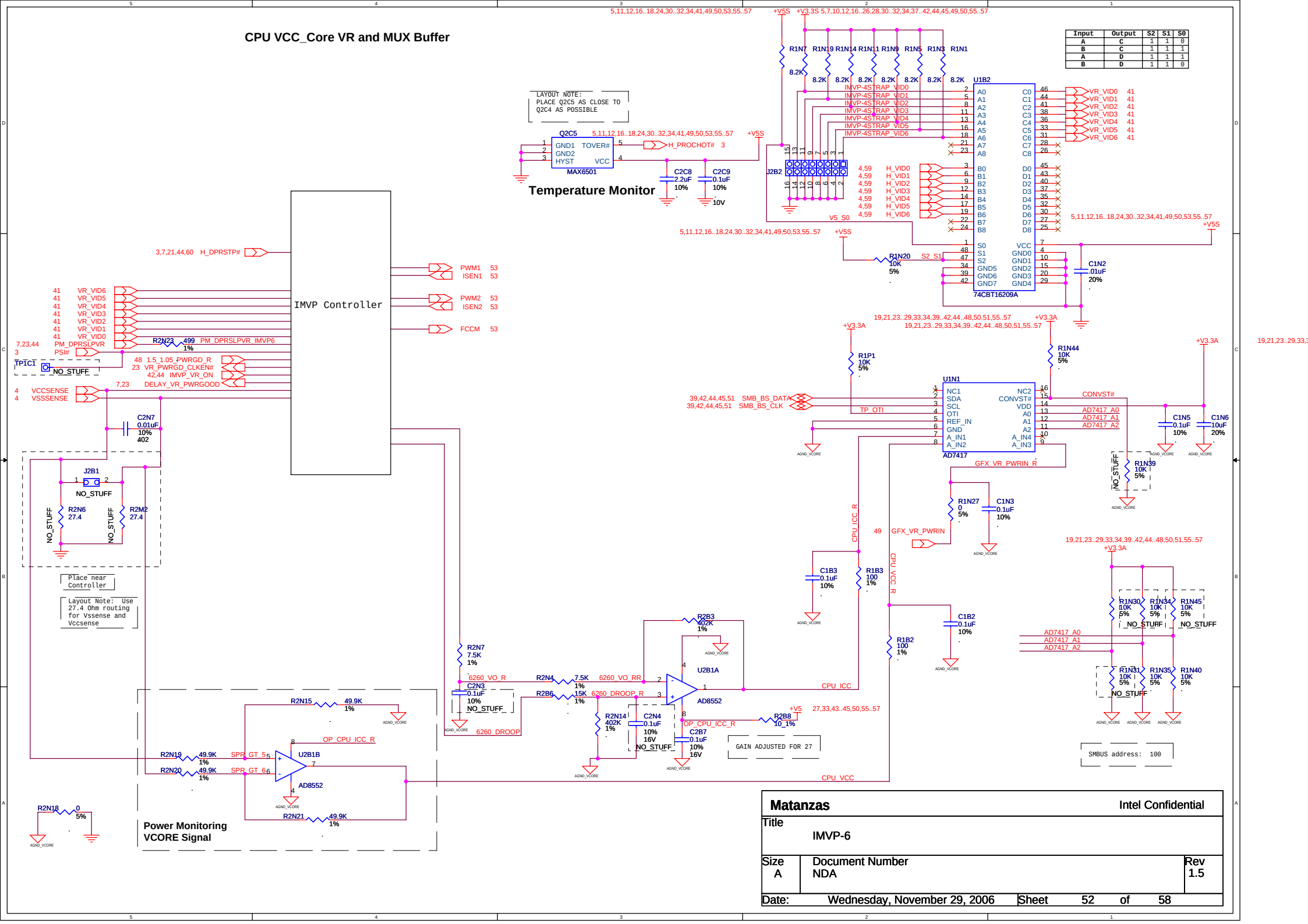
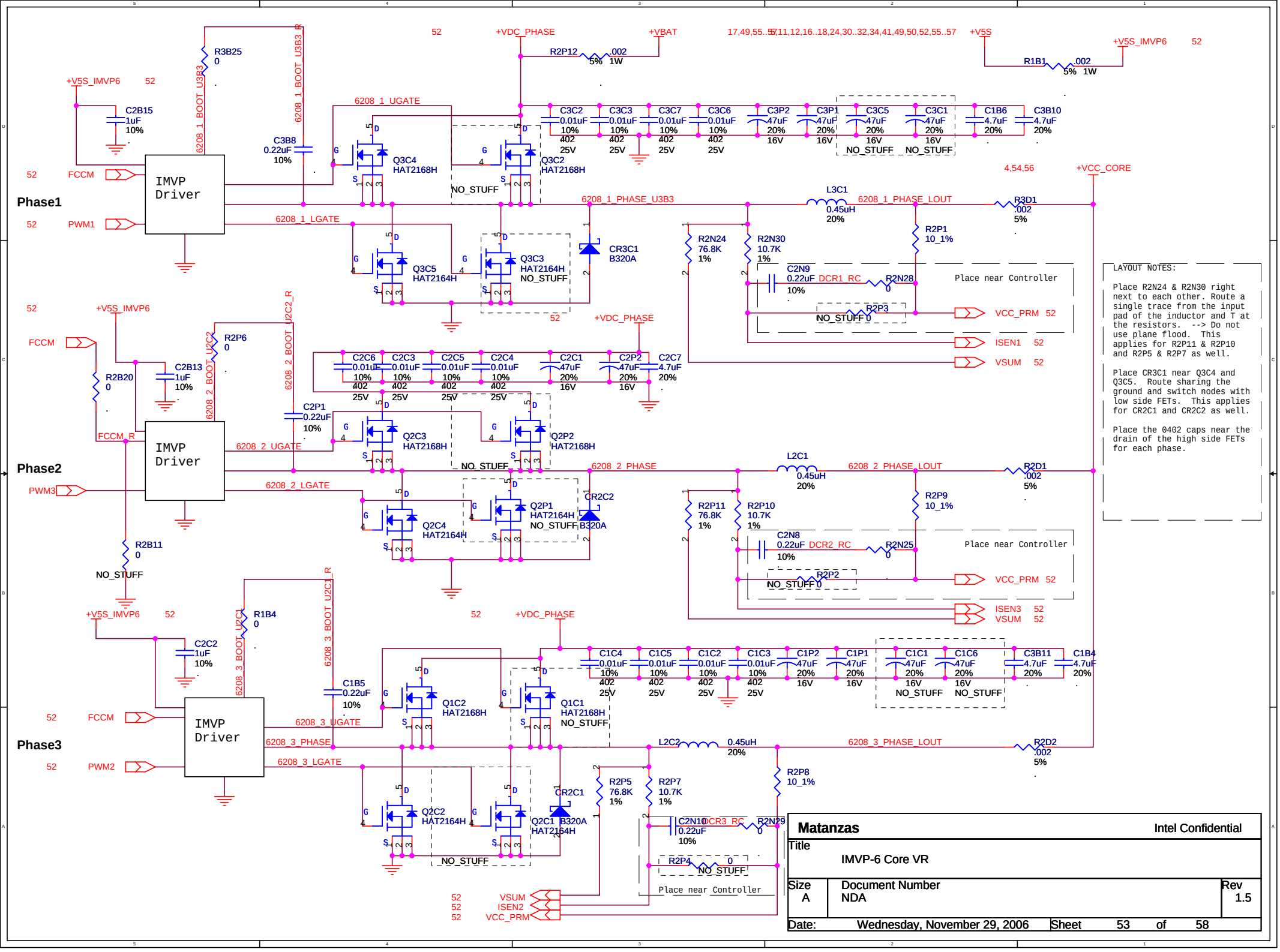
CPU VCC_Core VR and MUX Buffer




Phase1
Phase2
Phase3
IMVP Driver
+VDC_PHASE
+VBAT
+V5S
+V5S_IMVP6
+VCC_CORE
FCCM
PWM1
PWM2
PWM3
6208_1_UGATE
6208_1_LGATE
6208_1_PHASE_U3B3
6208_1_PHASE_LOUT
6208_2_UGATE
6208_2_LGATE
6208_2_PHASE
6208_2_PHASE_LOUT
6208_3_UGATE
6208_3_LGATE
6208_3_PHASE
6208_3_PHASE_LOUT
Q3C4 HAT2168H
Q3C2 HAT2168H
Q3C5 HAT2164H
Q3C3 HAT2164H NO_STUFF
Q2C3 HAT2168H
Q2P2 HAT2168H
Q2C4 HAT2164H
Q2P1 HAT2164H NO_STUFF
Q1C2 HAT2168H
Q1C1 HAT2168H NO_STUFF
Q2C2 HAT2164H
Q2C1 HAT2164H
CR3C1 B320A
CR2C2 B320A
CR2C1 B320A
L3C1 0.45uH 20%
L2C1 0.45uH 20%
L2C2 0.45uH 20%
R3D1 .002 5%
R2D1 .002 5%
R2D2 .002 5%
R2P1 10_1%
R2P9 10_1%
R2P8 10_1%
R2N24 76.8K 1%
R2N30 10.7K 1%
R2P11 76.8K 1%
R2P10 10.7K 1%
R2P5 76.8K 1%
R2P7 10.7K 1%
C2N9 0.22uF DCR1_RC 10%
C2N8 0.22uF DCR2_RC 10%
C2N10 0.22uF DCR3_RC 10%
R2N28 0
R2N25 0
R2N29 0
R2P3 NO_STUFF 0
R2P2 NO_STUFF 0
R2P4 NO_STUFF 0
Place near Controller
VCC_PRM 52
ISEN1 52
VSUM 52
ISEN3 52
ISEN2 52
LAYOUT NOTES:
Place R2N24 & R2N30 right next to each other. Route a single trace from the input pad of the inductor and T at the resistors. --> Do not use plane flood. This applies for R2P11 & R2P10 and R2P5 & R2P7 as well.
Place CR3C1 near Q3C4 and Q3C5. Route sharing the ground and switch nodes with low side FETs. This applies for CR2C1 and CR2C2 as well.
Place the 0402 caps near the drain of the high side FETs for each phase.
Matanzas
Intel Confidential
Title
IMVP-6 Core VR
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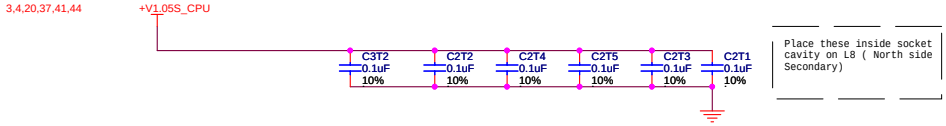
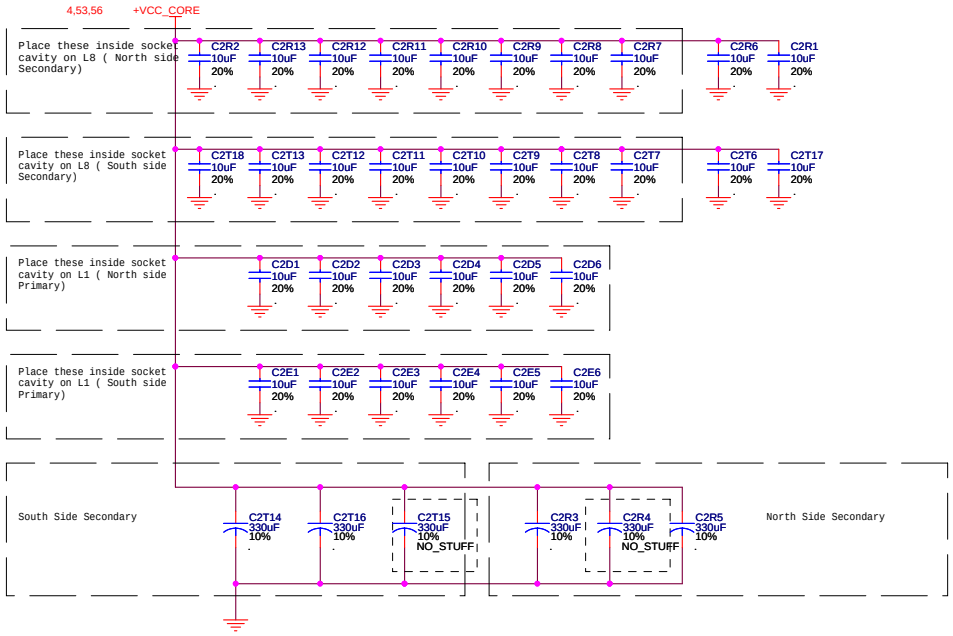
Vccp Core Decoupling



Vcc Core Decoupling



Matanzas		Intel Confidential
Title: CPU Decoupling		
Size: A	Document Number: NDA	Rev: 1.5
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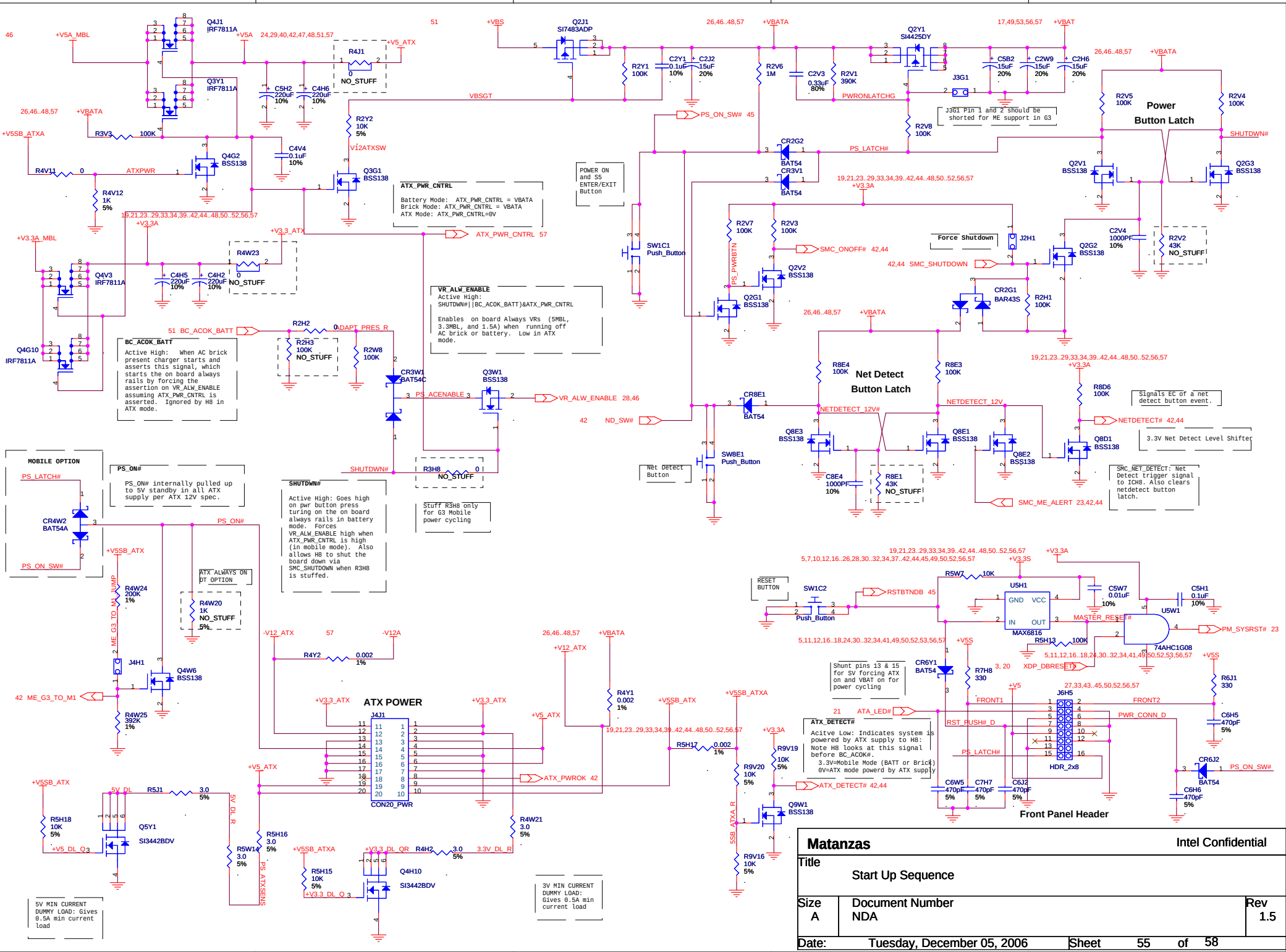
Power Button Latch
Net Detect Button Latch
ATX POWER
Front Panel Header
MOBILE OPTION
Force Shutdown
Matanzas
Intel Confidential
Start Up Sequence
Size A
Document Number NDA
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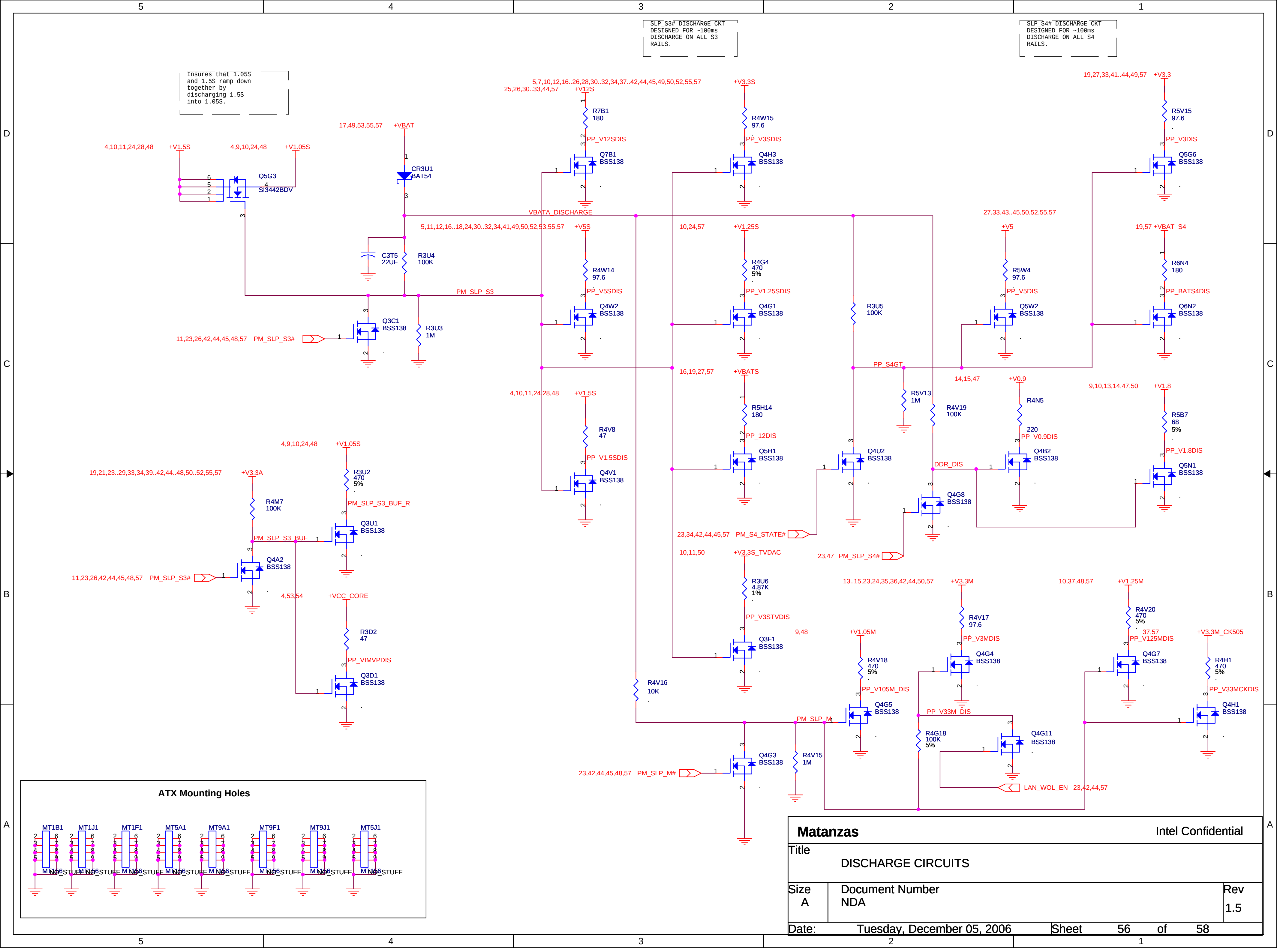
SLP_S3# DISCHARGE CKT DESIGNED FOR ~100ms DISCHARGE ON ALL S3 RAILS.
SLP_S4# DISCHARGE CKT DESIGNED FOR ~100ms DISCHARGE ON ALL S4 RAILS.
Insures that 1.05S and 1.5S ramp down together by discharging 1.5S into 1.05S.
+V1.5S
+V1.05S
Q5G3 SI3442BDV
+VBAT
CR3U1 BAT54
C3T5 22UF
R3U4 100K
R3U3 1M
Q3C1 BSS138
PM_SLP_S3
PM_SLP_S3#
VBATA_DISCHARGE
+V12S
R7B1 180
PP_V12SDIS
Q7B1 BSS138
+V3.3S
R4W15 97.6
PP_V3SDIS
Q4H3 BSS138
+V3.3
R5V15 97.6
PP_V3DIS
Q5G6 BSS138
+V5S
R4W14 97.6
PP_V5SDIS
Q4W2 BSS138
+V1.25S
R4G4 470 5%
PP_V1.25SDIS
Q4G1 BSS138
R3U5 100K
+V5
R5W4 97.6
PP_V5DIS
Q5W2 BSS138
+VBAT_S4
R6N4 180
PP_BATS4DIS
Q6N2 BSS138
PP_S4GT
+VBATS
R5H14 180
PP_12DIS
Q5H1 BSS138
R5V13 1M
R4V19 100K
+V0.9
R4N5 220
PP_V0.9DIS
Q4B2 BSS138
+V1.8
R5B7 68 5%
PP_V1.8DIS
Q5N1 BSS138
R4V8 47
PP_V1.5SDIS
Q4V1 BSS138
Q4U2 BSS138
DDR_DIS
Q4G8 BSS138
PM_S4_STATE#
PM_SLP_S4#
+V3.3A
R4M7 100K
PM_SLP_S3_BUF
Q4A2 BSS138
R3U2 470 5%
PM_SLP_S3_BUF_R
Q3U1 BSS138
+VCC_CORE
R3D2 47
PP_VIMVPDIS
Q3D1 BSS138
+V3.3S_TVDAC
R3U6 4.87K 1%
PP_V3STVDIS
Q3F1 BSS138
R4V16 10K
+V1.05M
R4V18 470 5%
PP_V105M_DIS
Q4G5 BSS138
PM_SLP_M
+V3.3M
R4V17 97.6
PP_V3MDIS
Q4G4 BSS138
PP_V33M_DIS
R4G18 100K 5%
Q4G11 BSS138
LAN_WOL_EN
+V1.25M
R4V20 470 5%
PP_V125MDIS
Q4G7 BSS138
+V3.3M_CK505
R4H1 470 5%
PP_V33MCKDIS
Q4H1 BSS138
Q4G3 BSS138
PM_SLP_M#
R4V15 1M
ATX Mounting Holes
MT1B1 MT1J1 MT1F1 MT5A1 MT9A1 MT9F1 MT9J1 MT5J1
NO_STUFF
Matanzas
Intel Confidential
Title
DISCHARGE CIRCUITS
Size A
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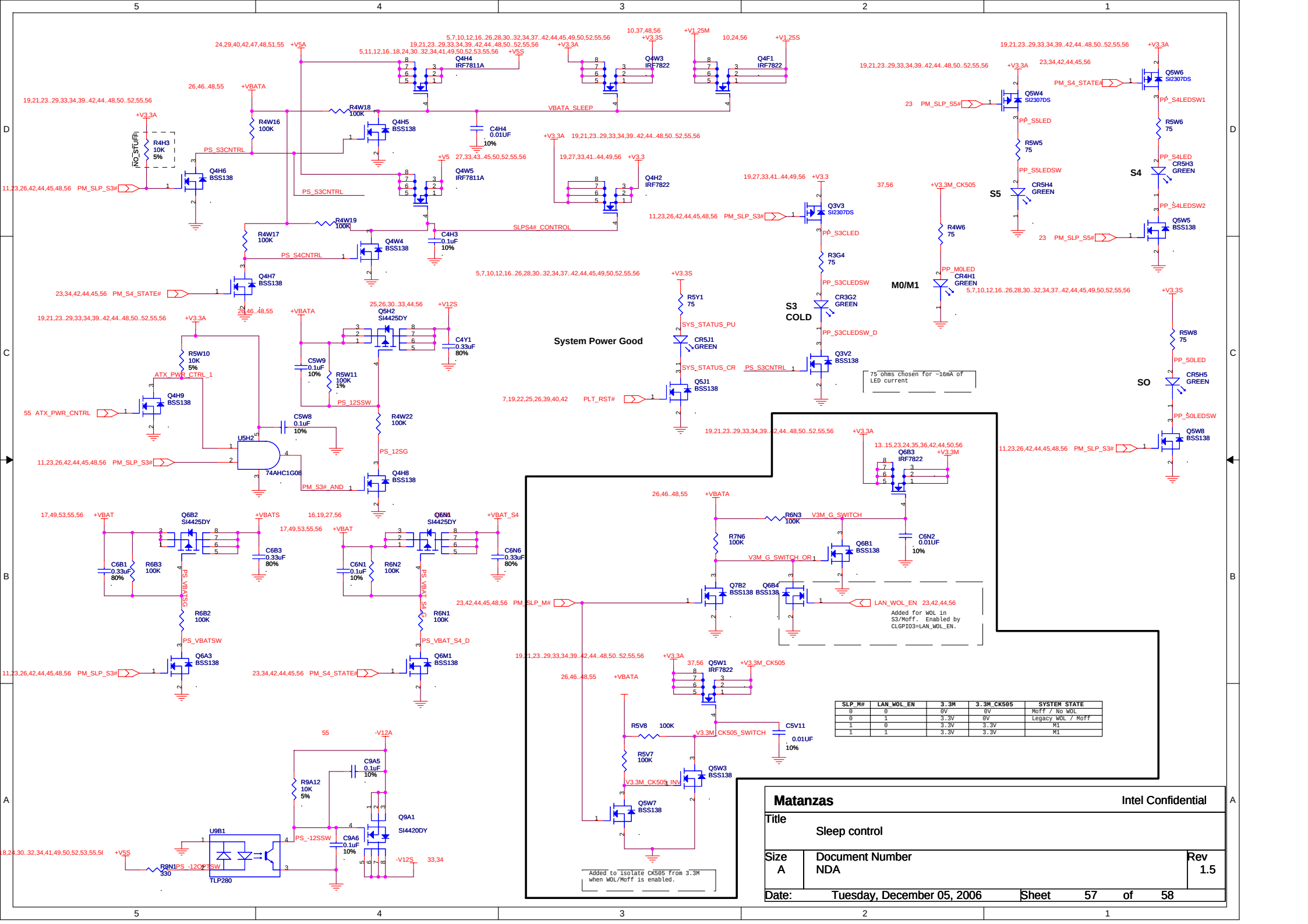
Q4H4 IRF7811A
Q4W3 IRF7822
Q4F1 IRF7822
Q4H5 BSS138
Q4H6 BSS138
Q4W5 IRF7811A
Q4H2 IRF7822
Q4W4 BSS138
Q4H7 BSS138
Q5H2 SI4425DY
Q4H9 BSS138
Q4H8 BSS138
U5H2 74AHC1G08
Q6B2 SI4425DY
Q6N1 SI4425DY
Q6A3 BSS138
Q6M1 BSS138
U9B1 TLP280
Q9A1 SI4420DY
Q3V3 SI2307DS
Q3V2 BSS138
Q5J1 BSS138
Q5W4 SI2307DS
Q5W6 SI2307DS
Q5W5 BSS138
Q6B3 IRF7822
Q6B1 BSS138
Q7B2 BSS138
Q6B4 BSS138
Q5W1 IRF7822
Q5W3 BSS138
Q5W7 BSS138
R4H3 10K 5%
R4W16 100K
R4W18 100K
R4W17 100K
R4W19 100K
R5W10 10K 5%
R5W11 100K 1%
R4W22 100K
R9A12 10K 5%
R9N1 330
R3G4 75
R5Y1 75
R4W6 75
R5W5 75
R5W6 75
R5W8 75
R7N6 100K
R6N3 100K
R5V8 100K
R5V7 100K
R6B2 100K
R6B3 100K
R6N1 100K
R6N2 100K
C4H4 0.01UF 10%
C4H3 0.1uF 10%
C4Y1 0.33uF 80%
C5W9 0.1uF 10%
C5W8 0.1uF 10%
C6B1 0.33uF 80%
C6B3 0.33uF 80%
C6N1 0.1uF 10%
C6N6 0.33uF 80%
C6N2 0.01UF 10%
C5V11 0.01UF 10%
C9A5 0.1uF 10%
C9A6 0.1uF 10%
CR5J1 GREEN
CR3G2 GREEN
CR4H1 GREEN
CR5H4 GREEN
CR5H3 GREEN
CR5H5 GREEN
S4
S5
S3 COLD
M0/M1
SO
System Power Good
NO_STUFF
+V3.3A
+V5A
+V5S
+VBATA
+VBAT
+VBATS
+VBAT_S4
+V3.3S
+V1.25M
+V1.25S
+V12S
-V12A
+V3.3M_CK505
PS_S3CNTRL
PS_S4CNTRL
VBATA_SLEEP
SLPS4#_CONTROL
PS_12SSW
PS_12SG
PM_S3#_AND
PS_VBATSW
PS_VBAT_S4_D
PS_-12SSW
PS_-12OUTSW
ATX_PWR_CTRL_1
SYS_STATUS_PU
SYS_STATUS_CR
PP_S3CLED
PP_S3CLEDSW
PP_S3CLEDSW_D
PP_S4LED
PP_S4LEDSW1
PP_S4LEDSW2
PP_S5LED
PP_S5LEDSW
PP_M0LED
PP_S0LED
PP_S0LEDSW
V3M_G_SWITCH
V3M_G_SWITCH_OR
V3.3M_CK505_SWITCH
V3.3M_CK505_INV
PM_SLP_S3#
PM_SLP_S5#
PM_S4_STATE#
PM_SLP_M#
PLT_RST#
LAN_WOL_EN
75 ohms chosen for ~16mA of LED current
Added for WOL in S3/Moff. Enabled by CLGPIO3=LAN_WOL_EN.
Added to isolate CK505 from 3.3M when WOL/Moff is enabled.
SLP_M# | LAN_WOL_EN | 3.3M | 3.3M_CK505 | SYSTEM STATE
0 | 0 | 0V | 0V | Moff / No WOL
0 | 1 | 3.3V | 0V | Legacy WOL / Moff
1 | 0 | 3.3V | 3.3V | M1
1 | 1 | 3.3V | 3.3V | M1
Matanzas
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Title
Sleep control
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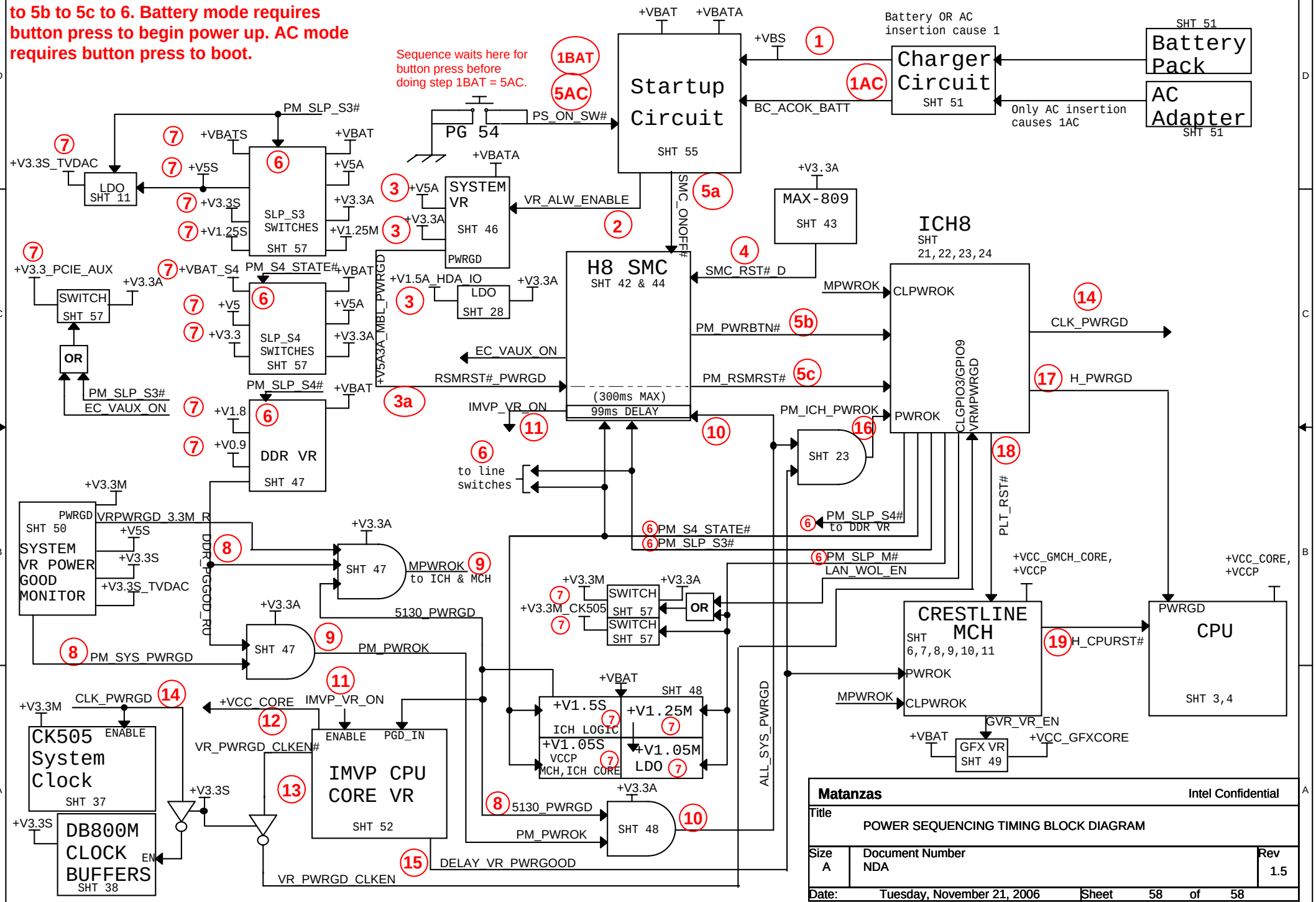
MATANZAS Mobile Power On Sequence

Steps 1 leads to either 1BAT for battery only mode or 1AC for AC mode. 5AC leads to 5a to 5b to 5c to 6. Battery mode requires button press to begin power up. AC mode requires button press to boot.



Matanzas		Intel Confidential
Title	POWER SEQUENCING TIMING BLOCK DIAGRAM	
Size A	Document Number NDA	Rev 1.5
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