

# *Concord River*


## Mobile Diamondville Single Core Processor with Intel 945GMS Express Chipset

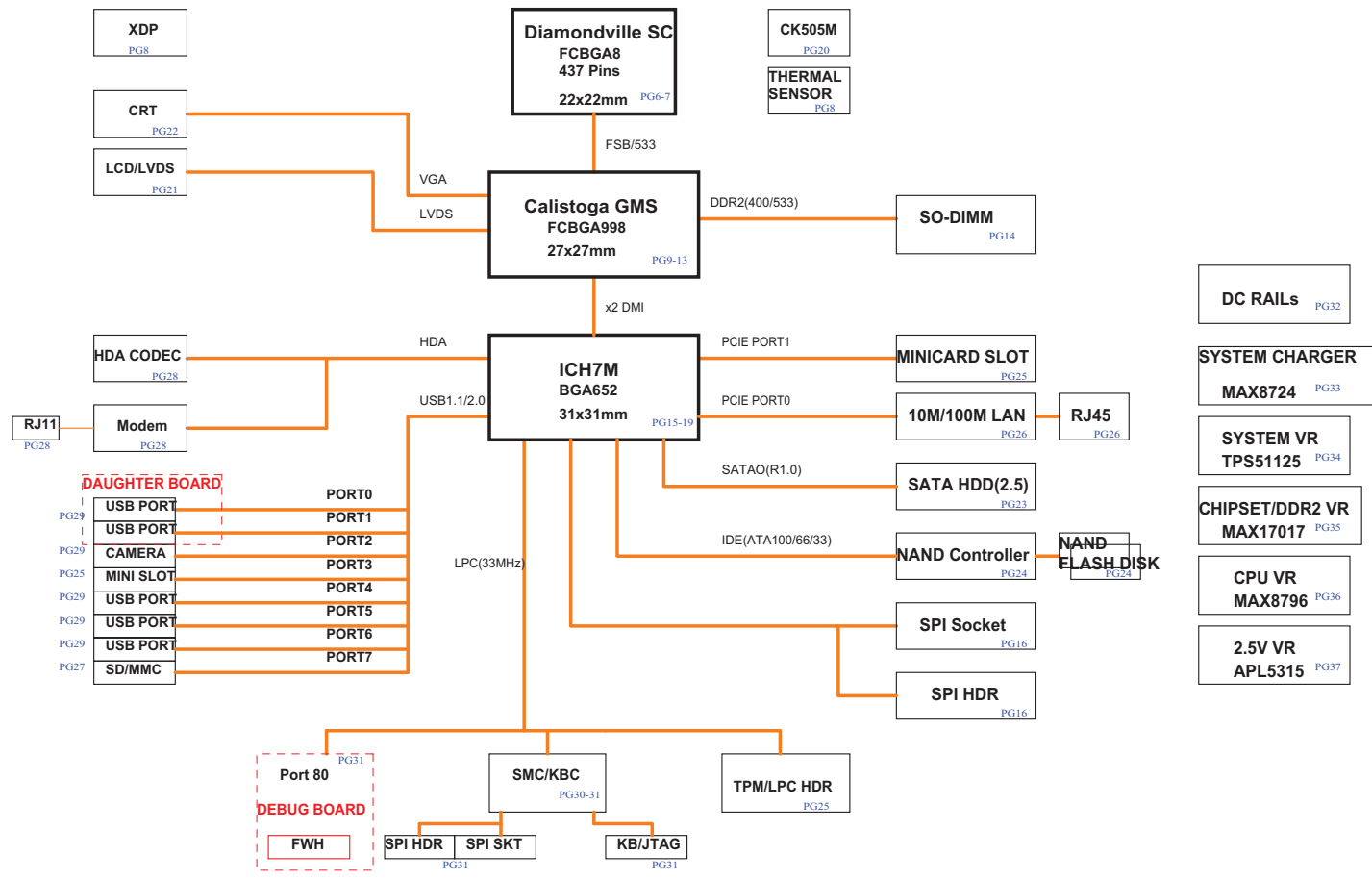
### Customer Reference Board Schematic

October 2007  
Revision 0.5

**Intel Confidential**



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# POWER RAILS, SMBUS ADDRESS, JUMPER SETTINGS, LED AND SWITCH LIST

## Voltage Rails

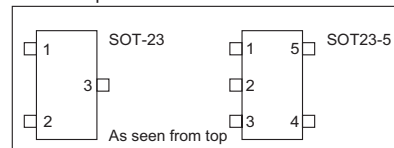
Power Plane	Description	Voltage	S0	S3	S4	S5
DCIN	Adapter power supply	19V	✓	✓	✓	✓
+VBATA	Battery power	6-8.4V	✓	✓	✓	✓
+VCC_CORE	Core voltage for CPU	0.5-1.2V	✓	✗	✗	✗
+V1.05S	Chipset Power Rail	1.05V	✓	✗	✗	✗
+V0.9	0.9V Reserved for DDR2 SSTL Term and COMP	0.9V	✓	✓	✗	✗
+V1.8	DDR2 SM	1.8V	✓	✓	✗	✗
+V1.5S	Chipset Power Rail	1.5V	✓	✗	✗	✗
+V3.3A_KSC	For EC	3.3V	✓	✓	✓	✓
+V3.3A	Peripheral Circuit	3.3V	✓	✓	✓	✗
+V3.3S	Peripheral Circuit	3.3V	✓	✗	✗	✗
+V5A	Peripheral Circuit	5V	✓	✓	✓	✗
+V5S	Peripheral Circuit	5V	✓	✗	✗	✗
+V15A	3.3V and 5V power rail gate power	15V	✓	✓	✓	✗

✓ ON  
✗ OFF

## Net Naming Conventions

Suffix
# = Active Low Signal
Prefix
H = Host M = DDR Memory TP = Test Point (does not connect anywhere else)

## PCB Footprints



## I<sup>2</sup>C / SMB Addresses

Device	Address	Hex	Bus
Clock Generator	1101 001x	D2	SMB_ICH_S
SO-DIMM0	1010 000x	A0	SMB_ICH_S
PCIE Mini Slot	TBD	TBD	SMB_ICH_A
CPU Thermal Sensor	1001 100x	98	SMB_EC_S
Battery	TBD	TBD	SMB_EC_A
TPM Header	TBD	TBD	SMB_ICH_S
XDP	TBD	TBD	SMB_GMS_S

## Jumper Settings

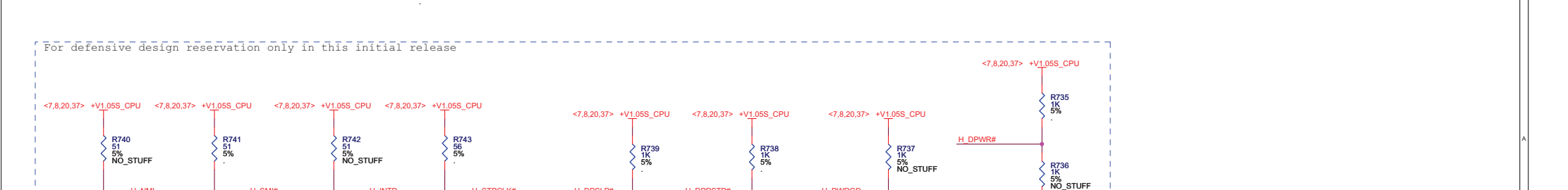
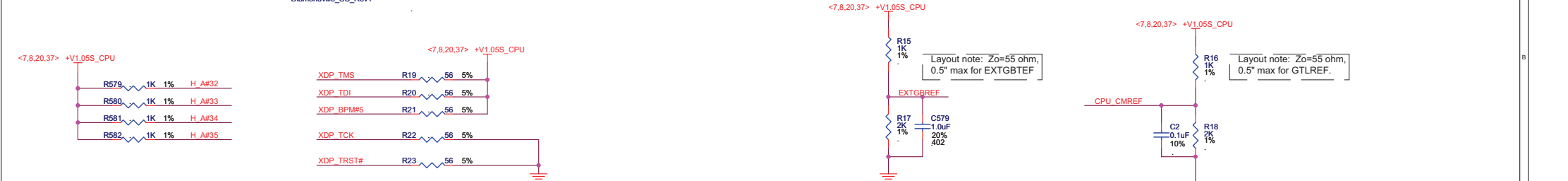
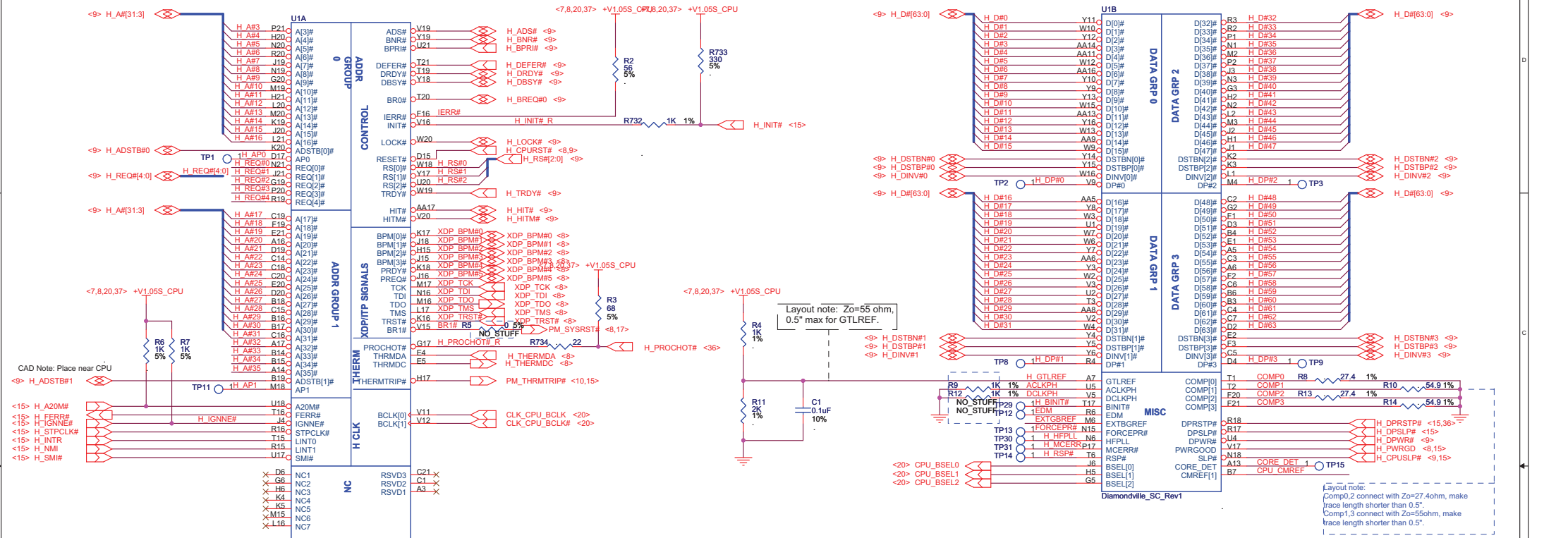
Jumper	Default	Description
PG1	Open	+V3.3S to LCD VDD
PG2	Short	DC IN
PG3	Short	DC IN
PG4	Short	+V3.3A Source
PG5	Short	+V3.3A Source
PG6	Short	+V5A Source
PG7	Short	+V5A Source
PG8	Short	+V1.05 Source(+V5A input)
PG9	Short	+V0.9 Source(+V1.8)
PG10	Open	+V0.9 Source(+V1.05S)
PG11	Short	+VCC_CORE Source(+VBAT)
PG12,PG15	Open	+VCC_CORE Source(+V5A)
PG13	Open	CMOS Clear
PG16,PG17	Open	Reserved for the Wimax card with PCI ECN Power input change
PG18	Short	For older version Mini card
PS1	Open	+V5S to LCD LED back light
PS2	Short	+VBAT to LCD CCFL Inverter
PS3	Short	+VBAT Input
PS4	Short	+VBAT Input
PS5	Short	+V3.3A Output
PS6	Short	+V5A Output
PS7	Short	+V1.05S Output
PS8	Short	+V1.5S Output
PS9	Short	+V1.8 Output
PS10	Short	+VCC_CORE Output
PS11	Short	+VCC_CORE Output
J35	All Open	CPU VID Selection
J37	1-x	Boot BIOS selection

## LEDs and Switches

LED	Page	Reference
VID0	37	CR30
VID1	37	CR31
VID2	37	CR32
VID3	37	CR33
VID4	37	CR34
VID5	37	CR35
VID6	37	CR36
Num Lock	30	CR13
Caps Lock	30	CR12
Power on	30	CR29
Battery full	30	CR11
Batter charging	30	CR11
HDD	30	CR14
WL	30	CR15

Switch	Description	Page
SW1	Power Button	31
SW2	Touchpad Left Button	31
SW3	Touchpad Right Button	31
U26	Lid SW	30

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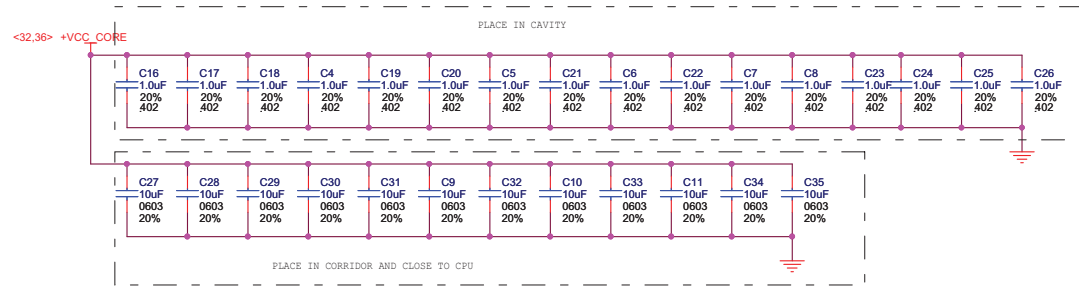
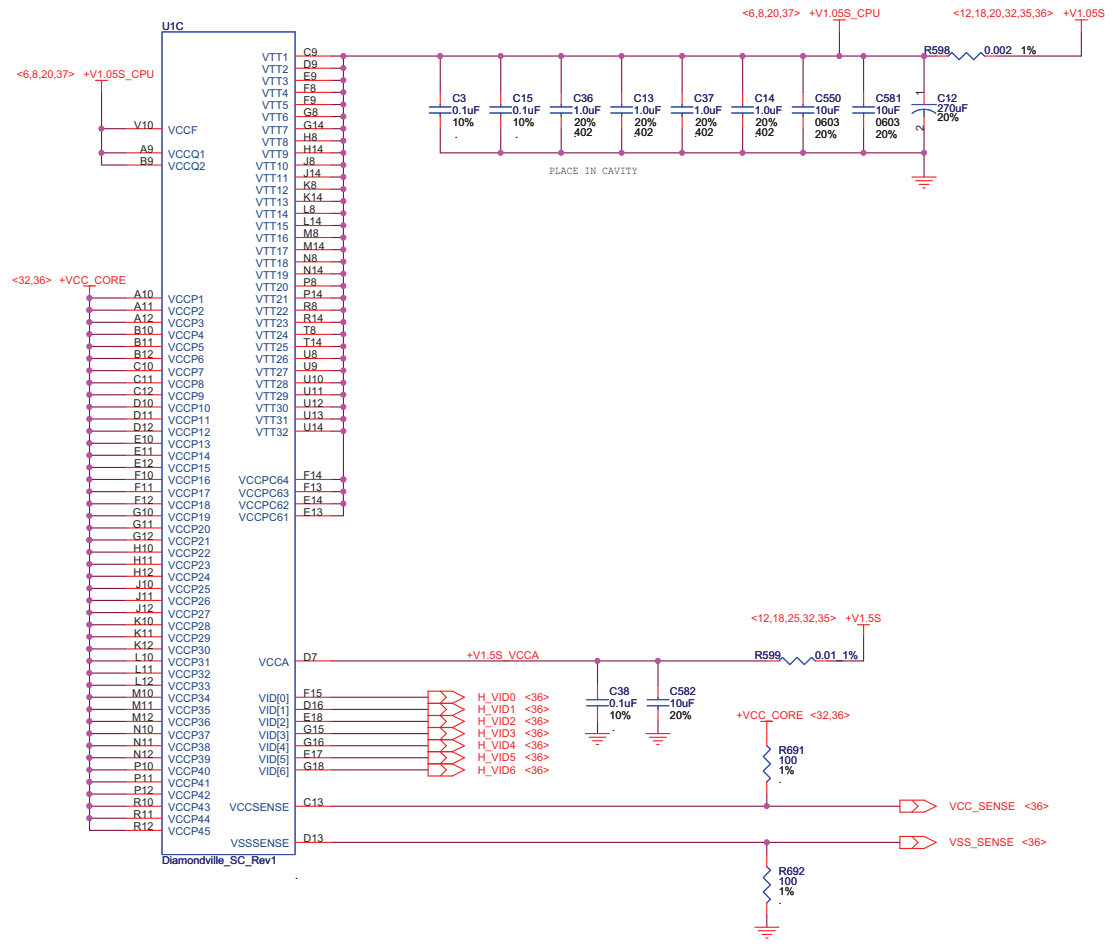


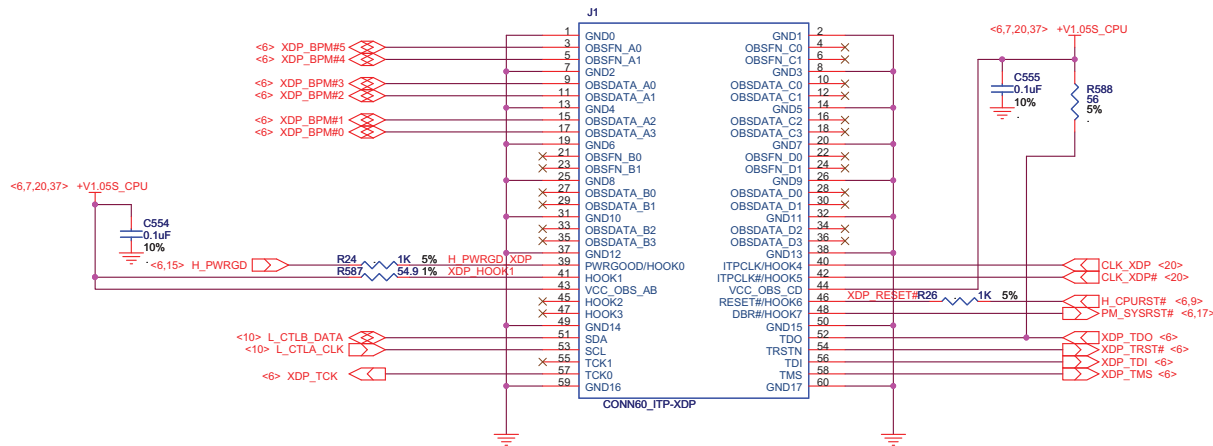
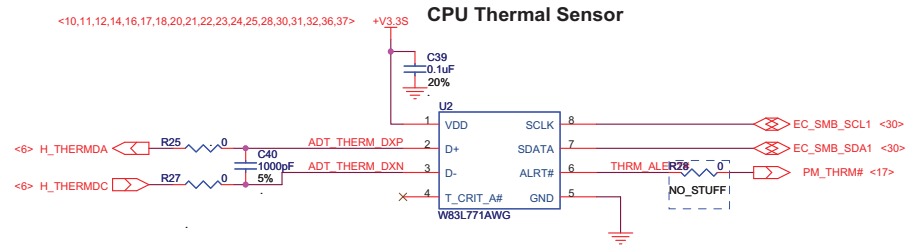
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A2	VSS1	VSS162
A4	VSS2	VSS161
A8	VSS4	VSS160
A15	VSS5	VSS159
A18	VSS6	VSS158
A19	VSS7	VSS157
A20	VSS8	VSS156
B1	VSS9	VSS155
B2	VSS10	VSS154
B5	VSS11	VSS153
B8	VSS12	VSS152
B13	VSS13	VSS151
B20	VSS14	VSS149
B21	VSS15	VSS148
C8	VSS16	VSS147
C17	VSS17	VSS146
D1	VSS18	VSS145
D5	VSS19	VSS144
D8	VSS20	VSS143
D14	VSS21	VSS142
D18	VSS22	VSS141
D21	VSS23	VSS140
E3	VSS24	VSS139
E6	VSS25	VSS138
E7	VSS26	VSS137
E8	VSS27	VSS136
E15	VSS28	VSS135
E16	VSS29	VSS134
E19	VSS30	VSS133
F4	VSS31	VSS132
F5	VSS32	VSS131
F6	VSS33	VSS130
F7	VSS34	VSS129
F17	VSS35	VSS128
F18	VSS36	VSS127
G1	VSS37	VSS126
G4	VSS38	VSS125
G7	VSS39	VSS124
G9	VSS41	VSS123
G13	VSS42	VSS122
G21	VSS45	VSS121
H3	VSS46	VSS120
H4	VSS48	VSS119
H7	VSS49	VSS118
H9	VSS51	VSS117
H13	VSS52	VSS116
H16	VSS53	VSS115
H18	VSS54	VSS114
H19	VSS55	VSS113
J5	VSS56	VSS112
J7	VSS57	VSS111
J9	VSS58	VSS110
J13	VSS59	VSS109
J17	VSS60	VSS108
K1	VSS61	VSS107
K6	VSS62	VSS106
K7	VSS63	VSS105
K9	VSS64	VSS104
K13	VSS65	VSS103
K15	VSS66	VSS102
K21	VSS67	VSS101
L3	VSS68	VSS100
L4	VSS69	VSS99
L5	VSS70	VSS98
L6	VSS71	VSS97
L7	VSS72	VSS96
L9	VSS73	VSS95
L13	VSS74	VSS94
L15	VSS75	VSS93
L18	VSS76	VSS92
L19	VSS77	VSS91
M1	VSS78	VSS90
M5	VSS79	VSS89
M7	VSS80	VSS88
M9	VSS81	VSS87
M13	VSS82	VSS86
M21	VSS83	VSS85
N4	VSS84	VSS84

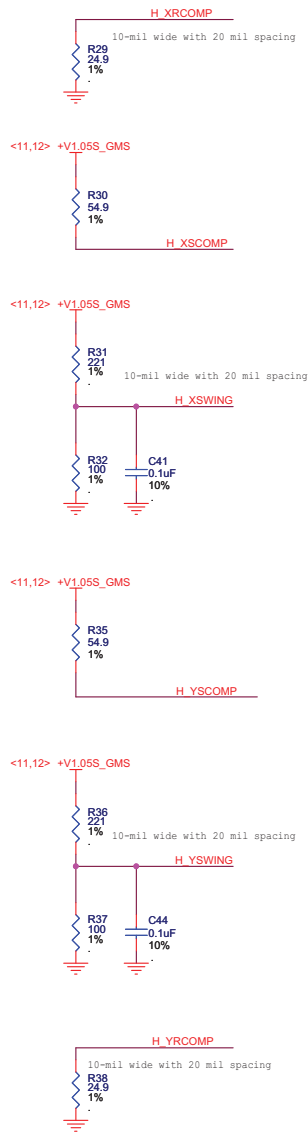
Diamondville\_SC\_Rev1

UIC		
VTT1	C9	
VTT2	D9	
VTT3	E9	
VTT4	F8	
VTT5	F9	
VTT6	G14	
VTT7	H8	
VTT8	H14	
VTT9	H14	
VTT10	J8	
VTT11	J14	
VTT12	K8	
VTT13	K14	
VTT14	L14	
VTT15	M8	
VTT16	M14	
VTT17	M14	
VTT18	N8	
VTT19	N14	
VTT20	P8	
VTT21	P14	
VTT22	R8	
VTT23	R14	
VTT24	T8	
VTT25	T14	
VTT26	U8	
VTT27	U9	
VTT28	U11	
VTT29	U10	
VTT30	U12	
VTT31	U13	
VTT32	U14	
VCCP1	A10	
VCCP2	A11	
VCCP3	A12	
VCCP4	B10	
VCCP5	B11	
VCCP6	B12	
VCCP7	C10	
VCCP8	C11	
VCCP9	C12	
VCCP10	D10	
VCCP11	D11	
VCCP12	D12	
VCCP13	E10	
VCCP14	E11	
VCCP15	E12	
VCCP16	F10	
VCCP17	F11	
VCCP18	F12	
VCCP19	G10	
VCCP20	G11	
VCCP21	G12	
VCCP22	H10	
VCCP23	H11	
VCCP24	H12	
VCCP25	J10	
VCCP26	J11	
VCCP27	J12	
VCCP28	K10	
VCCP29	K11	
VCCP30	K12	
VCCP31	L10	
VCCP32	L11	
VCCP33	L12	
VCCP34	M10	
VCCP35	M11	
VCCP36	M12	
VCCP37	N10	
VCCP38	N11	
VCCP39	N12	
VCCP40	P10	
VCCP41	P11	
VCCP42	P12	
VCCP43	R10	
VCCP44	R11	
VCCP45	R12	
VCCP84	F14	
VCCP83	F13	
VCCP82	E14	
VCCP81	E13	
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VCCQ2	B9	
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VCCP2	A11	
VCCP3	A12	
VCCP4	B10	
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VCCP6	B12	
VCCP7	C10	
VCCP8	C11	
VCCP9	C12	
VCCP10	D10	
VCCP11	D11	
VCCP12	D12	
VCCP13	E10	
VCCP14	E11	
VCCP15	E12	
VCCP16	F10	
VCCP17	F11	
VCCP18	F12	
VCCP19	G10	
VCCP20	G11	
VCCP21	G12	
VCCP22	H10	
VCCP23	H11	
VCCP24	H12	
VCCP25	J10	
VCCP26	J11	
VCCP27	J12	
VCCP28	K10	
VCCP29	K11	
VCCP30	K12	
VCCP31	L10	
VCCP32	L11	
VCCP33	L12	
VCCP34	M10	
VCCP35	M11	
VCCP36	M12	
VCCP37	N10	
VCCP38	N11	
VCCP39	N12	
VCCP40	P10	
VCCP41	P11	
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VCCP44	R11	
VCCP45	R12	

Diamondville\_SC\_Rev1







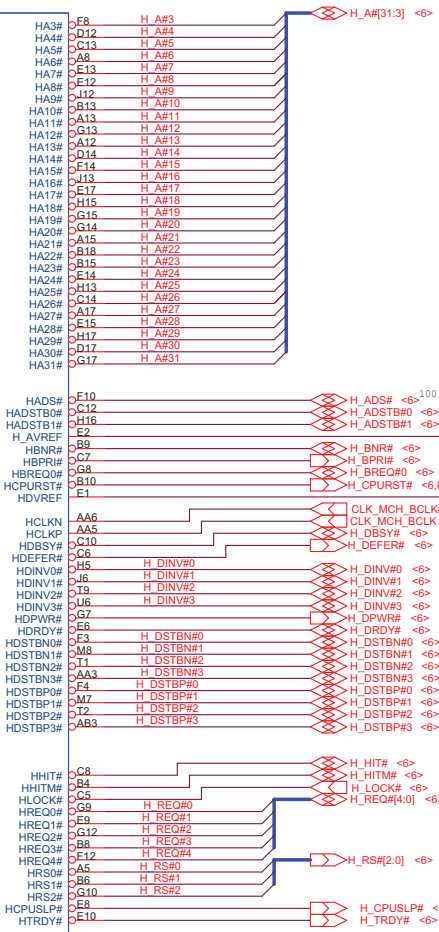
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H D#1	F6	HD1#
H D#2	H9	HD2#
H D#3	H6	HD3#
H D#4	E7	HD4#
H D#5	E3	HD5#
H D#6	C3	HD6#
H D#7	K9	HD7#
H D#8	F5	HD8#
H D#9	J7	HD9#
H D#10	K7	HD10#
H D#11	H8	HD11#
H D#12	E5	HD12#
H D#13	K8	HD13#
H D#14	J8	HD14#
H D#15	J2	HD15#
H D#16	J3	HD16#
H D#17	N1	HD17#
H D#18	M5	HD18#
H D#19	K5	HD19#
H D#20	J5	HD20#
H D#21	H3	HD21#
H D#22	N4	HD22#
H D#23	M4	HD23#
H D#24	M3	HD24#
H D#25	N6	HD25#
H D#26	K3	HD26#
H D#27	N9	HD27#
H D#28	M1	HD28#
H D#29	V8	HD29#
H D#30	V9	HD30#
H D#31	R6	HD31#
H D#32	T8	HD32#
H D#33	R2	HD33#
H D#34	N5	HD34#
H D#35	N2	HD35#
H D#36	R5	HD36#
H D#37	U7	HD37#
H D#38	R9	HD38#
H D#39	T4	HD39#
H D#40	T7	HD40#
H D#41	L5	HD41#
H D#42	L2	HD42#
H D#43	L3	HD43#
H D#44	L4	HD44#
H D#45	V6	HD45#
H D#46	V3	HD46#
H D#47	W2	HD47#
H D#48	W1	HD48#
H D#49	V2	HD49#
H D#50	W4	HD50#
H D#51	W7	HD51#
H D#52	W5	HD52#
H D#53	W6	HD53#
H D#54	V5	HD54#
H D#55	AB4	HD55#
H D#56	AB8	HD56#
H D#57	WA8	HD57#
H D#58	AA5	HD58#
H D#59	AA8	HD59#
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H D#62	AA2	HD62#
H D#63	AB5	HD63#

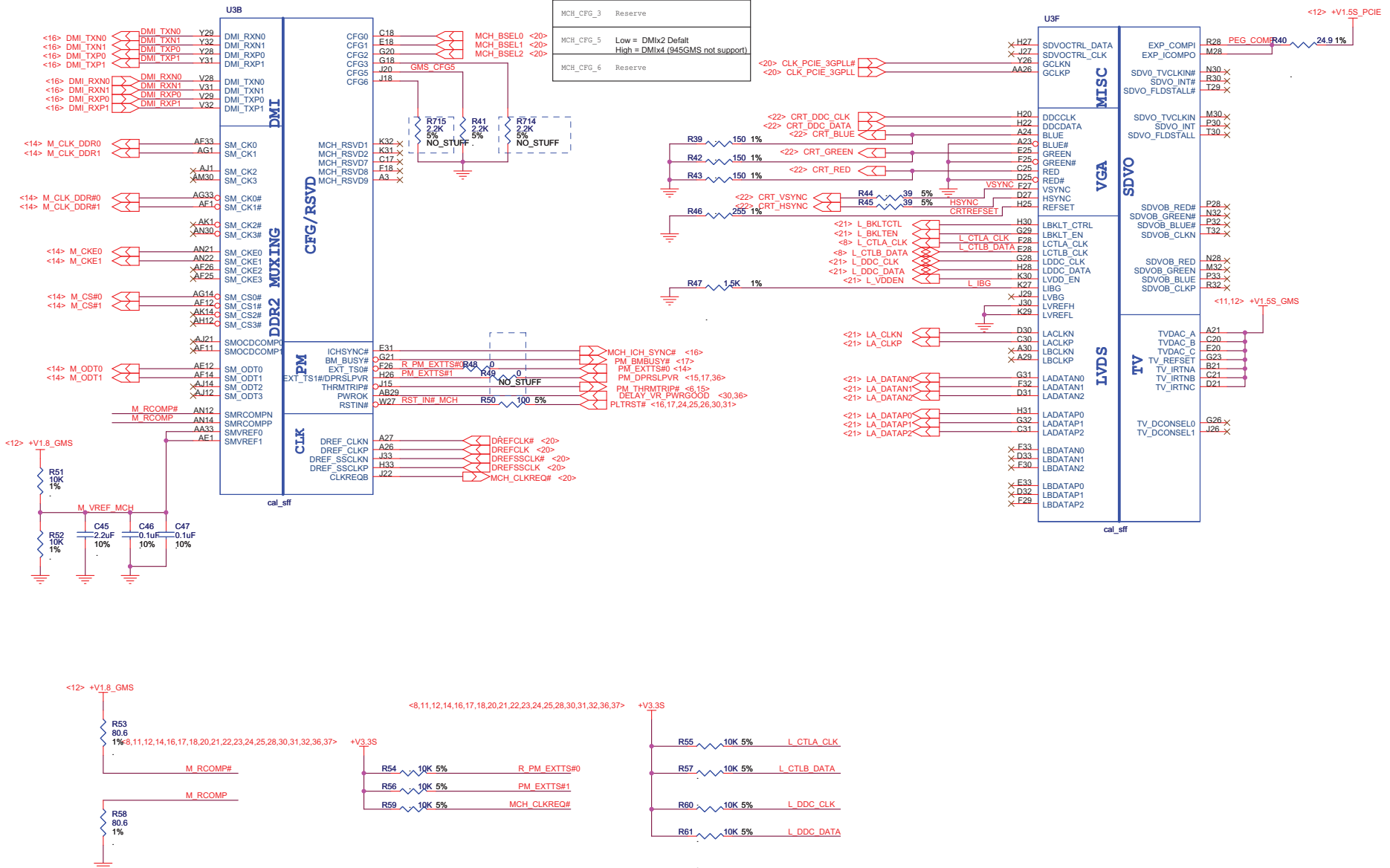
U3A

HOST

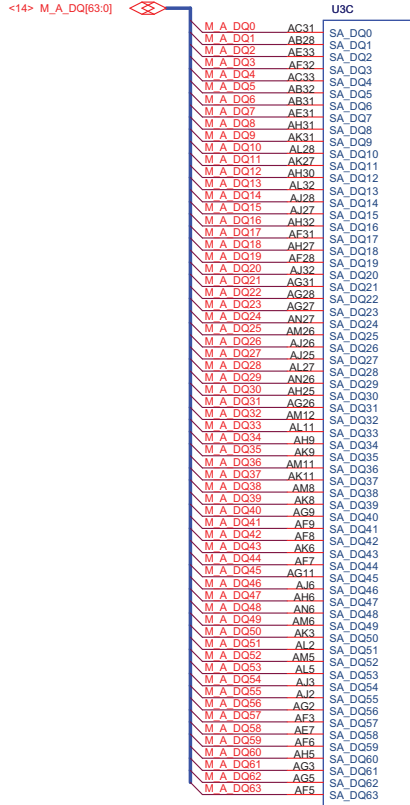
cal\_sff



Note: H\_CPURST# has T topology

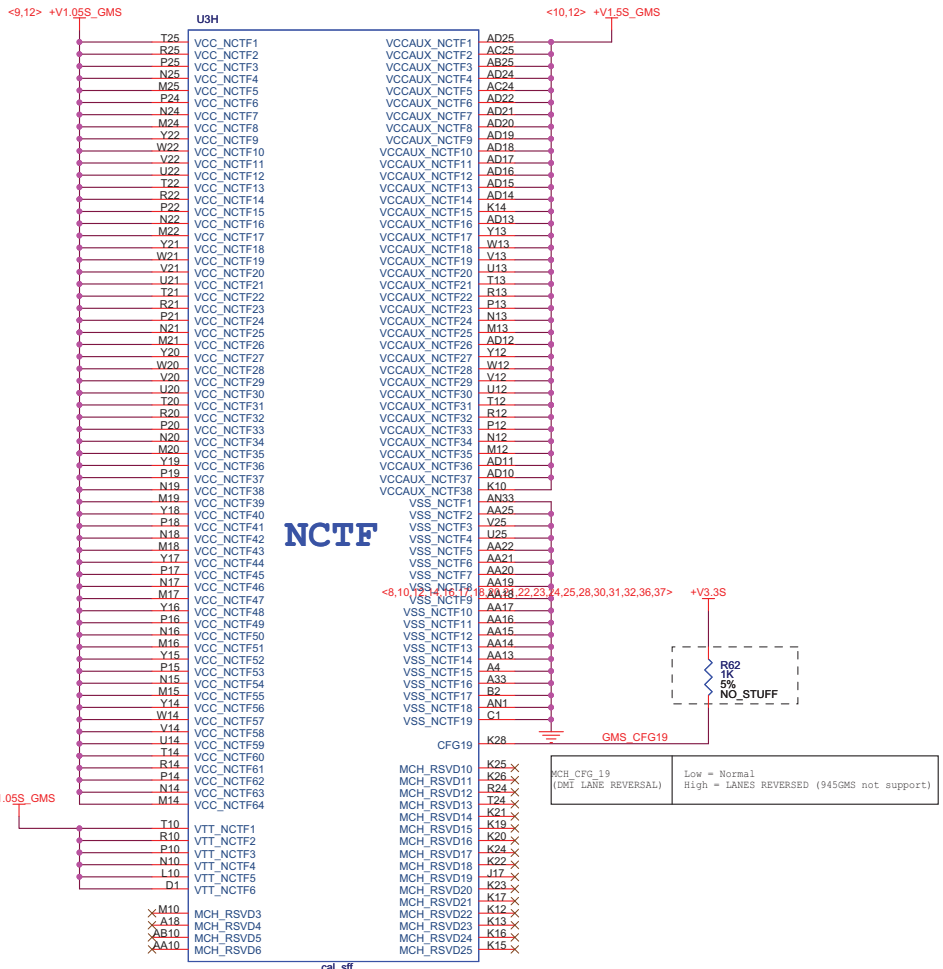






DDR2 SYSTEM MEMORY

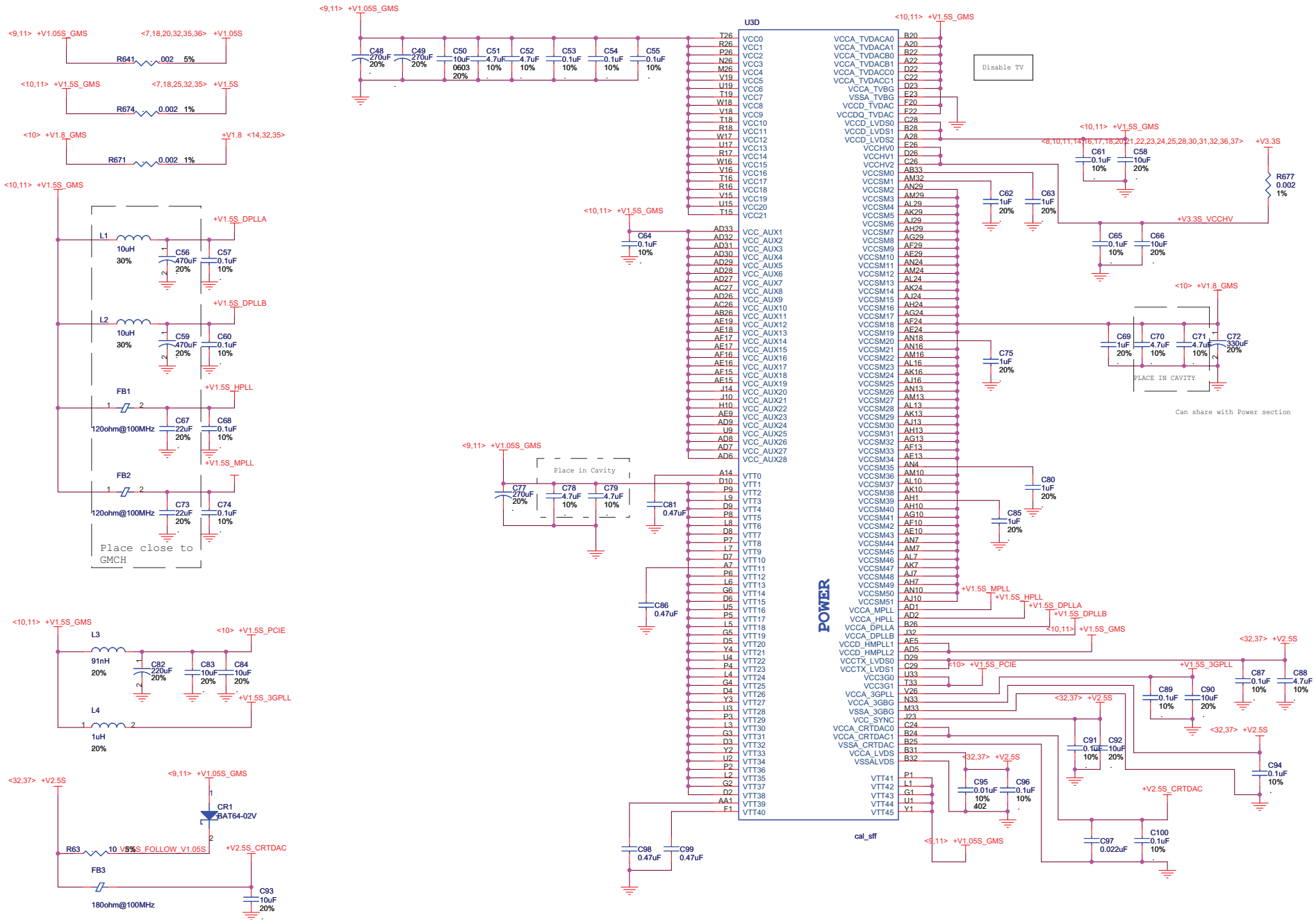
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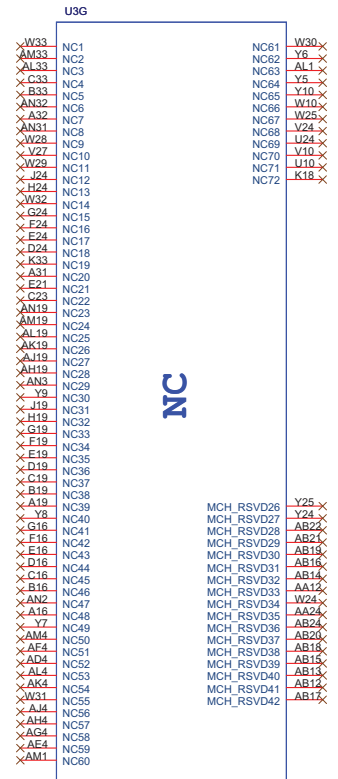
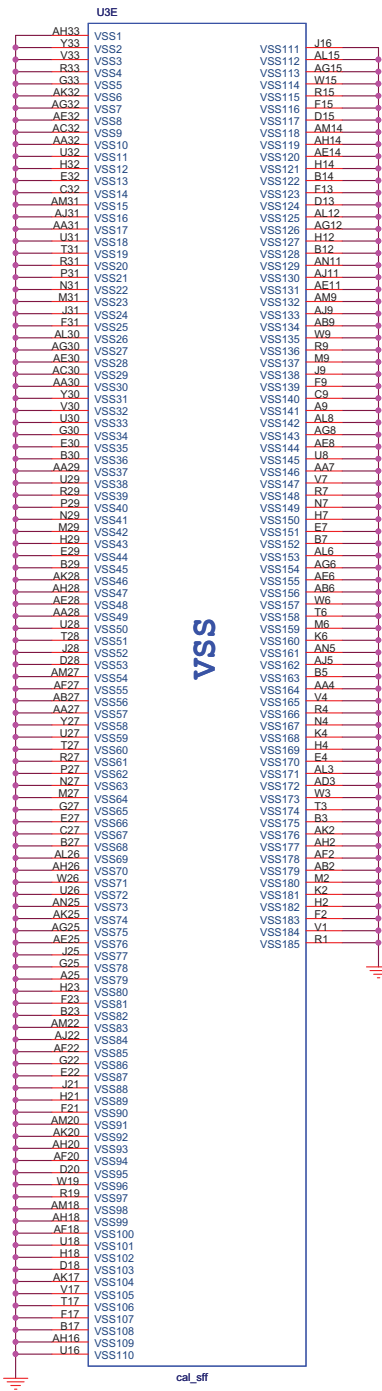


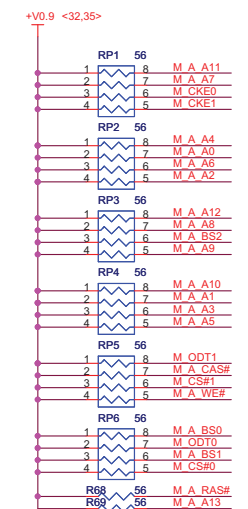
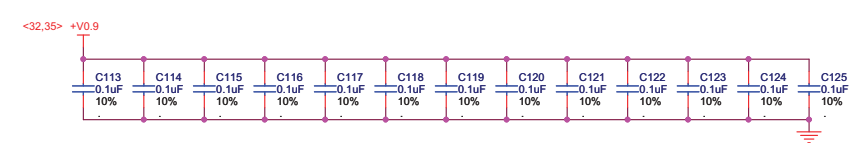
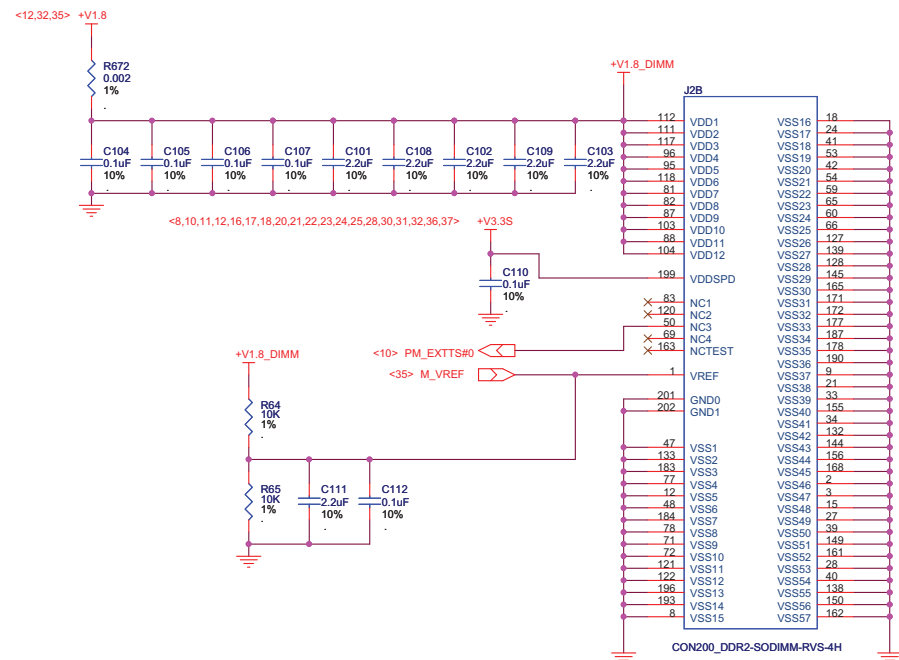
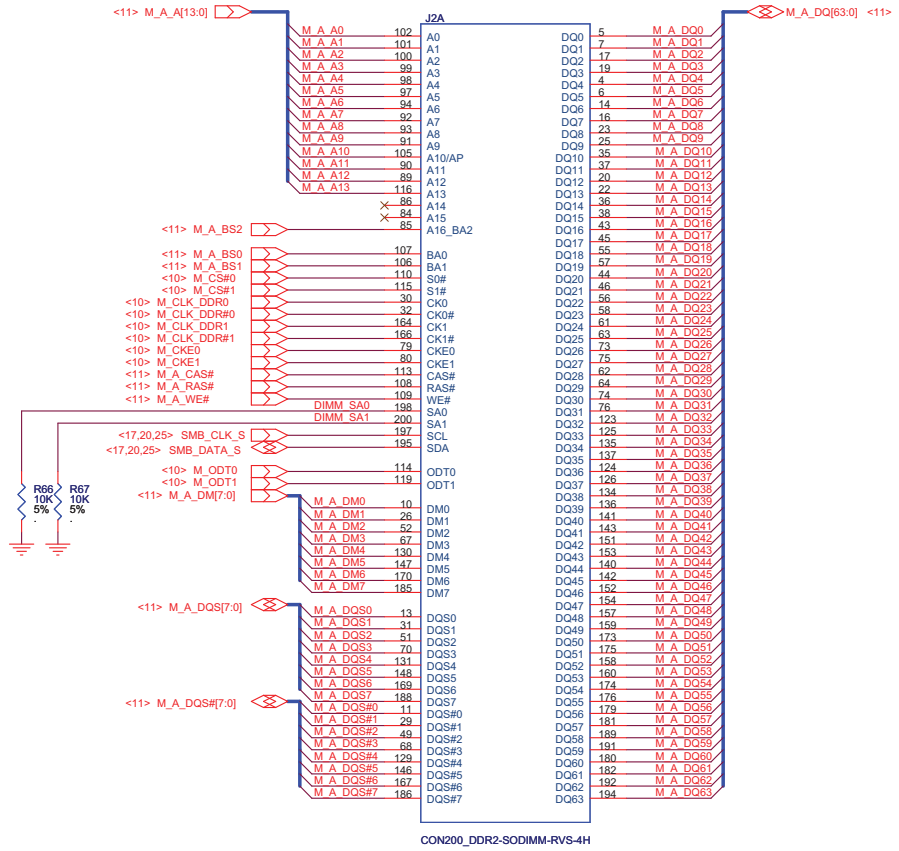
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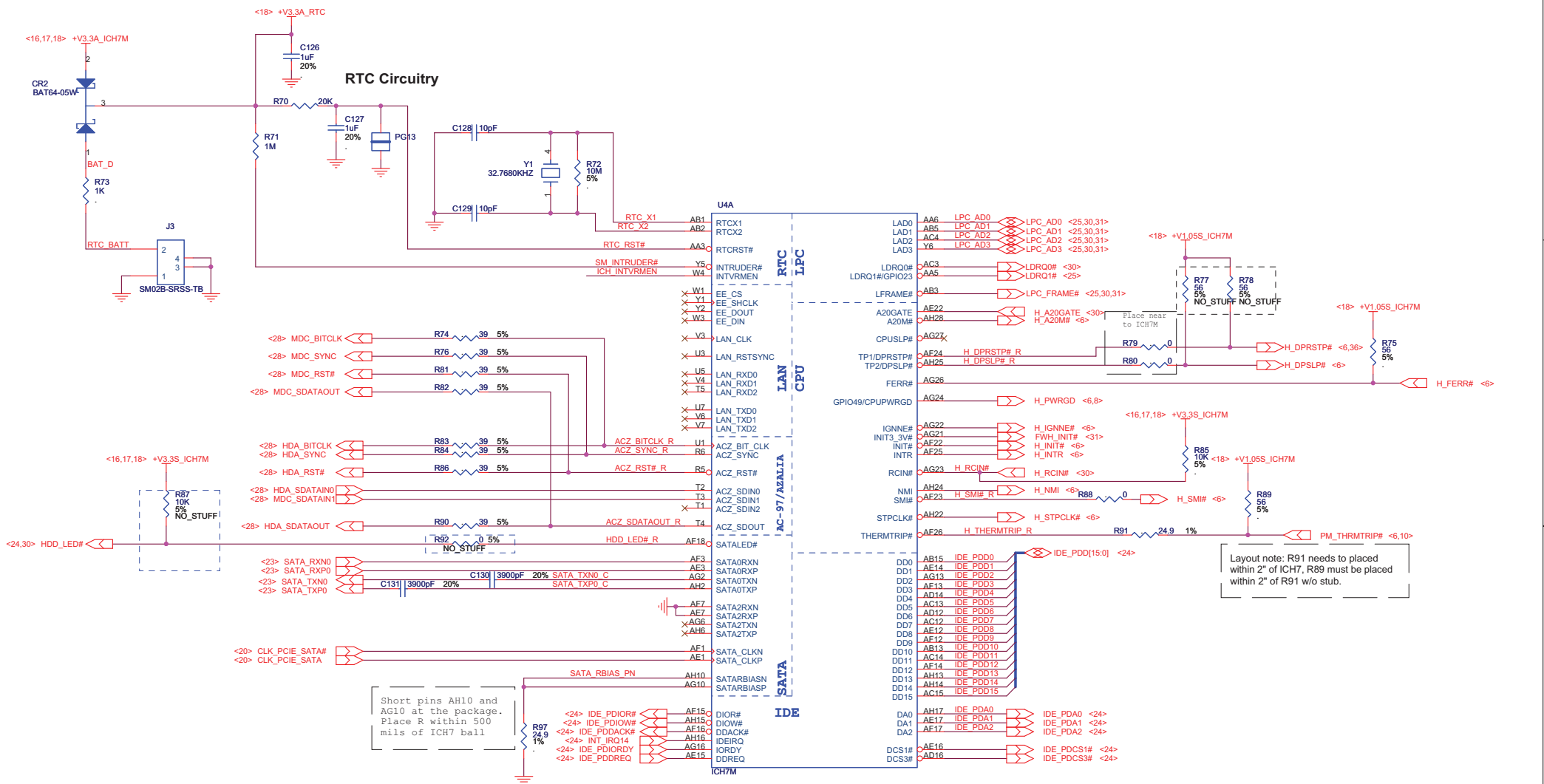
cal\_sff

MCH\_CFG19 (LOWE LAINE REVERSAL) Low = Normal High = LANE5 REVERSED (945GMS not support)

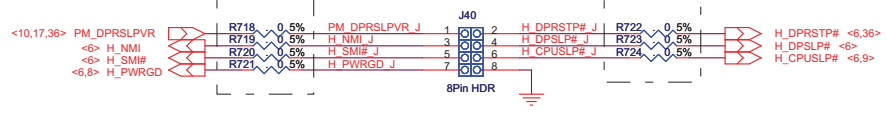
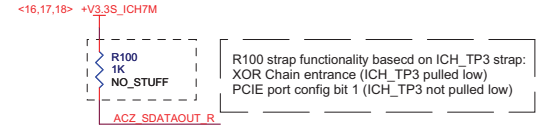
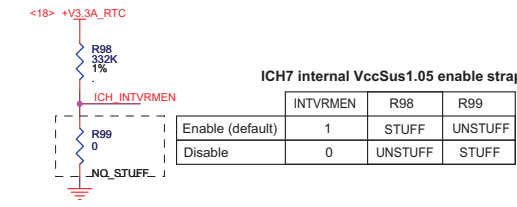


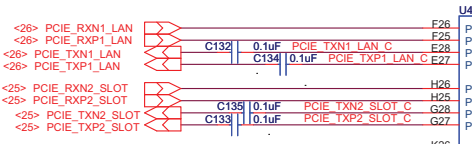
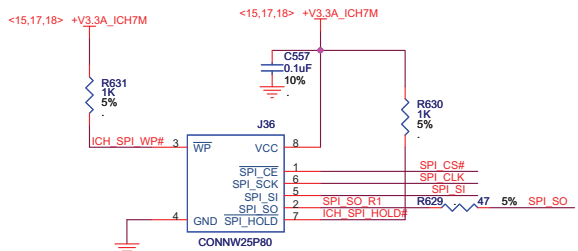




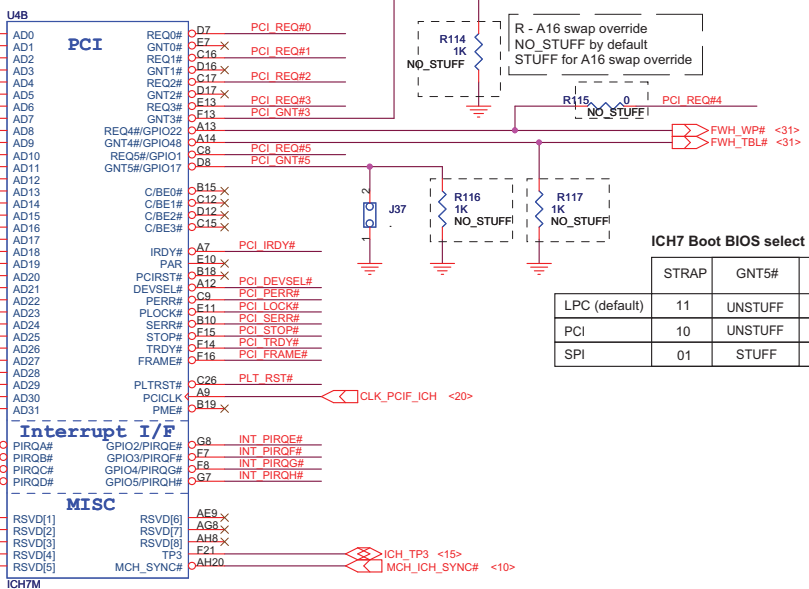
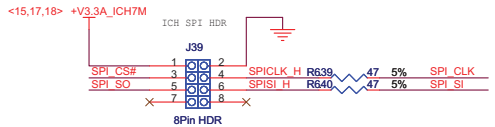
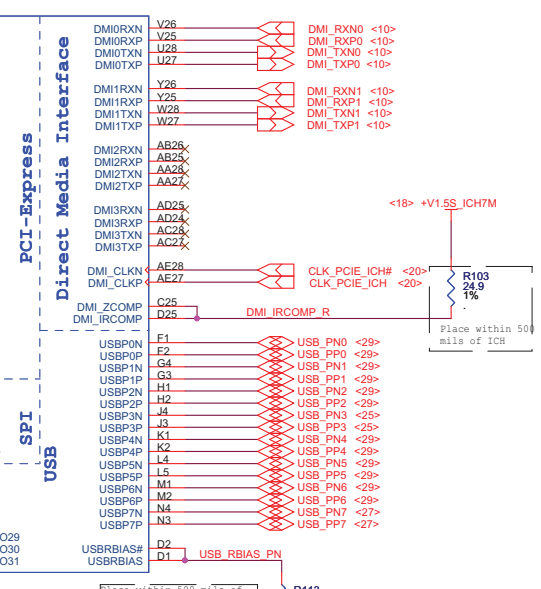
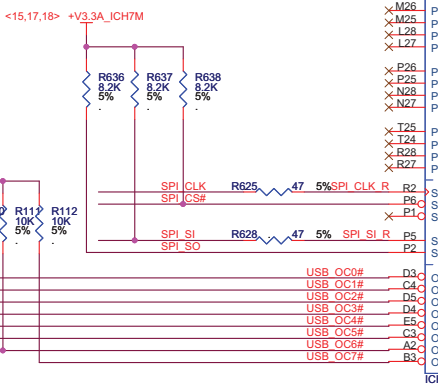


Layout note: R91 needs to be placed within 2" of ICH7, R89 must be placed within 2" of R91 w/o stub.



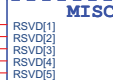
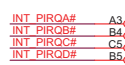
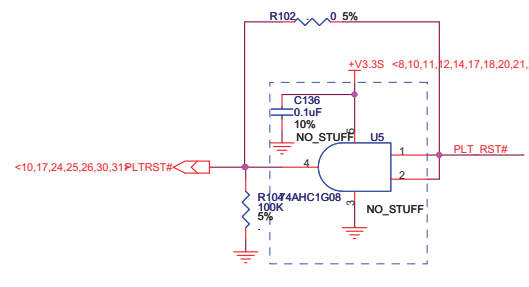
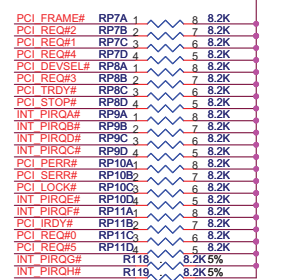


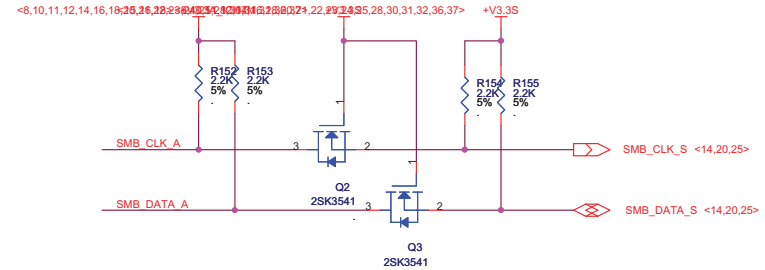
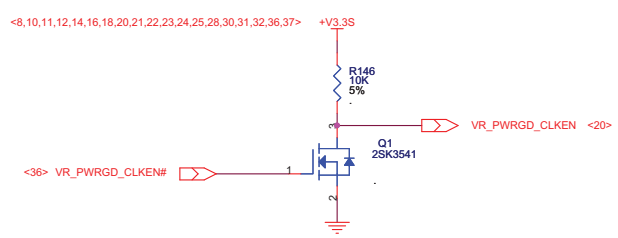
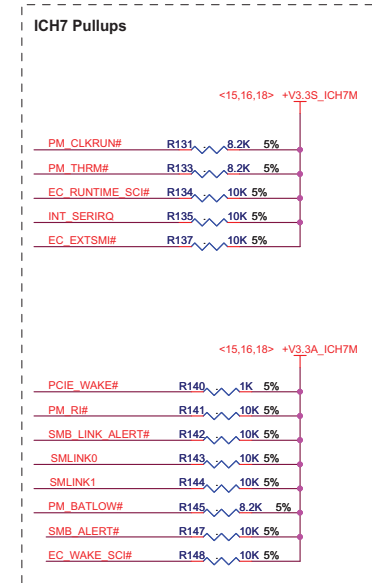
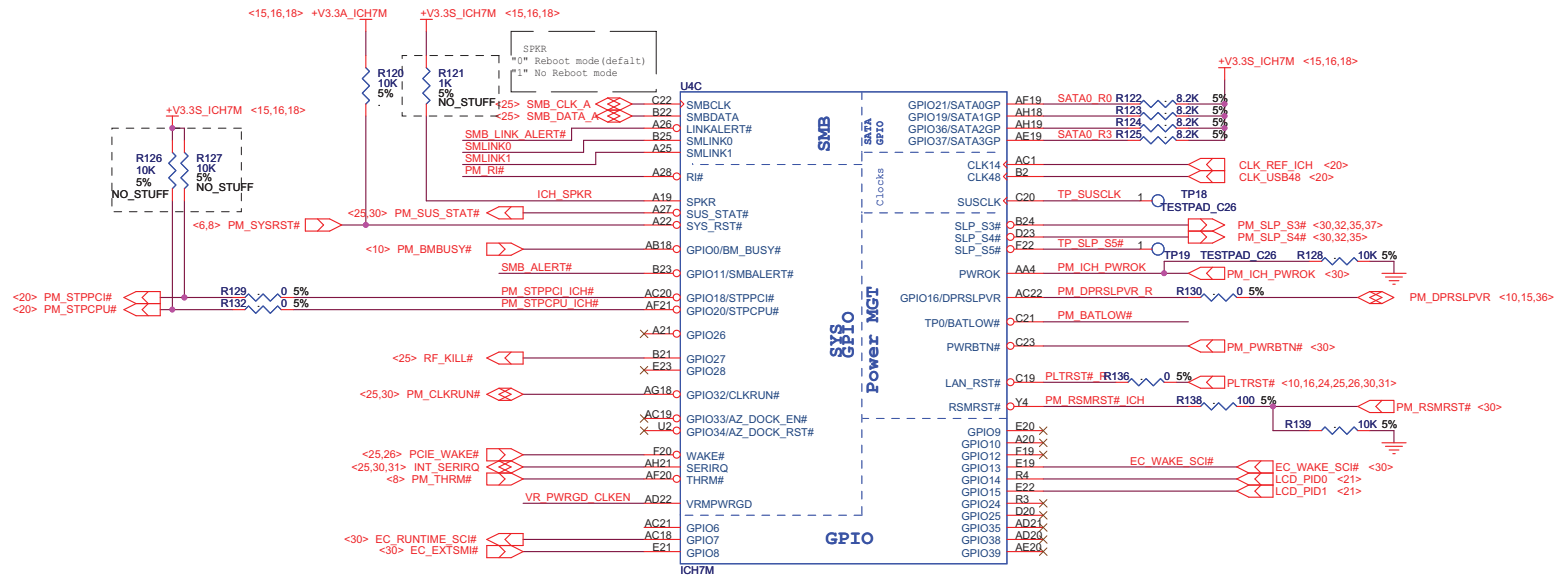
Layout note: PCIe AC coupling caps need to be within 250 mils of the driver.



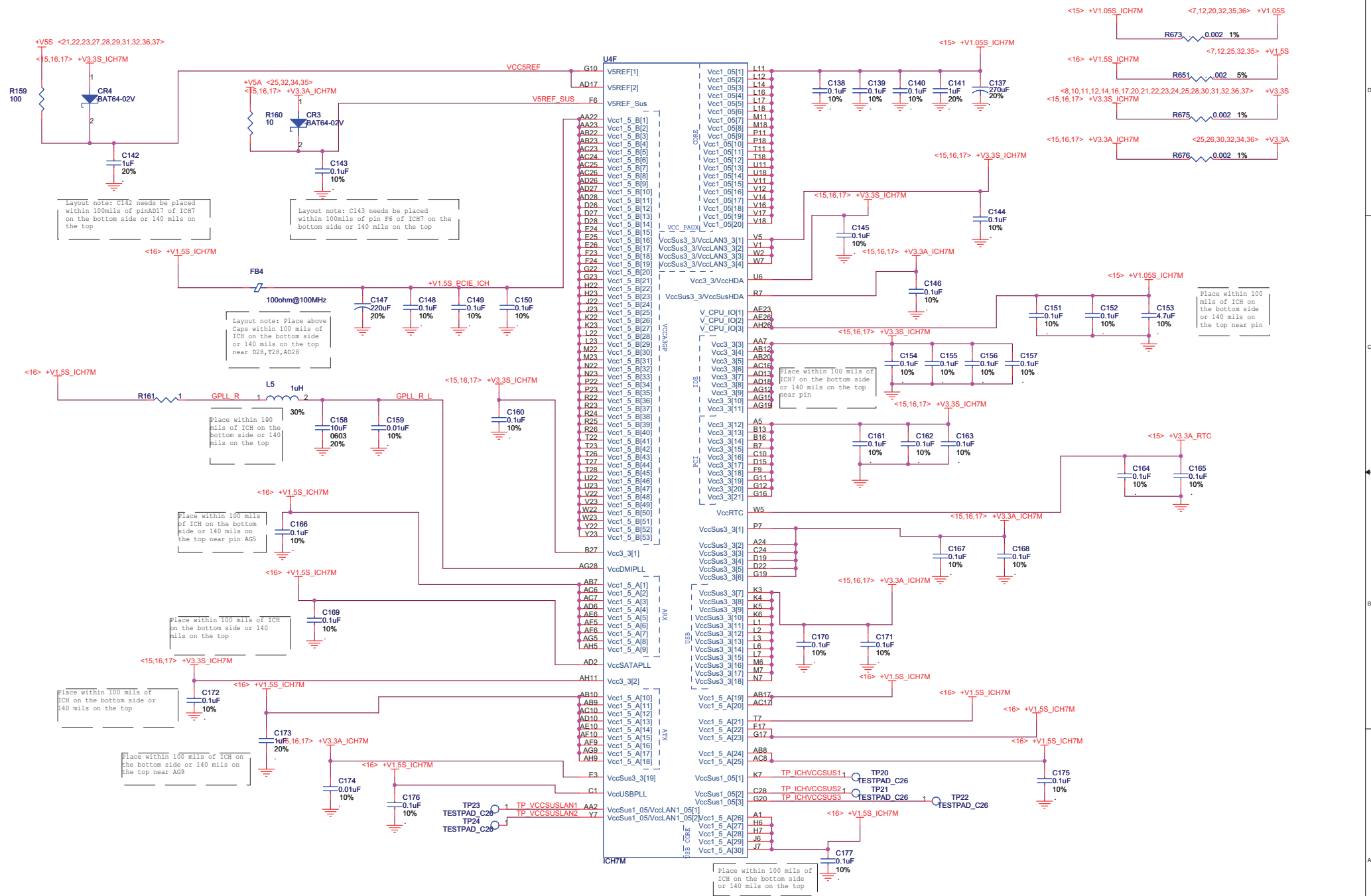
**ICH7 Boot BIOS select**

	STRAP	GNT5#	GNT4#
LPC (default)	11	UNSTUFF	UNSTUFF
PCI	10	UNSTUFF	STUFF
SPI	01	STUFF	UNSTUFF

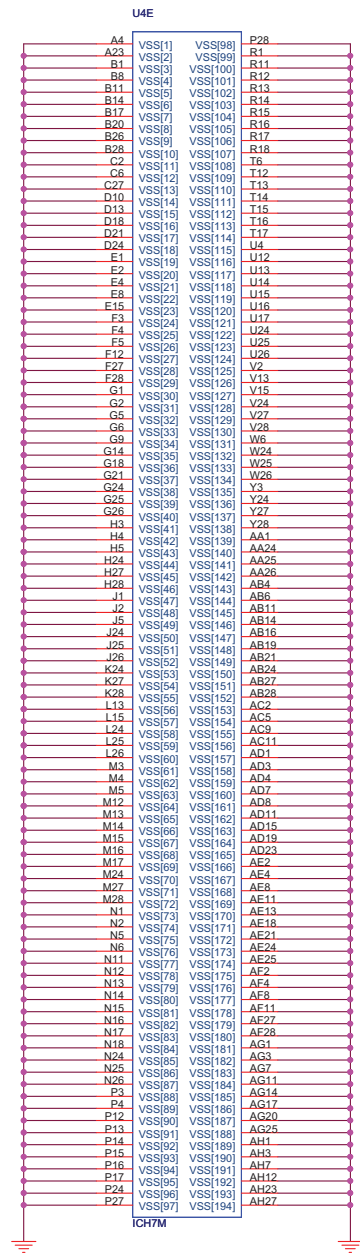


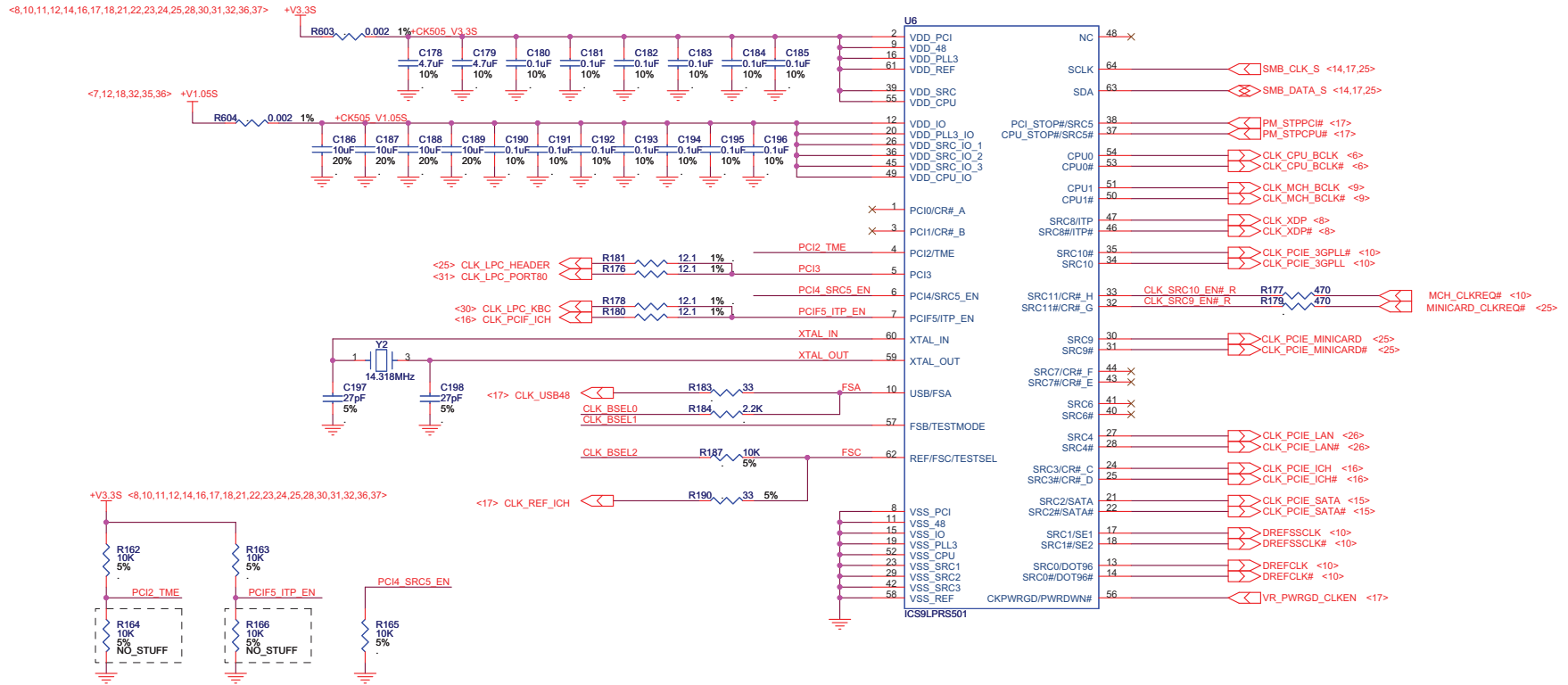






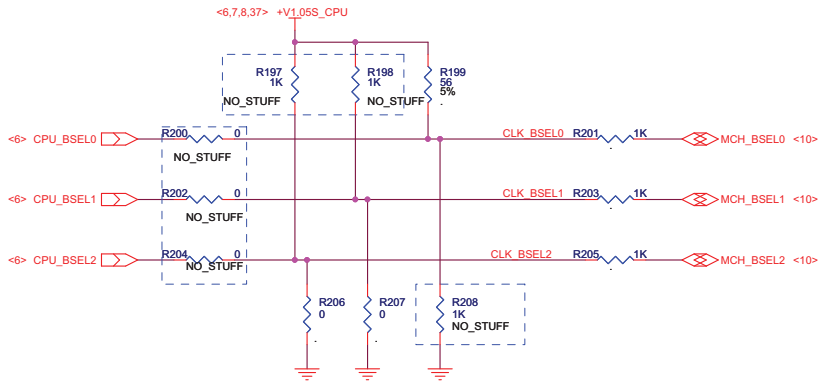


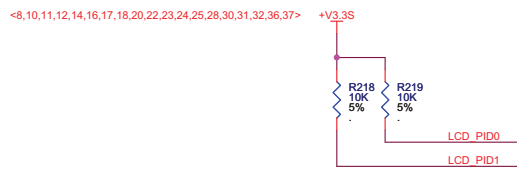
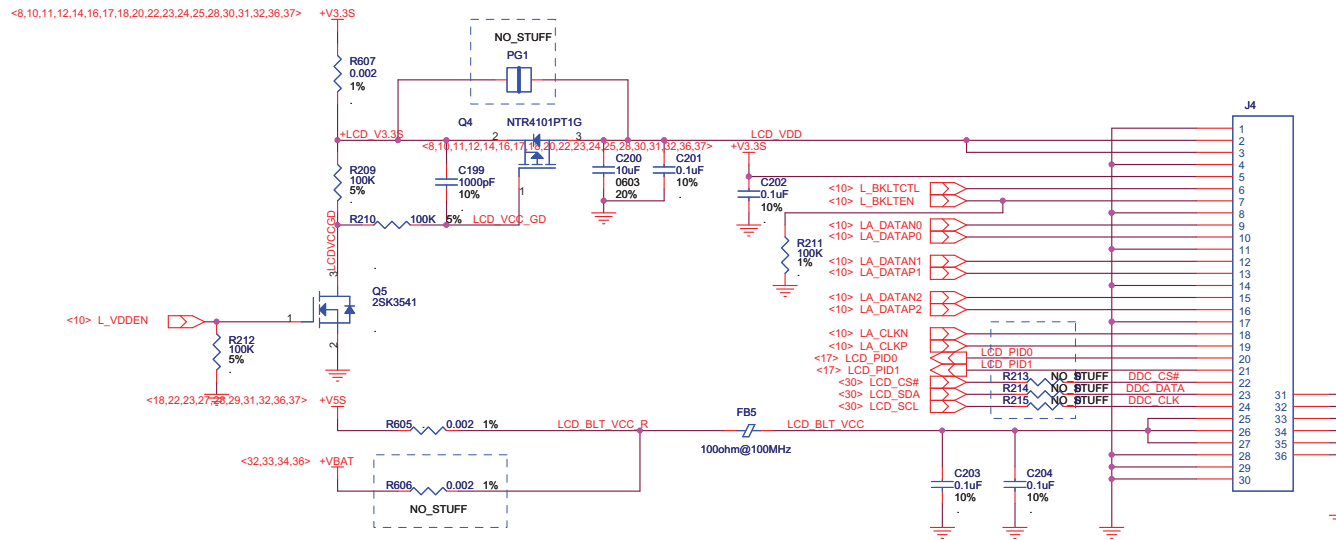




**CPU, MCH and XDP BCLK FREQUENCY SELECTION TABLE**

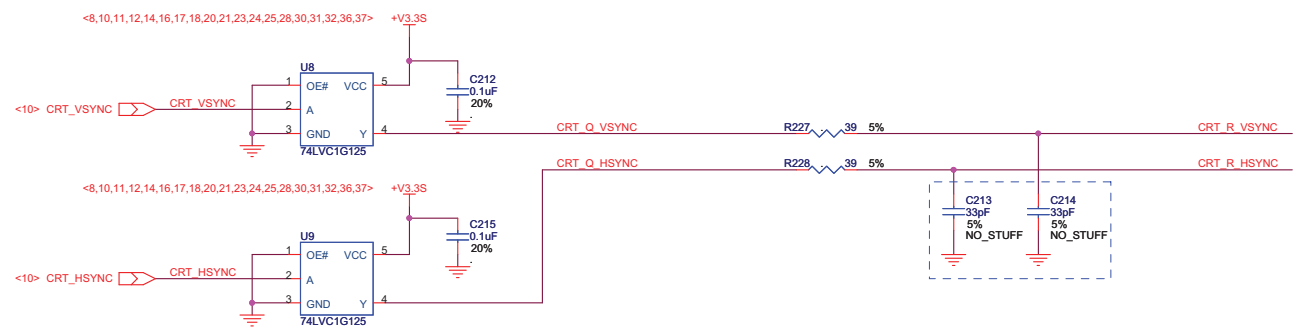
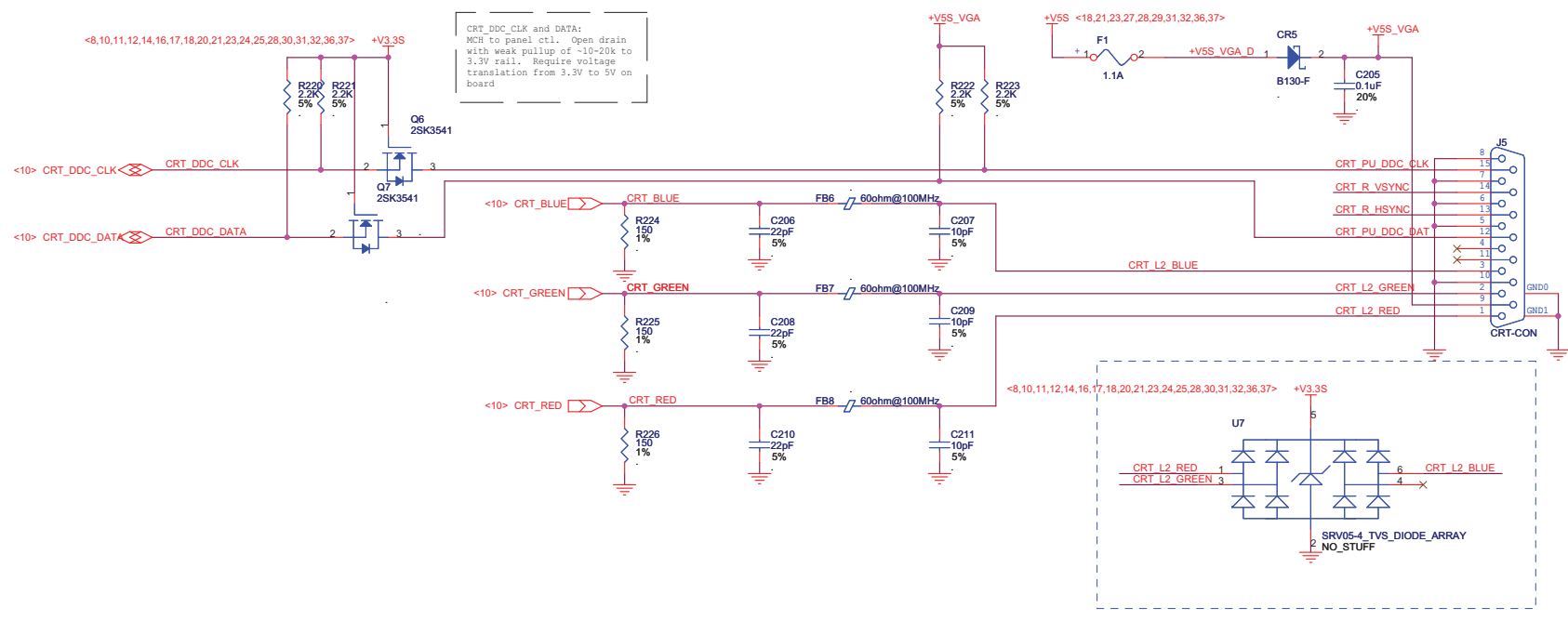
FSC	FSB	FSA	Host Clock frequency MHz
BSEL2	BSEL1	BSEL0	
1	0	1	100
0	0	1	133
0	1	1	166
0	1	0	200
0	0	0	266
1	0	0	333
1	1	0	400
1	1	1	Reserved

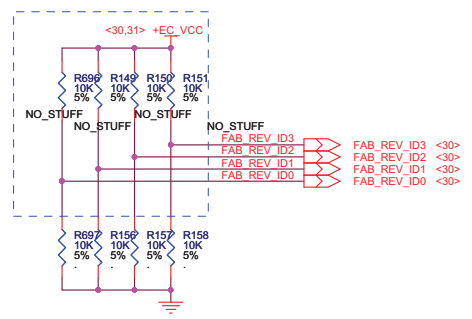
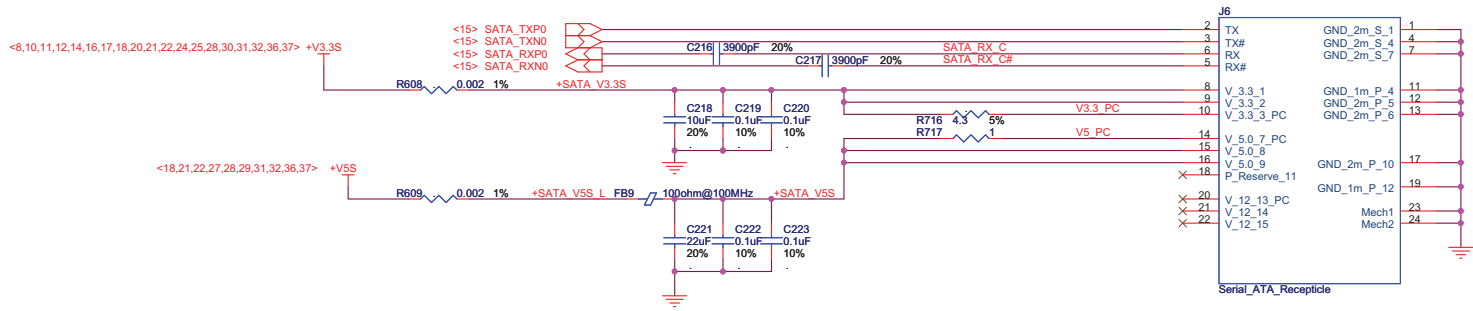




Panel ID Table

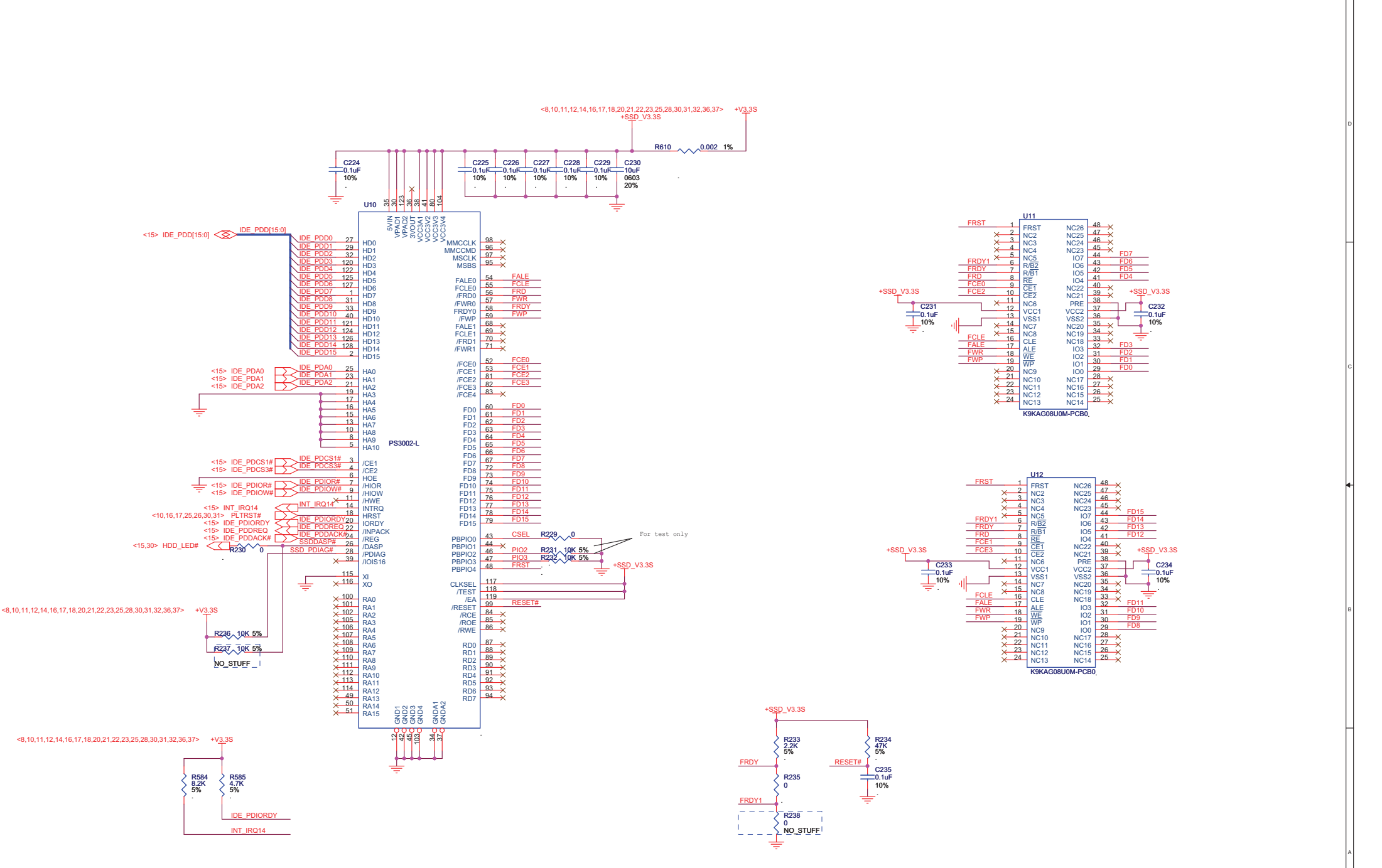
PID1	PID0	LCD Panel Type
0	0	Model A
0	1	Model B
1	0	Model C
1	1	Model D

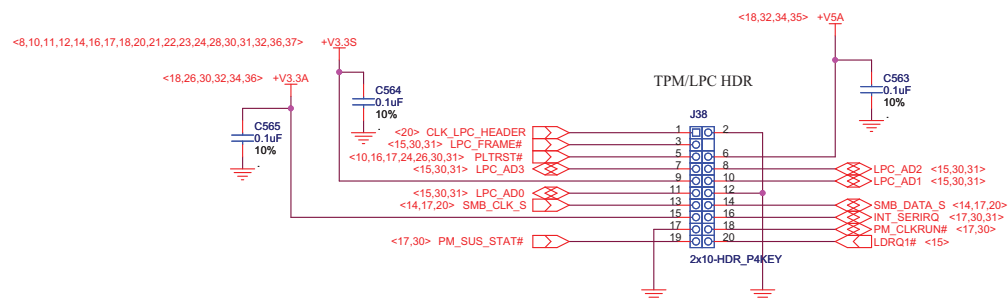
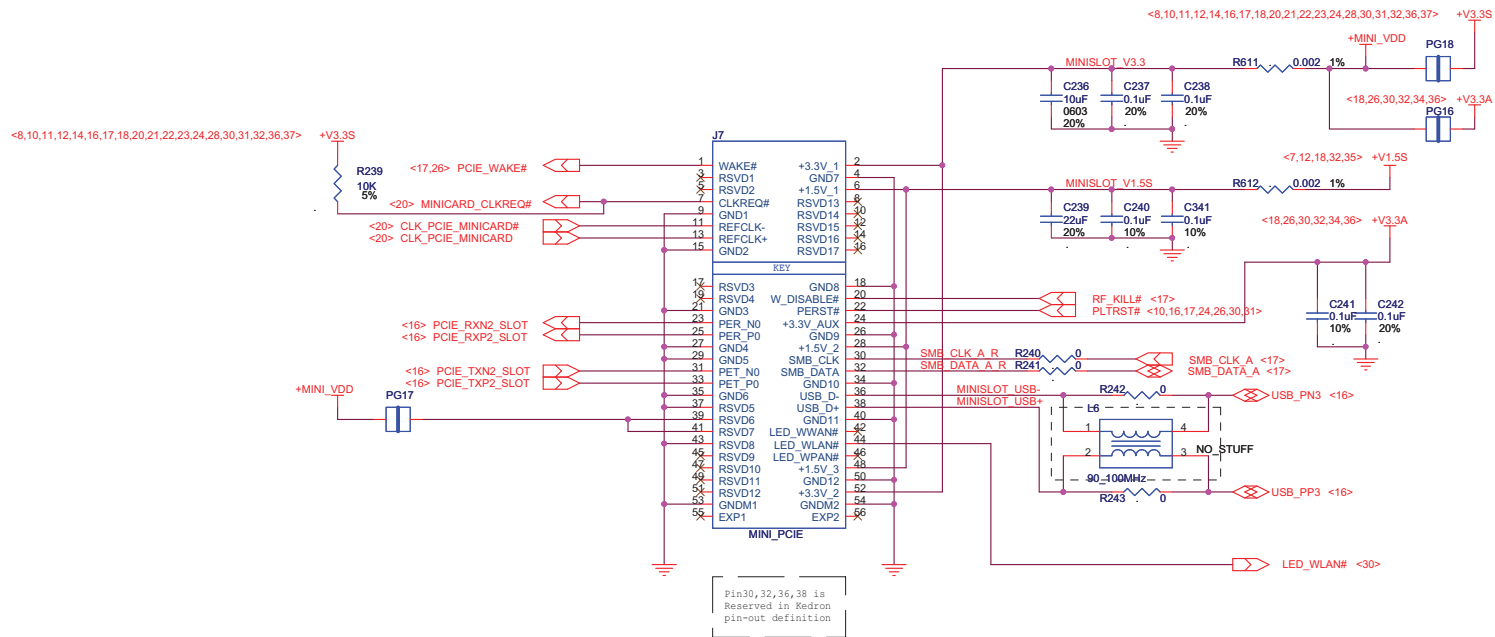


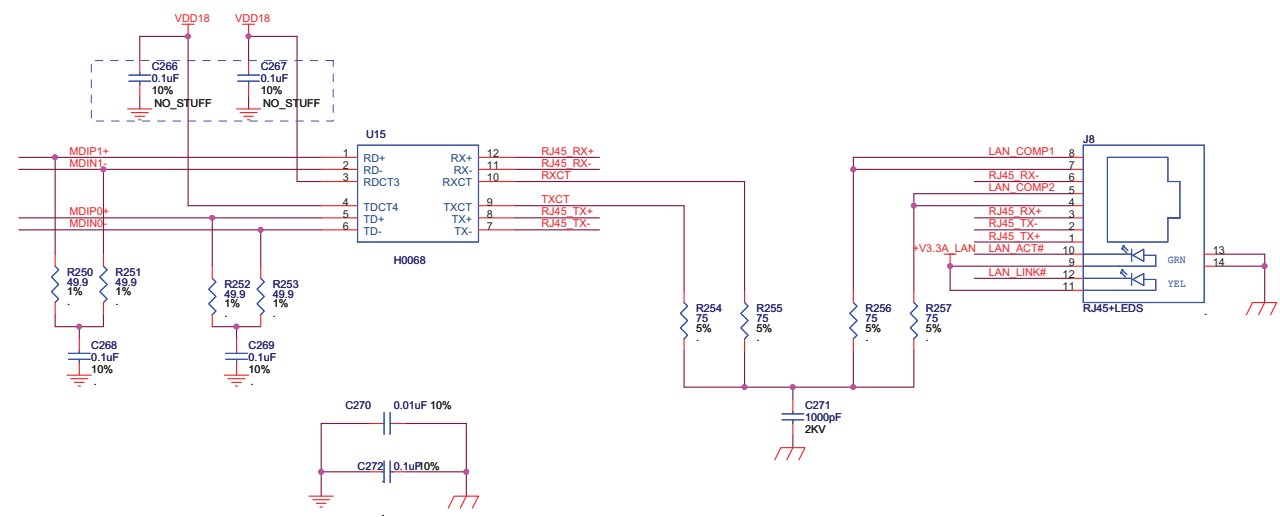
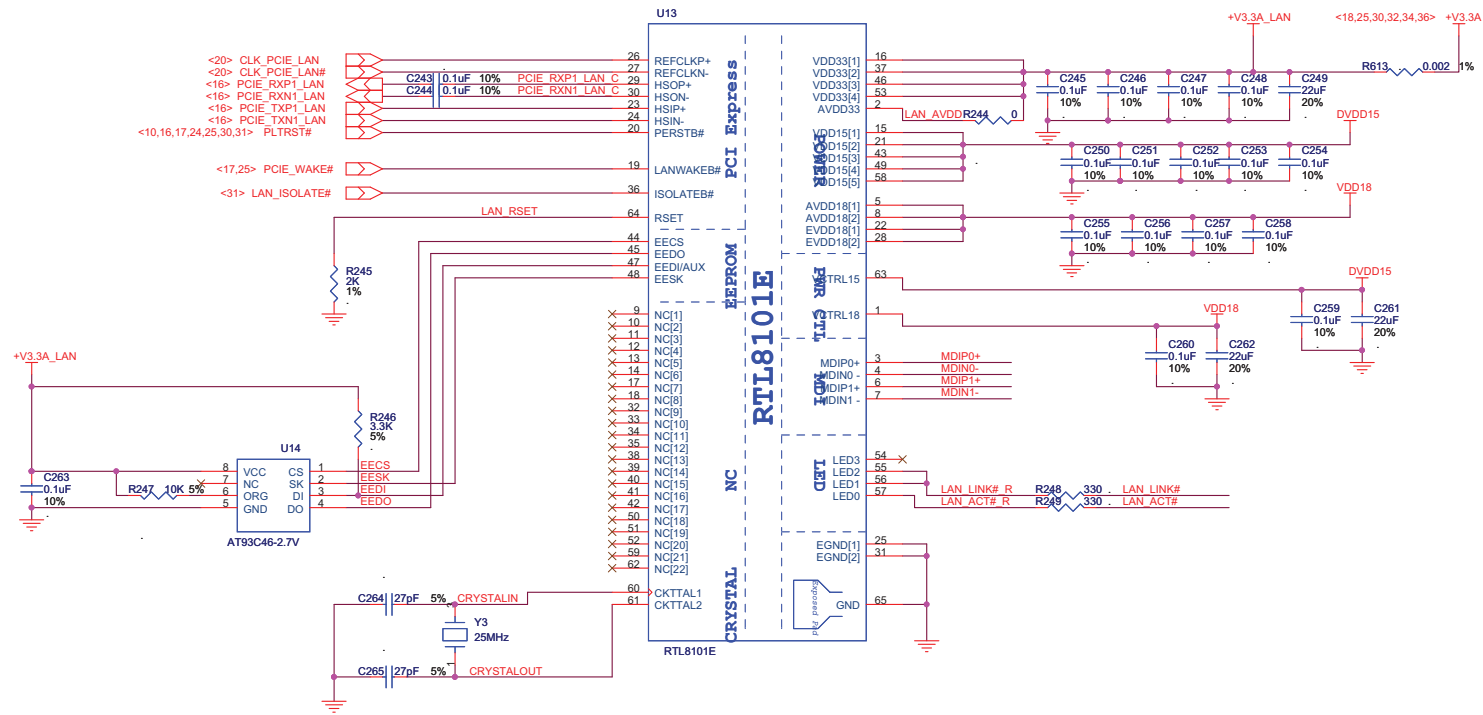


FAB ID Strapping Table

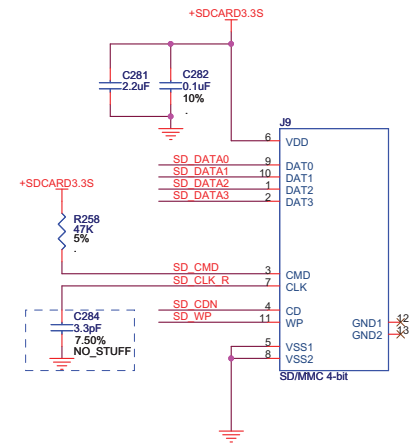
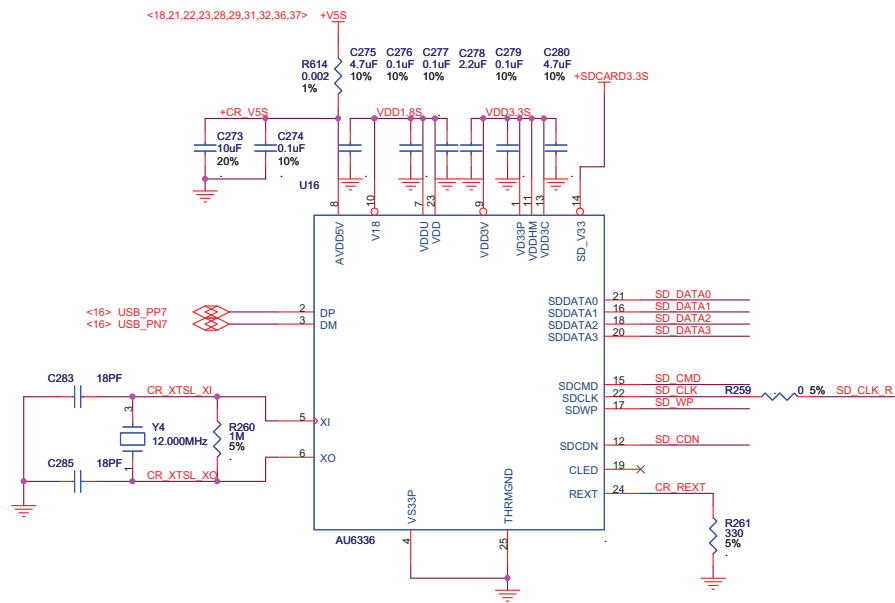
FAB REV ID				BOARD FAB
FAB_REV_ID3	FAB_REV_ID2	FAB_REV_ID1	FAB_REV_ID0	
0	0	0	0	1
0	0	0	1	2
0	0	1	0	3
0	0	1	1	4
0	1	0	0	5
0	1	0	1	6
0	1	1	0	7
0	1	1	1	8
1	0	0	0	9
1	0	0	1	10
1	0	1	0	11
1	0	1	1	12
1	1	0	0	13
1	1	0	1	14
1	1	1	0	15
1	1	1	1	16

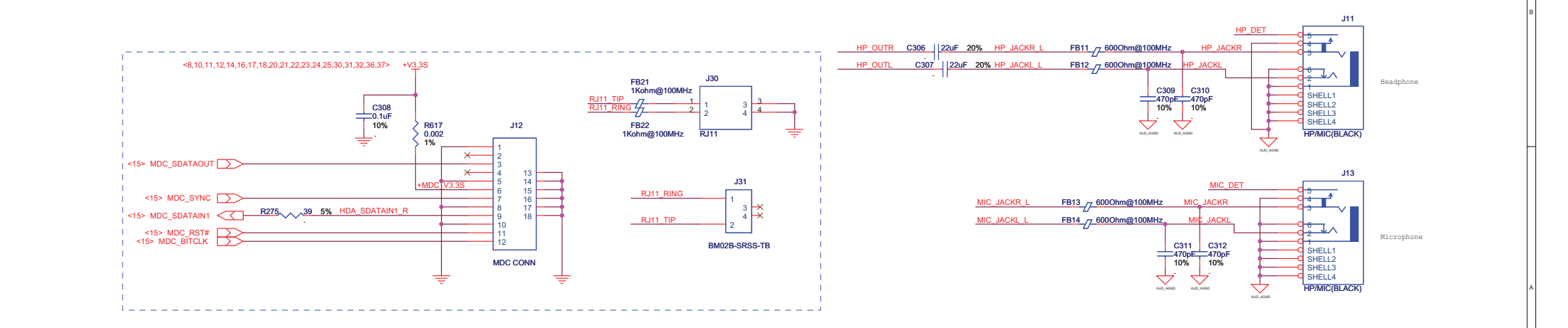
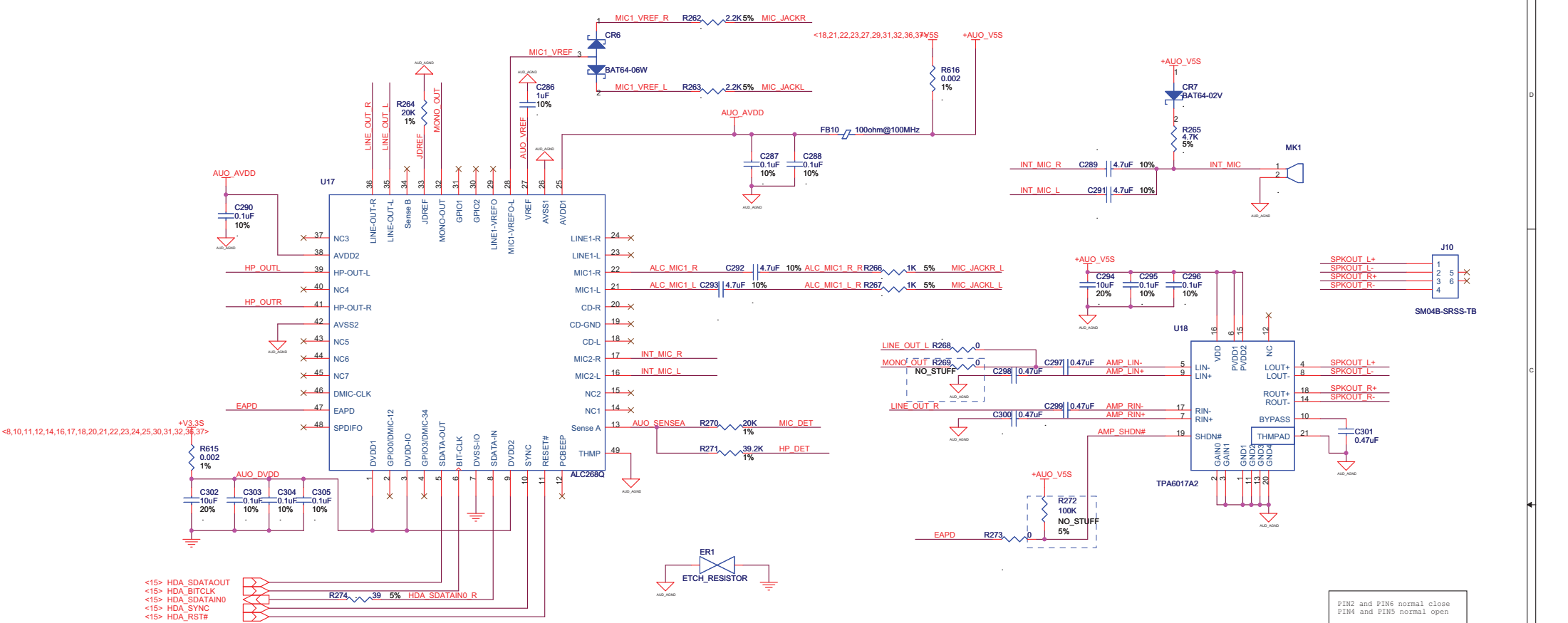




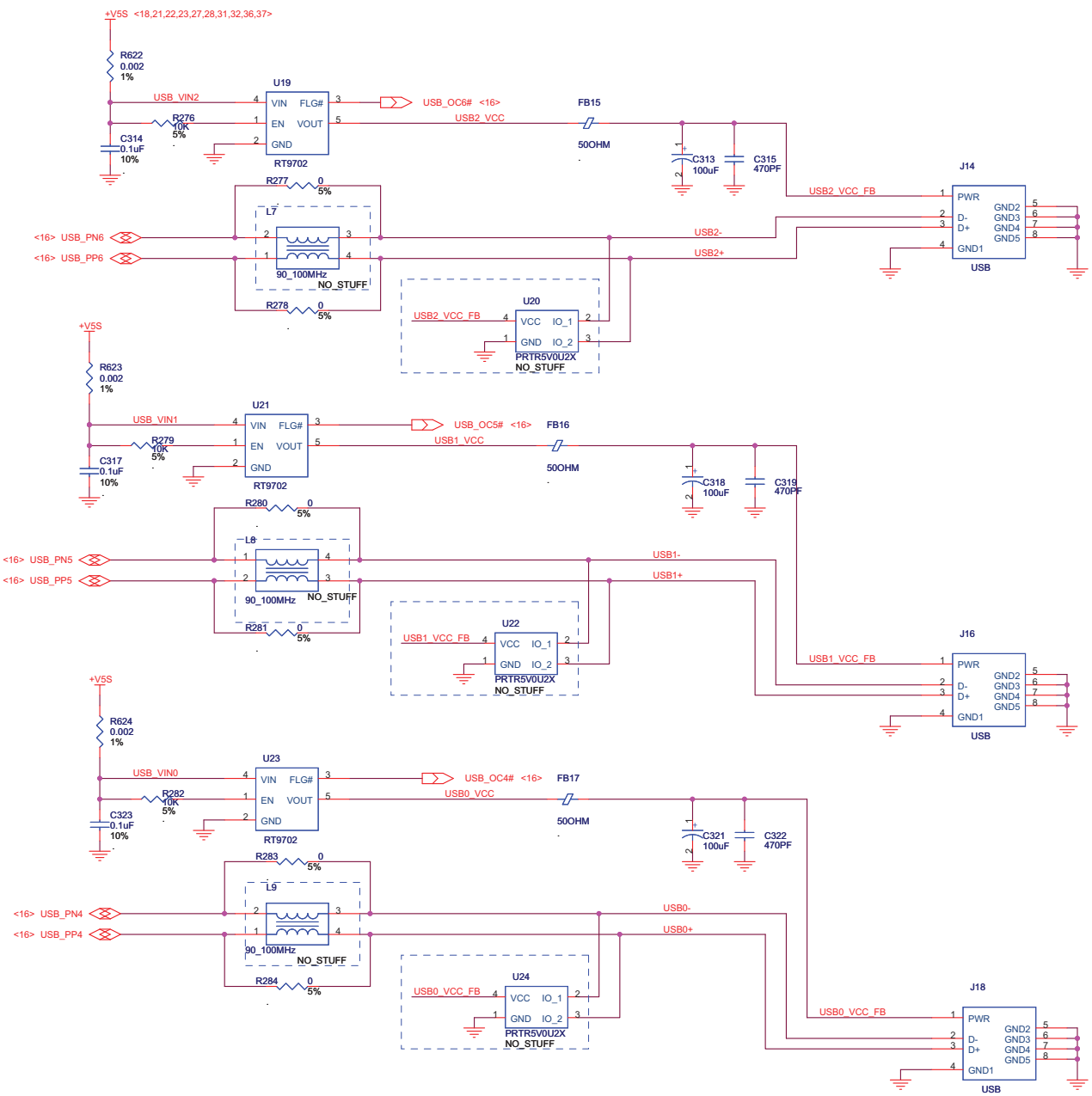




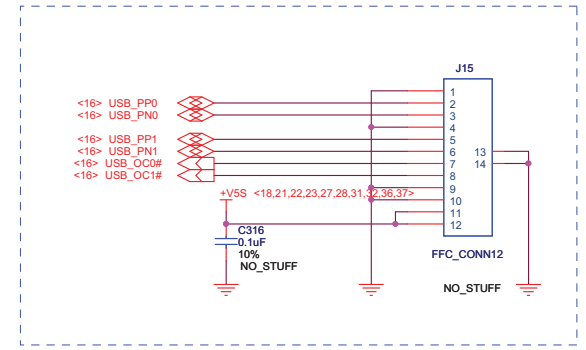




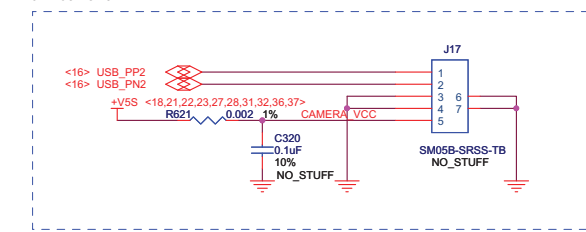
PIN2 and PIN6 normal close  
 PIN4 and PIN5 normal open



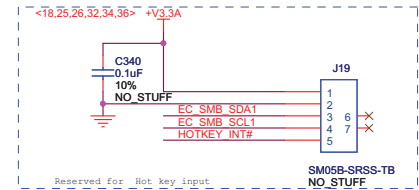
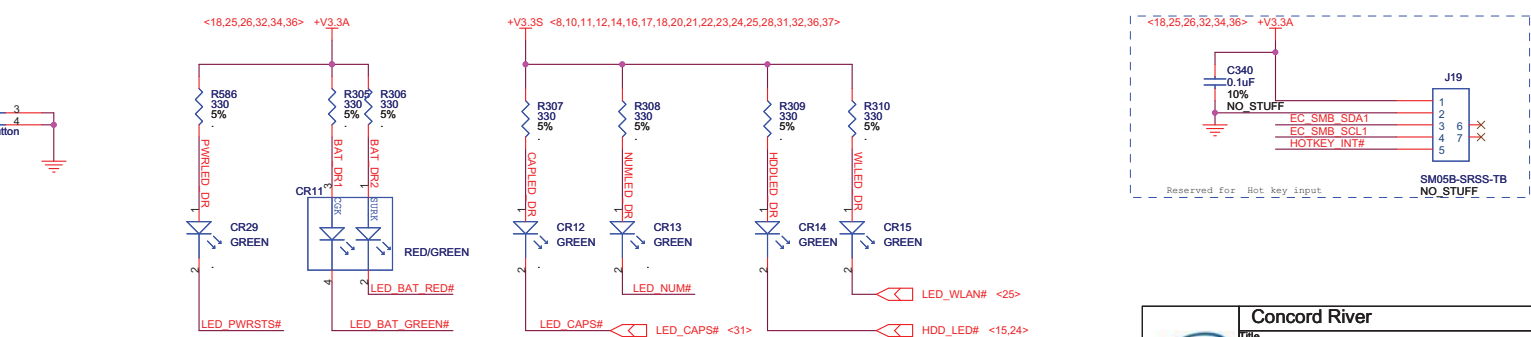
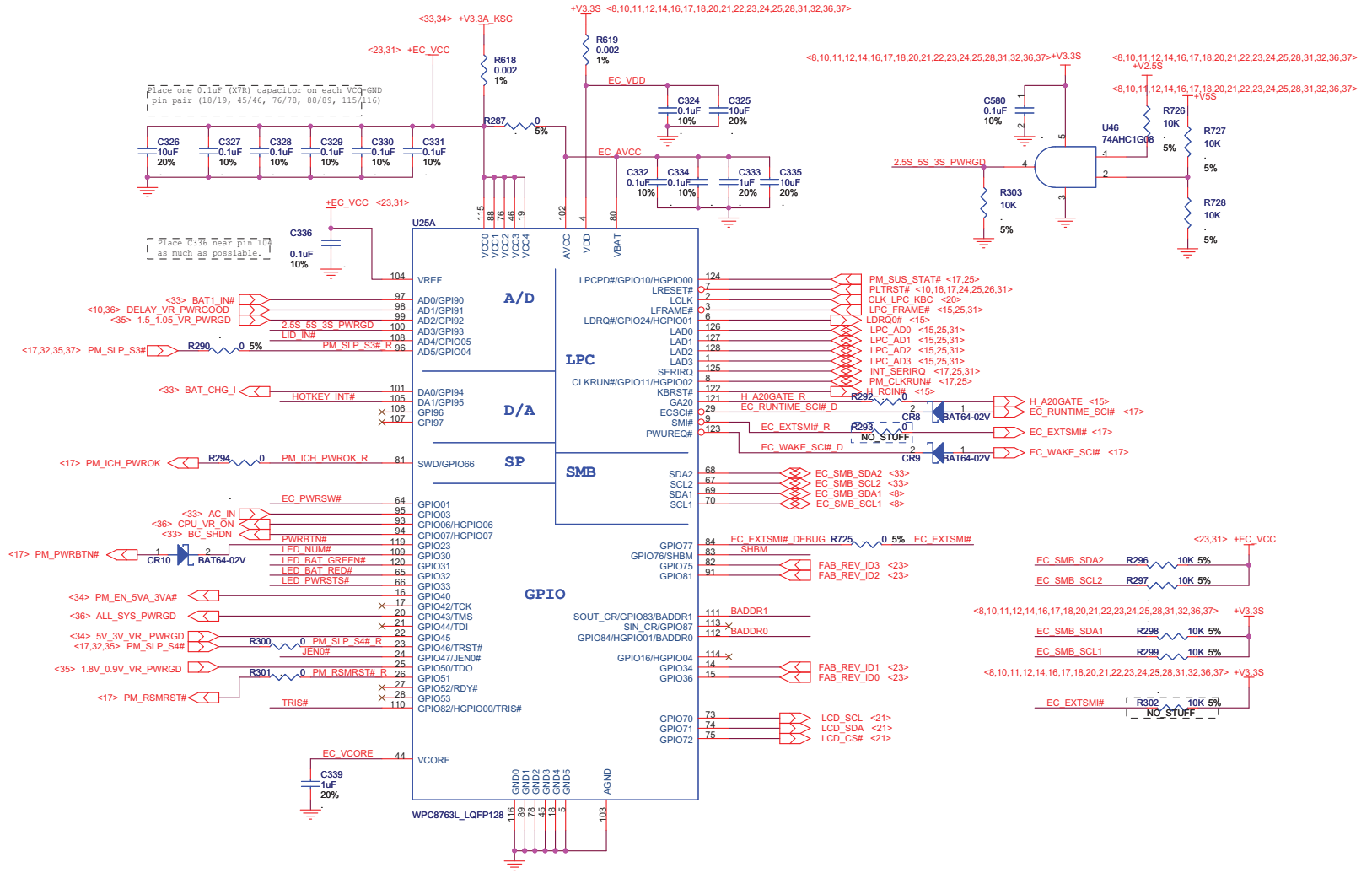
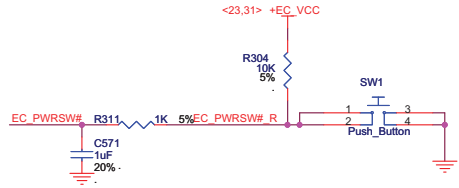
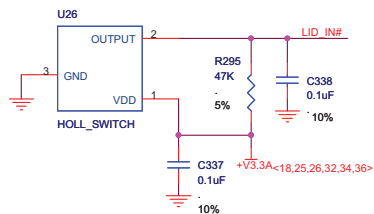
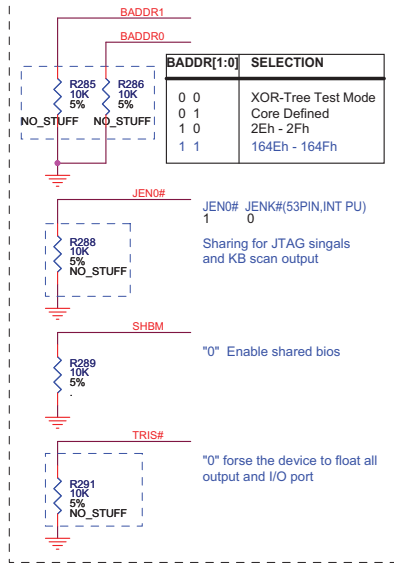
For Optional Ports



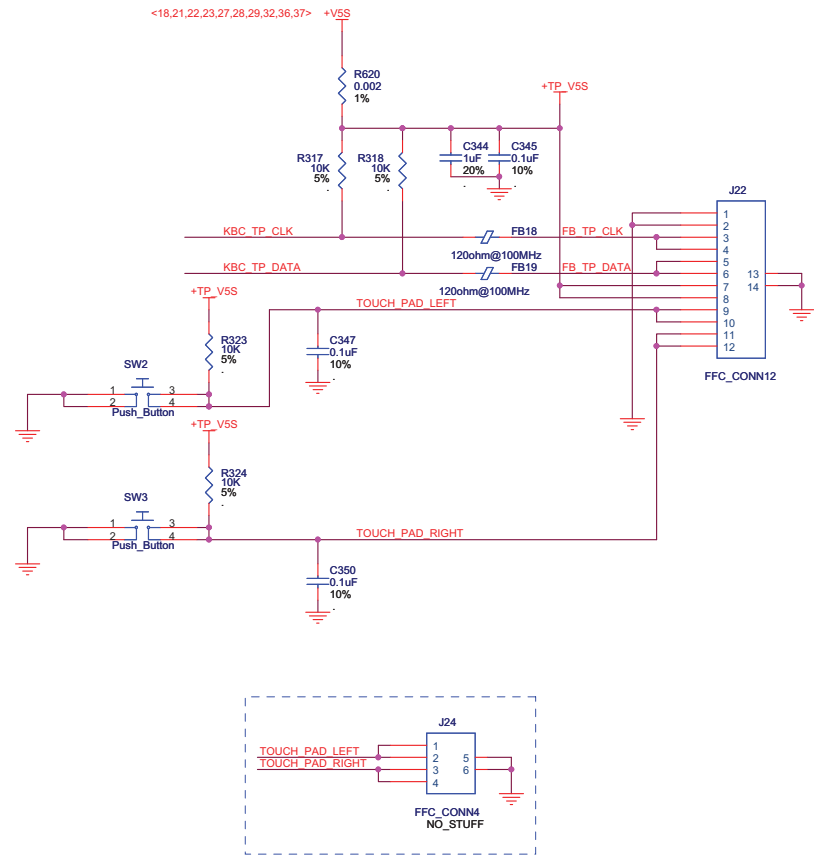
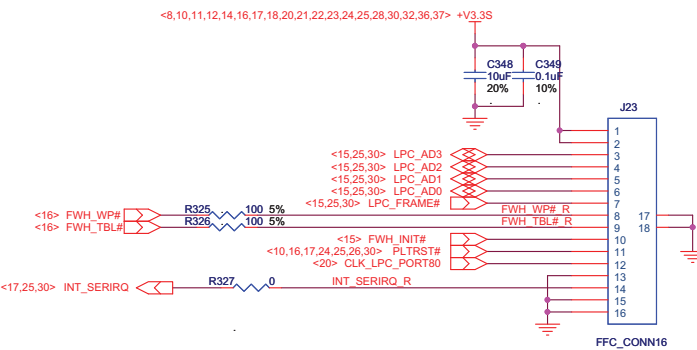
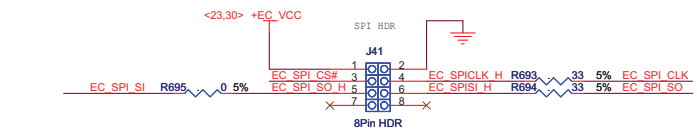
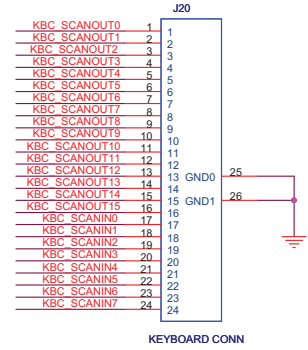
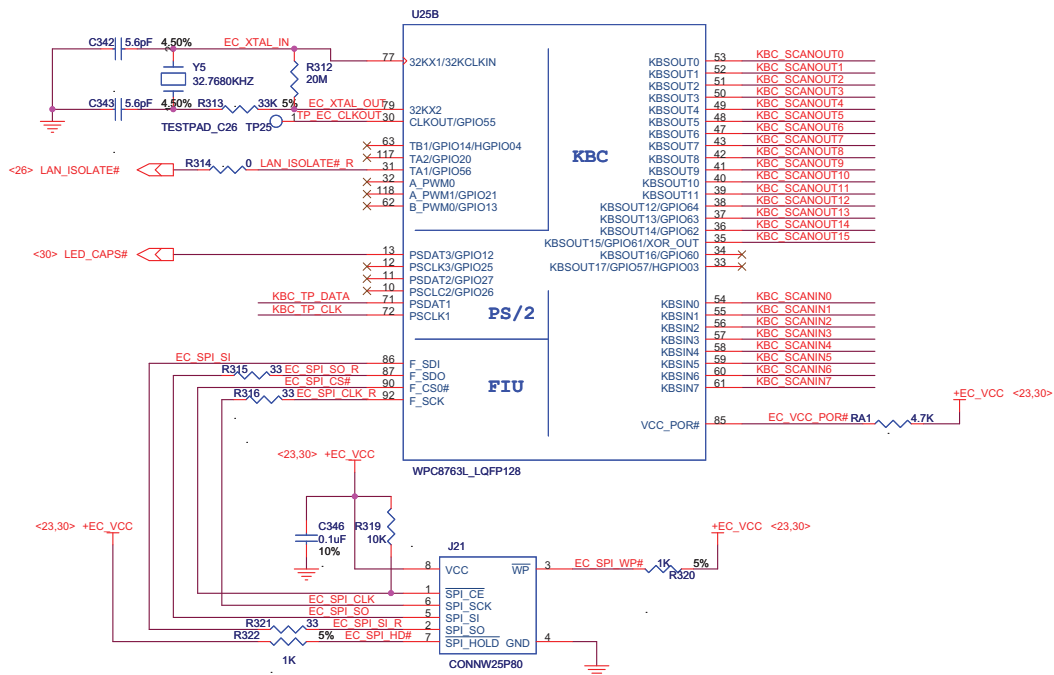
For Camera



## EC hardware strap



<b>Concord River</b>		Intel Confidential	
File <b>EC (1/2)</b>			
Size Custom		Document Number	
Date Friday, November 23, 2007	Sheet 28	Rev 0.5	



**Port80 and Reserved LPC Connector**

