Si4010

CRYSTAL-LESS SOC TRANSMITTER

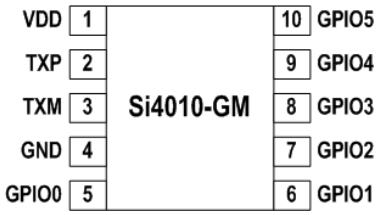
Features

- Single coin-cell battery transmitter, no external MCU, EEPROM, SAW oscillator, or crystal needed
- Integrated 8051 MCU with 128-bit AES security encryption algorithm
- Frequency band options: 315, 390, 433.92, 868, 915 MHz
- Support for multi-channel packet transmissions
  - Channel spacing up to ±1.83 MHz at 915 MHz carrier frequency (±2000 ppm)
- Supports OOK and FSK modulation
- Supply voltage from 1.8 to 3.6 V
- -40 to +85° C temperature range
- +10 dBm maximum transmit power, 19.5 dB programmable range
- Automatic antenna tuning and PA ramp shaping
- Ultra low power timer
  - Enforcement of transmit duty cycle for ETSI 434, 868 MHz
  - Self-wakeup for button independent applications
- Low current consumption
  - 13 mA @ +10 dBm transmit power OOK Manchester encoded
  - 100 nA standby current
- Programmable data rate up to 20 kbps
- Direct battery operation with on-chip low-drop out (LDO) voltage regulator
- Battery voltage measurements with high-resolution ADC
- ± 150 ppm (±137 kHz @ 915 MHz) frequency accuracy over 0° to 70° C with no external reference
  - ± 250 ppm (±229 kHz @ 915 MHz) frequency accuracy over full temperature range
  - Option for 1-pin crystal oscillator for tighter tolerance
- Memory configuration
  - 8 kB ROM (program)
  - 4 kB OTP (program)
  - 4 kB RAM (shared for both OTP program transcription and data)
  - 128-bit EEPROM for synchronization counters
- Five general purpose inputs/outputs with power-on push button and debounce capability
- 10-pin MSOP package (Pb free/ RoHS compliant)

Ordering Information:
See page 22.

Pin Assignments

Si4010



Patents pending

Applications

- Garage and gate door openers
- Home automation and security
- Remote keyless entry
- After market alarms
- Automotive immobilizers
- Wireless lock

Description

The Si4010 is a fully integrated crystal-less CMOS RF transmitter with operating frequency options at 315, 390, 433.92, 868, or 915 MHz. It is designed for high-volume cost sensitive secure RF transmitter applications such as remote keyless entry (RKE) systems, garage-door openers, after-market alarms, automotive immobilizers, and wireless locks. The device provides the entire electronics needed for an RKE keyfob transmitter by directly interfacing with the battery, antenna, and keyfob push buttons. This chip offers industry leading RF performance, high integration, flexibility, low BOM, small board area, and ease of design. No production alignment is necessary as all RF functions are integrated into the device. Users must comply with local radio-frequency transmission regulations.

Functional Block Diagram

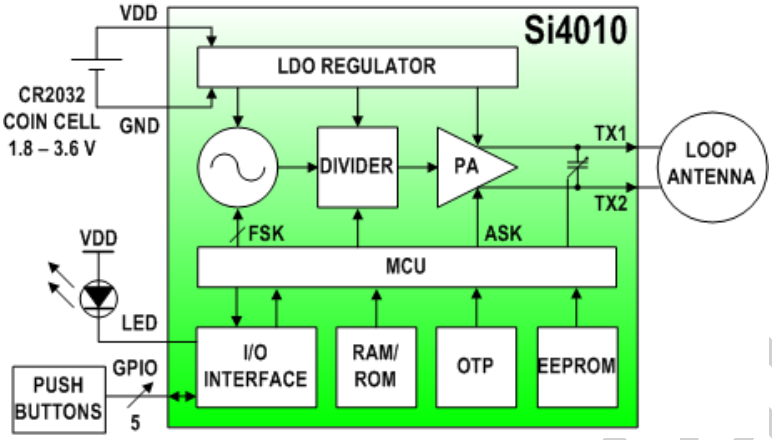


TABLE OF CONTENTS

1. Electrical Specifications

Table 1. Recommended Operating Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Supply Voltage	V_{DD}		1.8	—	3.6	V
Supply Voltage Powerup Rise Time	$V_{DD\text{-}RISE}$		10	—	—	µs
Ambient Temperature	T_A		–40	25	85	°C
Digital Input High Voltage	V_{IH}	Digital Input Signals	0.7 x V_{DD}	—	V_{DD} + 0.3	V
Digital Input Low Voltage	V_{IL}	Digital Input Signals	–0.3	—	0.3 x V_{DD}	V

Table 2. Absolute Maximum Ratings[1,2]

Parameter	Symbol	Value	Unit
Supply Voltage	V_{DD}	–0.5 to 3.9	V
Input Current[3]	I_{IN}	10	mA
Input Voltage[3]	V_{IN}	–0.3 to (V_{DD} + 0.3)	V
Operating Temperature	T_{OP}	–45 to 95	°C
Storage Temperature	T_{STG}	–55 to 150	°C

Notes:
1. Permanent device damage may occur if the absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as specified in the operational sections of this data sheet. Exposure beyond recommended operating conditions for extended periods may affect device reliability.
2. The Si4010 devices are high-performance RF integrated circuits with certain pins having an ESD rating of < 2 kV HBM. Handling and assembly of these devices should only be done at ESD-protected workstations.
3. For GPIO pins configured as inputs.

Table 3. DC Characteristics
(TA = 25° C, VDD = 3.3 V, RL = 750 Ω, unless otherwise noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Supply Current	I_{VDD}	+10 dBm output, OOK, Manchester	—	13.1	—	mA
		+6.5 dBm output, OOK, Manchester	—	10.6	—	mA
		+10 dBm, FSK	—	18.1	—	mA
		+6.5 dBm output, FSK	—	13.1	—	mA
Low Power Mode	I_{LP}	Only ultra-low power counter is enabled	—	700	—	nA
Standby Supply Current	I_{SB}	All GPIO floating or held high	—	100	800	nA
LED Sink Current	I_{LED}	GPIO5 configured as LED driver	—	1.0	1.3	mA
GPIO[0-5] Pull Up Resistance	R_{PU}		40	60	80	kΩ
High Level Input Voltage[1]	V_{IH}		0.7 x V_{DD}	—	V_{DD} + 0 .3	V
Low Level Input Voltage[1]	V_{IL}		–0.3	—	0.3 x V_{DD}	V
High Level Input Current[1]	I_{IH}		—	TBD	—	µA
Low Level Input Current[1]	I_{IL}		—	TBD	—	µA
High Level Output Voltage[2]	V_{OH}		—	TBD	—	V
Low Level Output Voltage[2]	V_{OL}		—	TBD	—	V

Notes:
1. For GPIO pins configured as inputs.
2. For GPIO pins configured as outputs.

Table 4. Si4010 Transmission Characteristics
(TA = 25° C, VDD = 3.3 V, RL = 750 Ω, unless otherwise noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Operating Frequency	F_{RF}	Discrete frequencies	—	315	—	MHz
			—	390	—	MHz
			—	433.92	—	MHz
			—	868	—	MHz
			—	915	—	MHz
Carrier Frequency Accuracy		F_{RF} = 315 MHz 0°C ≤ T_A ≤ 70° C	–47.3	—	47.3	kHz
		F_{RF} = 315 MHz –40°C ≤ T_A ≤ 85° C	–78.8	—	78.8	kHz
		F_{RF} = 433.92 MHz 0°C ≤ T_A ≤ 70° C	–65.1	—	65.1	kHz
		F_{RF} = 433.92 MHz –40°C ≤ T_A ≤ 85° C	–109	—	109	kHz
		F_{RF} = 868 MHz 0°C ≤ T_A ≤ 70° C	–130	—	130	kHz
		F_{RF} = 868 MHz –40°C ≤ T_A ≤ 85° C	–217	—	217	kHz
		F_{RF} = 915 MHz 0°C ≤ T_A ≤ 70° C	–137	—	137	kHz
		F_{RF} = 915 MHz –40°C ≤ T_A ≤ 85° C	–229	—	229	kHz
Multi-Packet Transmission Maximum Channel Spacing		F_{RF} = 315 MHz	–630	—	630	kHz
		F_{RF} = 433.92 MHz	–868	—	868	kHz
		F_{RF} = 868 MHz	–1.74	—	1.74	MHz
		F_{RF} = 915 MHz	–1.83	—	1.83	MHz
Transmit Power		Maximum programmed Tx power, with optimum differential load	—	10	—	dBm
		Minimum programmed TX power, with optimum differential load	—	–9.5	—	dBm
		Power variation vs temp and supply, with optimum differential load, Vdd > 2.2 V	–0.5	—	+0.5	dB
		Programmable range	—	19.5	—	dB
		Transmit power step size	—	0.25	—	dB
Data Rate		OOK (Manchester encoded)	1.2	—	20	kbps
		FSK	1.2	—	20	kbps

Table 4. Si4010 Transmission Characteristics
(TA = 25° C, VDD = 3.3 V, RL = 750 Ω, unless otherwise noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
FSK Deviation		Max frequency deviation, 315 MHz	—	80	—	kHz
		Deviation resolution, 315 MHz	—	630	—	Hz
		Max frequency deviation, 433.92 MHz	—	110	—	kHz
		Deviation resolution, 433.92 MHz	—	868	—	Hz
		Max frequency deviation, 868 MHz	—	220	—	kHz
		Deviation resolution, 868 MHz	—	1740	—	Hz
		Max frequency deviation, 915 MHz	—	232	—	kHz
		Deviation resolution, 915 MHz	—	1830	—	Hz
OOK Modulation depth			—	60	—	dB
PA Differential Output Impedance with capacitance control programmed to zero		Resistance, F = 315 MHz	—	16	—	kΩ
		Capacitive, F = 315 MHz	—	3.4	—	pF
		Resistance, F = 433.92 MHz	—	9	—	kΩ
		Capacitive, F = 433.92 MHz	—	3.4	—	pF
		Resistance, F = 868 MHz	—	2.2	—	kΩ
		Capacitive, F = 868 MHz	—	3.4	—	pF
		Resistance, F = 915 MHz	—	2	—	kΩ
		Capacitive, F = 915 MHz	—	3.4	—	pF
Battery Voltage Measurement Accuracy			–1	—	+1	%
Crystal Frequency		GPI0 configured as crystal oscillator		TBD		MHz
GPIO0 Input Capacitance		GPI0 configured as crystal oscillator		5		pF
Crystal ESR		GPI0 configured as crystal oscillator			50	Ω

2. Test Circuit

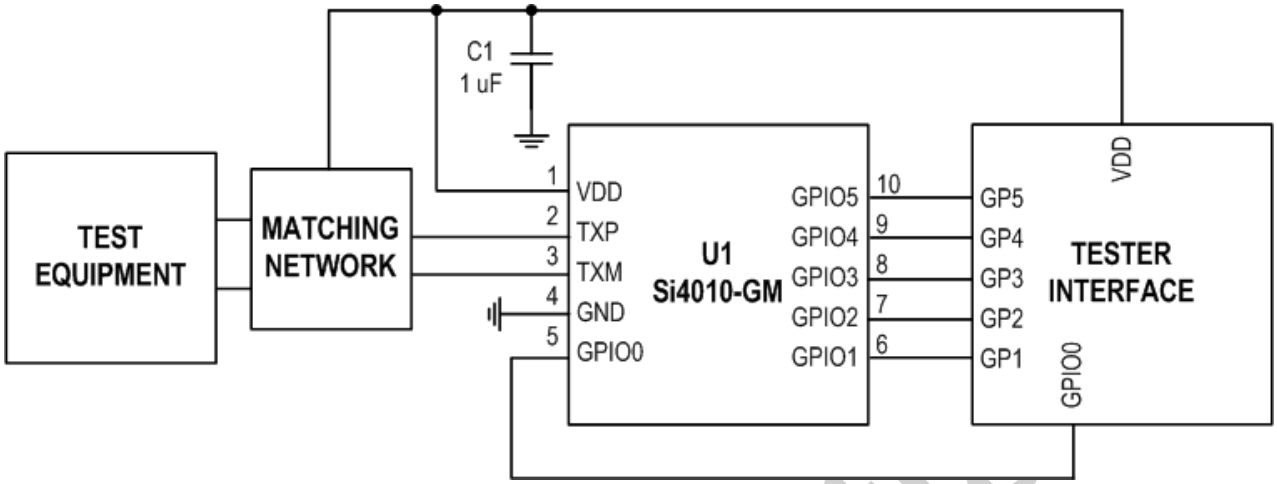


Figure 1. Test Block Diagram

3. Typical Application Schematic

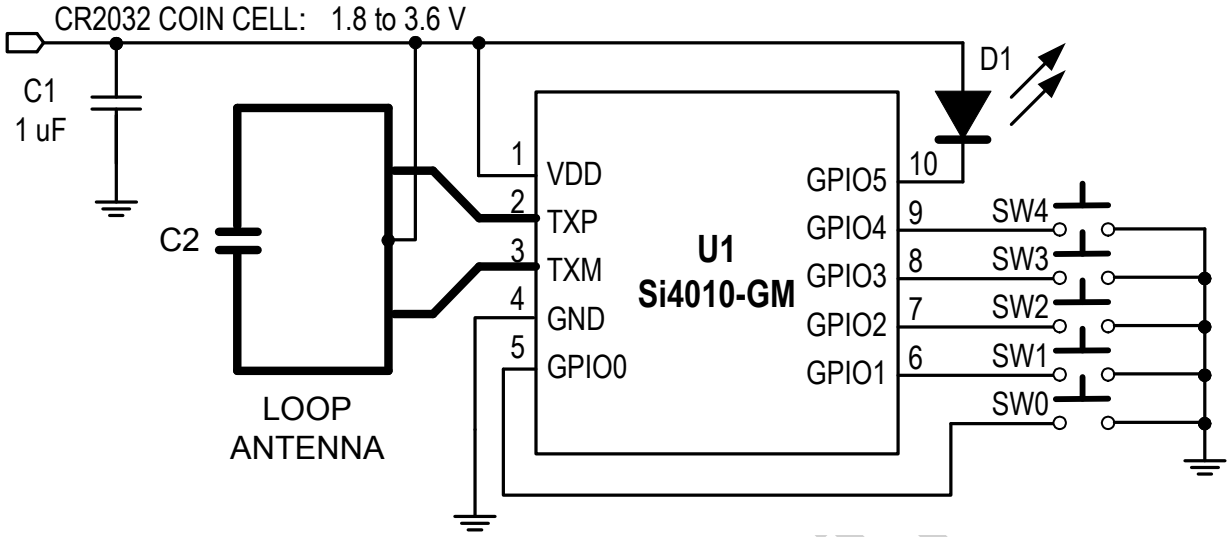


Figure 2. Si4010 used in a 5-button RKE System with LED Indicator

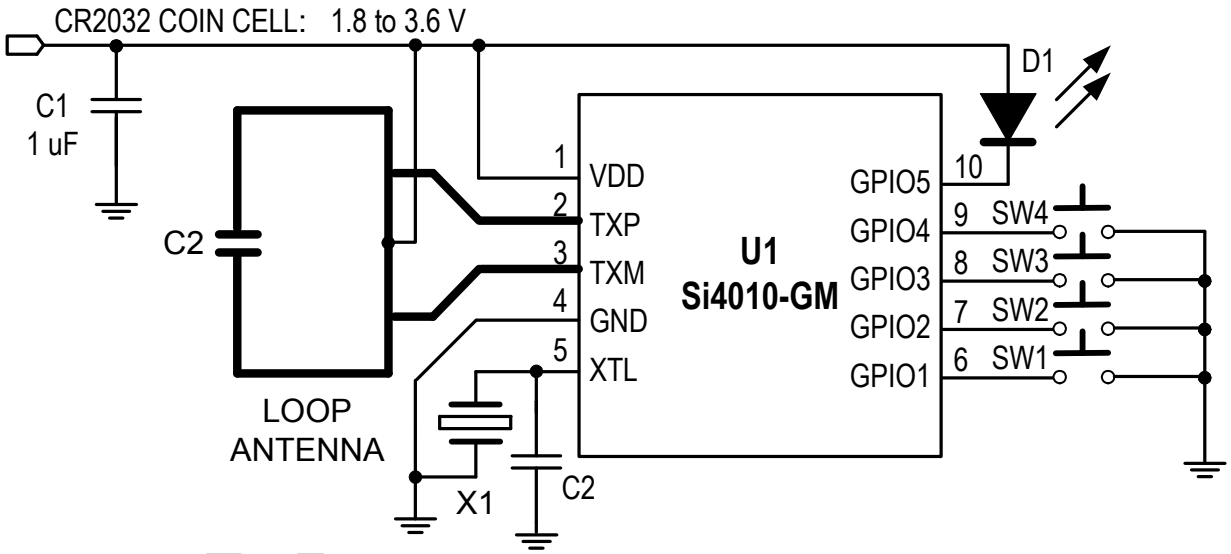


Figure 3. Si4010 with an External Crystal in a 4-button RKE System with LED Indicator

4. Functional Description

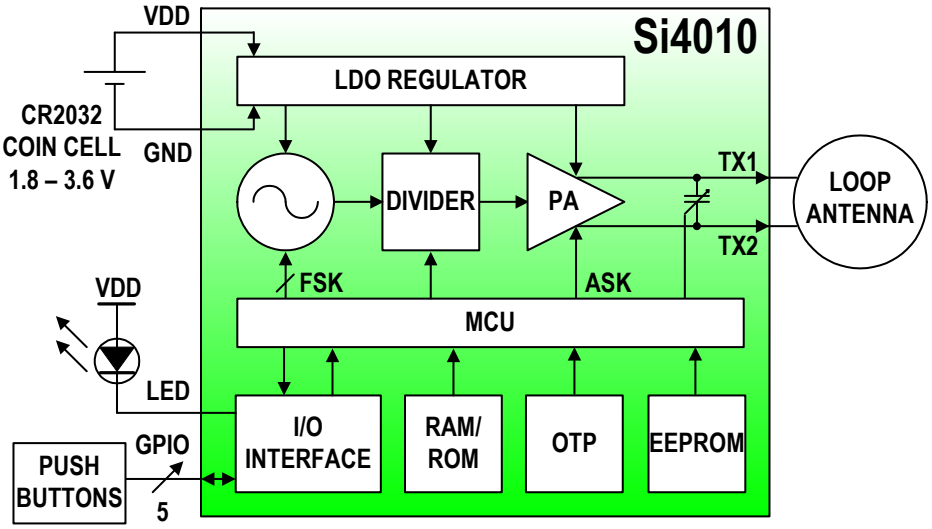


Figure 4. Functional Block Diagram

4.1. Overview

The Si4010 is a fully integrated, crystal-less CMOS RF transmitter with carrier frequency options at 315, 390, 433.92, 868, or 915 MHz. It is designed for high-volume, cost-sensitive secure RF transmitter applications such as remote keyless entry (RKE) systems, garage door openers, after market alarms, automotive immobilizers, and wireless locks. The device provides the entire electronics needed for an RKE keyfob transmitter by directly interfacing to the battery, antenna, and keyfob push buttons. Its low power modes and sub-microampere leakage current are ideal for portable applications where battery life is important.

The Si4010 contains all the hardware and software necessary for configuring a semi-custom RKE transmitter. It includes an integrated 8051 MCU, 128 bits of EEPROM, 3 kB of one-time programmable (OTP) memory, 3 kB of RAM, and 8 kB of ROM. The on-chip ROM incorporates all the software required for a turn-key RKE transmitter using the 128-bit Advanced Encryption Standard (AES) encryption algorithm as well as other library task functions. The turn-key solution also includes a patent-pending coding technique to convert 30 bits of the EEPROM into a 20-bit synchronization counter with a write endurance of 1,000,000 cycles. Complete customization of the encryption algorithm, synchronization counter, packet structure, or other functions is possible by writing custom firmware into the available 3 kB of OTP memory reserved for customer specific functions. Silicon Labs will provide engineering support to qualified customers interested in creating their own custom functions.

The device leverages Silicon Labs' patented and proven crystal-less oscillator technology and offers better than ±150 ppm carrier frequency stability over the temperature range of 0 to +70° C without the use of an external crystal or frequency reference. The internal MCU automatically calibrates the on-chip voltage controlled oscillator (VCO) for process and temperature variations and divides the VCO frequency to form the desired carrier frequency. An external 1-pin crystal oscillator option is available for applications requiring tighter frequency tolerances; in this application, the crystal is used for calibration.

On-off keying (OOK) modulation is realized by turning the power amplifier on and off and frequency shift keying (FSK) modulation is achieved by directly modulating the VCO frequency. Both digital modulation formats support data rates up to 20 kbps. The Si4010 also includes an integrated, low-drop out (LDO) voltage regulator, five general purpose input/output pins with push button power-on capability, and a programmable power amplifier capable of delivering +10 dBm output power into a differential 750 Ω load. The differential output power amplifier is programmable with 19.5 dB of output power range and has an integrated automatic antenna tuning circuit to maximize antenna efficiency. Users must comply with local radio frequency transmission regulations.

Digital integration reduces the amount of required external components compared to traditional offerings, resulting in a solution that only requires a printed circuit

board (PCB) implementation area of approximately 25 x 5 0mm (including battery, switches, and (25 mm)^2 antenna). The high integration of the Si4010 improves the system manufacturing reliability, quality, and minimizes costs. This chip also offers industry leading RF performance, high integration, flexibility, low BOM, small board area, and ease of design. No production alignment is necessary as all RF functions are integrated into the device.

4.2. Fully Compatible 8051 MCU

The Si4010 utilizes Silicon Laboratories' proprietary CIP-51 microcontroller core. The CIP-51 is fully compatible with the MCS-51™ instruction set; standard 803x/805x assemblers and compilers can be used to develop software. The CIP-51 employs a pipelined architecture that greatly increases its instruction throughput over the standard 8051 architecture. In a standard 8051, all instructions except for MUL and DIV take 12 or 24 system clock cycles to execute with a maximum system clock of 12 to 24 MHz. By contrast, the CIP-51 core executes 70% of its instructions in one or two system clock cycles, with only four instructions taking more than four system clock cycles. The CIP-51 has a total of 109 instructions. The CIP-51's maximum system clock is 25 MHz and has a peak throughput of 25 MIPS, but it typically runs at much lower clock rates to save power.

4.2.1. C2 Interface

The Si4010 device includes an on-chip Silicon Labs two-wire (C2) debug interface to allow OTP programming and in-system debugging with the production part installed in the end application. The C2 interface uses a clock signal (GPIO5) and a bi-directional C2 data signal (GPIO4) to transfer information between the device and a host system. The hardware and software details of the C2 interface are handled by the Si4010 development kit hardware and IDE. Most users choose to have their applications loaded into the Si4010 in Silicon Labs' production test process and will never need to learn the details of the C2 interface.

4.3. Power Amplifier

The CMOS power amplifier (PA) is a differential open drain amplifier capable of delivering +10 dBm of output power to a 750 Ω differential load. These differential outputs can be used to drive a differential loop antenna or they can be converted to a single-ended output to drive a single-ended antenna with external components. The output power can be adjusted in 0.25 dB steps over a range of 19.5 dB.

Impedance matching, biasing, and proper layout techniques are all necessary to ensure optimal performance. Figure 2 shows a typical application schematic of the Si4010 with the associated matching circuitry for a differential loop antenna with an impedance of 750 Ω. Application note “AN369: Antenna Interface for the Si401x Transmitters” provides detailed information about designing the antenna interface for the Si401X transmitters. With proper filtering and layout techniques, the Si4010 can conform to US FCC part 15.231 and European EN 300 220 regulations. Users must comply with local radio frequency transmission regulations.

Variations in the transmit center frequency due to off-chip capacitor tolerances, loop antenna manufacturing tolerances, and environmental variations can lead to large antenna inefficiencies and wasted power especially in high-Q power amplifiers. The Si4010 includes an automatic antenna tuning circuit to improve the antenna efficiency of the transmitter.

4.4. LDO Voltage Regulator and Low Voltage Battery Detector

The Si4010 works over a wide range of supply voltages from 1.8 to 3.6 V, enabling it to be directly connected to a single CR2032 lithium ion coin cell. The on-chip LDO voltage regulators generate internal supply voltages that are used throughout the chip for power supply rejection and power isolation of the digital and RF blocks.

A low voltage battery detector is integrated into the Si4010 and can be transmitted as 3 bits of the status register in the packet data field. The eight possible outputs are:

Table 5. Battery Voltage Logic Table

VB[2:0]	Voltage[V]	VB[2:0]	Voltage[V]
000	1.8	100	2.2
001	1.9	101	2.3
010	2.0	110	2.4
011	2.1	111	2.5

The battery voltage is sampled when transmitting the first bit, and stored for the next message composition. This ensures that it is the loaded battery voltage which is sampled. Depending on the PA drive level setting, the battery charge state, and the temperature, the loaded voltage can be substantially lower than the low-current battery voltage.

An 8-bit view of the battery voltage is available for users who may wish to transmit more than 3 bits of battery voltage information.

4.5. General Purpose Input/Output (GPIOs)

General purpose input/output (GPIO) pins, GPIO[4:0], are general purpose pins which can be configured as digital inputs or digital outputs (GPIO[0] can only be an input). As digital inputs, the Si4010 will power itself on once it detects a negative edge transition button press condition. After detecting a button press, the input will go through a programmable debounce time before the button press condition is latched into the MCU and placed into the function register. The function register is described in detail in section “4.8. Turn-key RKE Transmitter” .

Function Register

B7	B6	B5	B4	B3	B2	B1	B0
S2	S1	S0	GPIO4	GPIO3	GPIO2	GPIO1	GPIO0

When a GPIO pin is configured as a digital output it can output a logic high, logic low, and tri-state (with a 60K pull up resistor enabled).

GPIO5 is an output only pin and can be configured to drive a light emitting diode (LED). If it is not driving an LED it serves as the C2 debug interface C2CLK input. It cannot be programmed as general purpose input or output but only as an LED driver. The LED drive can be programmed on for a specific time, blink rate, PWM density, and drive level. The LED drive is a current source output which produces a more voltage independent brightness compared to a simple resistor connection to a normal GPIO output.

GPIO0 is an input only pin with push button power-on capability and can also be configured as an input pin for a crystal. See Optional Crystal Oscillator section for more details.

4.5.1. Optional Crystal Oscillator

An on-chip crystal oscillator is provided on the device for applications requiring frequency tolerances better than ±250 ppm over the -40 to 85°C temperature range. GPIO0 pin can be configured as a crystal oscillator input pin. The crystal should be capacitively loaded with the capacitance value recommended by the crystal vendor, including the 2.0 pF representing the GPIO0 pin.

The crystal oscillator is powered for a programmable wake-up time and then used as a reference clock to count and adjust the frequency of the on-chip LC oscillator to precisely match the target frequency, which need not be an integer or rational multiple of the crystal frequency. Afterwards, the crystal oscillator is powered down, and the known temperature sensitivity of the on-chip oscillator is used to cancel response to subsequent temperature changes in the normal way.

4.6. Memory

The Si4010 contains 8 kB of ROM, 3 kB of OTP, 3 kB of RAM and 128 bits of EEPROM. The MCU can operate with program stored in ROM and RAM only. The code can be executed from RAM and ROM at the same time. On each wake-up event, the program is transcribed from OTP into RAM where the MCU is able to execute code. In addition, various calibration factors are transcribed into data RAM and other internal registers. The system boot code and all the functions and tasks required for a secure RKE transmitter are stored in ROM. Three kilobytes of OTP memory are available for customer specific code, which may supply parameters to ROM functions calls, and replace all or some of the message composition, encryption, and association functions.

The Si4010 has 128 bits of on-chip EEPROM available for customer use. This technology allows 50,000 memory cycles on a per bit basis. Silicon Labs’ turn-key RKE transmitter solution includes a 20-bit synchronization counter that uses a patent-pending coding technique to convert 30 bits of the EEPROM into a 20 bit synchronization counter with a write endurance of 1,000,000 cycles and a data retention greater than 40 years. This allows the 128-bit EEPROM to be used for up to 4 different 20-bit counters. Silicon Lab's RKE turn-key transmitter solution is described in section “4.8. Turn-key RKE Transmitter” .

4.7. Security Features

Multiple features safeguard the customers' program, keys, encryption keys, etc., from access after programming.

The customer may choose two levels of code protection with the Si4010. As explained in section “4.2.1. C2 Interface” , the chip implements Silicon Labs’ C2 MCU debugging interface. This enables customers to use the IDE software environment for code development. After the customer program load is finished, the customer can choose to set specific protection control bits in the OTP as part of the load.

The available protection levels of the chip are:

- C2 enabled but OTP and MTP content protected. When the chip is fully programmed, the only way to open it for debug communication in this mode is to hold C2CLK=0 when the chip is being powered up. The C2 interface is enabled for debugging only after the OTP or MTP contents are protected, all RAMs are cleared, and all accesses to OTP and MTP are disabled. This mode is useful if there is some issue with the analog circuits later on and the customer or Silicon Labs wants to investigate it without revealing any of the customer data loaded into OTP or MTP.
- No protection. If the chip is fully programmed and if C2CLK=0 during power on reset, the C2 interface will become active and debugging of the current customer load program is possible. There is no protection for memories on chip. This mode is useful for debugging the customer load program.

4.8. Turn-key RKE Transmitter

The Si4010 in conjunction with Silicon Labs’ Si4310 and MCUs forms a complete, secure, unidirectional RKE system that allows customers to rapidly develop, test, and deploy a unidirectional RKE system. The Si4010 integrates all the software required for a RKE transmitter including the secure 128-bit AES encryption algorithm. The encryption key and device ID are stored in dedicated read-only OTP memory space preventing unauthorized users access to this sensitive information.

The turnkey solution consists of several configurable options as listed below:

- Operating frequency: 315, 433.92, 868, 915 MHz
- Modulation type: OOK/ FSK
- Code format: Manchester, NRZ, (4,5) RLL code
- Data rate: 1.2 to 20 kbps
- Output power: –9.5 to +10 dBm, 0.25 dBm steps, antenna tuning enable/disable, 1% duty cycle enable/disable
- Button timing parameters: Debounce time, interval_2nd, interval_extend, interval_timeout, interval_association
- Synchronization counter: 3-byte initial count
- AES: enable/disable, 6-byte pad for AES encryption
- Transmit format parameters: Transmit_period, packet_repetition, ETSI_duty_cycle_enable
- Association: Association_encryption_key, association_packet_repetition

With read-only OTP registers for:

- Transmit device identification (ID) number, enable thermal random number generator for transmit device identification number
- 16-byte AES encryption key

These configuration parameters are explained in detail in section “4.8.4. Si4010 Turn-key Transmitter Configuration Registers” .

The Si4010 turn-key RKE transmitter is normally powered down until a button press condition occurs, which wakes up the transmitter to transmit the button press information. The turn-key solution responds to button presses according to the following rules:

[1] **First button press**: Wakes up the transmitter, updates the synchronization counter, and begins composing the packet with a message "first button press" along with the associated button that was pressed. This button press condition also initiates a button_press_timer to measure how long the button has been held. The chip polls the GPIO pins every 100 ms to measure the button hold time and stops polling when the chip detects the button has been released. After the packet is composed, transmission begins.

[2] **New button press**: Any new button presses occurring after transmission and a programmable time interval, "interval_2nd", re-initiates rule [1]. Any new button presses occurring before the completion of transmission causes the transmitter to stop and set up for a new transmission. The new transmission will update the synchronization counter and compose the packet with a message "second or more button press" along with the associated button that was pressed. This new button press condition will also reset and start the button_press_timer to measure how long this new button has been held. After the packet is composed, transmission begins with the new packet.

[3] **Extended button press**: Any button presses occurring past a programmable time interval, "interval_extend", initiates a new packet transmission with the message "extended press" along with the associated button that caused this condition. The extended button press condition occurs when the button_press_time is greater than the "interval_extend" time.

[4] **Release button**: Only after an "extended press" message has been initialized can a "release" message be sent. The transmitter will send the "release" message after it has detected the button has been released and that it was in the "extended press" condition. If the button is not released after a time interval, "interval_timeout", the transmitter stops waiting for the button release condition, sends a message "stuck button", and powers down.

Function Register

B7	B6	B5	B4	B3	B2	B1	B0
S2	S1	S0	GPIO4	GPIO3	GPIO2	GPIO1	GPIO0

S2	S1	S0	Status Message
0	0	0	First button press
0	0	1	Second or more button press
0	1	0	Extended button press
0	1	1	Release button
1	0	0	Stuck button
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

For "simultaneous button presses", it is impossible to press two buttons at exactly the same time. Therefore, one of the two buttons from the "simultaneous button press" will initiate the first button press rule [1]. The second button will then act as a new button press, rule [2], and cause the transmitter to send out the message "second or more button press" and indicate which of the two buttons were pressed. For example, if GPIO4 and GPIO3 were pressed simultaneously and GPIO4 occurred slightly before GPIO3, then GPIO4 would initiate a first button press according to rule [1] with the button status register contents of 0001 0000. However, GPIO3 appears almost immediately after GPIO4 (well before the "interval_2nd" time) and thus would initiate rule [2] and the contents of the button status register would be 0011 1000, indicating both GPIO4 and GPIO3 were pressed with the message "second or more button press". The receiver's program will interpret these messages and respond accordingly.

Below is a list of timing registers:

- Button_press_timer: 8-bit register indicates the time the button has been pressed.
- Interval_debounce: 8-bit register for programming button debounce time.
- Interval_2nd: 8-bit register to set time after completion of an entire set of packets before considering a next button push as a "new" button push.
- Interval_extend: 8-bit register to set time after completion of an entire set of packets where, if same buttons are still held down, we transmit the extended button press code.
- Interval_timeout: 8-bit register to set time after completing set of packets for extended press code before we give up and shut down if the button is still being held down.

The following three sections cover the transmit packet structure, transmission format, and transmitter/receiver association for the turn-key solution. User programmed custom functions are covered in section “4.8. Turn-key RKE Transmitter” .

4.8.1. Transmit Packet and AES Encoder

The factory installed Si4010 turn-key RKE solution generates two types of packets, one for normal transmission and one for association. Association is the process when the receiver is paired with the transmitter and needs to get information about the transmitter such as its transmit ID and security encryption key. This section describes the packet structure used in normal one-way communication between the transmitter and receiver and section “4.8.3. Transmitter and Receiver Association” describes the packet structure for association.

The factory installed packet structure consists of a 3-byte preamble, a 1-byte synchronization word, 4-byte transmit ID, 3-byte counter, 1-byte function, 1-byte status, and 4-byte encrypted coded message forming 17-byte length packet. The format of the packet is shown below with each block representing a byte of information.

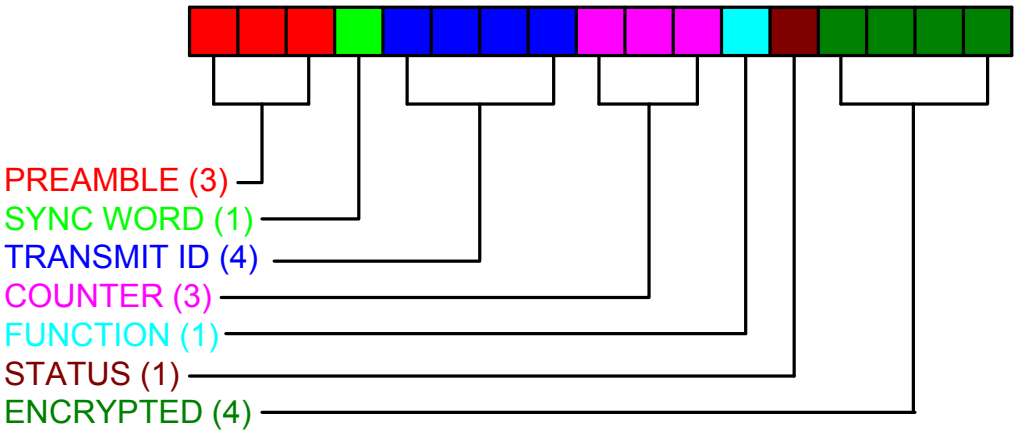


Figure 5. Packet Format

4.8.1.1. Preamble

The preamble is an all-zeros bit sequence. When the packet is Manchester encoded, the all-zeros data becomes an alternating sequence of 1's and 0's.

4.8.1.2. Sync Word

A synchronization word is added to notify the receiver the preamble is over and the packet is about to begin. The synchronization word is as follows:

- Normal packet transmission: 1010 0000
- Association packet transmission: 1010 0001

4.8.1.3. Transmit ID

The unique transmit device ID allows a transmitter to identify itself to a receiver. The default transmit device ID is 32 bits or 4 bytes in length for the Si4010. The device ID is written into a dedicated read-only OTP memory section or it can be generated automatically with Silicon Lab's patented thermal random number generator.

4.8.1.4. Counter

The next part of the packet is the counter. Appending a synchronization counter to the message enables each transmit message to be different from the previous message even if the same command is sent. If the receiver keeps track of the current transmitted count value and only responds to future count values, then this prevents an RF device from recording a transmitted message and retransmitting the same recorded message at a later time to break the security of the system. One potential problem with this approach is a mismatch in count values when the transmitter and receiver are out of range causing the transmitter's counter value to be larger than the receiver's counter value. This problem is overcome by having the receiver accept a window of count values such that when the transmitter is in detectable range, the count value transmitted by the transmitter is within the window of the receiver count values. For example, assume the transmitter and receiver counter values are in synchronization and at a value of 11 and the receiver has a window of 32 count values. The receiver is now ready to accept a count value of 12 from the transmitter and also other values of 13, 14, 15 up to 12 + 32 = 44 since the window has 32 values. Thus, the receiver can accommodate up to 32 out of range transmit button presses before it gets out of synchronization with the transmitter. Continuing with this example, if the transmitter was pressed 5 times when it was out of detectable range from the receiver then the 6th time the transmitter is activated its count value becomes 11 + 6 = 17. Assuming the receiver now receives this count value, it verifies 17 is within the count value window of 12 and 44 and thus accepts the command from the transmitter (assuming the rest of the encryption is decoded correctly) and will update its new count value to 17 and will also update the window range spanning from 18 to 50. Many secure practical systems use a 16 bit synchronization counter with an 8 bit window. The default synchronization counter size is 20 bits with a 4 bit MSB programmable address header. A 20-bit counter has 2^20 = 1,048,576 counts, which means a user can press a button 36 times per day and it would take 80 years before the count value repeats. The fixed 4-bit MSB counter header allows the user to assign different starting count addresses. The synchronization counter increments on each button press.

4.8.1.5. Function

The function byte specifies which buttons were pressed and gives the status of each of the buttons as described in section “4.8. Turn-key RKE Transmitter” . The function byte format is shown below.

Function Register

B7	B6	B5	B4	B3	B2	B1	B0
S2	S1	S0	GPIO4	GPIO3	GPIO2	GPIO1	GPIO0

S2	S1	S0	Status Comments
0	0	0	First button press
0	0	1	Second or more button press
0	1	0	Extended button press
0	1	1	Release button
1	0	0	Stuck button
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

4.8.1.6. Status

The status byte contains the battery voltage and the button_press_time up to 3100 ms. The battery voltage detector is described in section “4.4. LDO Voltage Regulator and Low Voltage Battery Detector” with the three bits, VB[2:0], representing the battery voltage code.

Status Register

B7	B6	B5	B4	B3	B2	B1	B0
VB2	VB1	VB0	T4	T3	T2	T1	T0

The button press time is quantized to 100 ms, with T[4:0] = 00000 representing the initial button press of 0 ms, and sequentially increments in 100 ms time steps with each binary bit increment up to 3100 ms corresponding to T[4:0] = 11111.

4.8.1.7. Encrypted

The Si4010 comes with the AES security encryption algorithm as the factory default security encryption encoder. AES was developed by the National Institute of Standards and Technology (NIST) in November of 2001 to replace the Data Encryption Standard (DES). It is a symmetric block cipher providing security strength equal to or better than DES with significantly improved efficiency. The details of AES are beyond the scope of this datasheet and the interested reader can refer to the original publication, FIPS Publication 197, for more information.

The encrypted code is generated by applying a 16-byte input to the AES encoder with a specific 16-byte encryption key. The encryption key is stored in a dedicated, read-only OTP memory preventing unauthorized users access to this sensitive information. A block diagram of the encryption method is shown in Figure 6.

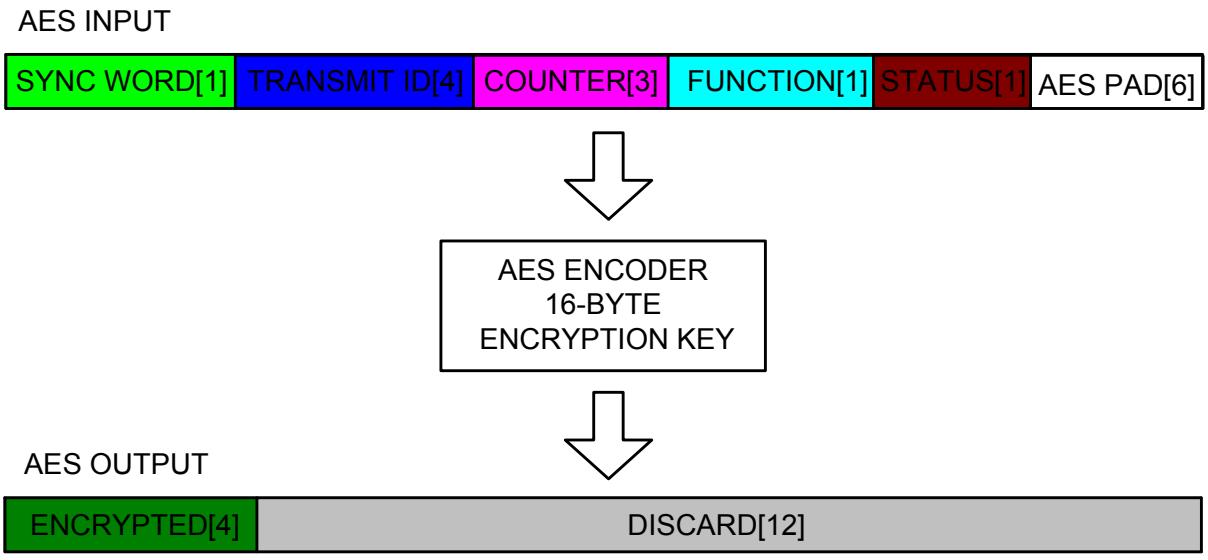


Figure 6. Encryption Method Block Diagram

The AES input consists of the 1-byte sync word, 4-byte transmit ID, 3-byte counter, 1-byte function, 1-byte status, and 6-byte AES pad. The AES pad is programmable with a default 10101010 byte pattern and is required to form the 16-byte input for the AES encoder. This input is applied to the 16-byte (128-bit) AES encoder to form a 16-byte AES encrypted output. In order to limit the packet size and conserve battery power, only the lower 4 bytes of the AES encrypted output is appended to the packet.

The encrypted message is different for each transmitter because of the unique 128-bit encryption key and the transmit ID of each transmitter. The transmit ID is transmitted in the open for the receiver to use for decryption but the unique 128-bit encryption key is only transmitted during association. Updating the synchronization counter on each button press guarantees each encrypted message is different from the previous message even if the same command is repeated. This prevents attacks from a RF recording and re-broadcasting device.

When encryption is disabled, the 4-byte encrypted message has a 10101010 byte pattern.

4.8.2. Transmission Format

The Si4010 supports Manchester, non-return-to-zero (NRZ), and run-length limited (RLL) data encoding. Manchester encoded data contains a transition within each bit period of data and is derived by exclusive ORing (XOR) the binary data with its clock signal and thus inherently contains clock information. A logic zero is represented by a low to high transition and a logic one is represented by a high to low transition where the transition occurs in the middle of the bit period. NRZ encoding is binary encoding of the data where a logic high is represented by one constant level and a logic low is represented by another constant level. NRZ data does not inherently contain clock information like Manchester encoded data. One by-product of Manchester encoding is that it needs twice the bandwidth of a similar NRZ encoded data resulting in a larger signal spectrum. RLL codes bound the length of repeated bits during which the signal does not change and thus helps with clock and data recovery as compared to NRZ codes. The default code format for OOK transmission is Manchester encoding and the default code format for FSK is (4,5) RLL.

The data rate of the Si4010 can range from 1.2 kbps to 20 kbps with 4.8 kbps as the default data rate. Thus the total time of one default packet with OOK modulation is 17 x 8 bits x (1/4.8 kbps) = 28.33 ms.

The Si4010 has a programmable transmit period and packet repetition rate. The transmit period consists of the transmit packet time, which is equal to 28.33 ms for

the default case, and an automatic low power mode time, which is equal to the transmit period minus the transmit packet time. During the low power time, an ultra-low power counter is enabled to keep track of time. The default transmit period is 100 ms. The packet repetition rate is defined as the number of times a packet is transmitted for a single button press. For example, if the repetition rate is equal to 1, then the transmitter only transmits the packet once for a single button press and then shuts down after transmission is complete. If the packet_repetition rate is x, where x > 1, the transmitter transmits the packet x number of times for a single button press condition. After the transmitter has transmitted the packet for the repetition rate, the device powers down, assuming the button is not held down. The default packet_repetition rate is 3.

ETSI 300 200 states that the RF transmit operation at 434 and 868 MHz requires duty cycle enforcement. The ultra-low power counter in the Si4010 can be enabled for this function by setting the ETSI_duty_cycle bit to a logic 1, but it is the responsibility of the users of this device to enforce and comply with all local radio-frequency transmission regulations.

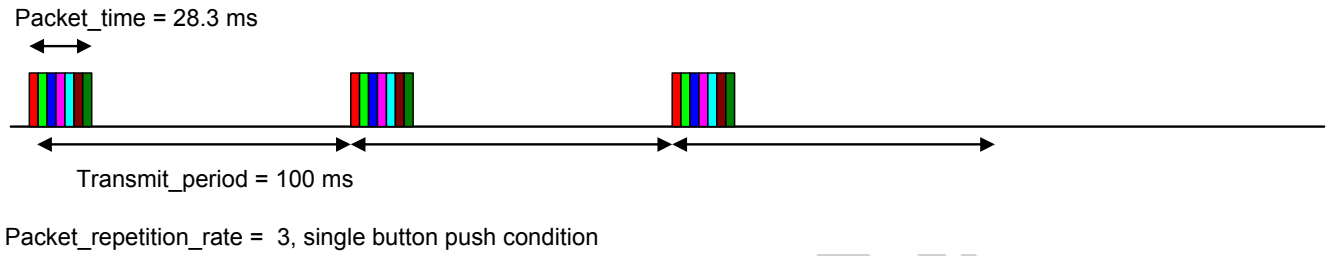


Figure 7. Transmission Format

4.8.3. Transmitter and Receiver Association

In order to have a receiver respond to a group of known transmitters, the receiver must pair up with its intended transmitter and obtain the transmitters' unique encryption key, transmit ID, and initial count value. The process of pairing the receiver to the transmitter is known as association and is used when receivers and transmitters are first paired together and when a new transmitter is introduced into an existing system such as when a previous transmitter is lost or stolen and needs to be replaced.

The Si4010 is placed into association mode when GPIO1 and GPIO2 are simultaneously held together for a time greater than the interval_association time, which is 3 seconds by default. In association mode, it is assumed the receiver is always on and the transmitter is near the receiver. Since security of the AES encryption key is of utmost importance, the transmit output power is reduced by a factor of 4 from normal transmit operation to comply with FCC regulations and also to reduce the transmission distance.

The association packet consists of a 3-byte preamble followed by a 1-byte sync word (1010 0001) and an AES encrypted message containing the transmitter's unique ID (4 bytes), initial count value (3 bytes), and the transmitter's unique AES encryption key (16 bytes) for a total packet length of 27-bytes. This encrypted message for the association packet is coded with a user programmable 16-byte association_encryption_key. This association_encryption_key is only used during the association process and the receiver must know this encryption key apriori in order to properly decode and store the transmit ID, initial count value, and encryption key for normal communication.

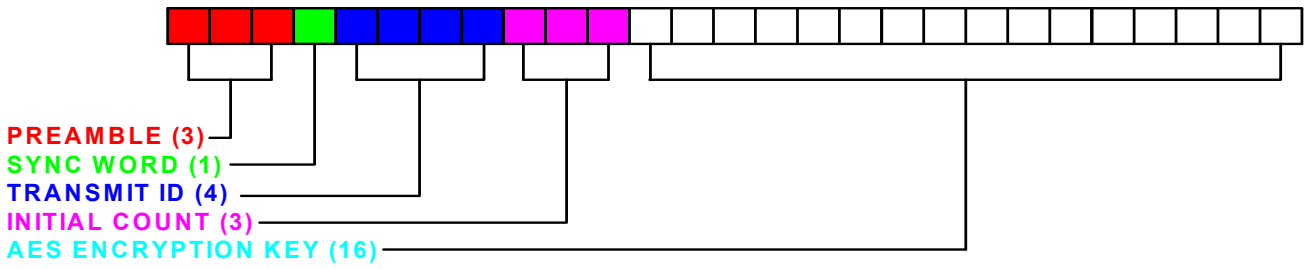


Figure 8. Association Packet Format

The association packet length of 27 bytes gives a transmit time of 27 x 8 bits x (1/4.8 kbps) = 45 ms. The packet repetition rate in association mode is set by the association_repeation_rate register and the default is 10.

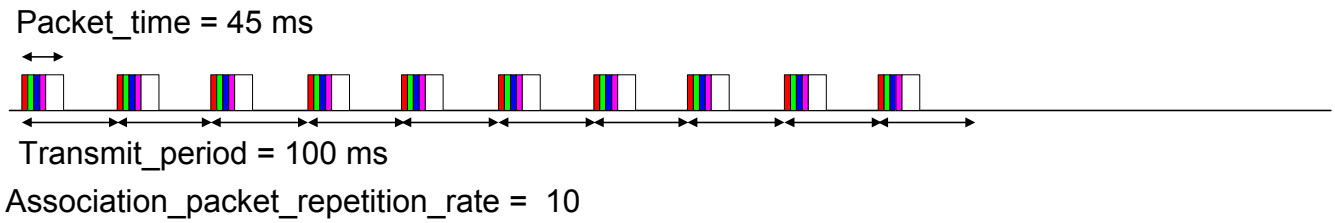


Figure 9. Association Transmission Format

4.8.4. Si4010 Turn-key Transmitter Configuration Registers

The following describes the turn-key Si4010 transmitter configuration registers. Development kit application parametrization software will allow modification of the registers through C2 interface for customer experimentation with turn-key application.

- Operating frequency: 315, 433.92, 868, 915 MHz
- Modulation type: OOK/ FSK
- Code format: Manchester, NRZ, (4,5) RLL code
- Data rate: 1.2 to 20 kbps
- Output power: –9.5 to +10 dBm, 0.25 dBm steps, antenna tuning enable/disable, 1% duty cycle enable/disable
- Button timing parameters: Debounce time, interval_2nd, interval_extend, interval_timeout, interval_association
- Synchronization counter: 3-byte initial count
- AES: enable/disable, 6-byte pad for AES encryption
- Transmit format parameters: Transmit_period, packet_repetition, ETSI_duty_cycle_enable
- Association: Association_encryption_key, association_packet_repetition

With read-only OTP registers for:

- Transmit device identification (ID) number, enable thermal random number generator for transmit device identification number
- 16-byte AES encryption key

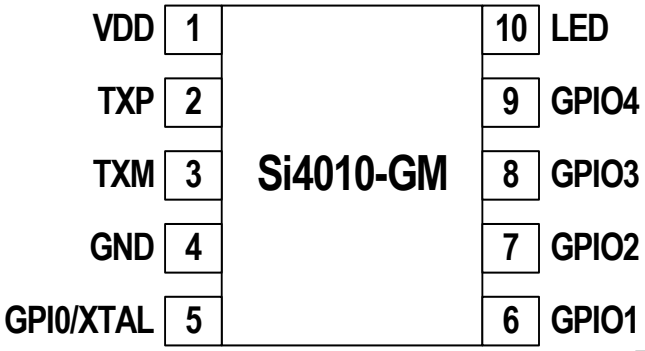
4.9. Custom Function Development

The Si4010 features a modular structure of library functions in ROM that can be overwritten in OTP memory to accommodate customers who have their own proprietary RKE communication protocol. Three kilobytes of OTP memory are available to customers who want to develop their own custom functions. The memory requirements for the functions are rather small. For example, the total memory requirements for the 128-bit AES encryption algorithm encoder is 671 bytes. Other typical custom functions include the encryption algorithm, synchronous counter, command register, GPIO functions, packet structure, transmission format, and the association packet.

The procedure for implementing a custom function involves identifying the function(s) that need to be replaced and re-writing the function(s) such that the new function(s) receives/passes the same parameters as the original function(s). After all of the new functions are complete, the main program must be re-written to address the new functions instead of the original ROM functions. Silicon Labs will provide engineering support to qualified customers interested in creating their own custom functions.

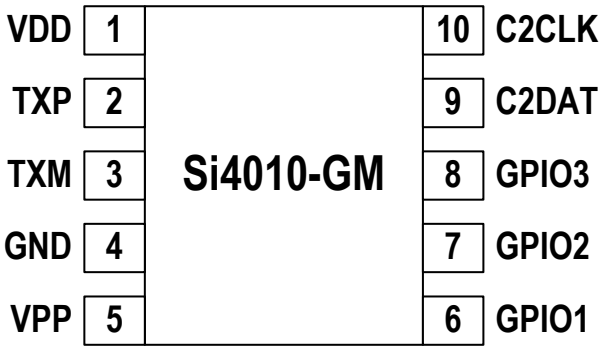
5. Pin Descriptions

5.1. Typical Application



Pin Number(s)	Name	Description
1	VDD	Power.
2,3	TXP, TXM	Transmitter differential outputs.
4	GND	Ground. Connect to ground plane on PCB.
5	GPI0/XTAL	General purpose input pin. Can be configured as an input pin for a crystal.
6, 7, 8, 9	GPIO[1:4]	General purpose input/output pins.
10	LED	Dedicated LED driver.

5.2. Programming/Debug Mode



Pin Number(s)	Name	Description
1	VDD	Power.
2	TXP	Transmitter differential output.
3	TXM	Transmitter differential output.
4	GND	Ground. Connect to ground plane on PCB.
5	VPP	+6.5 V required for OTP programming.
6, 7, 8	GPIO[1:3]	General purpose input/output pins.
9	C2DAT	C2 data input/output pin.
10	C2CLK	C2 clock interface.

6. Ordering Guide

Part Number*	Description	Package Type	Operating Temperature
Si4010-A10-GM	Crystal-less SoC Transmitter	QFN Pb-free	–40 to 85 °C
***Note:** Add an “(R)” at the end of the device part number to denote tape and reel option; 2500 quantity per reel.			

7. Package Markings

TBD.

8. Package Outline

Figure 10 illustrates the package details for the Si4010. Table 6 lists the values for the dimensions shown in the illustration.

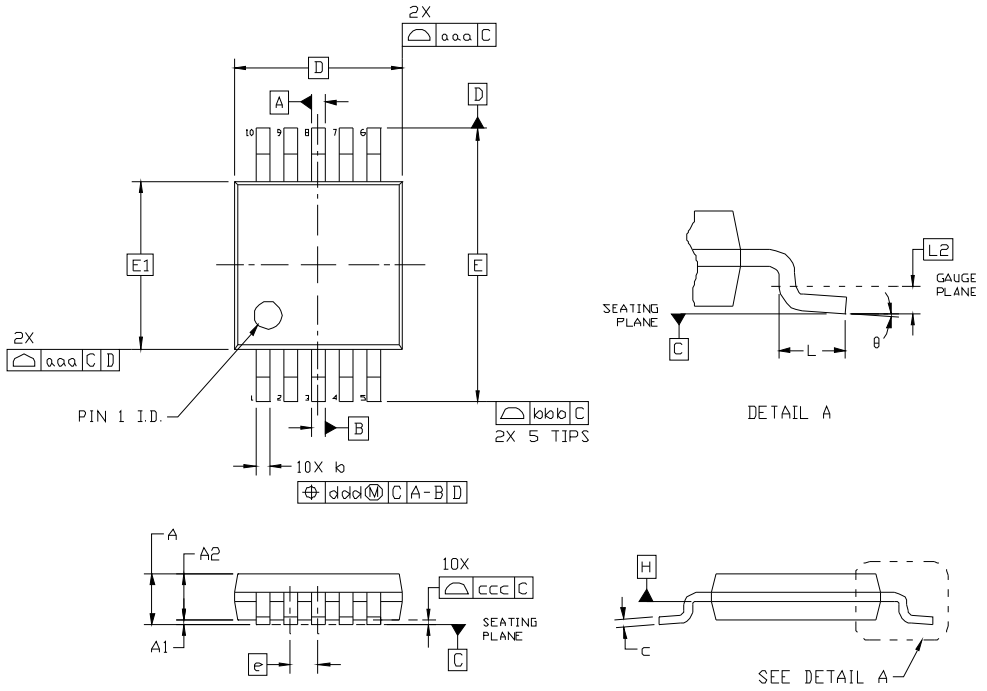


Figure 10. 10-pin MSSOP Package

Table 6. Package Dimensions

Symbol	Millimeters		
	Min	Nom	Max
A	—	—	1.10
A1	0.00	—	0.15
A2	0.75	0.85	0.95
b	0.17	—	0.33
c	0.08	—	0.23
D	3.00 BSC		
E	4.90 BSC		
E1	3.00 BSC		

Symbol	Millimeters		
	Min	Nom	Max
e	0.50 BSC		
L	0.40	0.60	0.80
L2	0.25 BSC		
θ	0°	—	8°
aaa	—	—	0.20
bbb	—	—	0.25
ccc	—	—	0.10
ddd	—	—	0.08

Notes:

1. All dimensions are shown in millimeters (mm).
2. Dimensioning and tolerancing per ASME Y14.5M-1994.
3. This drawing conforms to JEDEC Outline MO-187, Variation “BA.”
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

9. PCB Land Pattern

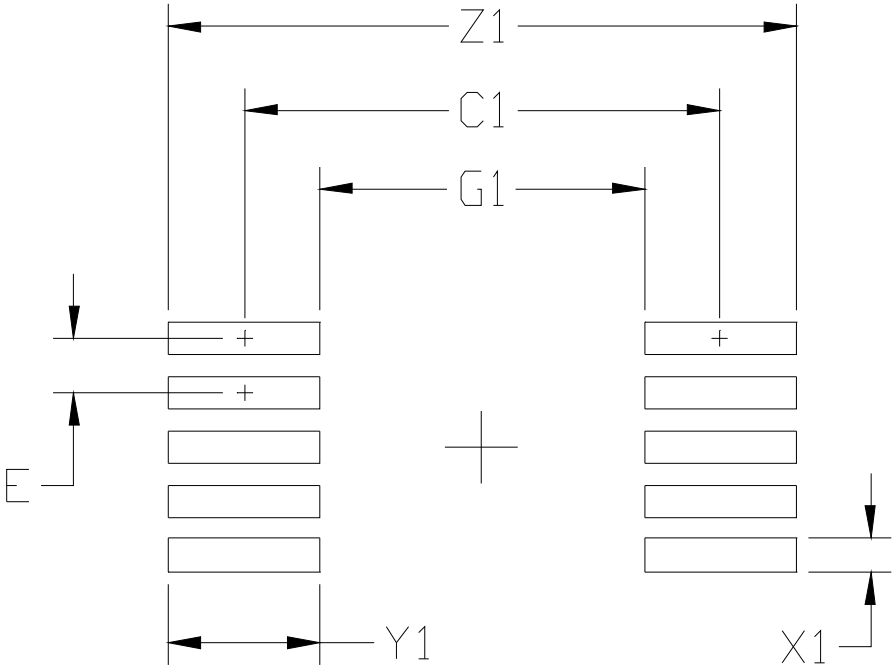


Figure 11.

Table 7.

Dimension	MIN	MAX
C1	4.40 REF	
E	0.50 BSC	
G1	3.00	—
X1	—	0.30
Y1	1.40 REF	
Z1	—	5.80

Notes:

General

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ASME Y14.5M-1994.
3. This Land Pattern Design is based on the IPC-7351 guidelines.
4. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05mm.

Solder Mask Design

1. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 m minimum, all the way around the pad.

Stencil Design

1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 1:1.

Card Assembly

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

10. Additional References

- FIPS Publication 197, Advanced Encryption Standard (AES), U.S. DoC/NIST, November 26, 2001. http://csrc.nist.gov/publications/fips/fips197/fips-197.pdf
- AN369: Antenna Interface for the Si401x Transmitters
- AN370: A Secure Unidirectional RKE System using the Si4010, Si4310, and MCU
- AN371: Software and C2 Interface

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