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Application Note
(Internal ROM Booting)

S3C2450X

RISC Microprocessor

June 25, 2008

Preliminary REV 0.03

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S3C2450X RISC Microprocessor
IROM(Internal ROM) Booting Application Note, Preliminary Revision 0.03

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Revision History

Revision No	Description of Change	Refer to	Author(s)	Date
0.00	- Initial release for review	-	Gr.Moon	Jan 16, 2008
0.01	- Circuit Check Point		Gr.Moon	April 25, 2008
0.02	- Clock Configuration		Gr.Moon	May 13, 2008
0.021	- eMMC		Gr.Moon	June 4, 2008
0.03	- GPA/GPK ports configuration in Group		Gr.Moon	June 25, 2008

NOTE: Revised parts are written in blue.

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1 Overview

This chapter explains overall scheme of internal ROM(IROM) boot with memory devices such as Samsung MoviNAND/iNand, MMC Card and pure Nand. eMMC boot with IROM is supported. In MMC specs ver 4.3 eMMC sends boot data when command signal is low and SD power is on. This type of eMMC boot is not supported

In S3C2450 IROM boot releases retention I/O(resets I/O) when it wakes up for recognizing Boot Device by GPC5/6/7. Refer section1.4.

1.1 H/W Feature

To use IROM bootloader, several hardware features are required.

- S3C2450X microprocessor based on ARM926EJ-S
- 32KB Internal ROM (IROM)
- 64KB SRAM (64-8KB)
- 8KB Stepping Stone (Internal SRAM)
- General SDRAM and Controller
- 4 Bit High Speed MMC Controller (channel 1)
- Nand Flash Controller

1.2 Feature

- MMC Boot (MMC Specification 4.2 compatible)
- Nand Boot (With H/W 8-Bit ECC)
- Secure mode support(Verify Integrity of Bootloader for all boot-up device)

1.3 Advantage of I-Rom booting

1. Reduce BOM Cost

   => In I-Rom booting with Movinand/INAND/MMC Card, System can boot without booting Rom

     So. There is no need other booting rom (like nor flash)

2. Improve the Read Disturbance

   => In I-Rom booting with nand flash, S3C2450 can support 8-bit H/W ECC

3. Reduce the production cost (Option)

   => you can program nand flash memory with SD card

   => so. There is no need Gang programmer

1.4 Circuit Design Check Point

① **To select IROM boot device GPC5/6/7 is used. These I/Os are recommended using only for IROM booting device selection.**

② **When S3C2450 wakes up using IROM, all GPIO ports in VDD_SD domain are automatically released from the retention state. Whereas other GPIO ports are not released from the retention state include GPC5/6/7 ports which are applied to check the booting devices (NAND, moviNAND, iNAND). Therefore users are careful to control GPC5/6/7 ports. After wake-up from the sleep mode, these ports must contain a booting device configuration value. Therefore, these ports must be properly configured before entering the sleep mode. (Input and pull-up/down resister disable)**

The retention GPIO ports are reset after releasing the retention state by S/W (write '1' to PWROFF_SLP bit in RSTCON register). That means all of these ports have a reset value (input and pull-down enable) after releasing the retention state.
For example, if the port is set to 'output high state' during the retention state, it will be automatically changed to 'input and pull-down state'.

GPA, GPK, GPG[7:0] and GPF ports are the alive GPIO. These ports are not reset even though user writes '1' into PWROFF_SLP bit in RSTCON register. These ports are useful to maintain the continuous signal.

But, GPA and GPK ports have some restrictions. These ports are controlled by PDDMCON and PDSMCON registers in sleep mode instead of GPACON, GPADAT, GPKCON, GPKDAT and GPKUDP registers. PDDMCON and PDSMCON registers do not control each port individually. That is to say, if the ports are same group in PDDMCON and PDSMCON register it is impossible to have different state(high, low or Hi-z)

I/O ports in VDD_SD power domain (automatically releasing from the retention state after wakeup)

VDD_SD	1.7 ~ 3.6V	SPIMISO[1:0], SPIMOSI[1:0], SPICLK[1:0], TXD[3;2], RXD[3:2], SS[1:0], SD0_nWP, SD0_nCD, SD0_LED, SD0_CLK, SD0_CMD, SD0_DAT[7:0], SD1_CLK, SD1_CMD, SD1_DAT[3:0], **PCM1_FSYNC(2450), PMC1-SCLK(2450), PCM1-CDCLK(2450), PCM1-SDI(2450), PCM1-SDO(2450), I2S1_LRCK(2450), I2S1_SCLK(2450), I2S1_CDCLK(2450), I2S1_SDI(2450), I2S1_SDO(2450)** **Note:** Blue characters are added ports compare to S3C2443.
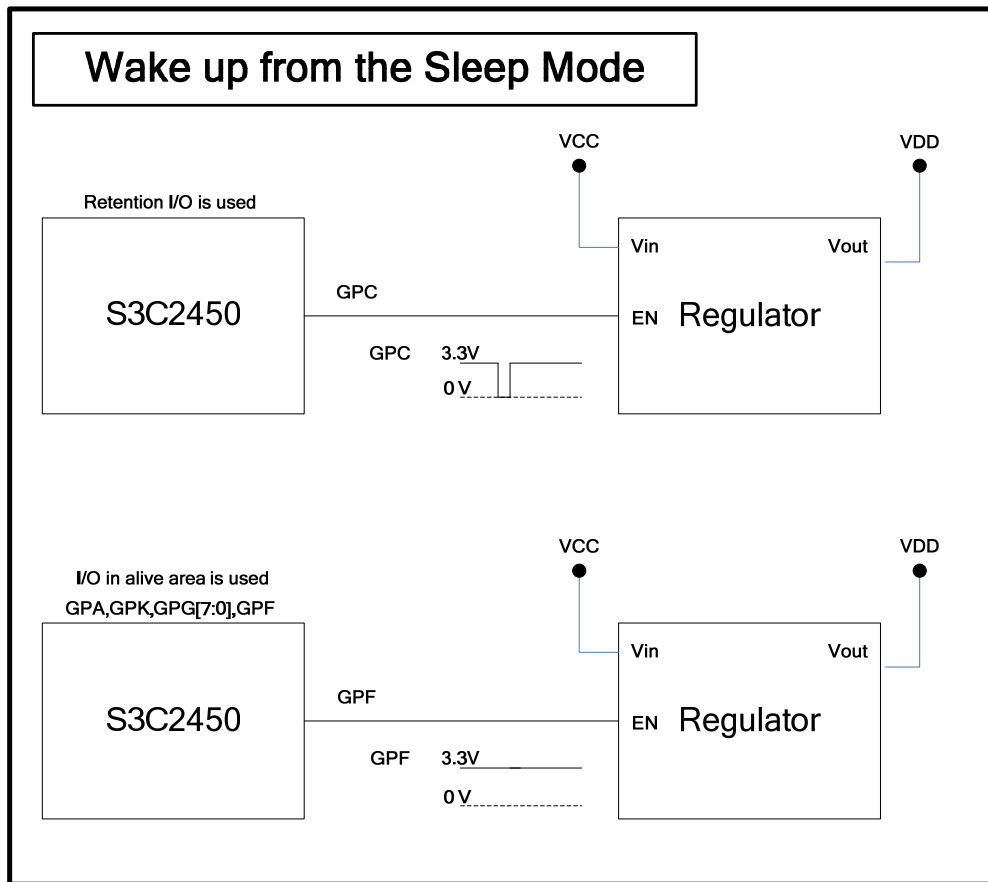
Figure 1. When retention is released, Two examples of the I/O signal change

1.5 Version

: 2450 Internal ROM V1.0

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2 Operation

2.1 Operating Sequence
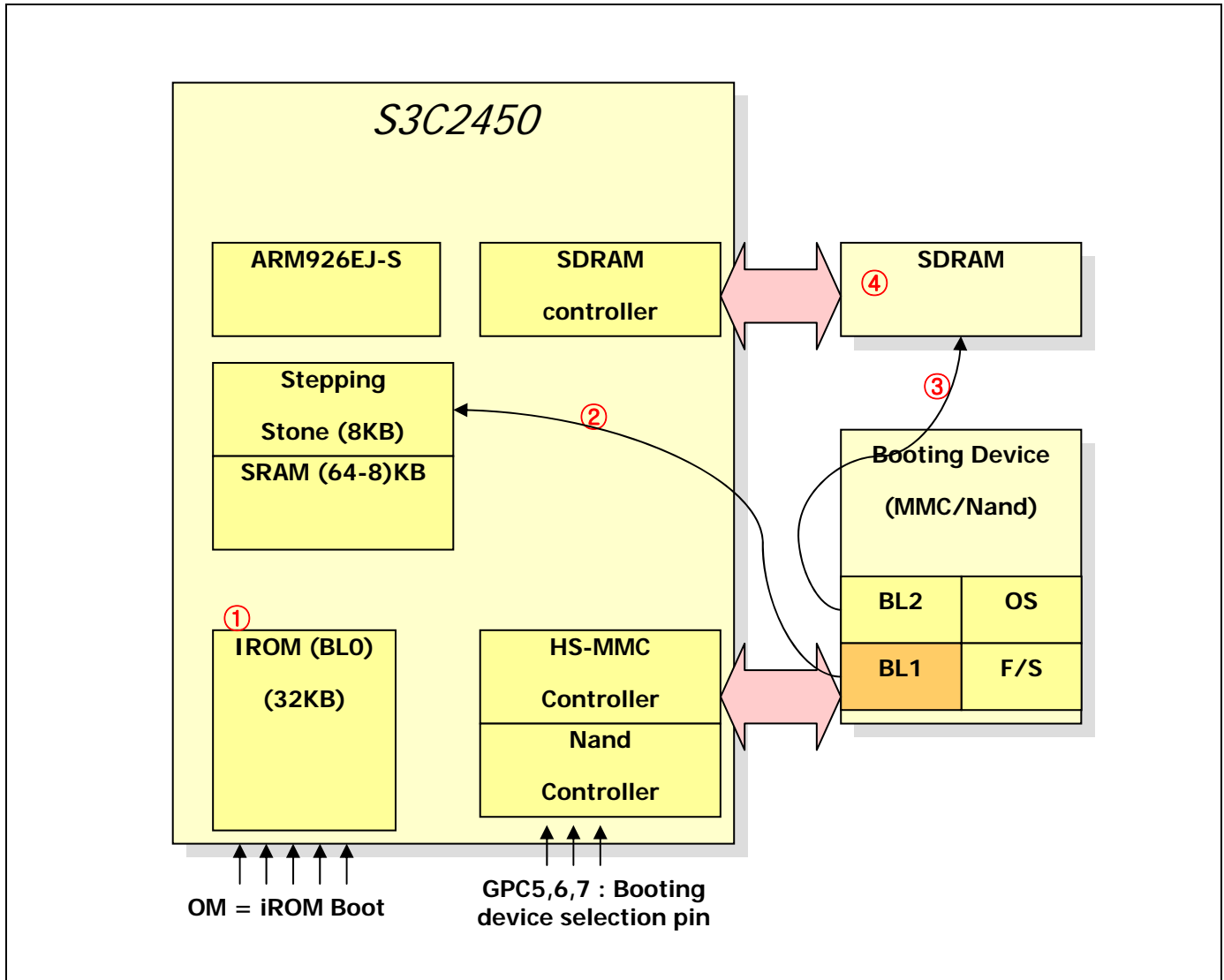
Figure 1. Overall boot-up diagram

BL1 : Its size should be under 8K because BL1 is located in Stepping Stone(8K)

BL2 : There is no limit in its size, so it can locate any place in SDRAM area

① IROM can do initial boot up : initialize system clock, device specific controller and booting device.

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② IROM boot codes can load 8KB of bootloader to stepping stone. The 8KB boot loader is called BL1.

③ BL1 will do : BL1 can initialize system clock, UART, and SDRAM for user. Thereafter, BL1 will load remained boot loader which is called BL2 on the SDRAM

④ Finally, jump to start address of BL2. That will make good environment to use system.

2.2 IROM(BL0) boot-up sequence

1. Disable the Watch-Dog Timer

2. Initialize the Block Device Copy Function. (see "Device Copy Function" on chap 2.6)

3. Initialize the stack region (see "memory map" on chap 2.4)

4. Initialize the PLL. (see "clock configuration" on chap 2.7)

5. Initialize the instruction cache

6. Initialize the heap region. (see "memory map" on chap 2.4)

7. Copy the BL1 to the stepping stone region (see "Device Copy Function" on chap 2.6)

8. Verify the integrity of BL1

9. Jump to the stepping stone

2.3 IROM(BL0) boot-up diagram
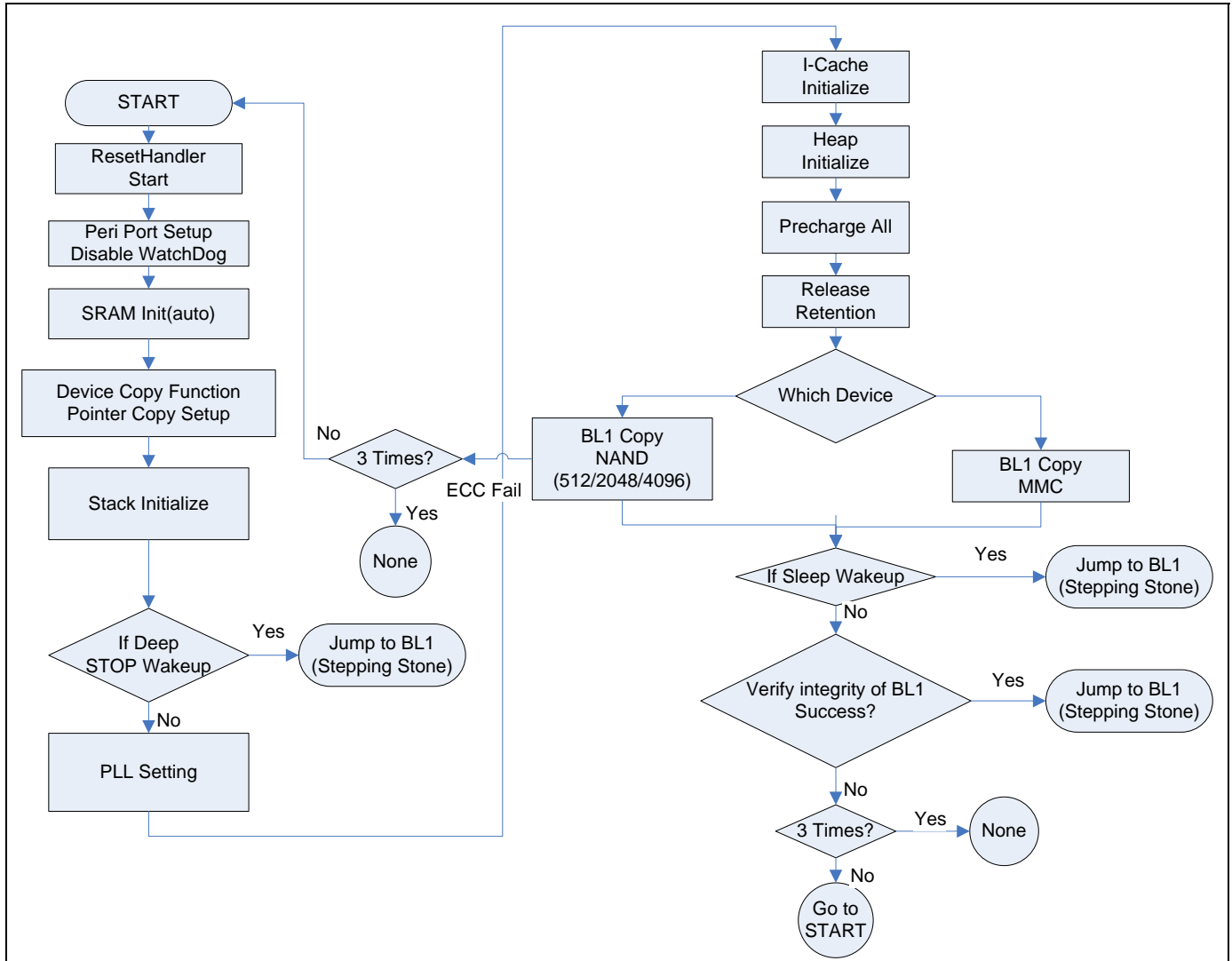
Figure 2. IROM(BL0) boot-up diagram

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2.4 Memory Map

Type	Address	Usage	Size
I-RAM	0x40000000 ~ 0x40001FFF	Stepping Stone (BL1)	8KB
SRAM	0x40002000 ~ 0x400021FF	Secure Key(512Bytes)	(64-8)KB
	0x40002200 ~ 0x40002FFF	Reserved	
	0x40003000 ~ 0x40003FFF	Heap (Reserved for global variable)	
	0x40004000 ~ 0x40010000	Device Copy Function Pointer (12Byte) Stack	

Table1. Memory Map

2.5 Global Variable

   If the MMC device is used to boot up, the information of MMC card must be saved in the special area. Refer to table 2 and Figure 3.

Address	Name	Usage
0x40003FFC	globalBlockSizeHide	Total block count of the MMC device.
0x40003FF8	globalSDHCInfoBit	globalSDHCInfoBit[31:16] : RCA(Relative Card Address) Data globalSDHCInfoBit[2] : SD Card globalSDHCInfoBit[1] : MMC Card globalSDHCInfoBit[0] : High Capacity Enable
0x40003FF4	globalNandECCfailureCount	Total number of ECC Fail

Table2. Special global variable for MMC & Nand boot mode.

```
// Card Information
#define globalSDHCInfoBit              *((volatile unsigned int*) GLOBAL_VAL_BASE -0x8))
// SD/MMC Card Block Size.
#define globalBlockSizeHide            *((volatile unsigned int*)( GLOBAL_VAL_BASE -0x4))
// Nand ECC Fail Counter
#define globalNandECCfailureCount      *((volatile unsigned int*)(GLOBAL_VAL_BASE-0x10))
// O/S kernel loading…
CopyMovitoMem( globalBlockSizeHide - 100, 80, (unsigned int*)0x50200000, 12000000, false);
```

Figure 3. Code reference

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2.6 Device Copy Function

The S3C2450 internally has a ROM code of block copy function for boot-u device. Therefore, developer may not needs to implements device copy functions. These internal functions can copy any data from memory devices to SDRAM. User can use these function after ending up the internal ROM boot process completely.

Address	Name	Usage
0x40004000	NF8_ReadPage	This internal function can copy any data from Nand device to SDRAM. User can use this function after ending up to the IROM boot process completely. (8-Bit ECC Check) Note. 512 Page Nand Only
0x40004004	NF8_ReadPage_Adv	This internal function is advanced NF8_ReadPage function. (8-Bit ECC Check) Note. 2048, 4096 Page Nand Only.
0x40004008	CopyMovitoMem	This internal function can copy any data from MMC device to SDRAM. User can use this function after ending up to the IROM boot process completely.

Table3. Device Copy Function Pointer

● **Nand Flash Copy Function Address (8-Bit ECC Check)**

```
/**
 * This Function copies a block of page to destination memory.( 8-Bit ECC only )
 * @param uint32 block : Source block address number to copy.
 * @param uint32 page : Source page address number to copy.
 * @param uint8 *buffer : Target Buffer pointer.
 * @return int32 - Success or failure.
 */
#define NF8_ReadPage(a,b,c) (((int(*)(uint32, uint32, uint8*))(*((uint32 *)0x0C004000)))(a,b,c))
```

Figure 4. Definition Nand Flash Block Copy Function for 8-Bit-ECC

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● **Nand Flash Copy Function Address (8-Bit ECC Check)**

```
/**
 * This Function copies a block of page to destination memory( 8-Bit ECC only )
 * @param u32 block : Source block address number to copy.
 * @param u32 page : Source page address number to copy.
 * @param u8 *buffer : Target Buffer pointer.
 * @return int  - Success or failure.
 */
#define NF8_ReadPage_Adv(a,b,c) (((int(*)(uint32, uint32, uint8*))(*((uint32 *)0x40004004)))(a,b,c))
```

Figure 5. Definition Nand Flash Block Copy Function for 8-Bit-ECC

● **MMC Copy Function Address**

External source clock parameter is used to fit EPLL source clock at 25MHz.

```
/**
 * This Function copy MMC(MoviNAND/iNand) Card Data to memory.
 * Always use EPLL source clock.
 * This function works at 25Mhz.
 * @param u32 StartBlkAddress : Source card(MoviNAND/iNand MMC)) Address.(It must block address.)
 * @param u16 blockSize : Number of blocks to copy.
 * @param u32* memoryPtr : Buffer to copy from.
 * @param u32 extClockSpeed : External clock speed(per HZ)
 * @param bool with_init : determined card initialization.
 * @return bool(u8) - Success or failure.
 */
#define CopyMovitoMem (a,b,c,d,e)(((bool(*)(u32,u16,u32*,u32,bool)) \
(*((u32 *)0x40004008))) (a,b,c,d,e))
```
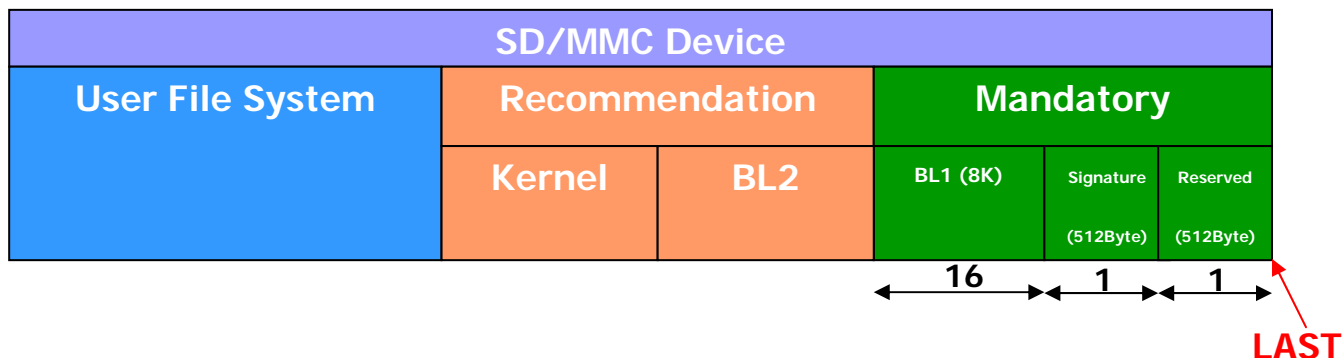
Figure 6. Definition MMC Block Copy Function

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2.7 Boot Block Assignment Guide

2.7.1 SD/MMC Device Boot Block Assignment
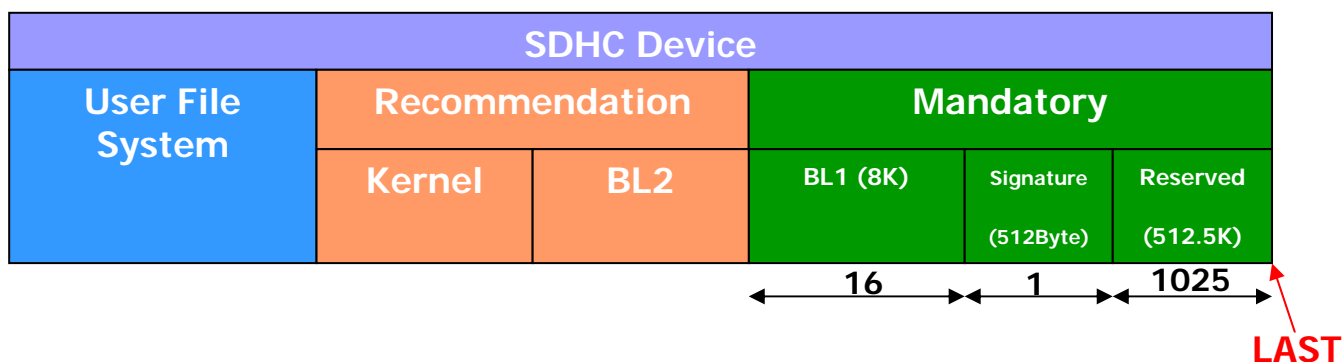
[SD/MMC 1Block = 512 Byte]

This guide is a sample but there are 3 mandatory rules.

- The last one block shouldn't be used. (Reserved)

- One block has to be assigned for signature which is located at offset [LAST – 2]

- BL1(1st Boot loader) should be located at offset [LAST – 18]

2.7.2 SDHC Device Boot Block Assignment

[SD/MMC 1Block = 512 Byte]

This guide is a sample but there are 3 mandatory rules.

- The last 1025 blocks shouldn't be used. (Described below known problem)

- One blocks has to be assigned for signature which is located at offset [LAST – 1026]

- BL1(1st Boot loader) should be located at offset [LAST – 1042]

Known Problem

When iROM boot with SDHC card, calculated card size is smaller than original card size, exactly 1024 blocks. So, SDHC card has additional reserved blocks(512Kbyte).

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2.8 Clock Configuration

The IROM bootloader has a fixed value of PLL setting. So developer has to change PLL setting value at the stepping stone bootloader. Fixed PLL has been influenced by the external crystal oscillator. Refer to table4.

- MPLL : M:320, P:4, S:2

- EPLL : M:60, P:2, S:4, K:0

Ext. Crystal(Mhz)	ARM Clock (MHz)	HCLK (MHz)	EPLL Clock (MHz)
10	100.000	50	18.8
11	110.000	55	20.6
12	120.000	60	22.5
13	130.000	65	24.4
14	140.000	70	26.3
15	150.000	75	28.1
16	160.000	80	30.0
17	170.000	85	31.9
18	180.000	90	33.8
19	190.000	95	35.6
20	200.000	100	37.5

Table 4. S3C2450 IROM clock configuration (BL0 Execution Time Only)

Note. MPLL configuration

$$FOUT = MDIV \times FIN / (PDIV \times 2^{SDIV})$$

EPLL configuration

$$FOUT = (MDIV + KDIV / 2^{16}) \times FIN / (PDIV \times 2^{SDIV})$$

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3 Circuit Description with SMDK Board

3.1 IROM Jumper Configuration (refer to S3C2450 cpu board schematic)
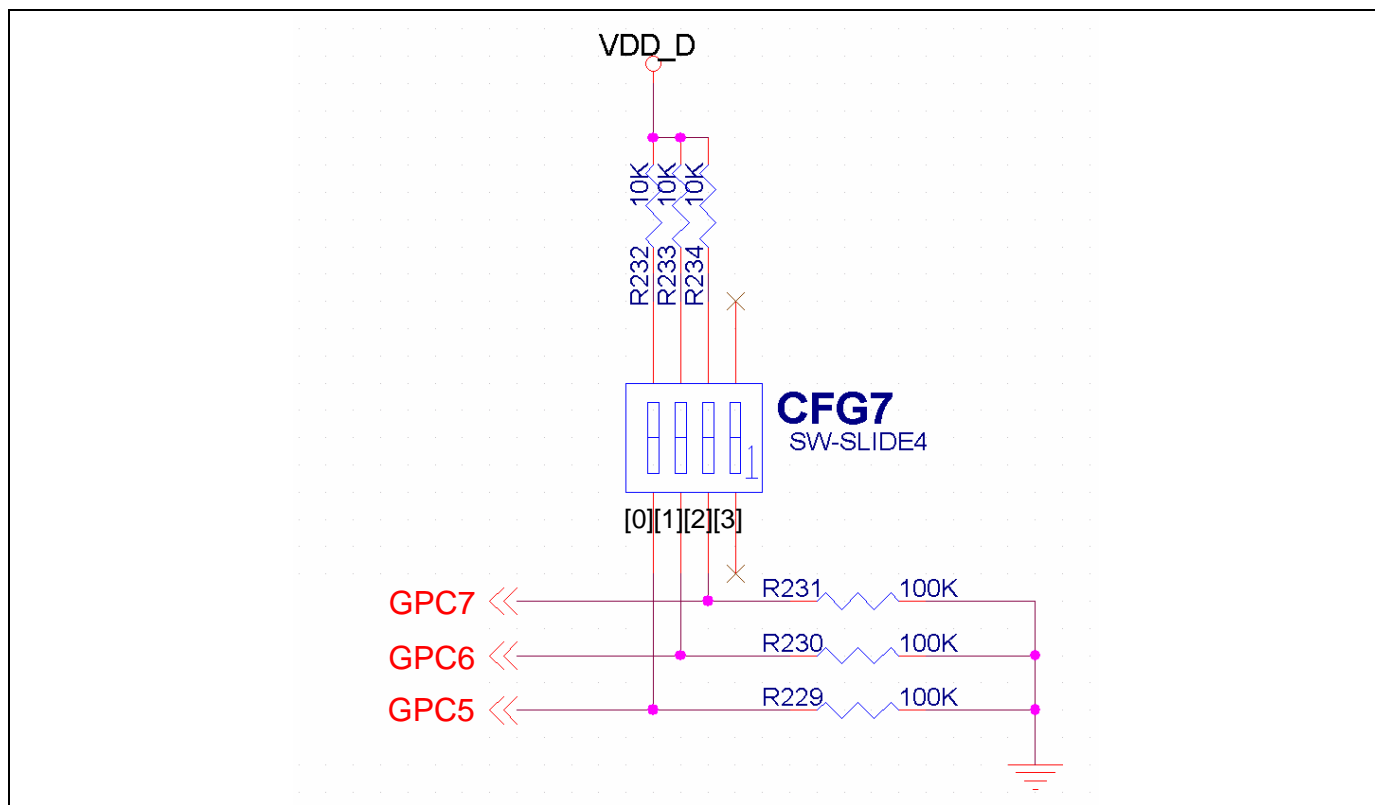

Figure 9. Boot device selection logic.

Note. Rising time is influenced by R232, R233, R234 Strength. (GPIO default input is pull-down.)

3.2 IROM Booting Device Configuration.

	Page	Address Cycle	GPC7, [2]	GPC6, [1]	GPC5, [0]
MMC(MoviNAND/iNand)	-	-	0	0	0
Reserved	-		0	0	1
Nand	512	3	0	1	0
		4	0	1	1
	2048	4	1	0	0
		5	1	0	1
	4096	5	1	1	0

Table 3. IROM boot pin description.

4 Error handling

4.1 Nand ECC failure

When Nand uncorrectable ECC error detected, GPC5 is toggled refer to Figure 10.

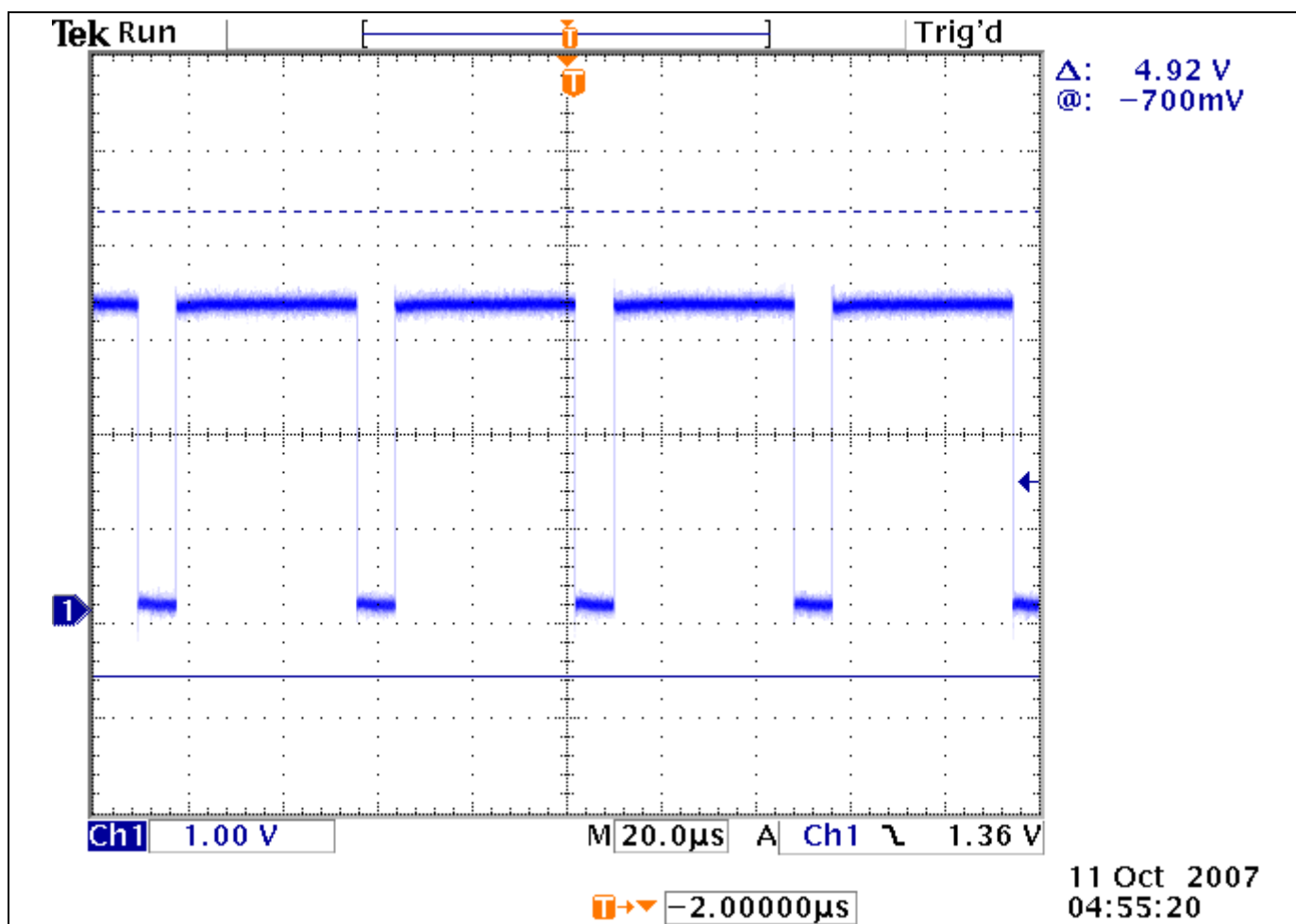Duty rate is 90% high duration, 10% Low (High Toggle)

Figure 10. Nand ECC failure waveform

4.2 Verification failure of BL1 integrity (Secure boot mode only)

When verification of BL1 integrity failure is detected, GPC5 is toggled refer to Figure 11.

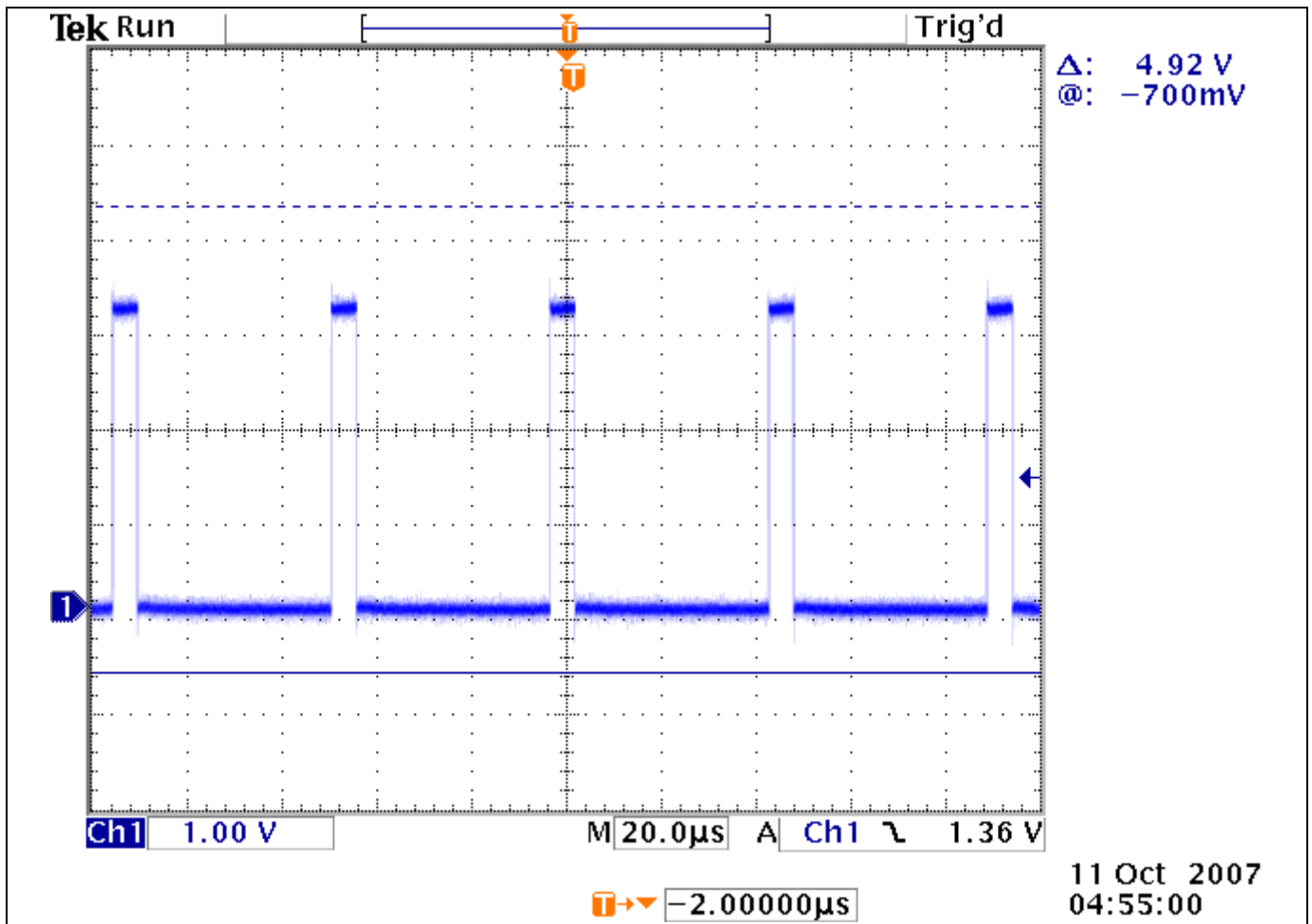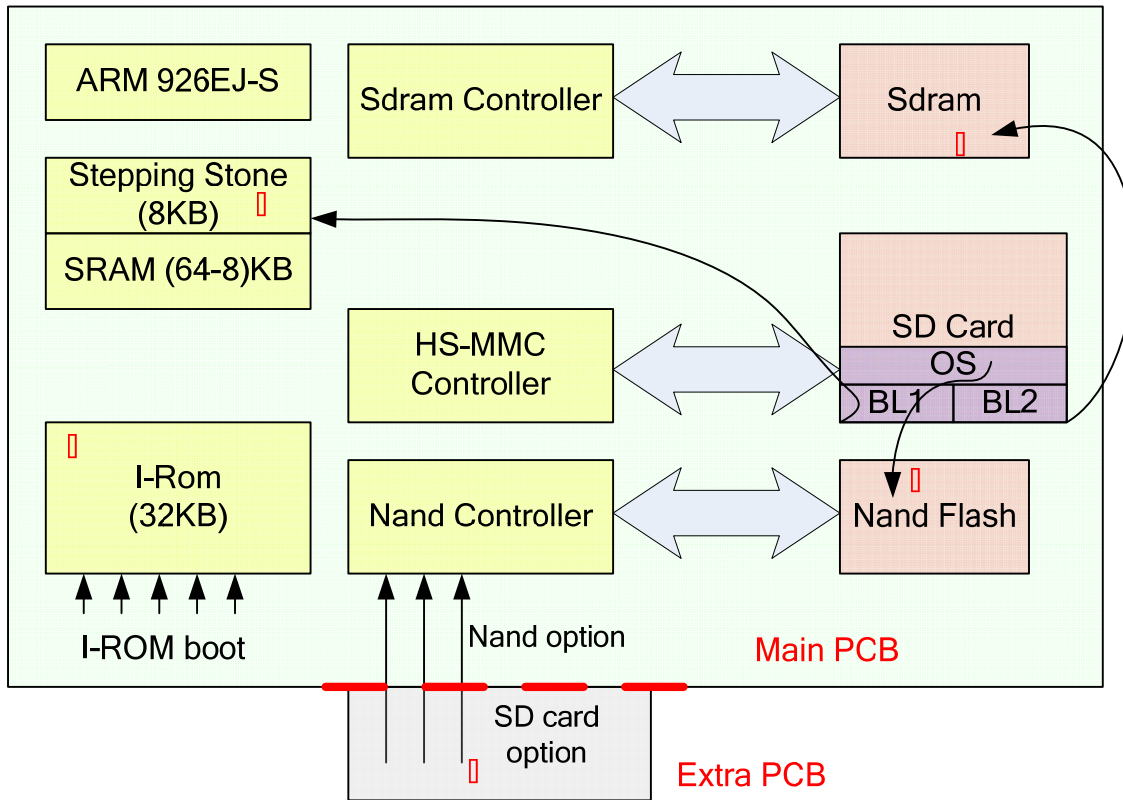Duty rate is 10% high duration, 90% Low (Low Toggle)

Figure 11. Bootloader integrity failure waveform

5. How to Program nand flash without Gang writer

5.1 Block Diagram

① IROM can do initial boot up with SD Card Option

=> initialize system clock, device specific controller and booting device.

② IROM boot codes can load BL1 to stepping stone.

③ BL1 will do : BL1 can initialize system clock, UART, and SDRAM for user. Thereafter, BL1 will load remained boot loader which is called BL2 on the SDRAM

④ jump to start address of BL2. and Program OS image to Nand flash memory

⑤ Finally, Cut Extra PCB Off, then you can boot I-ROM with Nand option

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