Document Title

A7103 Data Sheet

Revision History

Rev. No.	History	Issue Date	Remark
0.0	Initial issue	Aug. 18th, 2006	Preliminary
0.1	Modify DC, AC spec	March 2 2007	
0.2	Modify pin configuration		
0.3	Add 315,868,915 option	2007/4/17	

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Preliminary ***315/433/868/915MHz ASK/FSK Transceiver***

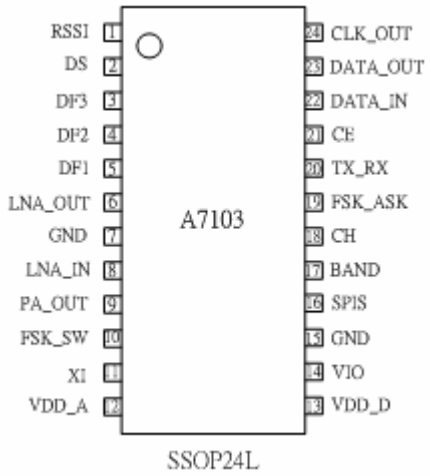
Typical Applications

- Remote Control.
- AMR (Auto Meter Reading).
- Security system.
- TPMS (Tire Pressure Measure System).

Features

· A7103A for 315MHz/433MHz, A7103B for 868/ 915MHz.
· High link budget: Distance up to 1Km is possible.
For 433MHz, Tx +10dBm, Rx -108dBm@ FSK 20Kbps BER<10E-3.
-109dBm @ ASK 20Kbps BER<10E-3.
· Very low current consumption: Typical Tx 14.5mA @ FSK, 7.5mA@ ASK.
Rx 8.5mA.
· Very simple control interface: 3~6 control signals.
· Support multi channels.
· High integration: VCO, PLL, PA, LNA, Image Reject Mixer, IF Filter, Limiter, RSSI, Data Slicer, AFC, AGC…
· Very few external components: No need external filters.
· Build in image rejection mixer. Selectable IF band width (100, 200, 300 KHz).
· Wide operating range: VDD=2.2~3.3V (IO 2.0~4.2V). T=-40~+85/125℃.
· Auto ramp-up sequence control to optimize power consumption. Xtal→PLL→ T/RX.
· One receiver for different systems: Switching between ASK/FSK is possible.
· Auto calibration to compensate process/temperature/voltage variation.
· Support typical 4/12/13.56/16MHz low cost crystal.

Pin Configuration



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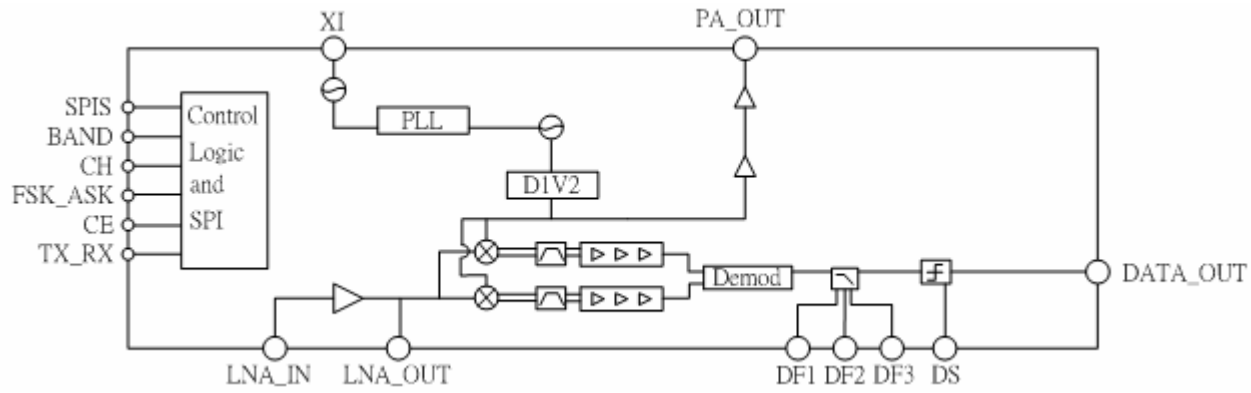
Pin Description

Pin No.	Pin Name	
1	RSSI	Analog RSSI output. Connect a capacitor to GND.
2	DS	Data slicer bypass. Connect a capacitor to GND
3	DF3	Data filter capacitors.
4	DF2	
5	DF1	
6	LNA_OUT	LNA output matching.
7	GND	Connect to PCB ground.
8	LNA_IN	LNA input matching.
9	PA_OUT	Tx power amplifier output.
10	FSK_SW	FSK deviation setting. Connect to a capacitor.
11	XI	Crystal oscillator input.
12	VDD_A	Analog power input.
13	VDD_D	Digital power input.
14	VIO	Digital I/O voltage. For internal level shift VDD.
15	GND	Connect to PCB ground.
16	SPIS	SPI selection. Low→disable SPI. Pin 17~19 will be configured as BAND, CH and FSK_ASK. High→ enable SPI. Pin 17~19 will be configured as SPI_STB, SPI_CLK and SPI_DATA.
17	BAND	Frequency selection. Low→315MHz. High→ 433MHz .
	SPI_STB	SPI latch strobe.
18	CH	Channel selection. Low→Channel 0. High→ Channel 1.
	SPI_CLK	SPI clock input.
19	FSK_ASK	Modulation selection. Low→ASK. High→FSK.
	SPI_DATA	SPI data input.
20	TX_RX	TX/RX selection. Low→RX. High→TX. With internal 300KΩ pull low resistor.
21	CE	Chip enable. Low→Sleep mode. High→Active mode.
22	TX_DATA	Transmitted data input. With internal 300KΩ pull low resistor.
23	RX_DATA	Received data output.
24	CLK_OUT	Clock output for micro controller. $F_{CLK\_OUT}=F_{xtal}/4$ or 16.

Notes: Please refer to page 4 "**Circuit Description**" for detail definitions.

Block Diagram



Specification

General Test Condition: Ta = 25ºC, Fin=434MHz, VDD=3.0V

Parameter	Description		Min.	Typ.	Max.	Unit
General						
Operating temperature			-40		85/125	°C
Supply voltage	VDD_A, VDD_D		2.2	2.8	3.3	V
Current consumption	Sleep mode (all circuit off)		0.1	0.5		uA
	Standby mode			0.8		mA
	PLL mode			3.5		
	Rx mode			8.5		
	Tx mode (FSK), +10dBm output			14.5		
	Tx mode (ASK) , +10dBm output, 50% duty.			7.5		
Crystal Frequency				4~16		MHz
Crystal Tolerance	Depends on application			+/-50	+/-100	ppm
Tx						
Frequency Range	A7103A			300 ~ 500		MHz
	A7103B			800~1000		
Data Rate	FSK		2		20	kbps
	ASK		2		20	
Output Power	F=314.8Hz. VDD=3.0V		8	10	11	dBm
	F=434MHz. VDD=3.0V		8	10	11	
	F=868.2MHz. VDD=3.0V		6	8	9	
	F=915MHz. VDD=3.0V		5	7	8	
Phase Noise	F=434MHz.	Offset=100KHz		-85		dBc/Hz
		Offset=1MHz		-98		
Reference Spur	F=434MHz.			-45		dBc
Rx						
Sensitivity	434MHz	FSK Bit rate=20K, Fdev=38KHz, BER<1E-3. IFBW=100KHz		-108		dBm
		ASK Bit rate=20K, BER<1E-3, IFBW=100KHz		-109		
	314.8MHz	FSK Bit rate=20K, Fdev=38KHz, BER<1E-3. IFBW=100KHz		-108		

		ASK Bit rate=20K, BER<1E-3, IFBW=100KHz		-109		
	868.2MHz	FSK Bit rate=20K, Fdev=38KHz, BER<1E-3. IFBW=100KHz		-106		
		ASK Bit rate=20K, BER<1E-3, IFBW=100KHz		-106		
	915MHz	FSK Bit rate=20K, Fdev=38KHz, BER<1E-3. IFBW=100KHz		-105		
		ASK Bit rate=20K, BER<1E-3, IFBW=100KHz		-105		
IF bandwidth	BW[1:0]=00			100		KHz
	BW[1:0]=01			200		
	BW[1:0]=1X			300		
Max input	Enable AGC, ASK			-10		dBm
	Enable AGC, FSK			0		
Image rejection	434MHz		20	27		dB
RSSI	Dynamic range			85		dB
	Lower level			-120		dBm
	Upper level			-35		dBm
Outband blocking	+/- 1.5MHz			50		dBc
	+/- 2MHz			60		
	+/- 3MHz			65		
	+/- 10MHz			70		
	+/- 20MHz			70		

Maximum Ratings

Characteristic	Pin name/symbol	Rating	Unit
Power supply voltage	All VDD	5.5	V
Input pin voltage		5	V
Storage temperature range	T_{stg}	-55~150	°C

Circuit Description

1. Control interface:

User can control A7103 by hardware pins only or through SPI for performance optimization.

For A7103A (433/315MHz band), chip state can be controlled by SPI or hardware pins.

(1) Total by hardware pins: Set pin 16 **SPIS** to low to disable SPI.

All comment can be send by control pin 17~21. Also,

a. Crystal frequency: Must be around 13.56MHz.

b. Channel: Support two channels only.

c. IF filter bandwidth: Fix 300KHz.

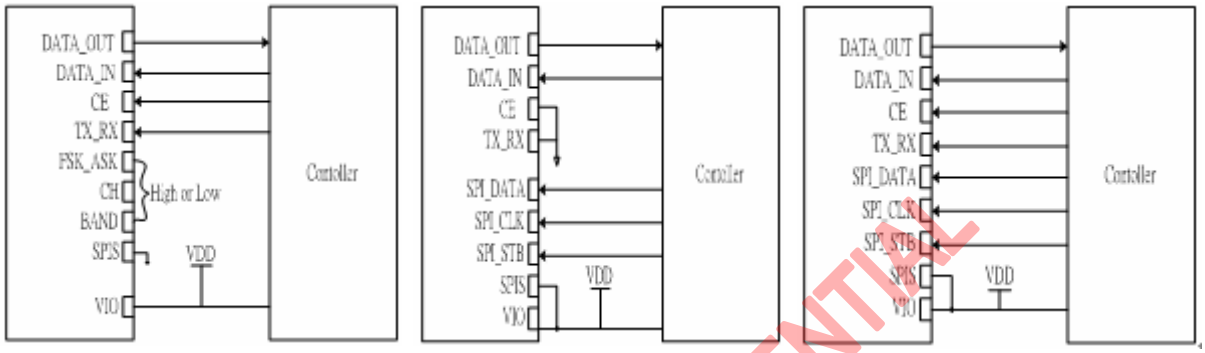
d. CLK_OUT divider ratio: Fix /16.

(2) Total by SPI: Set pin 16 **SPIS** to high and **Register 1** bit 1 **CTLS**=0.

All comment should be send through SPI. (Include TX_RX, CE)

(3) Partial by SPI: Set pin 14 **SPIS** to high and **Register 1** bit 1 **CTLS**=1.

TX_RX and CE should be controlled by pin 20~21. Other parameters set by SPI.



(1) By hardware pins (2) Total by SPI (3) Partial by SPI

For A7103B (868/915MHz band), SPI must be used. (ie, pin 14 **SPIS must be** high)

(1) Total by SPI: Set pin 16 **SPIS** to high and **Register 1** bit 1 **CTLS**=0.

All comment should be send through SPI. (Include TX_RX, CE)

(2) Partial by SPI: Set pin 14 **SPIS** to high and **Register 1** bit 1 **CTLS**=1.

TX_RX and CE should be controlled by pin 20~21. Other parameters set by SPI.

2. SPI:

There are two registers in SPI.

Register 0

No	D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15
Name	**0**	**0**	**NA0**	**NA1**	**NA2**	**NA3**	**NB0**	**NB1**	**NB2**	**NB3**	**NB4**	**NB5**	**NB6**	**NB7**	**R0**	**R1**
Reset			**1**	**0**	**1**	**1**	**1**	**1**	**0**	**0**	**0**	**0**	**1**	**0**	**0**	**1**

Register 1

No	D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15
Name	**0**	**1**	**CTLS**	**TX_RX**	**CE**	**FSK_ASK**	**CH**	**IFB0**	**IFB1**	**CKS**	**STBY**	**ULS**	**TB0**	**TB1**	**TB2**	**TB3**
Reset			**0**	**0**	**0**	**1**	**0**	**0**	**1**	**0**	**0**	**1**	**1**	**1**	**0**	**0**

Register 2

No	D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15
Name	**1**	**0**	**TB4**	**TB5**	**TB6**	**TB7**	**TB8**	**TB9**	**TB10**	**TB11**	**TB12**	**TB13**	**TB14**	**TB15**	**TB16**	**TB17**
Reset			**0**	**0**	**0**	**1**	**1**	**0**	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

← **LSB**

Note: (1) D0, D1 is address bit.

(2) All bits will be reset to default value after VIO powered on.

Register 0: Used for RF/Crystal frequency setting. F_{RF} = Fcrystal X N / R ,

N[11:0]: Binary format of PLL N counter. Used for RF frequency channel control.

N=(16XNB)+NA. NB=46~144, NA=0~15.

R[1:0]: Crystal reference frequency selection.

[00]: R=10 for 4MHz crystal.

[01]: R=30 for 12MHz crystal.

[10]: R=32 for 13.56MHz crystal.

[11]: R=40 for 16MHz crystal.

Register 1: Used for comment and parameters setting.

CTLS: Control selection.

0: TX_RX and CE will be controlled by Register1 D3, D4. IO pin 20, 21 will be don't cared.

1: TX_RX and CE will be controlled by IO pin 20, 21. Register1 D3, D4 will be don't cared.

TX_RX: Active mode (transmission/receiving) selection. 0: receiving. 1: transmission.

CE: Chip enable. 0: go to sleep mode. 1: go to active mode.

FSK_ASK: FSK_ASK selection. 0: ASK. 1: FSK.

BAND: RF band selection.

For A7103A, 0: 315MHz band. 1: 433MHz band.

For A7103B, 0: 868MHz band. 1: 915MHz band.

IFB[1:0]: IF filter band width selection.

[00]: 100KHz.

[01]: 200KHz.

[1X]: 300KHz.

CKS: Output clock (pin 24 **CLK_OUT**) divider ratio selection. 0: crystal frequency /16. 1: crystal frequency /4.

STBY: Standby mode selection. Chip will keep crystal oscillator running. **CLK_OUT** will output clock even **CE**=0.

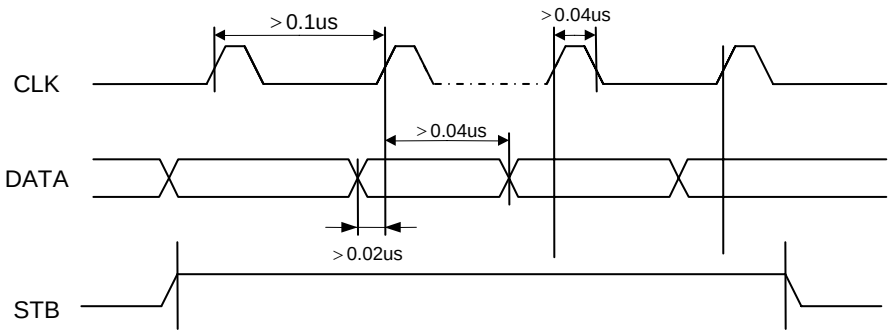
0:normal mode. 1:into standby mode.

ULS: Receiver Up/Low side band selection. Used for TX/RX FDD application.

0: low side band .1:up side band.

TB[4:0]: Test bits. Set to default value for normal operation.

SPI timing:



3. RF frequency and crystal frequency:

A7103 support multi RF frequency and up to four crystal frequency, which can be set by different approach.

(1) Not use SPI (A7103A only): F_{RF} = Fcrystal X N/32, Recommend crystal frequency is around 13.56MHz.

	315MHz (BAND=0)		433MHz (BAND=1)	
	CH0	**CH1**	**CH0**	**CH1**
N	**787**	**788**	**1084**	**1085**
F_{RF} (MHz)*	**314.846**	**315.27**	**433.496**	**434.768**

* For crystal= 13.560000MHz.

(2) Use SPI: F_{RF} = Fcrystal X N/R, Recommend crystal can be 4/12/13.56/16MHz.

R could be 10, 30, 32 or 40.

Used crystal	**4MHz**	**12MHz**	**13.56MHz**	**16MHz**
Recommended R value	**10**	**30**	**32**	**40**
SPI setting (R)	**R[1:0]=[00]**	**R[1:0]=[01]**	**R[1:0]=[10]**	**R[1:0]=[11]**

N could be 736~2319.

RF frequency band	**315MHz**	**433MHz**	**868NHz**	**915MHz**
Recommended N value	**742~788**	**1022~1085**	**2171~2174**	**2256~2318**
SPI setting (NA, NB)	**N=(16XNB) + NA**			

For example:

4MHz crystal, 433MHz BAND, set N=1084→ F_{RF}=4X1084/10=433.6MHz.

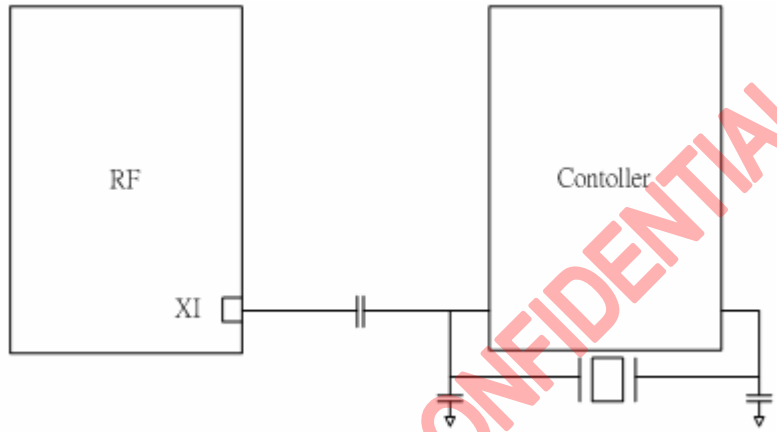
12MHz crystal, 433MHz BAND, set N=1085→ F_{RF}=12X1085/30=434MHz.

13.56MHz crystal, 315MHz BAND, set N=787→ F_{RF} =13.56X743/32=314.846MHz.

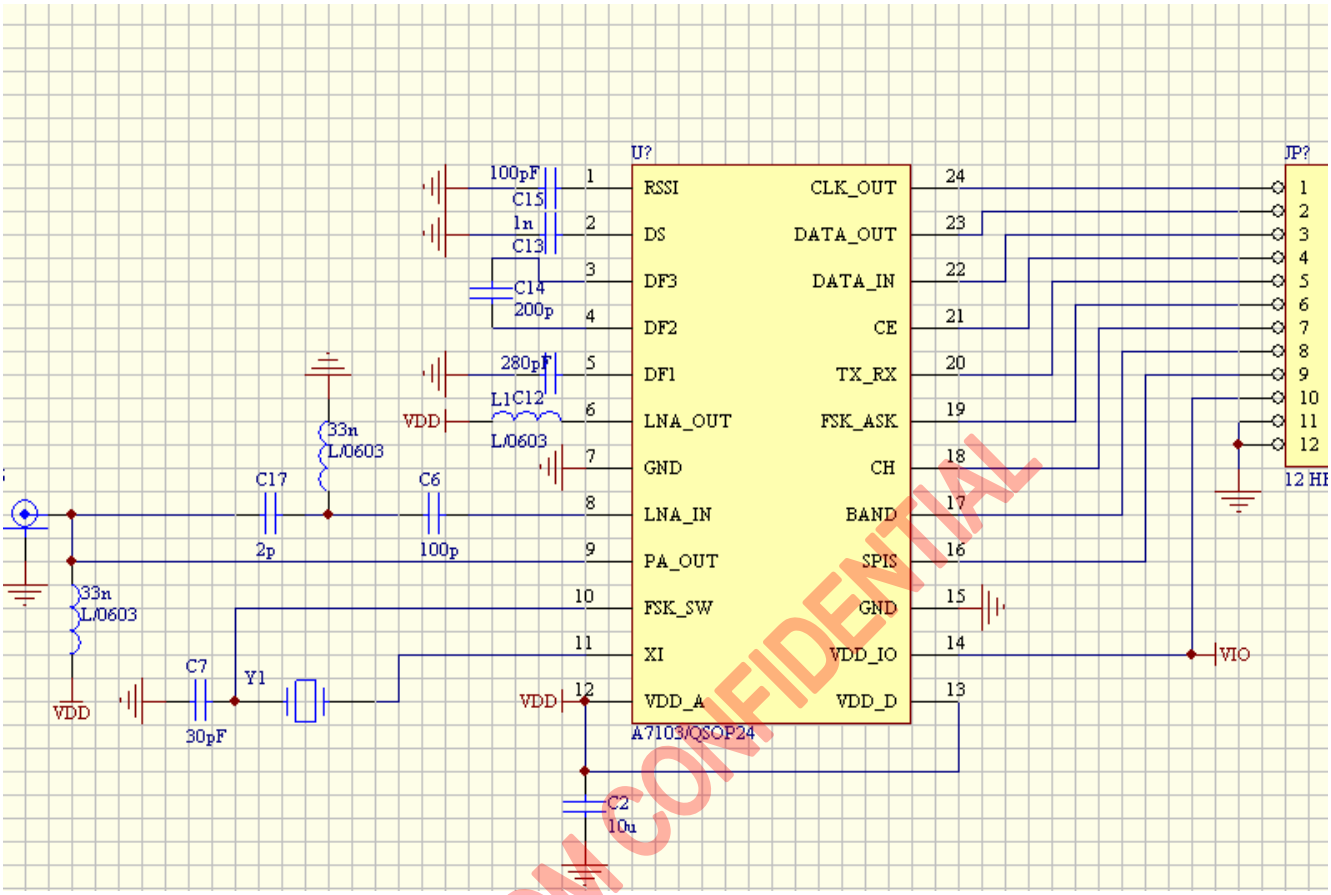
16MHz crystal, 915MHz BAND, set N=2260→ F_{RF} =16X2260/40=904MHz.

4. Share crystal with micro controller.

Figure shows the circuit connection of A7103 and micro controller share the crystal. User can connect a capacitor from micro controller and couple the reference signal to XI pin. The amplitude of XI should > 300mVpp.



Application Circuit

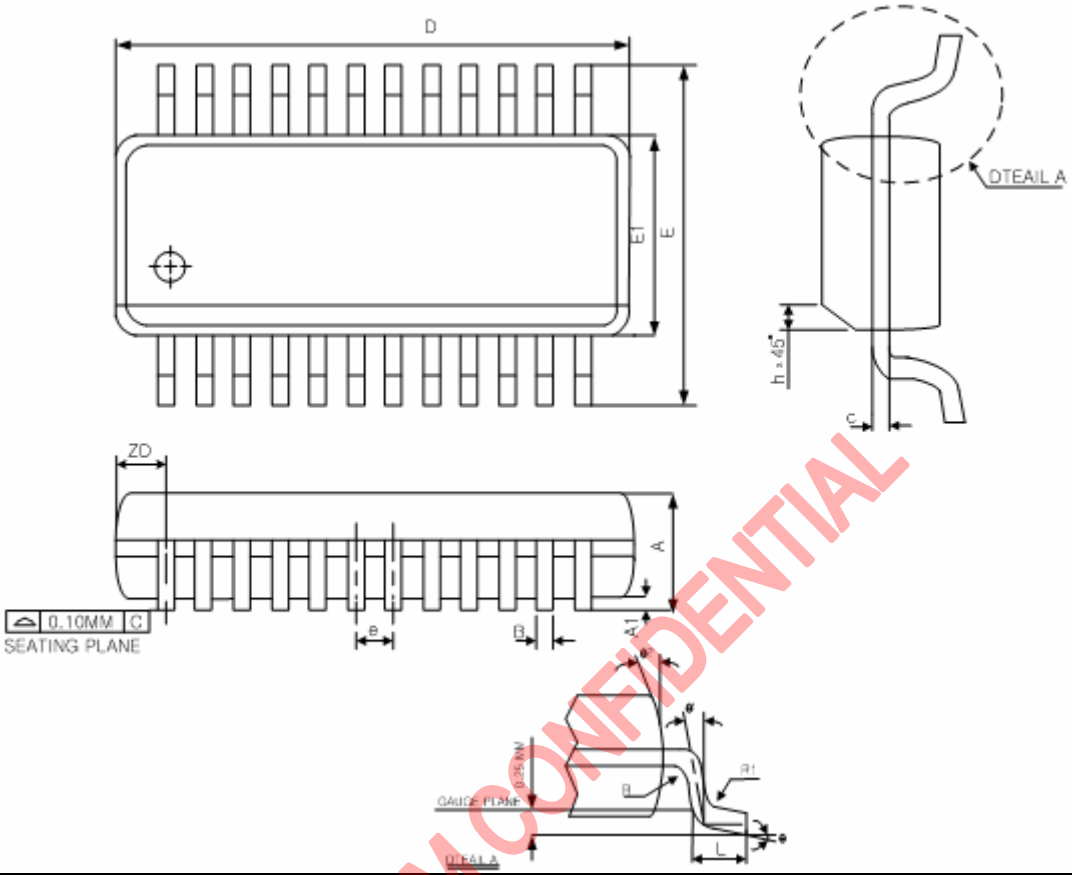


Ordering Information

Part No.	Package	Units Per Reel / Tray
A71C03AUF	SSOP 24L , Tape & Reel, Pb free	2.5K
A71C03AQF	QFN4X4 24L Tape & Reel, Pb free	3K

Package Information

SSOP24 Outline Dimensions



SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NCM.	MAX.
A	1.35	1.63	1.75	0.053	0.064	0.069
A1	0.10	0.15	0.25	0.004	0.006	0.010
A2			1.50			0.059
B	0.20		0.30	0.008		0.012
c	0.18		0.25	0.007		0.010
e	0.635 BASIC			0.025 BASIC		
D	8.56	8.85	8.74	331	341	344
E	5.79	5.99	6.20	0.228	0.236	0.244
E1	3.81	3.91	3.99	0.150	0.154	0.157
L	0.41	0.635	1.27	0.016	0.025	0.050
h	0.25		0.50	0.010		0.020
ZD	0.838 REF			0.033 REF.		
R1	0.20		0.33	0.008		0.013
R	0.20			0.008		
θ	0°		8°	0°		8°
θ 1	0°			0°		
θ 2	5°	10°	15°	5°	10°	15°
JEOEC	M0-137 (AF)					