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| SUBJECT:     | Critical Pa | rts List - Vers      | sion 1.1                 |

# **Smart Distributed System**

# Critical Parts List Version 1.1

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| DATE            | EVENT  |
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# Smart Distributed System—An Open Network Specification

# **Internet Access to Specifications**

All Smart Distributed System General Specifications are available for viewing and/or downloading on the World Wide Web:

#### http://www.honeywell.com/sensing/prodinfo/sds/sdspec.stm

Or to request additional *Smart Distributed System* information and/or literature, send E-Mail to:

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SDSCouncil@micro.honeywell.com

# 1. Introduction

### 1.1 Purpose

The primary purpose of this document is to establish a controlled list of certain critical parts that are required in a *Smart Distributed System* based product, and the procedure necessary to manage revisions to the list.

# 1.2 Scope

The scope of this document is the control of a list of *Smart Distributed System* Critical Parts and the criteria for including each part.

### 1.3 Overview

Certain parts which are required for a *Smart Distributed System* based product are critical to achieving full compatibility as viewed through Verification Testing (re., GS 052 108, Verification Test Procedure Specification for Common I/O Devices). These critical parts have been identified because part selection from all available parts could lead to device conformance and/or interoperability problems. Each part on the Critical Parts List has been evaluated and/or tested to prevent these types of problems both in Verification Testing and in user applications.

For each group of Critical Parts, the CPL gives the reason for its critical classification and the qualification test criteria that each part type must meet before a new part can be added to the list. When the configuration of a part is critical to its use in a *Smart Distributed System* product, the configuration requirements are also included in this document.

Partners use the CPL during the development of a *Smart Distributed System* based product making certain that any critical parts used are either on the CPL or can be qualified.

Certified Test Agents, when performing Verification Testing on a Partner Product, verify that any critical parts are declared by the Partner and are on the current CPL.

# 1.4 Definition of Terms

| CPL                              | Critical Parts List   |
|----------------------------------|---|
| Critical Parts                   | Certain physical parts, which are required to implement a <i>Smart Distributed System</i> Physical Component, are classified as Critical Parts because they have special requirements that may not be met by all of the available standard parts. |
| Critical Parts List              | A list of qualified Critical Parts by manufacturer and part<br>number for each of the specified Critical Part types.  |
| Critical Parts Test Coordinator  | Coordinates all Critical Parts testing. Refer to <i>Smart Distributed System</i> web page for contact information.  |
| Physical Qualification Test      | A Critical Part qualification test that is conducted with a sample part (i.e., requires part sample).   |
| New Family Member                | A Critical Part candidate that is a member of a family of similar parts when one or more of the other parts are qualified as Critical Parts.  |
| New Part                         | A Critical Part candidate that has no significant similarity with any qualified Critical Parts.   |
| Specification Qualification Test | A Critical Part qualification test that is conducted via specification review (i.e., without a sample part).  |

# 1.5 References

- /1/ Bosch CAN Specification, Version 2.0, Sept. 1991.
- /2/ Honeywell, MICRO SWITCH GS 052 104, Honeywell Smart Distributed System Physical Layer Specification.
- /3/ Honeywell, MICRO SWITCH GS 052 108, Honeywell Smart Distributed Verification Test Procedure Specification for Common I/O Devices.

International Standards can be purchased from the originating body or from a distributor such as Global (see below). The various manufacturer's documents are available from the respective companies. The following is a partial list of suppliers.

American National Standards Institute (ANSI)212-642-4900Global Engineering Documentshttp://global.his.comHoneywell, MICRO SWITCH815-235-5940Robert Bosch Corporation708-865-5200

# 2. Critical Parts—Physical Component

# 2.1 CAN Controllers

#### 2.1.1 Rationale

The *Smart Distributed System* protocol is a highly specialized application of CAN technology. Therefore some current and future CAN controllers may not be capable of fully supporting all of the *Smart Distributed System* specifications. Therefore, CAN Controllers are Critical Parts. Furthermore, because improper configuration of capable CAN Controllers can result in network/system performance and/or functionality problems, configuration specifications for CAN Controllers are also specified in this section.

#### 2.1.2 Qualification Requirements

The minimum requirement for *Smart Distributed System* CAN Controllers is Bosch approval because Bosch is the holder of the CAN specification (*Reference* /1/).

CAN Controllers must also be capable of detecting and reporting bus signal status in order to support *Smart Distributed System* Autobaud. CAN Controllers must also have a passive (listen only) mode where messages can be received while the transmitter is held in the recessive state. Exceptions<sup>1</sup> may be granted on a case-by-case basis where external circuitry is utilized for the bus signal status and passive mode functions.

<sup>1</sup>Any such exception could allow a product to pass Verification Testing (see *Reference/3/*) without a qualified CAN Controller. It would NOT place a non-qualified part on the CPL.

### 2.1.3 Configuration Requirements

#### 2.1.3.1 MC68HC CAN Controllers - Required Initialization

This section specifies the required configuration for use in *Smart Distributed System* components. The bit positions with values must be configured as specified. The values of the other bit positions depend on the specific functionalities implemented.

#### 2.1.3.1.1 Control Register

The Control Register determines the global behavior of the controller.

|                    | Bit 7        | Bit 6         | Bit 5    | Bit 4                          | Bit 3                        | Bit 2                           | Bit 1                          | Bit 0            |
|--------------------|--------------|---------------|----------|--------------------------------|------------------------------|---------------------------------|--------------------------------|------------------|
| Bit<br>Function    | Test<br>Mode | Speed<br>Mode | reserved | Overrun<br>Interrupt<br>Enable | Error<br>Interrupt<br>Enable | Transmit<br>Interrupt<br>Enable | Receive<br>Interrupt<br>Enable | Reset<br>Request |
| Required<br>Values | 0            | 0             |          |                                |                              |                                 |                                |                  |

# Bit 6: Speed Mode

Always set to 0.

# Bit 7: Test Mode

Always set to 0.

### 2.1.3.1.2 Command Register

The Command Register is used to initiate various actions. This register is *write only* (all bits always indicate a value of 1 if read).

|                   | Bit 7          | Bit 6          | Bit 5           | Bit 4          | Bit 3                      | Bit 2                        | Bit 1                      | Bit 0                        |
|-------------------|----------------|----------------|-----------------|----------------|----------------------------|------------------------------|----------------------------|------------------------------|
| Bit<br>Function   | CRX0<br>Active | CRX1<br>Active | Comp.<br>Select | Go To<br>Sleep | Clear<br>Overrun<br>Status | Release<br>Receive<br>Buffer | Abort<br>Trans-<br>mission | Trans-<br>mission<br>Request |
| Required<br>Value | 0              | 0              | 0               | 0              |                            |                              |                            |                              |

#### Bit 4: Go To Sleep

Writing a 1 will place the controller in the Sleep Mode. This mode is never used and must be set to 0.

#### Bits 5: Comparator Selector

This control bit is never used and must be set to 0.

#### Bit 6-7: Receiver input enable bits

These bits are not used and must be set to 0.

#### 2.1.3.1.3 Bus Timing Registers

The two Bus Timing Registers determine the baud rate and bit times. They must be configured with the values shown in the following tables. These values are to be used (with a 16 MHz crystal) because they allow the longest possible cable lengths for each baud rate. Failure to use these specified values may result in a device that is unable to function in an application with a maximum cable length trunk.

|  |             | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |      |  |  |
|--|-------------|-------|-------|-------|-------|-------|-------|-------|-------|------|--|--|
|  | Bit Name    | SJW.1 | SJW.0 | BRP.5 | BRP.4 | BRP.3 | BRP.2 | BRP.1 | BRP.0 |      |  |  |
|  | 1000 K Baud | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0x00 |  |  |
|  | 500 K Baud  | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0x00 |  |  |
|  | 250 K Baud  | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 1     | 0x01 |  |  |
|  | 125 K Baud  | 0     | 0     | 0     | 0     | 0     | 0     | 1     | 1     | 0x03 |  |  |

#### Bus Timing Register 0

| ••• | 1 111111 2 1 10 2 |       |         |         |         |         |         |         |         |      |
|-----|-------------------|-------|---------|---------|---------|---------|---------|---------|---------|------|
|     |                   | Bit 7 | Bit 6   | Bit 5   | Bit 4   | Bit 3   | Bit 2   | Bit 1   | Bit 0   |      |
|     | Bit Name          | SAM   | TSEG2.2 | TSEG2.1 | TSEG2.0 | TSEG1.3 | TSEG1.2 | TSEG1.1 | TSEG1.0 |      |
|     | 1000 K Baud       | 0     | 0       | 0       | 1       | 0       | 1       | 0       | 0       | 0x14 |
|     | 500 K Baud        | 0     | 0       | 0       | 1       | 1       | 1       | 0       | 0       | 0x1C |
|     | 250 K Baud        | 0     | 0       | 0       | 1       | 1       | 1       | 0       | 0       | 0x1C |
|     | 125 K Baud        | 0     | 0       | 0       | 1       | 1       | 1       | 0       | 0       | 0x1C |

#### **Bus Timing Register 1**

### 2.1.3.1.4 Output Control Register

The Output Control Register determines the output behavior. The values used in the Output Control Register are dependent on the transceiver circuit and the present transmission mode. The values in the following table are required with the noted exceptions.

|                                  | Bit 7             | Bit 6             | Bit 5              | Bit 4 | Bit 3 | Bit 2 | Bit 1  | Bit 0  |      |
|----------------------------------|-------------------|-------------------|--------------------|-------|-------|-------|--------|--------|------|
| Bit Name                         | TP.1 <sup>1</sup> | TN.1 <sup>1</sup> | POL.1 <sup>1</sup> | TP.0  | TN.0  | POL.0 | MODE.1 | MODE.0 |      |
| Guest Autobaud<br>(passive) Mode | 0                 | 0                 | 0                  | 0     | 0     | 0     | 1      | 0      | 0x02 |
| Normal Run<br>(active) Mode      | 1                 | 1                 | 1                  | 1     | 1     | 0     | 1      | 0      | 0xFA |

<sup>1</sup> Bit positions 5 through 7 are "don't care" when TX1 is not used (e.g., with Integrated Transceiver).

The setting for Guest Autobaud allows a Physical Component to operate in a *listen only mode*. In this mode a component is allowed to receive messages, but is not allowed to disturb the bus.

#### 2.1.3.2 82C200 CAN Controllers - Required Initialization

This section specifies the required configuration for use in *Smart Distributed System* components. The bit positions with values must be configured as specified. The values of the other bit positions depend on the specific functionalities implemented.

#### 2.1.3.2.1 Control Register

The Control Register determines the global behavior of the controller.

|                    | Bit 7        | Bit 6 | Bit 5    | Bit 4                          | Bit 3                        | Bit 2                           | Bit 1                          | Bit 0            |
|--------------------|--------------|-------|----------|--------------------------------|------------------------------|---------------------------------|--------------------------------|------------------|
| Bit<br>Function    | Test<br>Mode | Sync  | reserved | Overrun<br>Interrupt<br>Enable | Error<br>Interrupt<br>Enable | Transmit<br>Interrupt<br>Enable | Receive<br>Interrupt<br>Enable | Reset<br>Request |
| Required<br>Values | 0            | 0     |          |                                |                              |                                 |                                |                  |

Bit 6: Sync Always set to 0.

#### Bit 7: Test Mode

Always set to 0.

#### 2.1.3.2.2 Command Register

The Command Register is used to initiate various actions. This register is *write only* (all bits always indicate a value of 1 if read).

|                   | Bit 7    | Bit 6    | Bit 5    | Bit 4          | Bit 3                      | Bit 2                        | Bit 1                      | Bit 0                        |
|-------------------|----------|----------|----------|----------------|----------------------------|------------------------------|----------------------------|------------------------------|
| Bit<br>Function   | reserved | reserved | reserved | Go To<br>Sleep | Clear<br>Overrun<br>Status | Release<br>Receive<br>Buffer | Abort<br>Trans-<br>mission | Trans-<br>mission<br>Request |
| Required<br>Value |          |          |          | 0              |                            |                              |                            |                              |

#### Bit 4: Go To Sleep

Writing a 1 will place the controller in the Sleep Mode. This mode is never used and must be set to 0.

#### 2.1.3.2.3 Bus Timing Registers

The two Bus Timing Registers determine the baud rate and bit rates. They must be configured with the values shown in the following tables. These values are to be used (with a 16 MHz crystal) because they allow the longest possible cable lengths for each baud rate. Failure to use these specified values may result in a device that is unable to function in an application with a maximum cable length trunk.

| <br>Thing Reg |       |       |       |       |       |       |       |       |      |
|---------------|-------|-------|-------|-------|-------|-------|-------|-------|------|
|               | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |      |
| Bit Name      | SJW.1 | SJW.0 | BRP.5 | BRP.4 | BRP.3 | BRP.2 | BRP.1 | BRP.0 |      |
| 1000 K Baud   | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0x00 |
| 500 K Baud    | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0x00 |
| 250 K Baud    | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 1     | 0x01 |
| 125 K Baud    | 0     | 0     | 0     | 0     | 0     | 0     | 1     | 1     | 0x03 |

#### **Bus Timing Register 0**

|  |             | Bit 7 | Bit 6   | Bit 5   | Bit 4   | Bit 3   | Bit 2   | Bit 1   | Bit 0   |      |
|--|-------------|-------|---------|---------|---------|---------|---------|---------|---------|------|
|  | Bit Name    | SAM   | TSEG2.2 | TSEG2.1 | TSEG2.0 | TSEG1.3 | TSEG1.2 | TSEG1.1 | TSEG1.0 |      |
|  | 1000 K Baud | 0     | 0       | 0       | 1       | 0       | 1       | 0       | 0       | 0x14 |
|  | 500 K Baud  | 0     | 0       | 0       | 1       | 1       | 1       | 0       | 0       | 0x1C |
|  | 250 K Baud  | 0     | 0       | 0       | 1       | 1       | 1       | 0       | 0       | 0x1C |
|  | 125 K Baud  | 0     | 0       | 0       | 1       | 1       | 1       | 0       | 0       | 0x1C |

#### **Bus Timing Register 1**

### 2.1.3.2.4 Output Control Register

The Output Control Register determines the output behavior. The values used in the Output Control Register are dependent on the transceiver circuit and the present transmission mode. The values in the following table are required with the noted exceptions.

|                                  | Bit 7             | Bit 6             | Bit 5              | Bit 4 | Bit 3 | Bit 2 | Bit 1  | Bit 0  |      |
|----------------------------------|-------------------|-------------------|--------------------|-------|-------|-------|--------|--------|------|
| Bit Name                         | TP.1 <sup>1</sup> | TN.1 <sup>1</sup> | POL.1 <sup>1</sup> | TP.0  | TN.0  | POL.0 | MODE.1 | MODE.0 |      |
| Guest Autobaud<br>(passive) Mode | 0                 | 0                 | 0                  | 0     | 0     | 0     | 1      | 0      | 0x02 |
| Normal Run<br>(active) Mode      | 1                 | 1                 | 1                  | 1     | 1     | 0     | 1      | 0      | 0xFA |

<sup>1</sup> Bit positions 5 through 7 are "don't care" when TX1 is not used (e.g., with Integrated Transceiver).

The setting for Guest Autobaud allows the device to operate in a *listen only mode*. In this mode the component is allowed to receive messages, but is not allowed to disturb the bus.

#### 2.1.3.3 SJA1000 CAN Controllers - Required Initialization

This section specifies the required configuration for use in *Smart Distributed System* components. The bit positions with values must be configured as specified. The values of the other bit positions depend on the specific functionalities implemented.

The SJA CAN Controller has a mode that emulates the 82C200 CAN Controller. The required initialization for SJA CAN Controllers running in this mode is specified in this section.

#### 2.1.3.3.1 Clock Divider

The Clock Divider Register determines the global behavior of the controller.

|                    | Bit 7       | Bit 6 | Bit 5   | Bit 4    | Bit 3        | Bit 2 | Bit 1 | Bit 0 |
|--------------------|-------------|-------|---------|----------|--------------|-------|-------|-------|
| Bit<br>Function    | CAN<br>Mode | СВР   | RXINTEN | reserved | Clock<br>Off | CD.2  | CD.1  | CD.0  |
| Required<br>Values | 0           |       |         | 0        |              |       |       |       |

#### Bit 7: CAN Mode

This bit defines the CAN Mode. If bit 7 is 0 the controller operates in the 82C200, Basic CAN mode. The default value at power-up is 0.

#### Bit 4: reserved

This bit is reserved for future features. This bit must always be set to 0.

#### 2.1.3.3.2 Control Register

The Control Register determines the global behavior of the controller.

|                    | Bit 7    | Bit 6    | Bit 5    | Bit 4                          | Bit 3                        | Bit 2                           | Bit 1                          | Bit 0            |
|--------------------|----------|----------|----------|--------------------------------|------------------------------|---------------------------------|--------------------------------|------------------|
| Bit<br>Function    | reserved | reserved | reserved | Overrun<br>Interrupt<br>Enable | Error<br>Interrupt<br>Enable | Transmit<br>Interrupt<br>Enable | Receive<br>Interrupt<br>Enable | Reset<br>Request |
| Required<br>Values | 0        |          |          |                                |                              |                                 |                                |                  |

#### Bit 5: reserved

This bit has no required setting however, reading it always reflects a 1.

#### Bit 6: reserved

This bit has no required setting.

#### Bit 7: reserved

Always set to 0.

#### 2.1.3.3.3 Command Register

The Command Register is used to initiate various actions. This register is *write only* (all bits always indicate a value of 1 if read).

|                   | Bit 7    | Bit 6    | Bit 5    | Bit 4          | Bit 3                      | Bit 2                        | Bit 1                      | Bit 0                        |
|-------------------|----------|----------|----------|----------------|----------------------------|------------------------------|----------------------------|------------------------------|
| Bit<br>Function   | reserved | reserved | reserved | Go To<br>Sleep | Clear<br>Overrun<br>Status | Release<br>Receive<br>Buffer | Abort<br>Trans-<br>mission | Trans-<br>mission<br>Request |
| Required<br>Value |          |          |          | 0              |                            |                              |                            |                              |

Bit 4: Go To Sleep

Writing a 1 will place the controller in the Sleep Mode. This mode is never used and must be set to 0.

#### 2.1.3.3.4 Bus Timing Register

The two Bus Timing Registers determine the baud rate and bit times. They must be configured with the values shown in the following tables. These values are to be used (with a 16 MHz crystal) because they allow the longest possible cable lengths for each baud rate. Failure to use these specified values may result in a device that is unable to function in an application with a maximum cable length trunk.

#### Bus Timing Register 0

| 0 0         | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |      |
|-------------|-------|-------|-------|-------|-------|-------|-------|-------|------|
| Bit Name    | SJW.1 | SJW.0 | BRP.5 | BRP.4 | BRP.3 | BRP.2 | BRP.1 | BRP.0 |      |
| 1000 K Baud | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0x00 |
| 500 K Baud  | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0x00 |
| 250 K Baud  | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 1     | 0x01 |
| 125 K Baud  | 0     | 0     | 0     | 0     | 0     | 0     | 1     | 1     | 0x03 |

#### **Bus Timing Register 1**

| 8 8         | Bit 7 | Bit 6   | Bit 5   | Bit 4   | Bit 3   | Bit 2   | Bit 1   | Bit 0   |      |
|-------------|-------|---------|---------|---------|---------|---------|---------|---------|------|
| Bit Name    | SAM   | TSEG2.2 | TSEG2.1 | TSEG2.0 | TSEG1.3 | TSEG1.2 | TSEG1.1 | TSEG1.0 |      |
| 1000 K Baud | 0     | 0       | 0       | 1       | 0       | 1       | 0       | 0       | 0x14 |
| 500 K Baud  | 0     | 0       | 0       | 1       | 1       | 1       | 0       | 0       | 0x1C |
| 250 K Baud  | 0     | 0       | 0       | 1       | 1       | 1       | 0       | 0       | 0x1C |
| 125 K Baud  | 0     | 0       | 0       | 1       | 1       | 1       | 0       | 0       | 0x1C |

#### 2.1.3.3.5 Output Control Register

The Output Control Register determines the output behavior. The values used in the Output Control Register are dependent on the transceiver circuit and the present transmission mode. The values in the following table are required with the noted exceptions.

|                                  | Bit 7             | Bit 6             | Bit 5              | Bit 4 | Bit 3 | Bit 2 | Bit 1  | Bit 0  |      |
|----------------------------------|-------------------|-------------------|--------------------|-------|-------|-------|--------|--------|------|
| Bit Name                         | TP.1 <sup>1</sup> | TN.1 <sup>1</sup> | POL.1 <sup>1</sup> | TP.0  | TN.0  | POL.0 | MODE.1 | MODE.0 |      |
| Guest Autobaud<br>(passive) Mode | 0                 | 0                 | 0                  | 0     | 0     | 0     | 1      | 0      | 0x02 |
| Normal Run<br>(active) Mode      | 1                 | 1                 | 1                  | 1     | 1     | 0     | 1      | 0      | 0xFA |

<sup>1</sup> Bit positions 5 through 7 are "don't care" when TX1 is not used (e.g., with Integrated Transceiver).

The setting for Guest Autobaud allows the device to operate in a *listen only mode*. In this mode the device is allowed to receive messages, but is not allowed to disturb the bus.

#### 2.1.4 Specification Qualification Test

- 1. Bosch approval candidate part documentation must clearly show that Bosch has specifically approved the part by recognizing its compliance with the Bosch CAN Specification.
- 2. Configuration requirements configuration requirements must be specified and provided for publication in this specification.

#### 2.1.5 Physical Qualification Test

1. A Test Product, including the candidate part, must also pass a complete Product Verification Test as specified in the Verification Test Procedure Specification, GS 052 108.

# 2.2 CAN Crystal

### 2.2.1 Rationale

The CAN Crystal is a Critical Part because the critical time synchronization among devices in an application is critical and depends on the consistency of these components. The tolerance requirements for the CAN Crystal are based upon a detailed worst-case bit timing analysis.

#### 2.2.2 Qualification Requirements

The only qualification requirement for the CAN Crystal is that its overall Combined Frequency Tolerance not exceed  $\pm$  100 PPM in accordance with Physical Layer Specification, GS 052 104, paragraph 3.2.3 CAN Time Base Crystal Specifications.

For approval of new parts, the Partner shall submit the manufacturer's data sheet to the Critical Parts Test Coordinator for review.

### 2.2.3 Specification Qualification Test

1. Verify candidate part's documentation of overall frequency tolerance meets the *Smart Distributed System* requirements.

# 2.3 Integrated Transceivers

#### 2.3.1 Rationale

Integrated Transceivers are critical parts because they provide the electrical interface to *the Smart Distributed System* bus. The interface signals of each device must be compatible. This is accomplished via the specifications in the Physical Layer Specification, GS 052 104.

#### 2.3.2 Qualification Requirements

The qualification requirements for the Integrated Transceiver include the input/output signal levels and its propagation delays for each baud rate as specified in the Physical Layer Specification, GS 052 104, paragraph 3.2.4.2 Integrated Transceiver Specifications.

Another requirement is that these components must have reverse power protection.

For approval of new parts, the Partner shall submit the manufacturer's data sheet to the Critical Parts Test Coordinator for review and a *Smart Distributed System* product for testing.

### 2.3.3 Specification Qualification Test

1. Verify that the candidate's part documentation of signal specifications and reverse power protection are in accordance with *Smart Distributed System* specifications.

#### 2.3.4 Physical Qualification Test

- 1. Verify that the candidate's Test Product, including the candidate part, passes a maximum bus length test covering all specified conditions.
- 2. A Test Product, including the candidate part, must also pass a complete Product Verification Test as specified in the Verification Test Procedure Specification, GS 052 108.

# 2.4 Transceiver Isolation

### 2.4.1 Rationale

Transceiver Isolation devices are Critical Parts because they introduce an additional propagation delay to the transceiver. This Transceiver Isolation propagation delay must be limited to assure that *Smart Distributed System* devices can meet the required baud rates.

### 2.4.2 Qualification Requirements

The primary qualification requirements for the Transceiver Isolation components include its galvanic isolation voltage rating and its propagation delays for each baud rate (1 MBaud optional) as specified in the Physical Layer Specification, GS 052 104, paragraph 3.2.4.1. The specific minimum requirements for Transceiver Isolation devices (125/250/500 Kbaud) include:

- 1. Highest Allowable Overvoltage (Transient Overvoltage,  $t_{TR} = 10$  sec) shall be no less than 4000  $V_{PEAK}$ .
- 2. Data Rate shall be at least 15 M Baud.
- 3. If Data Rate is not specified, then the following propagation delay specifications must be met:
  - a. The total combined Propagation Delay of:
    - Propagation Delay Time to Logic Low Output (t<sub>PHL</sub>),
    - Propagation Delay Time to Logic High Output (t<sub>PLH</sub>), and
    - Propagation Delay Skew (t<sub>PSK</sub>)

shall be no longer than 150 nsec.

- b. Propagation Delay Skew  $(t_{PSK})$  shall be no longer than 30 nsec.
- Note: For reference only, Typical Propagation Delay Time from Output Enabled to Logic High Output (t<sub>PZH</sub>) is 13 nsec and Typical Propagation Delay Time from Output Enabled to Logic Lo Output (t<sub>PZL</sub>) is 11 nsec.

For approval of new parts, the Partner shall submit the manufacturer's data sheet to the Critical Parts Test Coordinator for review.

### 2.4.3 Specification Qualification Test

Verify candidate part's documentation of the required galvanic isolation and propagation delay specifications.

For example, a 82C200 CAN Controller, 82C251 integrated transceiver, and a 40/40 nanosecond transmit/receive delay optocoupler uses only 44% of the absolute maximum delay for 500 Kbaud.

#### 2.4.4 Physical Qualification Test

1. Verify that the candidate's Test Product, including the candidate part, passes a maximum bus length test covering all specified conditions.

A Test Product, including the candidate part, must also pass a complete Product Verification Test as specified in the Verification Test Procedure Specification, GS 052 108.

# 2.5 Bus Connectors

#### 2.5.1 Mini/Micro Connectors

#### 2.5.1.1 Rationale

Mini/Micro Connectors are Critical Parts because they provide the preferred trunk segment interconnections and the majority of the Physical Component to branch connections. The integrity of these connections is essential to the success of each *Smart Distributed System* application.

#### 2.5.1.2 Qualification Requirements

The primary qualification requirements for Mini/Micro connectors are:

- 1. Contacts shall be plated with  $30 \mu$  inch Au over  $30 \mu$  inch nickel in accordance with Physical Layer Specification, GS 052 104, paragraph 3.3.1.4.1 Mini/Micro Connector Specifications, and
- 2. Dimensions shall be in accordance with IEC 60947-5-2, 1997 Annex D, as specified in the Physical Layer Specification.

#### New Family Member

Approval of a new connector part number, which is a member of a product group or family that includes an approved CPL part number (same manufacturer), does not require a sample part. The Partner shall submit full part documentation for review. If the part specifications meet or exceed all applicable *Smart Distributed System* specifications, the part can be added to the CPL.

#### <u>New Part</u>

Approval of a new connector part number which is not similar to other Connectors on the CPL (i.e., not a member of a product family which includes a CPL part number, or manufacturer is not represented on CPL), includes some additional requirements. A sample part must be submitted along with the part documentation. If the part specifications meet or exceed all applicable *Smart Distributed System* specifications and the sample part visually matches the documentation and exhibits good industrial quality workmanship and materials, the part can be added to the CPL.

#### 2.5.1.3 Specification Qualification Test

#### **New Family Member or New Part**

1. Verify Partner certification of compliance with the dimensional requirements of IEC 60947-5-2.

2. Verify documentation of required contact material and dimensions.

#### 2.5.1.4 Physical Qualification Test

#### New Part only

- 1. General visual inspection of sample part for consistency with documentation, materials and workmanship.
- 2. A Test Product, including the candidate part, must also pass a complete Product Verification Test as specified in the Verification Test Procedure Specification, GS 052 108.

# **3. Qualification Procedure**

The Critical Parts Test Coordinator will evaluate Partner requests for approval of new part numbers for inclusion in the CPL. The following general procedure will be used.

| Developer                              | Identifies a candidate part that meets the requirements for the associated Critical Part type.            |
|--|---|
| Developer                              | Submits the part specifications and the sample part (if required) to the Critical Parts Test Coordinator. |
| <b>Critical Parts Test Coordinator</b> | Completes the qualification testing and notifies the Partner of the test results.                         |
| Smart Distributed System Council       | Adds the approved part to the CPL.  |

# 4. Maintaining the Critical Parts List

The Critical Parts List is maintained by the *Smart Distributed System* Council or a designated representative. Parts can be added to the CPL when they are shown to meet the qualification requirements specified in this document. Parts can be removed from the CPL when they are shown not to meet the qualification requirements of this document. Final approval of any changes to the CPL is by the reissue of this document.

# 5. Using a Critical Parts List

The primary users of the Critical Parts List are *Smart Distributed System* Partners who are the developers of *Smart Distributed System* based products, and Certified Test Agents who are authorized to do Verification Testing of *Smart Distributed System* based products.

# 5.1 Partners

Partners, or developers, must be aware of the CPL categories and entries to help them identify the qualified parts and/or the qualification requirements. The developer normally selects necessary critical parts from the CPL and must declare all critical parts used in a product when submitting it for Verification Testing.

# 5.2 Certified Test Agents

Certified Test Agents verify that the critical parts declared by the Partner are included in the current CPL. If a declared critical part is not on the CPL or if an undeclared critical part is discovered, the Product Under Test fails this test.

# 6. The List of Qualified Critical Parts

| GROUP           | DESCRIPTION    | MANUFACTURER     | PART NO.          | ТҮРЕ                    |
|-----------------|----------------|------------------|-------------------|-------------------------|
| CAN Controllers | CAN Cont. only | Philips          | 82C200            |                         |
|                 |                | -                | SJA1000           |                         |
|                 | CPU/CAN Cont.  | Motorolla        | MC68HC05X4        | 4K ROM                  |
|                 |                |                  | MC68HC705X4       | 4K EPROM                |
|                 |                |                  | MC68HC05X16       | 16K ROM, mux, and A/D   |
|                 |                |                  | MC68HC705X32      | 32K EPROM, mux, and A/D |
|                 |                |                  | MC68HC05X32       | 32K ROM, mux, and A/D   |
|                 |                | Philips          | 80C592            | no ROM, mux, and A/D    |
|                 |                |                  | 83C592            | 16K ROM, mux, and A/D   |
|                 |                |                  | 80CE598           | no ROM, mux, and A/D    |
|                 |                |                  | 83CE598           | 16K ROM, mux, and A/D   |
| Connectors      | Standard Bus   | "Micro Switch"   | FE-05216          | Micro                   |
|                 | Connectors     | Lumberg          | RSF 50DN-613/XX   | Mini                    |
|                 |                |                  | RSF 4/0.5M        | Micro                   |
|                 |                | Micro Switch     | SDS-BKHD-M-001    | Mini                    |
|                 |                | Molex            | 84814-9026        | Micro                   |
|                 |                |                  | 84814-9020        | Mini                    |
| Crystal         | CAN Crystal    | Epson            | CA-301 16.00 MHz  | 16 MHz                  |
|                 |                |                  | CA-303 16.00 MHz  | 16 MHz                  |
|                 |                |                  | SG-615P16.0000MC2 | 16 MHz                  |
|                 |                | Fox              | FOXS/160          | 16 MHz                  |
|                 |                | Kinseki, Limited | HC-49/U-S, 16 MHz | 16 MHz                  |
|                 |                | Pletronics       | LP49-SR           | 16 MHz                  |
| Integrated      | CAN Transcv'er | Philips          | PCA82C251T        | IC                      |
| Transceivers    |                |                  |                   |                         |
| Transmission    | Optocoupler    | Hewlett Packard  | HCPL7100          | IC                      |
| Isolation       |                |                  | HCPL7101          | IC                      |
|                 |                | Burr-Brown       | ISO150            | IC, dual optocoupler    |

A manufacturer's name in double quotes is a Partner's name and indicates that the part number is restricted to use by that Partner only (e.g., the part is fabricated by the Partner).

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