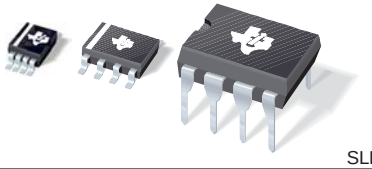


SLLS562B − MARCH 2003 − REVISED − FEBRUARY 2004

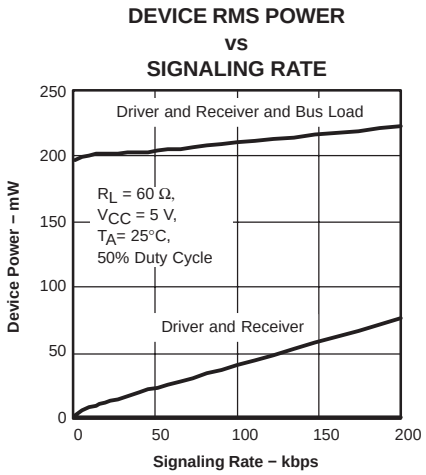
LOW-POWER RS-485 TRANSCEIVER
Available in Small MSOP-8 Package

FEATURES

- Available in Small MSOP-8 Pin Package
- Meets or Exceeds the Requirements of the TIA/EIA−485A Standard
- Low Quiescent Power
  - < 0.3 mA Active Mode
  - 1 nA Shutdown Mode
- Driver Outputs Optimized for Low EMI at Signaling Rates up to 200 kbps
- 1/8 Unit Load—Up to 256 Nodes on a Bus
- Bus-Pin ESD Protection Exceeds 16 kV
- Industry-Standard SN75176 Footprint
- Failsafe Receiver (Bus Open, Bus Shorted, Bus Idle)

APPLICATIONS

- Energy Meter Networks
- Motor Control
- Power Inverters
- Industrial Automation
- Building Automation Networks
- Industrial Process Control
- Battery-Powered Applications
- Telecommunications Equipment



DESCRIPTION

This device is a half-duplex transceiver designed for RS-485 data bus networks. Powered by a 5-V supply, it is fully compliant with the TIA/EIA-485A standard. With controlled output transition times, this device is suitable for signaling rates up to 200 kbps over long twisted-pair cables. The device is designed to operate with very low supply current, typically less than 0.6 mA, exclusive of the load. When in the inactive shutdown mode, the supply current drops to a few nanoamps, making these devices ideal for power-sensitive applications.

The wide common-mode range and high ESD protection levels of these devices make them suitable for demanding applications such as energy meter networks, electrical inverters, status/command signals across telecom racks, cabled chassis interconnects, and industrial automation networks where noise tolerance is essential. The SN65HVD3082E and SN75HVD3082E match the industry-standard footprint of the SN75176. Power-on reset circuits keep the outputs in a high-impedence state until the supply voltage has stabilized. A thermal shutdown function protects the device from damage due to system fault conditions. The SN75HVD3082E is characterized for operation from 0°C to 70°C and the SN65HVD3082E is characterized for operation from −40°C to 85°C air temperature.

DEVICE/SIGNALING RATE

DEVICE	SIGNALING RATE
SN65HVD3082E SN75HVD3082E	0.2 Mbps
SN65HVD3085E	1 Mbps
SN65HVD3088E	10 Mbps

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION

T_A	PLASTIC DUAL-IN-LINE	PLASTIC SMALL OUTLINE(1)	PLASTIC SMALL OUTLINE(2)
0°C to 70°C	SN75HVD3082EP Marked as 75HVD3082	SN75HVD3082ED Marked as VN3082	SN75HVD3082EDGK Marked as NWM
−40°C to 85°C	SN65HVD3082EP Marked as 65HVD3082	SN65HVD3082ED Marked as VP3082	SN65HVD3082EDGK Marked as NWN

(1) The D package is available taped and reeled. Add an R suffix to the device type (i.e., SN65HVD3082EDR).
(2) The DGK package is available taped and reeled. Add an R suffix to the device type (i.e., SN65HVD3082EDGKR).

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1) (2)

			UNITS
Supply voltage range, V_{CC}			−0.5 V to 7 V
Voltage range at A or B			−9 V to 14 V
Voltage range at any logic pin			−0.3 V to V_{CC} + 0.3 V
Receiver output current			−24 mA to 24 mA
Electrostatic discharge	HBM(3)	Bus terminals and GND	±16 kV
		All pins	4 kV
	Charged-Device Model(4)	all pins	1 kV
Voltage input range, transient pulse, A and B, through 100 Ω (see Figure 13)			−50 V to 50 V
Storage temperature range			−65°C to 130°C
Junction temperature, T_J			170°C
Continuous total power dissipation			Refer to Package Dissipation Table

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.
(3) Tested in accordance with JEDEC Standard 22, Test Method A114-A
(4) Tested in accordance with JEDEC Standard 22, Test Method C101.

PACKAGE DISSIPATION RATINGS

PACKAGE	JEDEC BOARD MODEL	T_A <25°C POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING
D	Low K	507 mW	4.82 mW/°C	289 mW	217 mW
P	Low K	686 mW	6.53 mW/°C	392 mW	294 mW
DGK	Low K	394 mW	3.76 mW/°C	255 mW	169 mW
	High K	583 mW	5.55 mW/°C	333 mW	250 mW

RECOMMENDED OPERATING CONDITIONS(1)

		MIN	TYP	MAX	UNIT
Supply voltage, V_{CC}		4.5		5.5	V
Input voltage at any bus terminal (separately or common mode), V_I		−7		12	V
High-level input voltage (D, DE, or $\overline{RE}$ inputs), V_{IH}		2		V_{CC}	V
Low-level input voltage (D, DE, or $\overline{RE}$ inputs), V_{IL}		0		0.8	V
Differential input voltage, V_{ID}		−12		12	V
Output current, I_O	Driver	−60		60	mA
	Receiver	−8		8	
Differential load resistance, R_L		54	60		Ω
Signaling rate, $1/t_{UI}$		0		200	kbps
Operating free−air temperature, T_A	SN65HVD3082E	−40		85	°C
	SN75HVD3082E	0		70	
Junction temperature, T_J(2)		−40		130	°C

(1) The algebraic convention, in which the least positive (most negative) limit is designated as minimum, is used in this data sheet.
(2) See *thermal characteristics* table for information on maintenance of this specification for the DGK package.

SUPPLY CURRENT

over recommended operating conditions unless otherwise noted

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
I_{CC}	Driver and receiver enabled	D at V_{CC} or open, No load	DE at V_{CC}, RE at 0 V,		425	900	μA
	Driver enabled, receiver disabled	D at V_{CC} or open, No load	DE at V_{CC}, RE at V_{CC}		330	600	μA
	Receiver enabled, driver disabled	D at V_{CC} or open, No load	DE at 0 V, RE at 0 V,		300	600	μA
	Driver and receiver disabled	D at V_{CC} or open,	DE at 0 V, RE at V_{CC}		0.001	2	μA

(1) All typical values are at 25°C and with a 5-V supply.

DRIVER ELECTRICAL CHARACTERISTICS

over recommended operating conditions unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
$\|V_{OD}\|$	Differential output voltage	I_O = 0, No load	3	4.3		V
		R_L = 54 Ω, See Figure 1	1.5	2.3		
		V_{TEST} = −7 V to 12 V, See Figure 2	1.5			
$\Delta\|V_{OD}\|$	Change in magnitude of differential output voltage	See Figure 1 and Figure 2	−0.2	0	0.2	V
$V_{OC(SS)}$	Steady-state common-mode output voltage	See Figure 3	1	2.6	3	V
$\Delta V_{OC(SS)}$	Change in steady-state common-mode output voltage		−0.1	0	0.1	
$V_{OC(PP)}$		See Figure 3		500		mV
I_{OZ}	High-impedance output current	See receiver input currents				µA
I_I	Input current	D, DE	−100		100	
I_{OS}	Short-circuit output current	−7 V ≤ V_O ≤ 12 V, See Figure 7	−250		250	mA

(1) All typical values are at 25°C and with a 5V-supply.

DRIVER SWITCHING CHARACTERISTICS

over recommended operating conditions unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	R_L = 54 Ω, C_L = 50 pF, See Figure 4		0.7	1.3	µs
t_{PHL}	Propagation delay time, high-to-low-level output			0.7	1.3	
t_r	Differential output signal rise time		0.5	0.9	1.5	
t_f	Differential output signal fall time		0.5	0.9	1.5	
$t_{sk(p)}$	Pulse skew ($\|t_{PHL} - t_{PLH}\|$)			0.02	0.2	
t_{PZH}	Propagation delay time, high-impedance-to-high-level output	R_L = 110 Ω, $\overline{RE}$ at 0 V, See Figure 5		3	7	µs
t_{PHZ}	Propagation delay time, high-level-to-high-impedance output			0.07	0.2	
t_{PZL}	Propagation delay time, high-impedance-to-low-level output	R_L = 110 Ω, $\overline{RE}$ at 0 V See Figure 6		2	7	µs
t_{PLZ}	Propagation delay time, low-level-to-high-impedance output			0.09	0.2	
$t_{PZH(SHDN)}$	Propagation delay time, shutdown-to-high-level output	R_L = 110 Ω, $\overline{RE}$ at V_{CC}, See Figure 5		4	7	µs
$t_{PZL(SHDN)}$	Propagation delay time, shutdown-to-low-level output	R_L = 110 Ω, $\overline{RE}$ at V_{CC}, See Figure 6		3	7	µs

RECEIVER ELECTRICAL CHARACTERISTICS

over recommended operating conditions unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage	I_O = −8 mA		−85	−10	mV
V_{IT-}	Negative-going input threshold voltage	I_O = 8 mA	−200	−115		mV
V_{hys}	Hysteresis voltage (V_{IT+} − V_{IT-})			30		mV
V_{OH}	High-level output voltage	V_{ID} = 200 mV, I_{OH} = −8 mA, See Figure 8	4	4.6		V
V_{OL}	Low-level output voltage	V_{ID} = −200 mV, I_{OH} = 8 mA, See Figure 8		0.15	0.4	V
I_{OZ}	High-impedance-state output current	V_O = 0 to V_{CC}, $\overline{RE}$= V_{CC}	−1		1	µA
I_I	Bus input current	V_{IH} = 12 V, V_{CC} = 5 V		0.04	0.1	mA
		V_{IH} = 12 V, V_{CC} = 0		0.06	0.125	
		V_{IH} = −7 V, V_{CC} = 5 V	−0.1	−0.04		
		V_{IH} = −7 V, V_{CC} = 0	−0.05	−0.03		
I_{IH}	High-level input current ($\overline{RE}$)	V_{IH} = 2 V	−60	−30		µA
I_{IL}	Low-level input current ($\overline{RE}$)	V_{IL} = 0.8 V	−60	−30		µA
C_{diff}	Differential input capacitance	V_I = 0.4 sin (4E6πt) + 0.5 V, DE at 0 V		7		pF

(1) All typical values are at 25°C and with a 5-V supply.

RECEIVER SWITCHING CHARACTERISTICS

over recommended operating conditions unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	V_{ID} = −1.5 V to 1.5 V, C_L = 15 pF, See Figure 9		75	200	ns
t_{PHL}	Propagation delay time, high-to-low-level output			79	200	
$t_{sk(p)}$	Pulse skew ($\lvert t_{PHL} - t_{PLH} \rvert$)			4	30	
t_r	Output signal rise time			1.5	3	ns
t_f	Output signal fall time			1.8	3	
t_{PZH}	Output enable time to high level	C_L = 15 pF, DE at 3 V, See Figure 10 and Figure 11		5	50	ns
t_{PZL}	Output enable time to low level			10	50	
t_{PHZ}	Output enable time from high level			5	50	
t_{PLZ}	Output enable time from low level			8	50	
$t_{PZH(SHDN)}$	Propagation delay time, shutdown-to-high-level output	C_L = 15 pF, DE at 0 V, See Figure 12		1.6	3.5	µs
$t_{PZL(SHDN)}$	Propagation delay time, shutdown-to-low-level output			1.7	3.5	

PARAMETER MEASUREMENT INFORMATION

NOTE: Test load capacitance includes probe and jig capacitance (unless otherwise specified). Signal generator characteristics: rise and fall time < 6 ns, pulse rate 100 kHz, 50% duty cycle. Z_O = 50 Ω (unless otherwise specified).

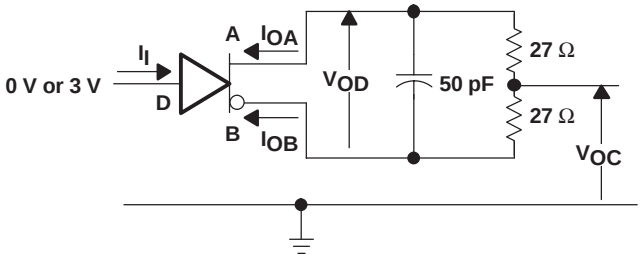


Figure 1. Driver Test Circuit, V_{OD} and V_{OC} Without Common-Mode Loading

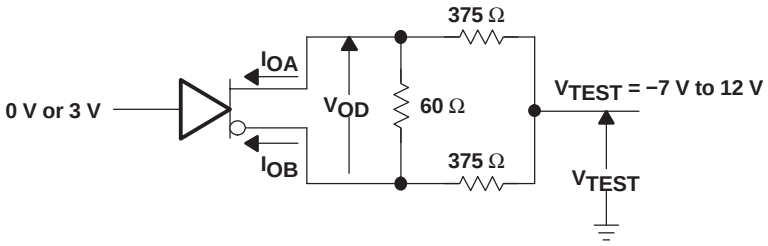


Figure 2. Driver Test Circuit, V_{OD} With Common-Mode Loading

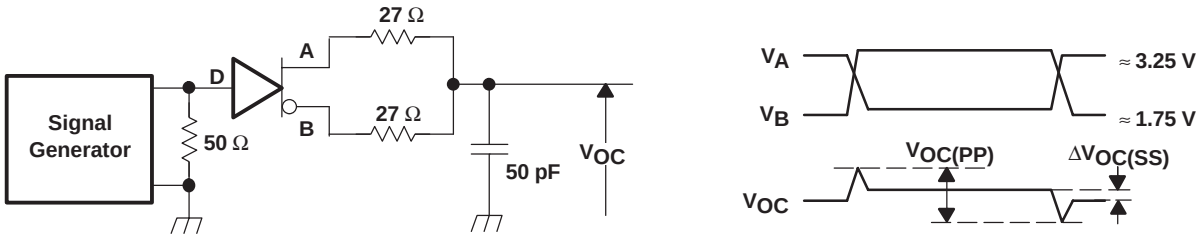


Figure 3. Driver V_{OC} Test Circuit and Waveforms

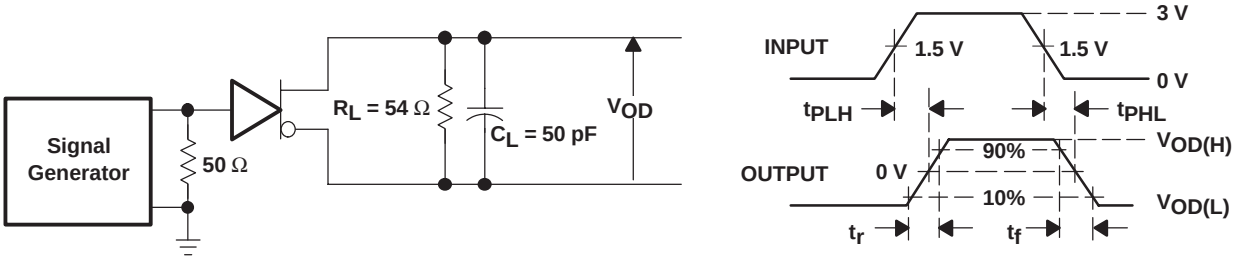


Figure 4. Driver Switching Test Circuit and Waveforms

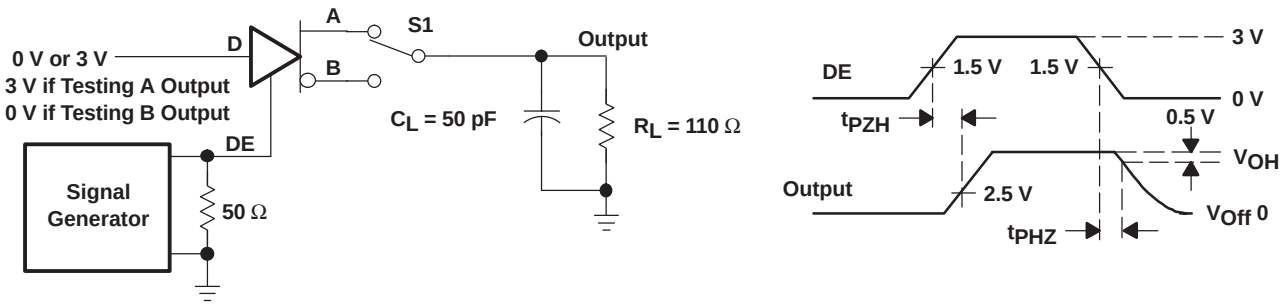


Figure 5. Driver Enable/Disable Test Circuit and Waveforms, High Output

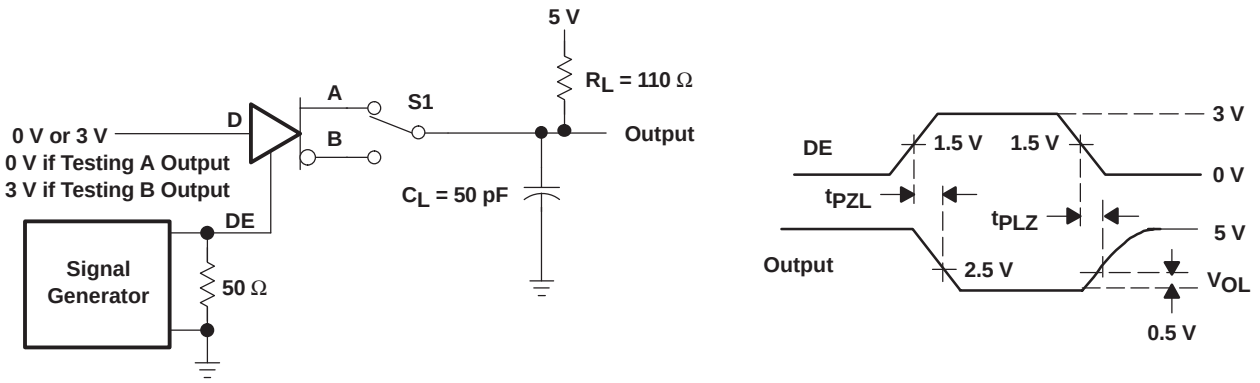


Figure 6. Driver Enable/Disable Test Circuit and Waveforms, Low Output

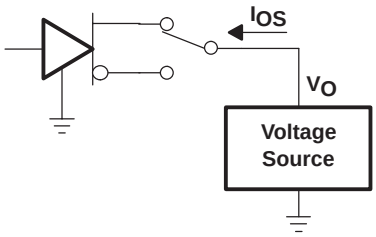


Figure 7. Driver Short-Circuit Test

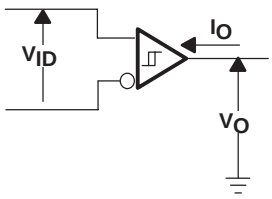


Figure 8. Receiver Parameter Definitions

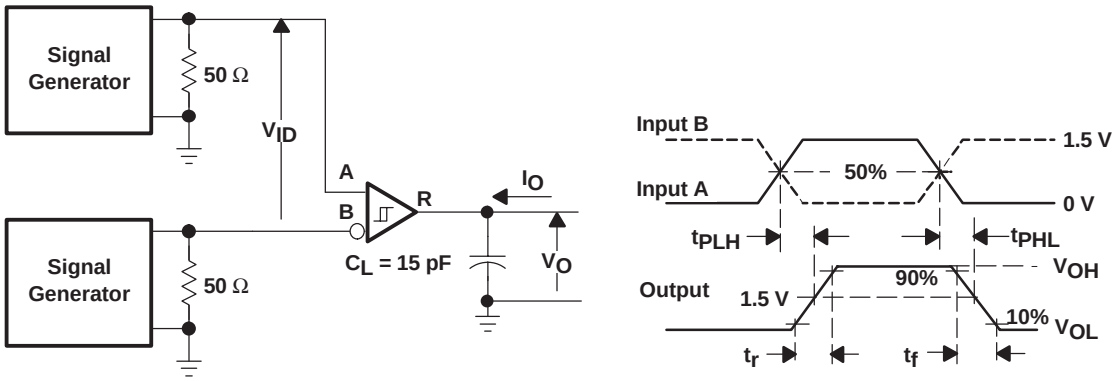


Figure 9. Receiver Switching Test Circuit and Waveforms

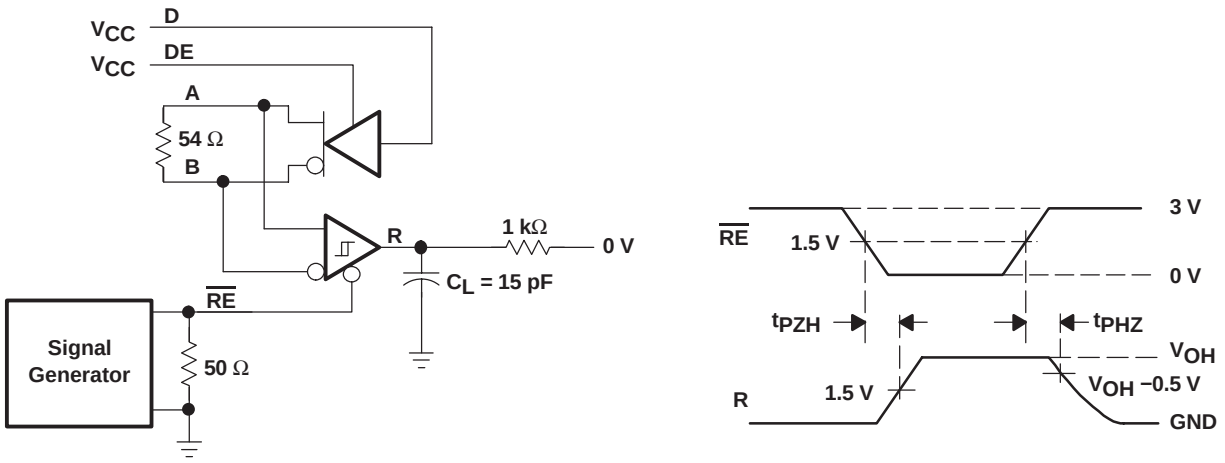


Figure 10. Receiver Enable/Disable Test Circuit and Waveforms, Data Output High

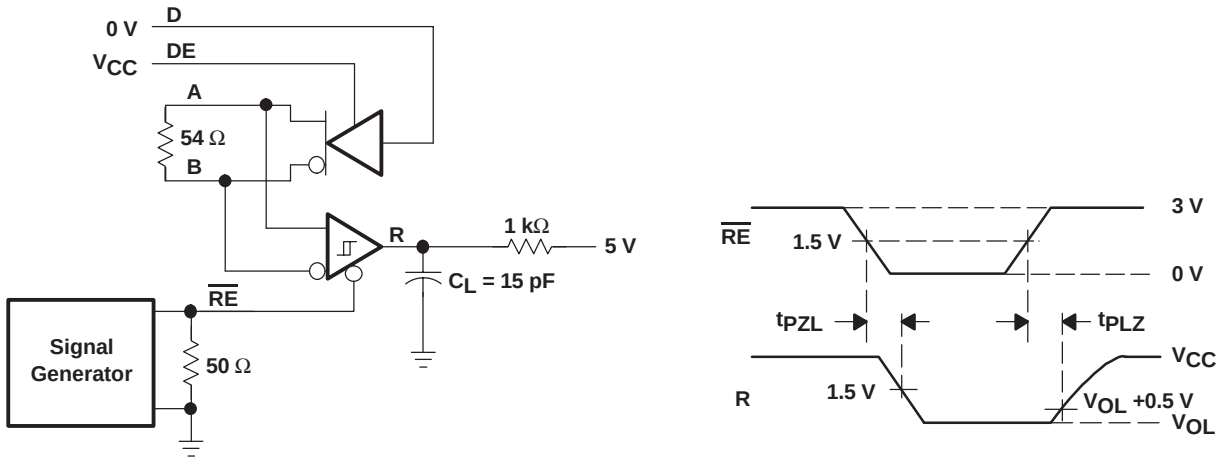


Figure 11. Receiver Enable/Disable Test Circuit and Waveforms, Data Output Low

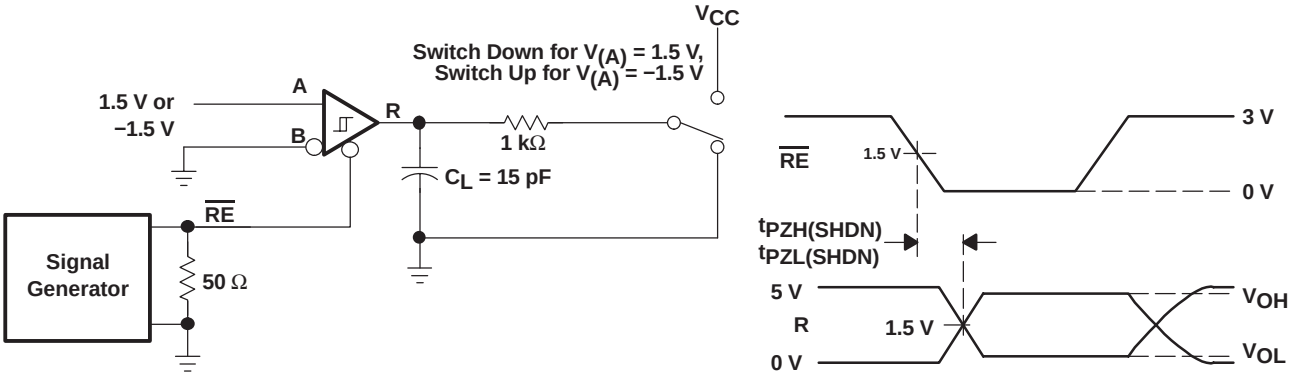


Figure 12. Receiver Enable From Shutdown Test Circuit and Waveforms

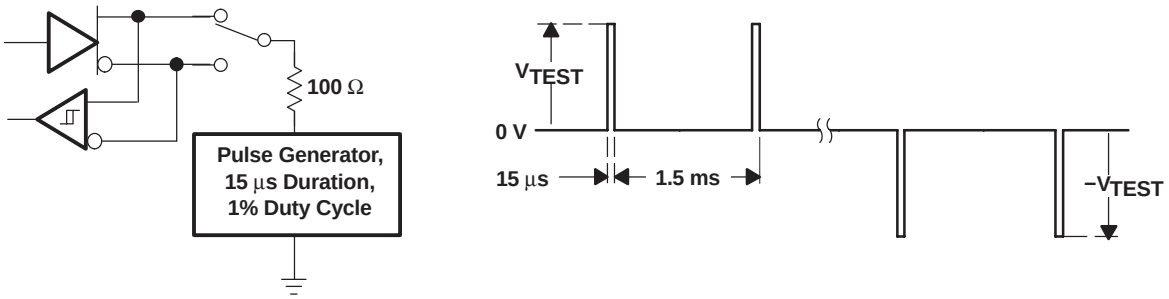
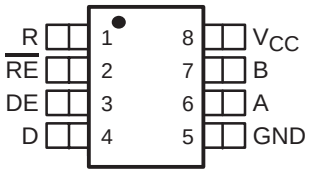


Figure 13. Test Circuit and Waveforms, Transient Over-Voltage Test

DEVICE INFORMATION

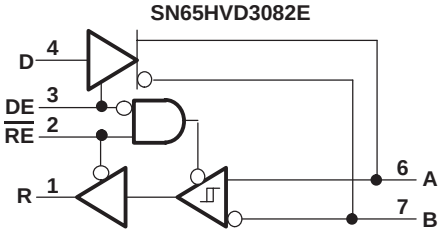
PIN ASSIGNMENTS

D, P OR DGK PACKAGE
(TOP VIEW)



LOGIC DIAGRAM (POSITIVE LOGIC)

SN65HVD3082E

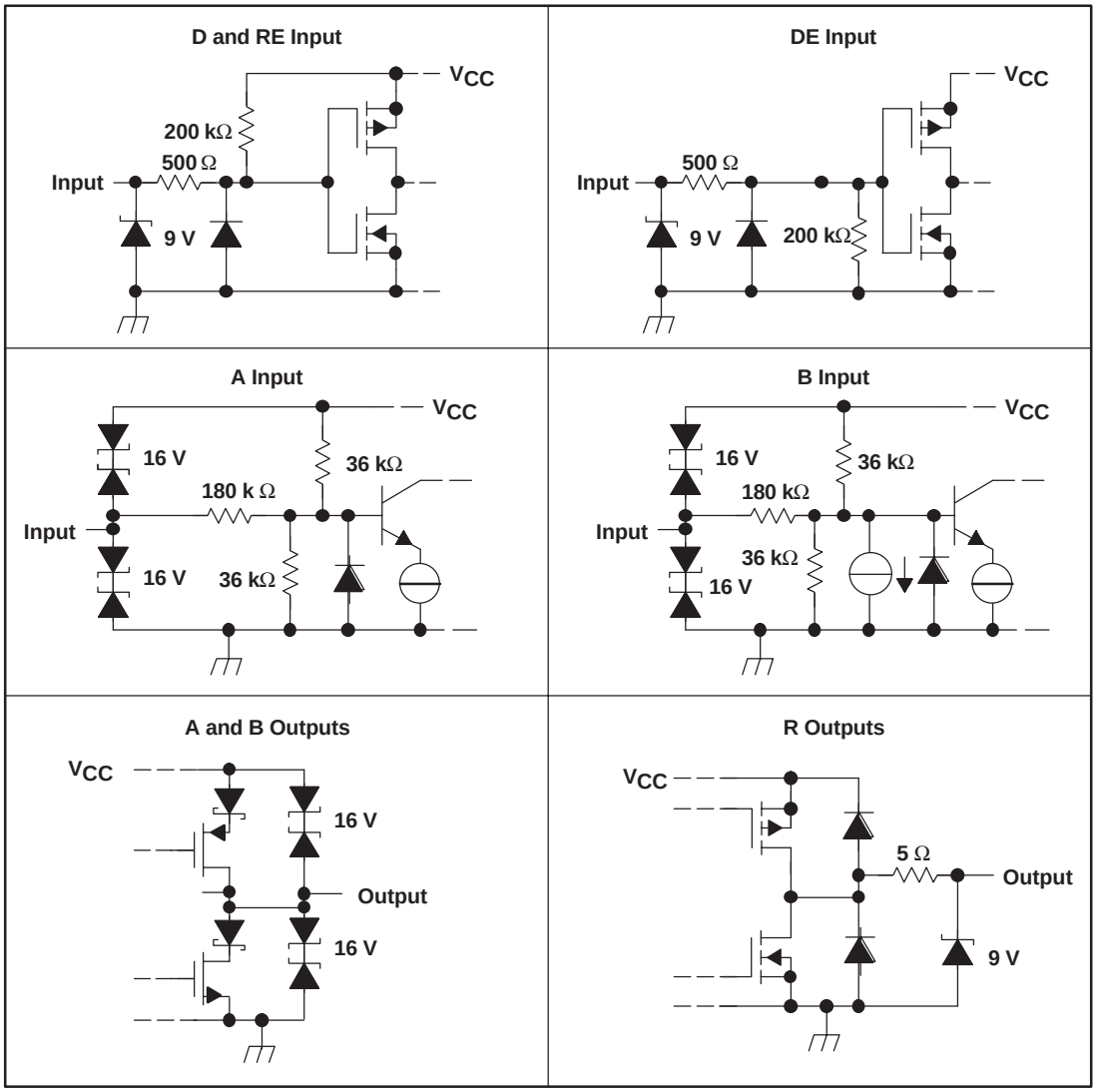


FUNCTION TABLE

DRIVER				RECEIVER		
INPUT D	ENABLE DE	OUTPUTS A	OUTPUTS B	DIFFERENTIAL INPUTS $V_{ID} = V_A - V_B$	ENABLE $\overline{RE}$	OUTPUT R
H	H	H	L	$V_{ID} \le -0.2$ V	L	L
L	H	L	H	-0.2 V $< V_{ID} < -0.01$ V	L	?
X	L	Z	Z	-0.01 V $\le V_{ID}$	L	H
Open	H	H	L	X	H	Z
X	Open	Z	Z	Open circuit	L	H
				Short circuit	L	H
				X	Open	Z

NOTE: H= high level; L = low level; Z = high impedance; X = irrelevant; ? = indeterminate

EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS



THERMAL CHARACTERISTICS

DGK Package

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Θ_{JA}	Junction-to-ambient thermal resistance(1)	Low-k(2) board, no air flow		266		°C/W
		High-k(3) board, no air flow		180		
Θ_{JB}	Junction-to-board thermal resistance	High-k(3) board, no air flow		108		°C/W
Θ_{JC}	Junction-to-case thermal resistance			66		
$P_{(AVG)}$	Average power dissipation	R_L = 54 Ω, Input to D is a 200 kbps 50% duty cycle square wave V_{CC} at 5.5 V, T_J = 130°C			203	mW
T_A	Ambient air temperature	JEDEC High K board model	−40		93	°C
		JEDEC Low K board model	−40		75	°C
T_{SD}	Thermal shut-down junction temperature			165		°C

(1) See TI application note literature number SZZA003, *Package Thermal Characterization Methodologies*, for an explanation of this parameter.
(2) JESD51-3 *Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
(3) JESD51-7 *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*

TYPICAL CHARACTERISTICS

BUS INPUT CURRENT vs BUS INPUT VOLTAGE

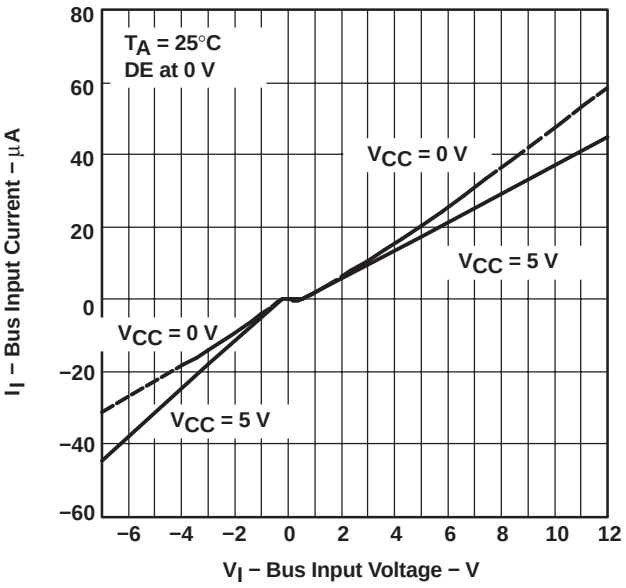


Figure 14

RMS SUPPLY CURRENT vs SIGNALING RATE

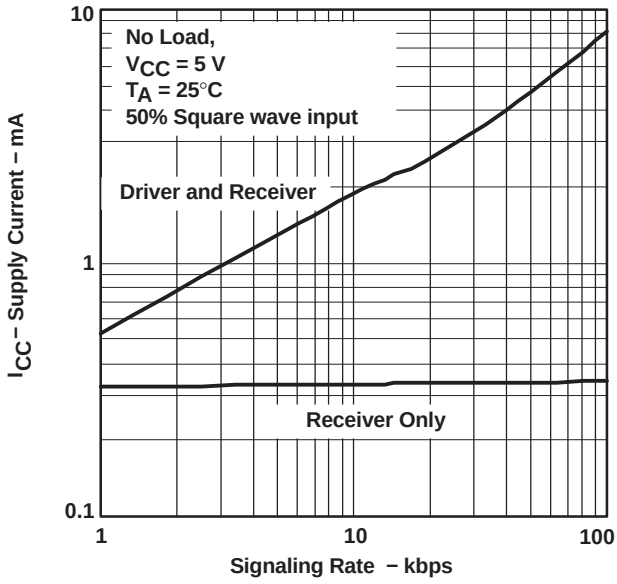


Figure 15

DRIVER DIFFERENTIAL OUTPUT VOLTAGE vs DIFFERENTIAL OUTPUT CURRENT

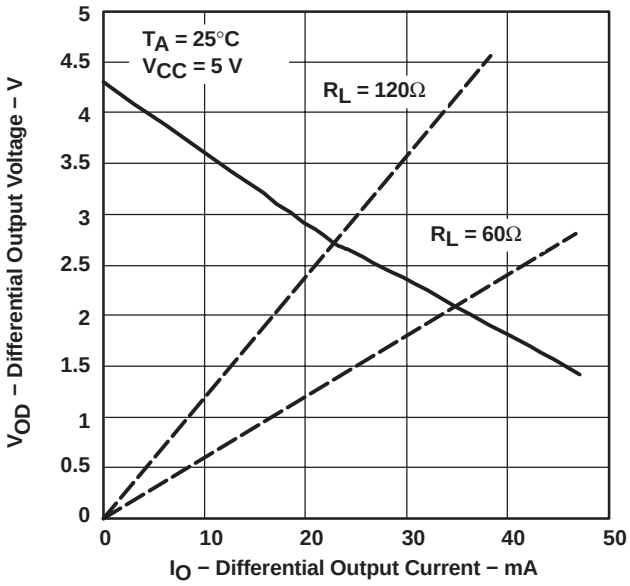


Figure 16

RECEIVER OUTPUT VOLTAGE vs DIFFERENTIAL INPUT VOLTAGE

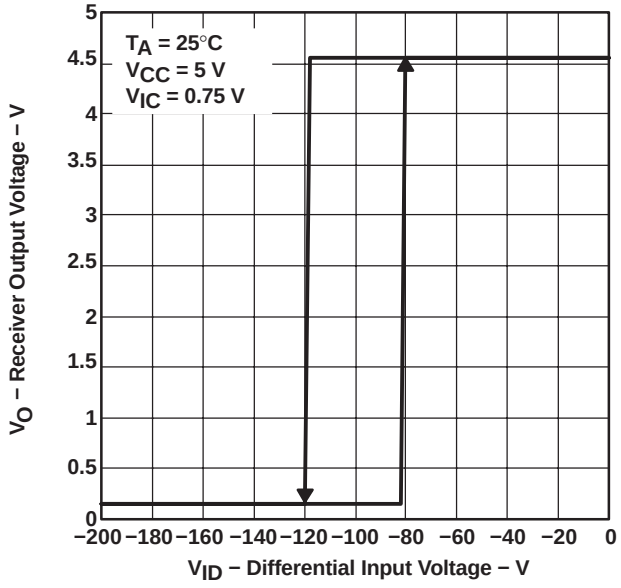
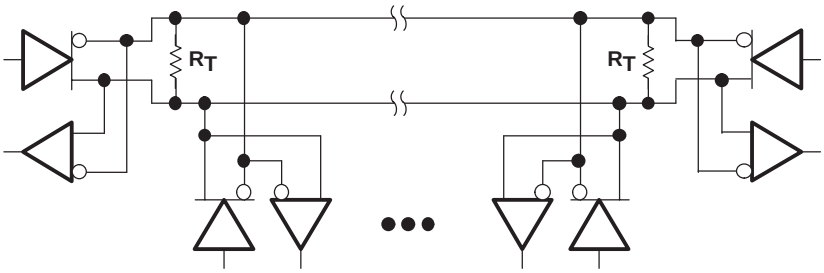


Figure 17

APPLICATION INFORMATION



NOTE: The line should be terminated at both ends with its characteristic impedance ($R_T = Z_O$). Stub lengths off the main line should be kept as short as possible.

Figure 18. Typical Application Circuit

POWER USAGE IN AN RS-485 TRANSCEIVER

Power consumption is a concern in many applications. Power supply current is delivered to the bus load as well as to the transceiver circuitry. For a typical RS-485 bus configuration, the load that an active driver must drive consists of all of the receiving nodes, plus the termination resistors at each end of the bus.

The load presented by the receiving nodes depends on the input impedance of the receiver. The TIA/EIA-485-A standard defines a unit load as allowing up to 1 mA. With up to 32 unit loads allowed on the bus, the total current supplied to all receivers can be as high as 32 mA. The HVD3082E is rated as a 1/8 unit load device. As shown in Figure 14, the bus input current is less than 1/8 mA, allowing up to 256 nodes on a single bus.

The current in the termination resistors depends on the differential bus voltage. The standard requires active drivers to produce at least 1.5 V of differential signal. For a bus terminated with one standard 120-Ω resistor at each end, this sums to 25 mA differential output current whenever the bus is active. Typically the HVD3082E can drive more than 25 mA to a 60 Ω load, resulting in a differential output voltage higher than the minimum required by the standard. (See Figure 16.)

Overall, the total load current can be 60 mA to a loaded RS-485 bus. This is in addition to the current required by the transceiver itself; the HVD3082E circuitry requires only about 0.4 mA with both driver and receiver enabled, and only 0.3 mA with either the driver enabled or with the receiver enabled. In low-power shutdown mode, neither the driver nor receiver is active, and the supply current is very low.

Supply current increases with signaling rate primarily due to the totum pole outputs of the driver (see Figure 15). When these outputs change state, there is a moment when both the high-side and low-side output transistors are conducting and this creates a short spike in the supply current. As the frequency of state changes increases, more power is used.

LOW-POWER SHUTDOWN MODE

When both the driver and receiver are disabled (DE low and $\overline{RE}$ high) the device is in shutdown mode. If the enable inputs are in this state for less than 60 ns, the device does not enter shutdown mode. This guards against inadvertently entering shutdown mode during driver/receiver enabling. Only when the enable inputs are held in this state for 300 ns or more, the device is assured to be in shutdown mode. In this low-power shutdown mode, most internal circuitry is powered down, and the supply current is typically 1 nA. When either the driver or the receiver is re-enabled, the internal circuitry becomes active.

If only the driver is re-enabled (DE transitions to high) the driver outputs are driven according to the D input after the enable times given by $t_{PZH(SHDN)}$ and $t_{PZL(SHDN)}$ in the driver switching characteristics. If the D input is open when the driver is enabled, the driver outputs defaults to A high and B low, in accordance with the driver failsafe feature.

If only the receiver is re-enabled ($\overline{RE}$ transitions to low) the receiver output is driven according to the state of the bus inputs (A and B) after the enable times given by $t_{PZH(SHDN)}$ and $t_{PZL(SHDN)}$ in the receiver switching characteristics. If there is no valid state on the bus the receiver responds as described in the failsafe operation section.

If both the receiver and driver are re-enabled simultaneously, the receiver output is driven according to the state of the bus inputs (A and B) and the driver output is driven according to the D input. Note that the state of the active driver affects the inputs to the receiver. Therefore, the receiver outputs are valid as soon as the driver outputs are valid.

THERMAL CHARACTERISTICS OF IC PACKAGES

Θ_{JA} (Junction-to-Ambient Thermal Resistance) is defined as the difference in junction temperature to ambient temperature divided by the operating power

Θ_{JA} is NOT a constant and is a strong function of

- the PCB design (50% variation)
- altitude (20% variation)
- device power (5% variation)

Θ_{JA} can be used to compare the thermal performance of packages if the specific test conditions are defined and used. Standardized testing includes specification of PCB construction, test chamber volume, sensor locations, and the thermal characteristics of holding fixtures. $_{\Theta JA}$ is often misused when it is used to calculate junction temperatures for other installations.

TI uses two test PCBs as defined by JEDEC specifications. The low-k board gives *average* in-use condition thermal performance and consists of a single trace layer 25 mm long and 2-oz thick copper. The high-k board gives *best case* in−use condition and consists of 2 1-oz buried power planes with a single trace layer 25 mm long with 2-oz thick copper. A 4% to 50% difference in $_{\Theta JA}$ can be measured between these two test cards

Θ_{JC} (Junction-to-Case Thermal Resistance) is defined as difference in junction temperature to case divided by the operating power. It is measured by putting the mounted package up against a copper block cold plate to force heat to flow from die, through the mold compound into the copper block.

Θ_{JC} is a useful thermal characteristic when a heatsink is applied to package. It is NOT a useful characteristic to predict junction temperature as it provides pessimistic numbers if the case temperature is measured in a non-standard system and junction temperatures are backed out. It can be used with Θ_{JB} in 1-dimensional thermal simulation of a package system.

Θ_{JB} (Junction-to-Board Thermal Resistance) is defined to be the difference in the junction temperature and the PCB temperature at the center of the package (closest to the die) when the PCB is clamped in a cold−plate structure. Θ_{JB} is only defined for the high-k test card.

Θ_{JB} provides an overall thermal resistance between the die and the PCB. It includes a bit of the PCB thermal resistance (especially for BGA's with thermal balls) and can be used for simple 1-dimensional network analysis of package system (see figure 19).

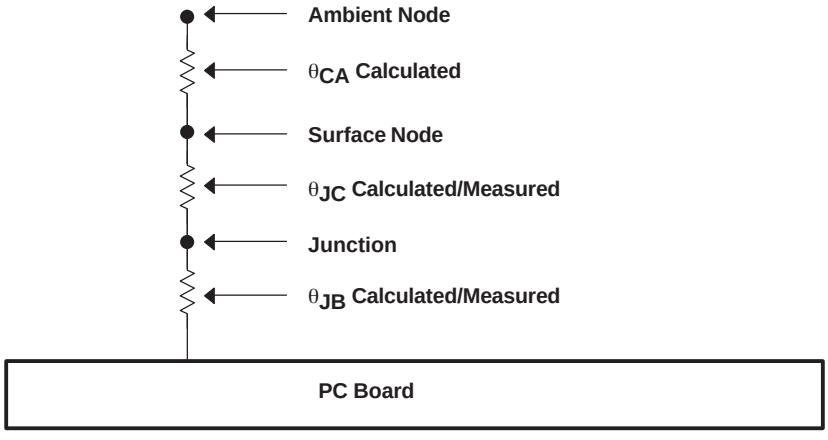
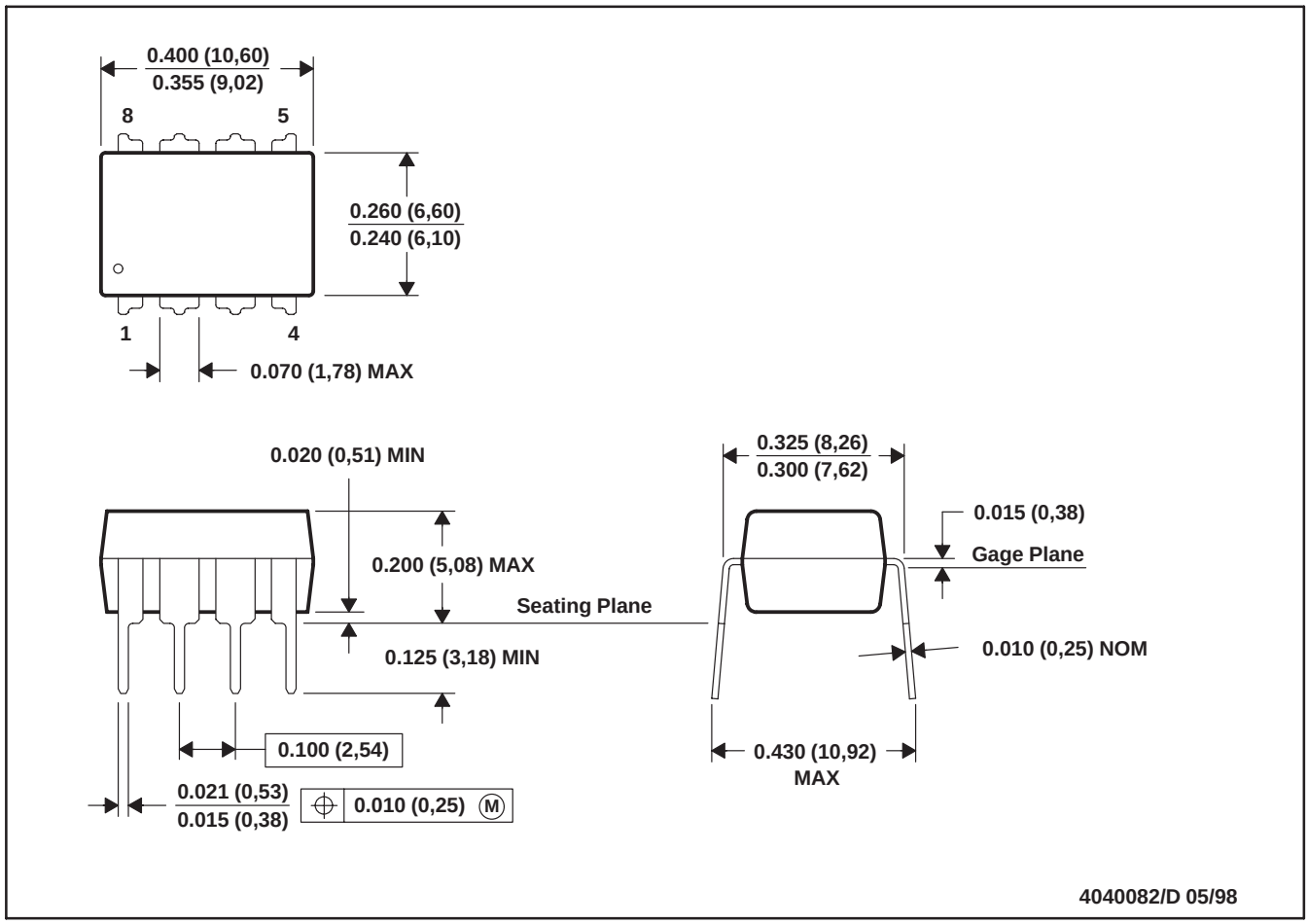


Figure 19. Thermal Resistance

MPDI001A – JANUARY 1995 – REVISED JUNE 1999

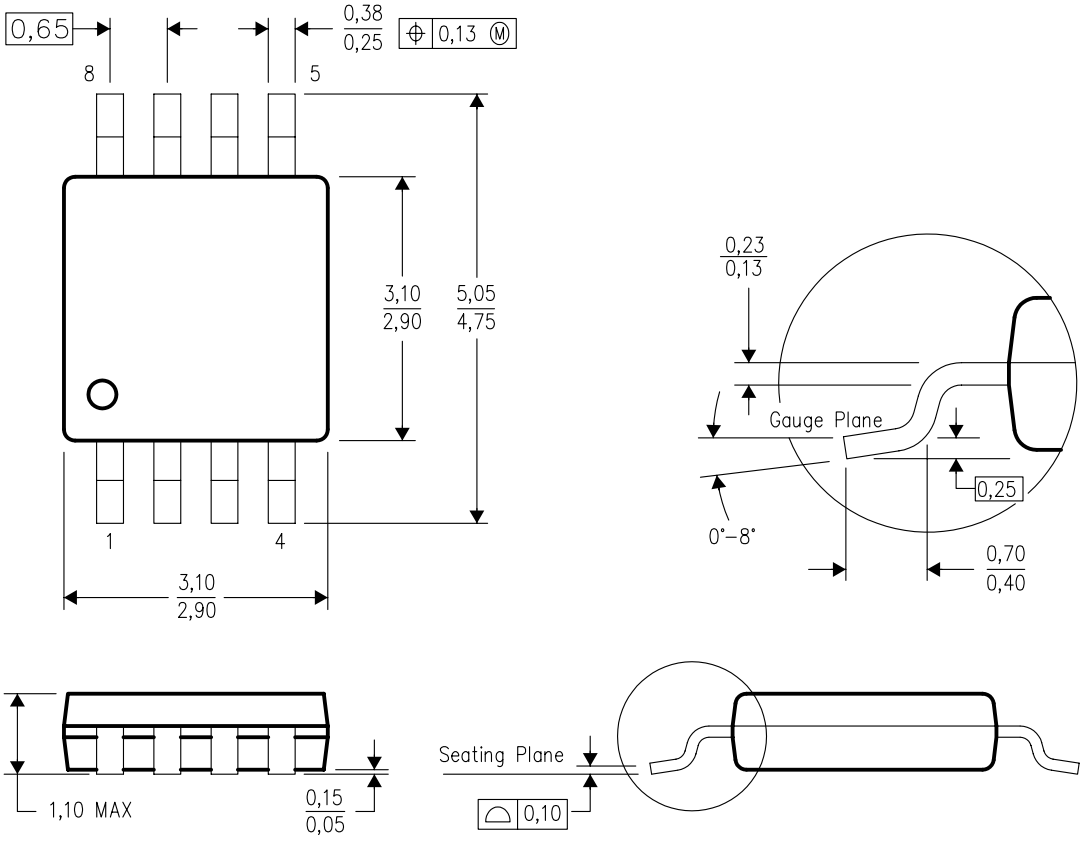
P (R-PDIP-T8) **PLASTIC DUAL-IN-LINE**



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-001

For the latest package information, go to http://www.ti.com/sc/docs/package/pkg_info.htm

DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/D 12/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO–187 variation AA.

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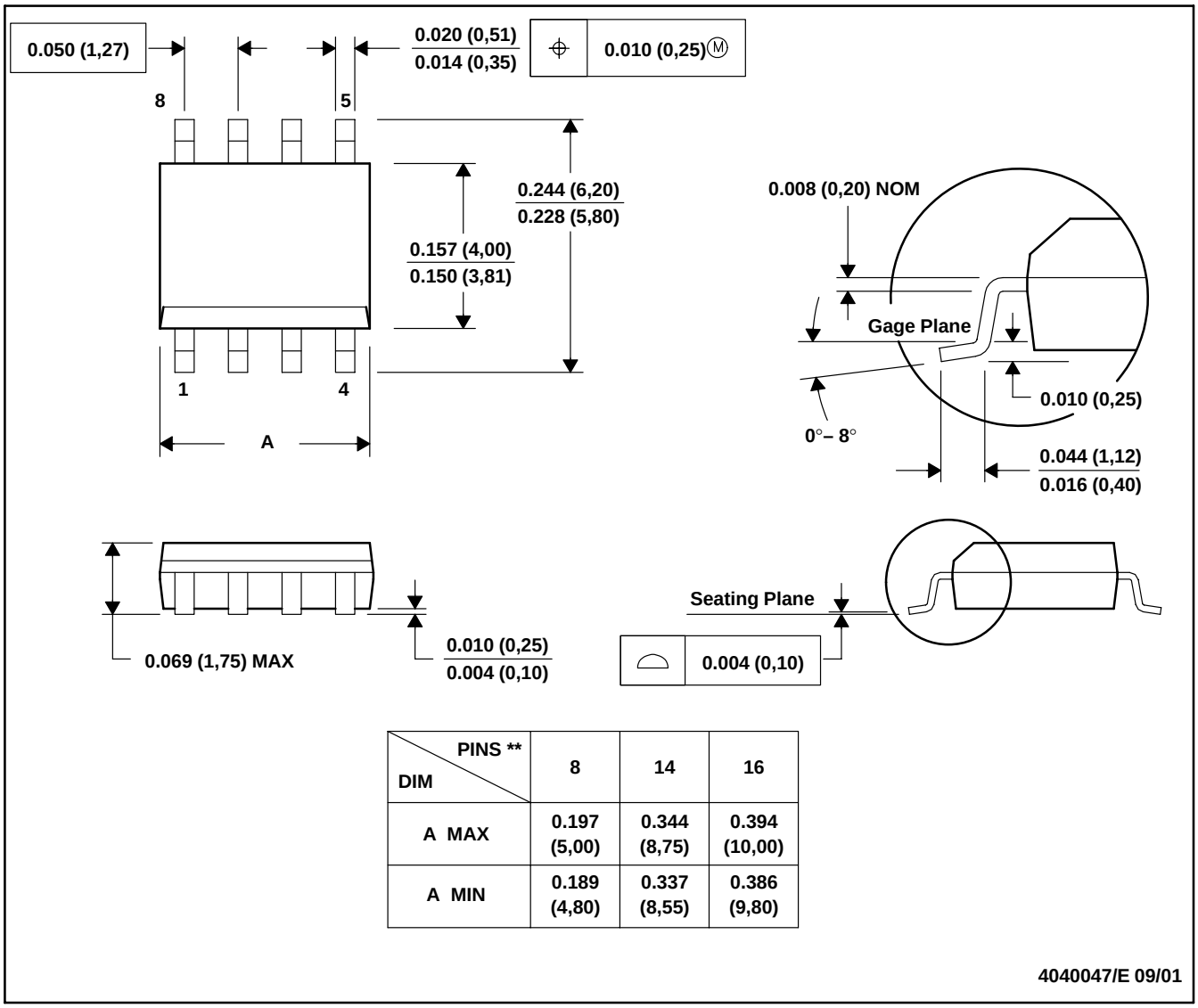
D (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

8 PINS SHOWN



DIM \ PINS **	8	14	16
A MAX	0.197 (5,00)	0.344 (8,75)	0.394 (10,00)
A MIN	0.189 (4,80)	0.337 (8,55)	0.386 (9,80)

4040047/E 09/01

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
D. Falls within JEDEC MS-012

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