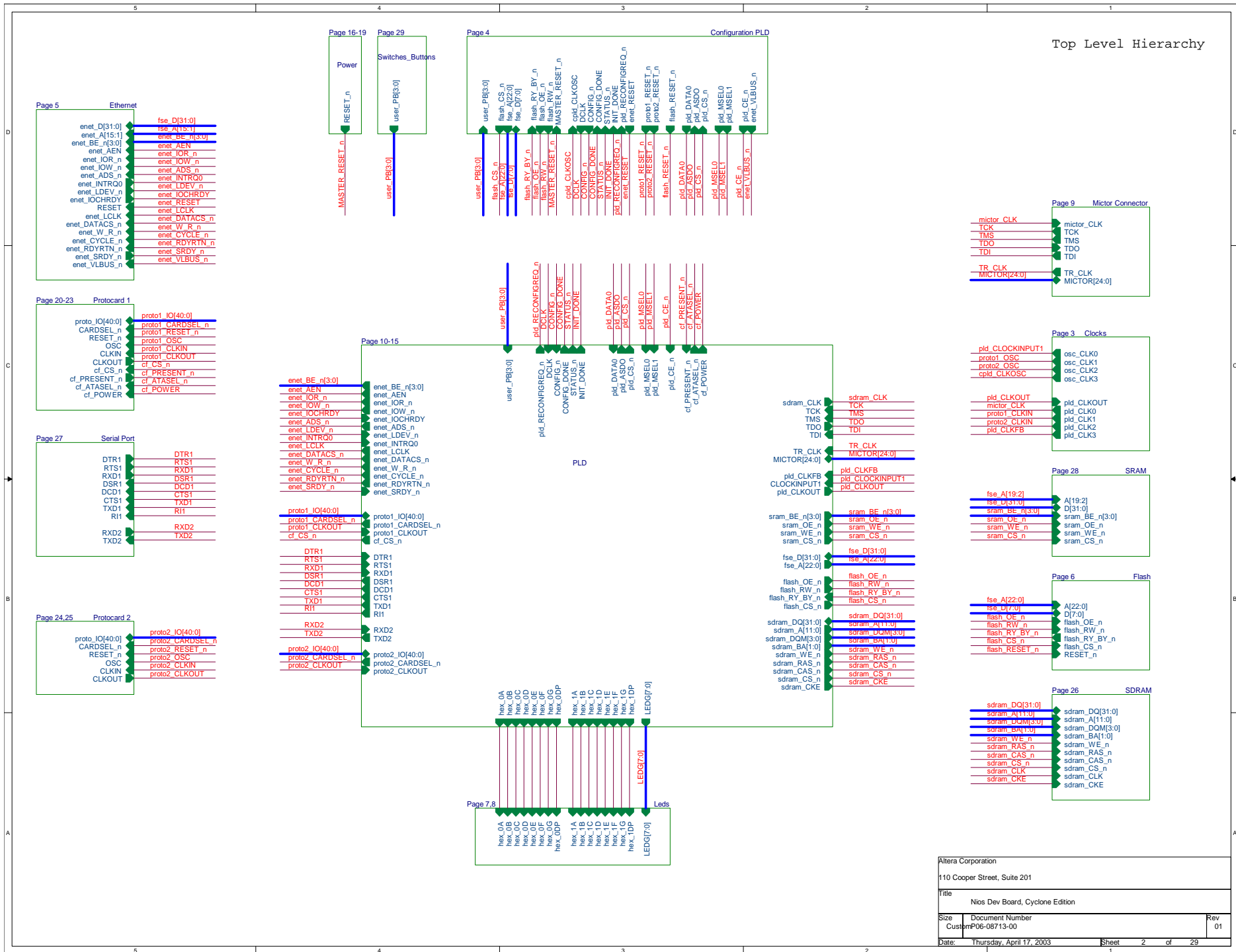


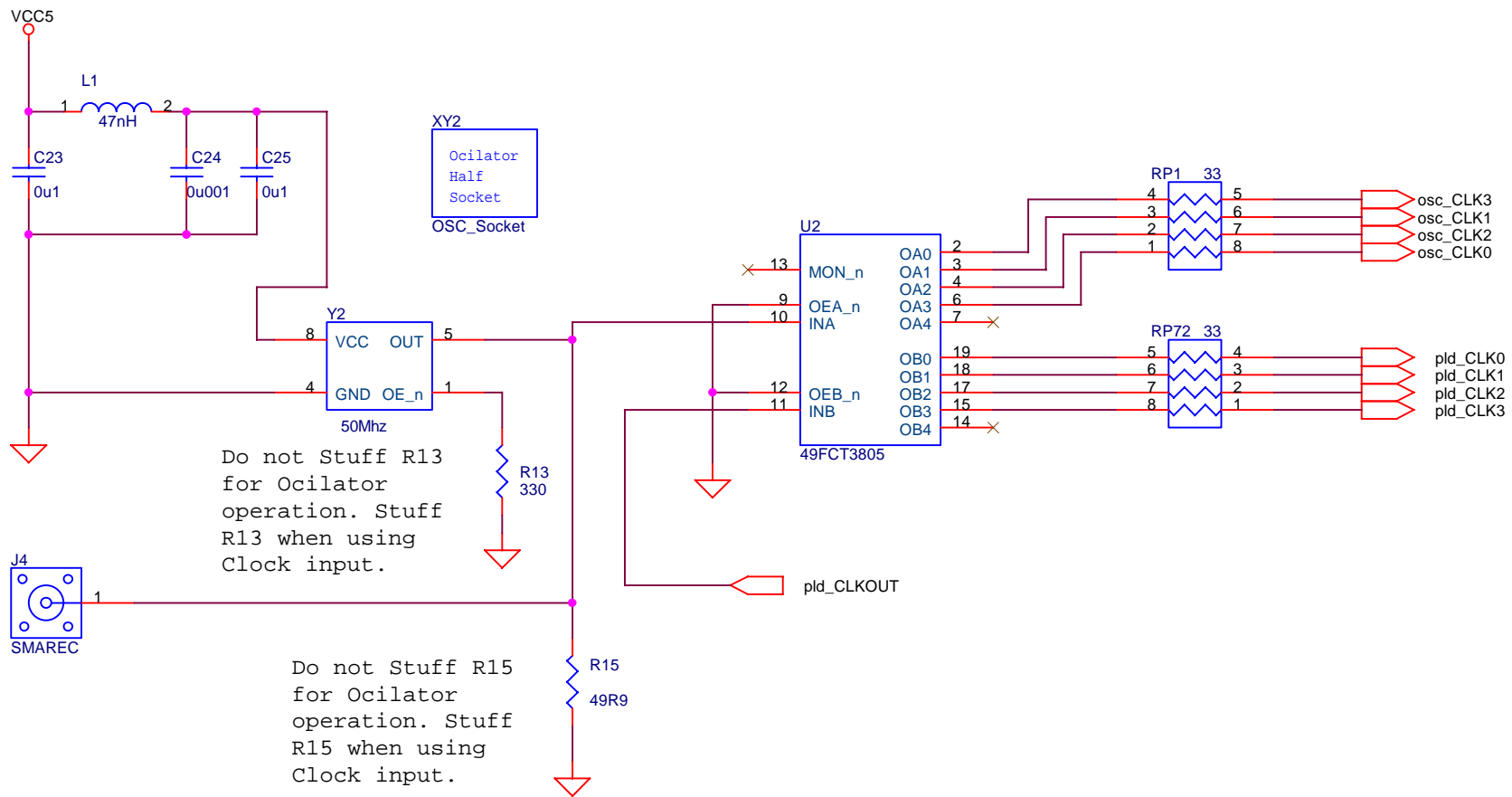
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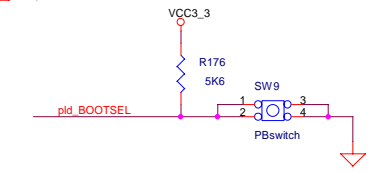
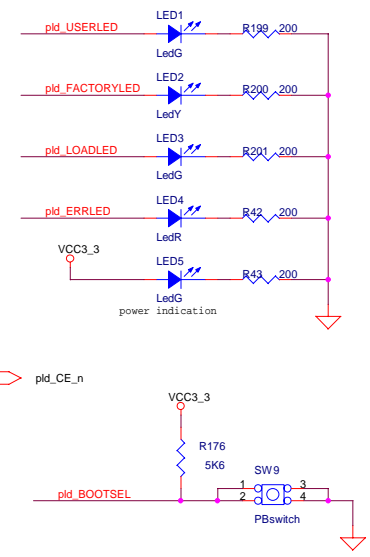
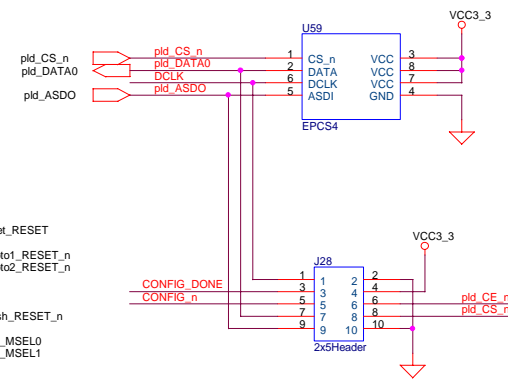
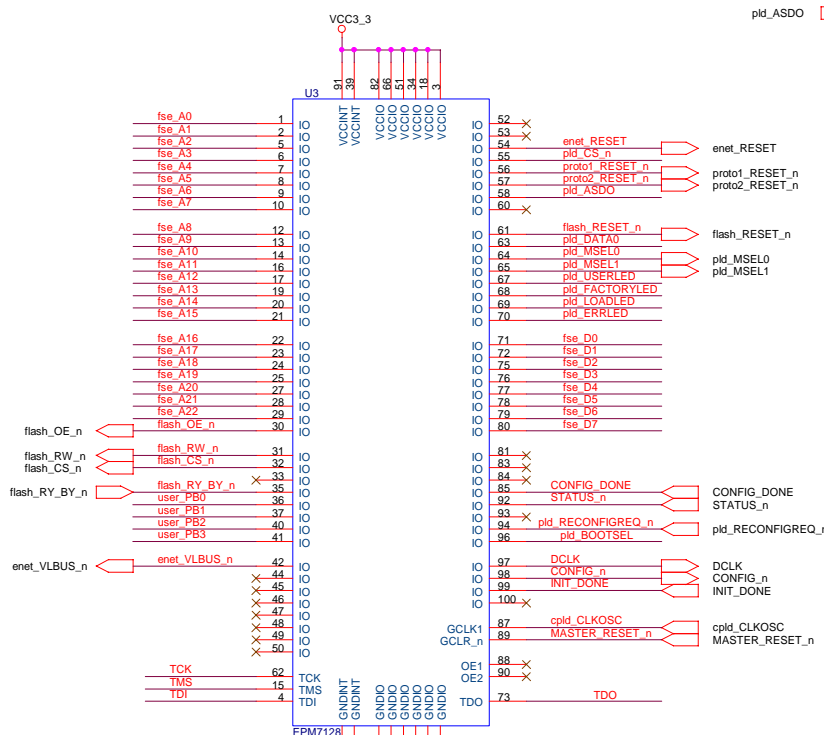
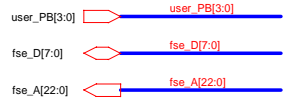
Top Level Hierarchy



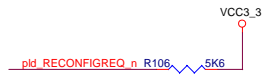
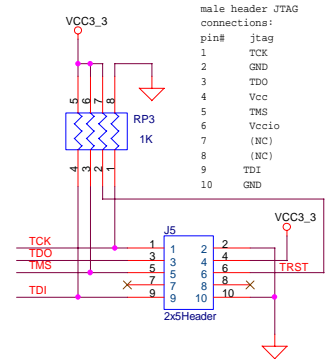
Clocks



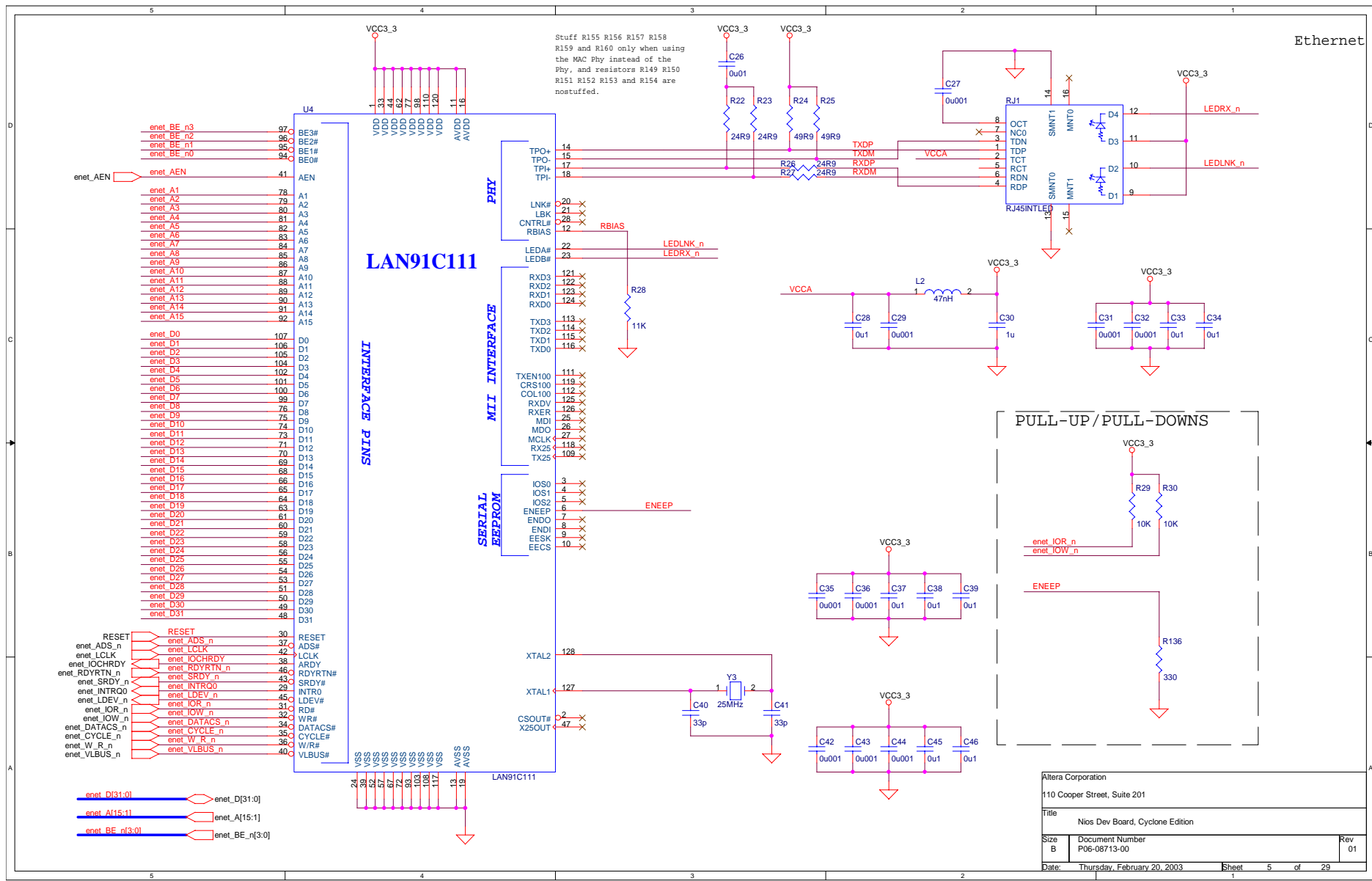
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pld_BOOTSEL determines whether to force a boot from the default boot sector, or the user-programmed boot sector.



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- enet_BE_n3 97 BE3#
- enet_BE_n2 96 BE2#
- enet_BE_n1 95 BE1#
- enet_BE_n0 94 BE0#
- enet_AEN 41 AEN
- enet_A1 78 A1
- enet_A2 79 A2
- enet_A3 80 A3
- enet_A4 81 A4
- enet_A5 82 A5
- enet_A6 83 A6
- enet_A7 84 A7
- enet_A8 85 A8
- enet_A9 86 A9
- enet_A10 87 A10
- enet_A11 88 A11
- enet_A12 89 A12
- enet_A13 90 A13
- enet_A14 91 A14
- enet_A15 92 A15
- enet_D0 107 D0
- enet_D1 106 D1
- enet_D2 105 D2
- enet_D3 104 D3
- enet_D4 102 D4
- enet_D5 101 D5
- enet_D6 100 D6
- enet_D7 99 D7
- enet_D8 76 D8
- enet_D9 75 D9
- enet_D10 74 D10
- enet_D11 73 D11
- enet_D12 71 D12
- enet_D13 70 D13
- enet_D14 69 D14
- enet_D15 68 D15
- enet_D16 66 D16
- enet_D17 65 D17
- enet_D18 64 D18
- enet_D19 63 D19
- enet_D20 61 D20
- enet_D21 60 D21
- enet_D22 59 D22
- enet_D23 58 D23
- enet_D24 56 D24
- enet_D25 55 D25
- enet_D26 54 D26
- enet_D27 53 D27
- enet_D28 51 D28
- enet_D29 50 D29
- enet_D30 49 D30
- enet_D31 48 D31
- RESET 30 RESET
- enet_ADS_n 37 ADS#
- enet_LCLK 42 LCLK
- enet_IOCHRDY 38 ARDY
- enet_RDYRTN_n 46 RDYRTN#
- enet_SRDY_n 43 SRDY#
- enet_INTRQ0 29 INTRQ
- enet_LDEV_n 45 LDEV#
- enet_IOR_n 31 RD#
- enet_IOW_n 32 WR#
- enet_DATACS_n 34 DATACS#
- enet_CYCLE_n 35 CYCLE#
- enet_W_R_n 36 W/R#
- enet_VLBUS_n 40 VLBUS#

- enet_D[31:0] enet_D[31:0]
- enet_A[15:1] enet_A[15:1]
- enet_BE_n[3:0] enet_BE_n[3:0]

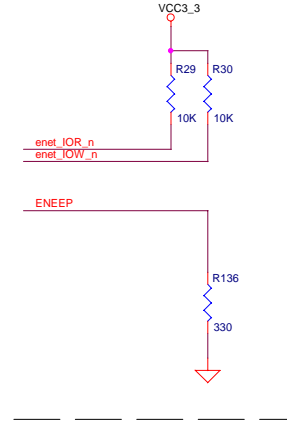
LAN91C111

INTERFACE PINS

LAN91C111

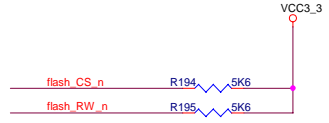
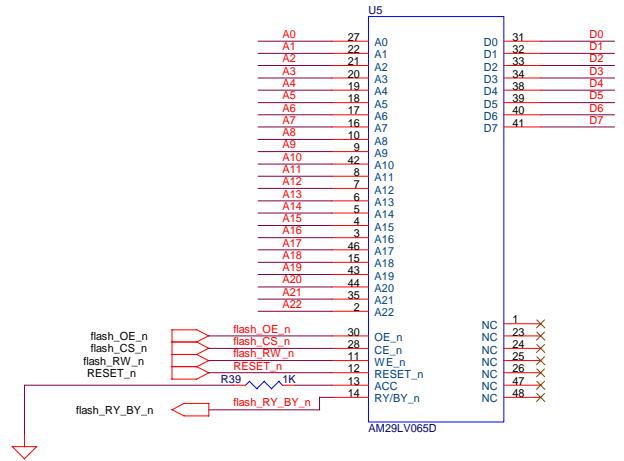
Stuff R155 R156 R157 R158 R159 and R160 only when using the MII Phy instead of the Phy, and resistors R149 R150 R151 R152 R153 and R154 are not stuffed.

PULL-UP / PULL-DOWNS



A[22:0]  A[22:0]

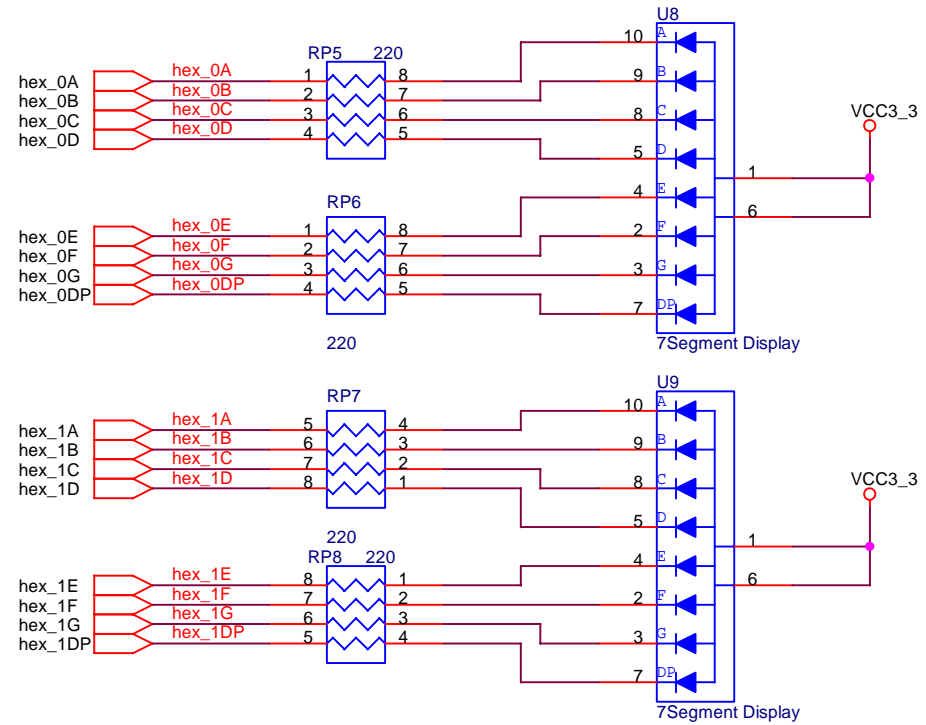
D[7:0]  D[7:0]



Flash chip is 8M x 8 for 8Mbytes of flash

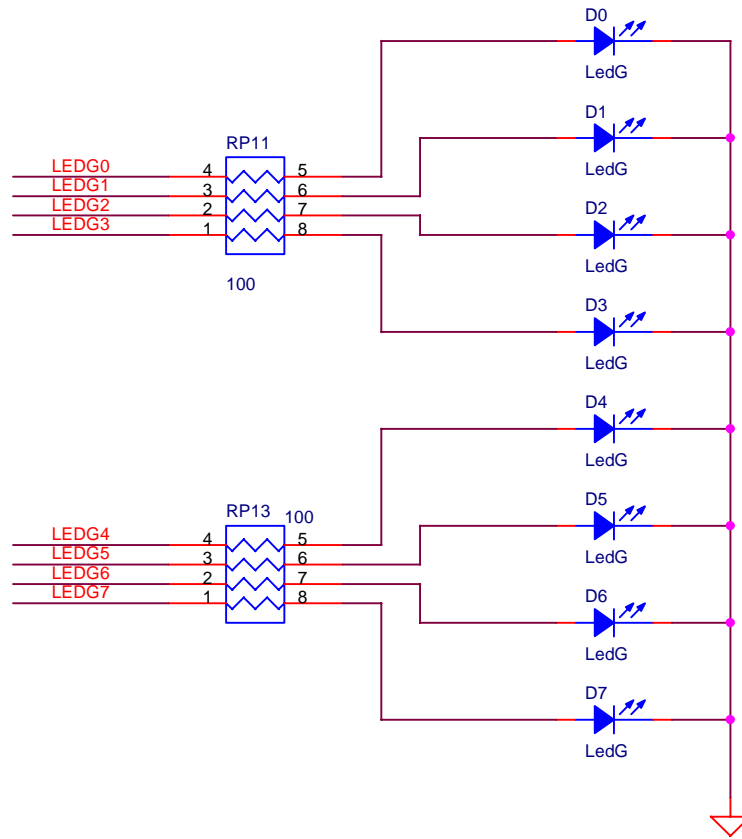
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Hex Display



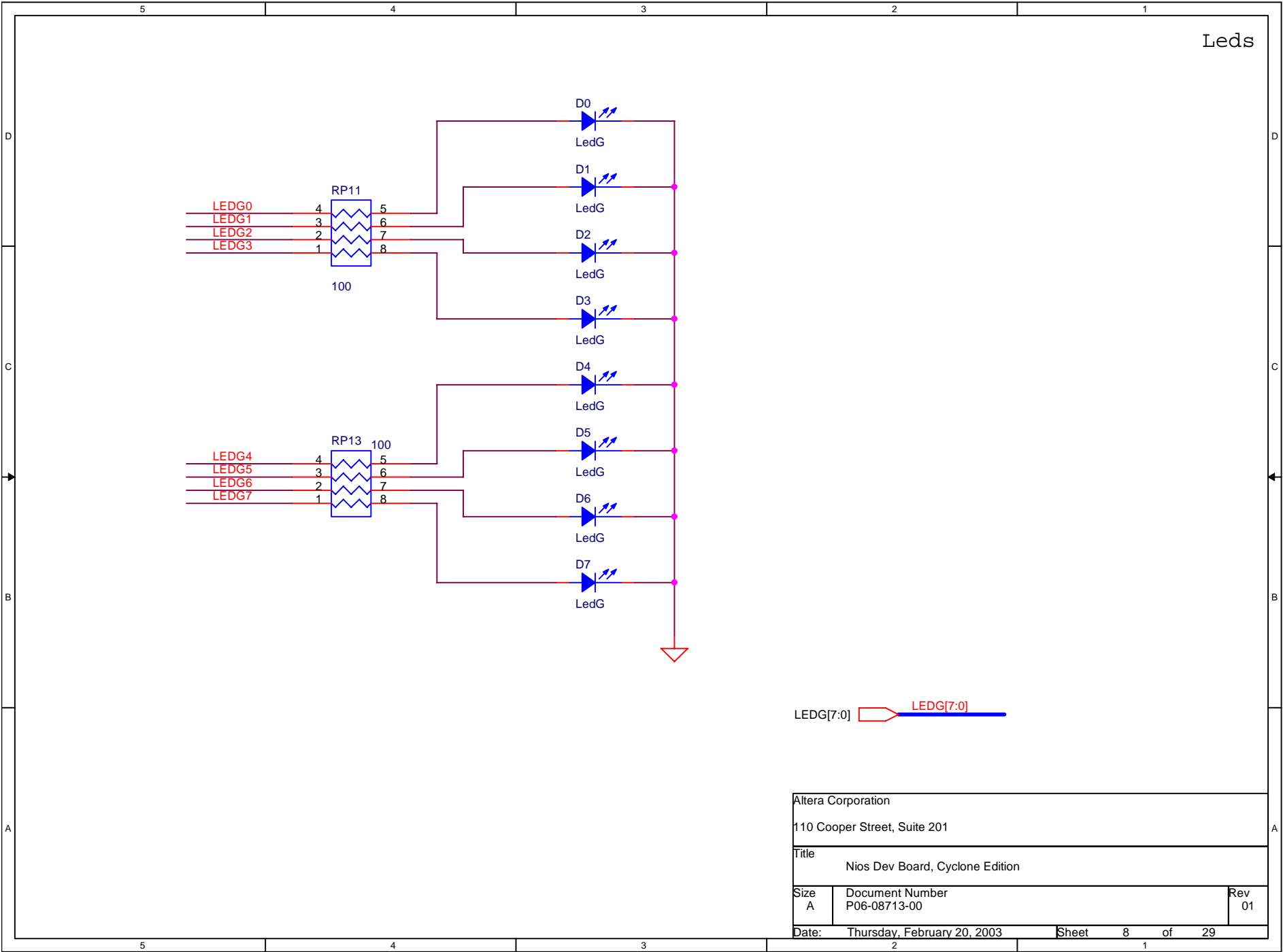
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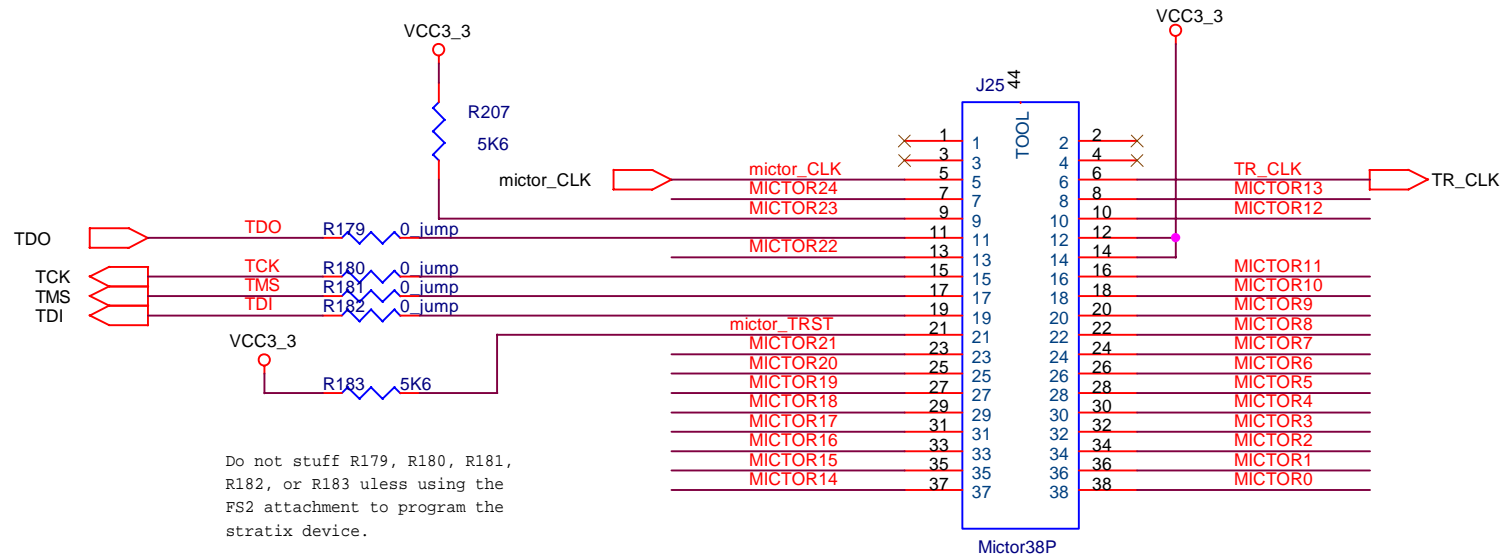
Leds



LEDG[7:0] LEDG[7:0]

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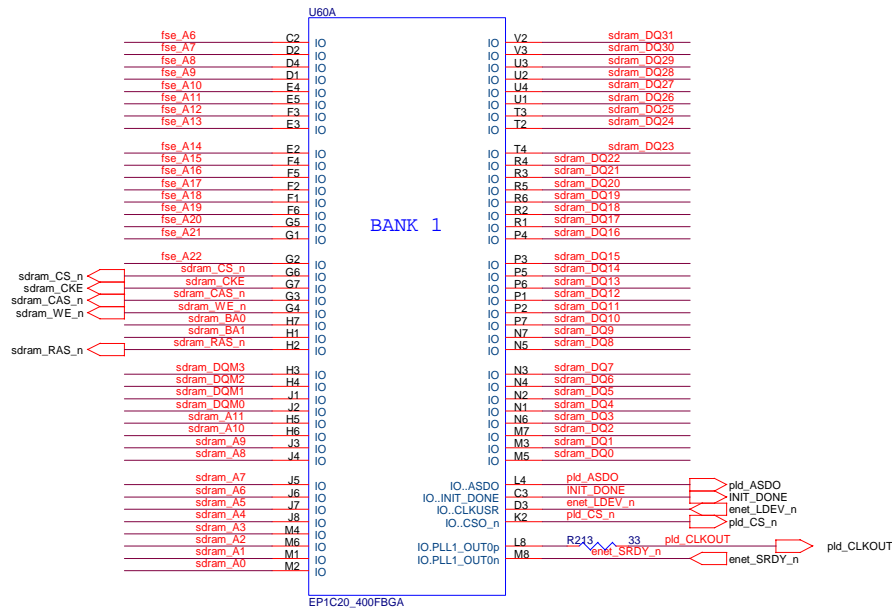


MICTOR[24:0]  MICTOR[24:0]

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PLD Bank 1

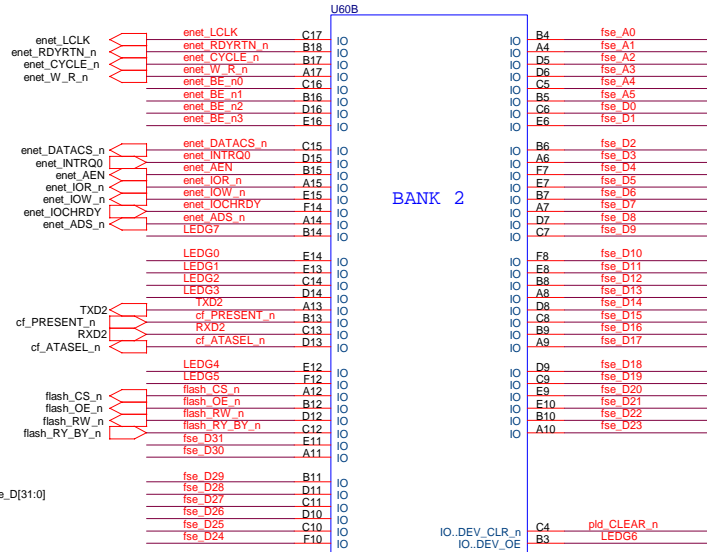
fse_A[22:0] → fse_A[22:0]



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PLD Bank 2

fse_A[22:0] → fse_A[22:0]



LEDG[7:0] → LEDG[7:0]

fse_D[31:0] → fse_D[31:0]

VCC3_3

R85
SK6
SW8

PBswitch

Label this button very clearly with the words: CPU RESET and put a box around the button and text.

IO_DEV_CLR_n
IO_DEV_OE

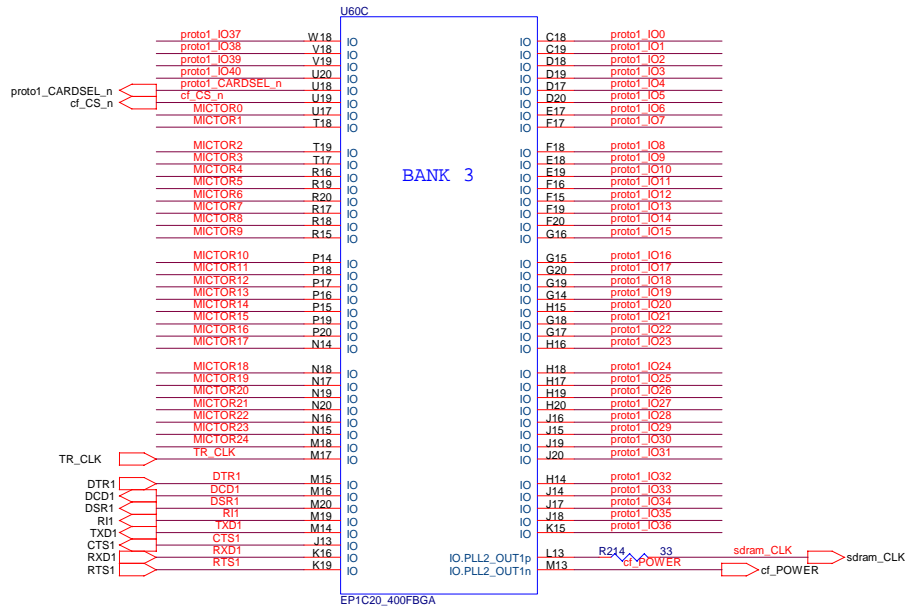
pld CLEAR_n

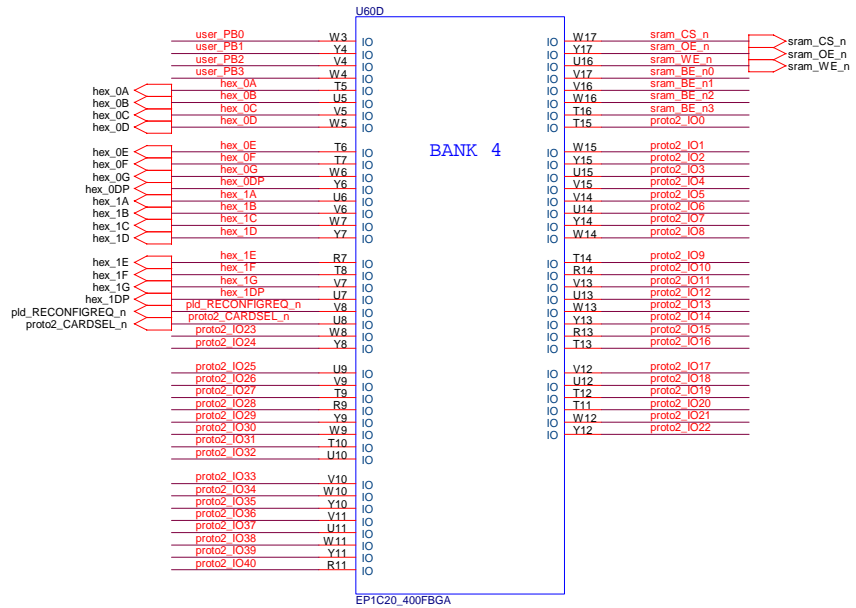
LEDG6

enet_BE_n[3:0] → enet_BE_n[3:0]

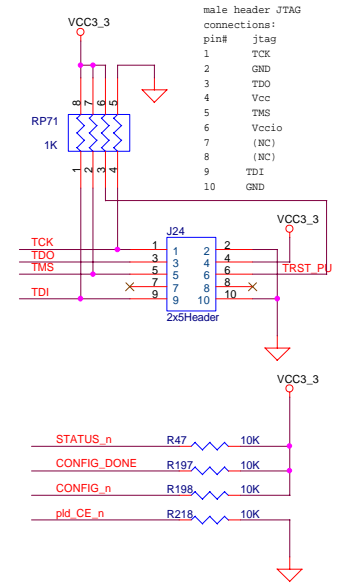
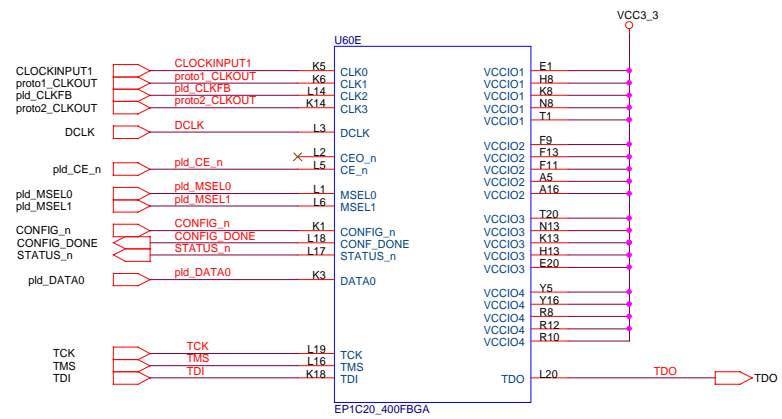
fse_D[31:0] → fse_D[31:0]

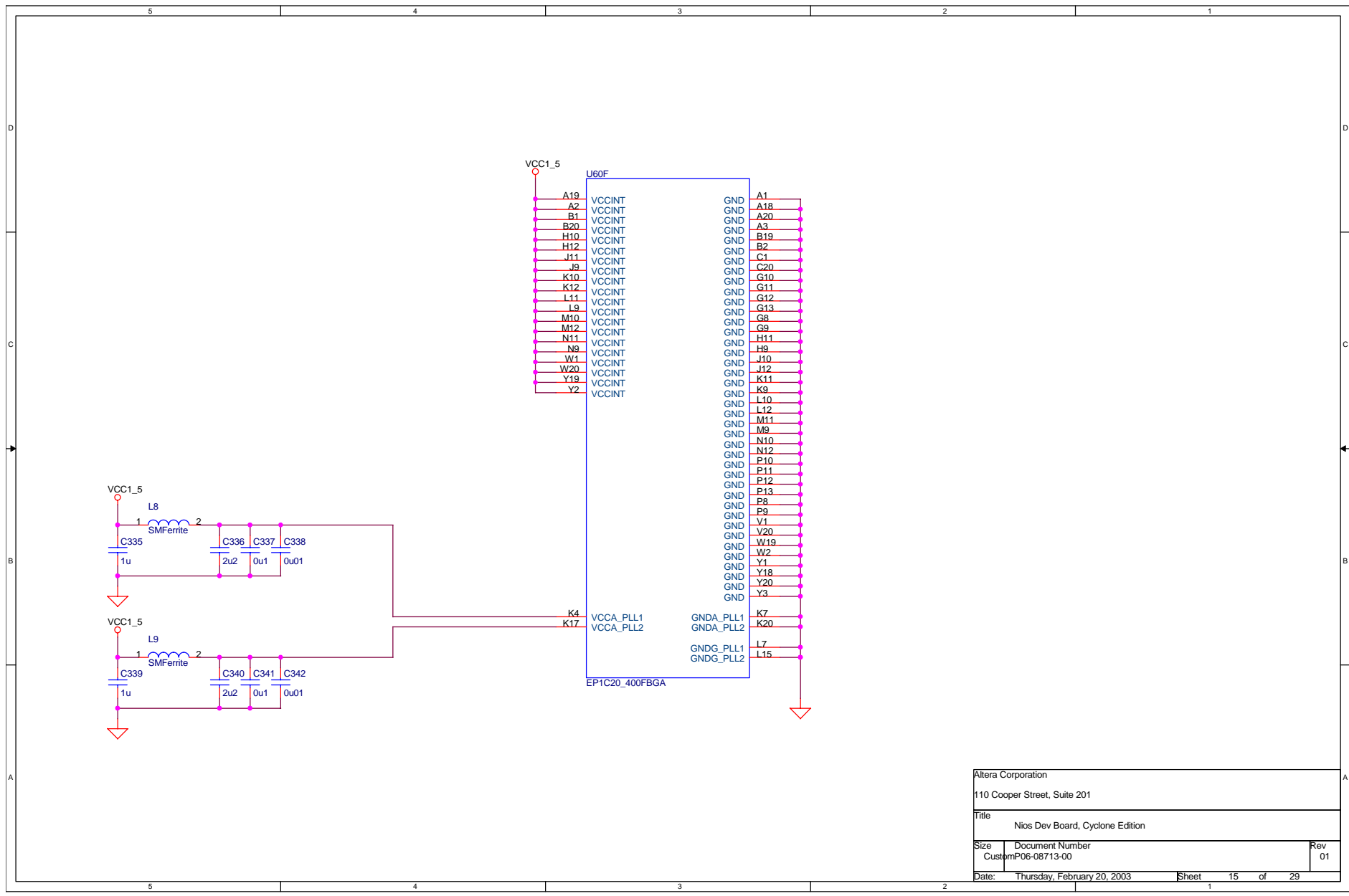
PLD Bank 3





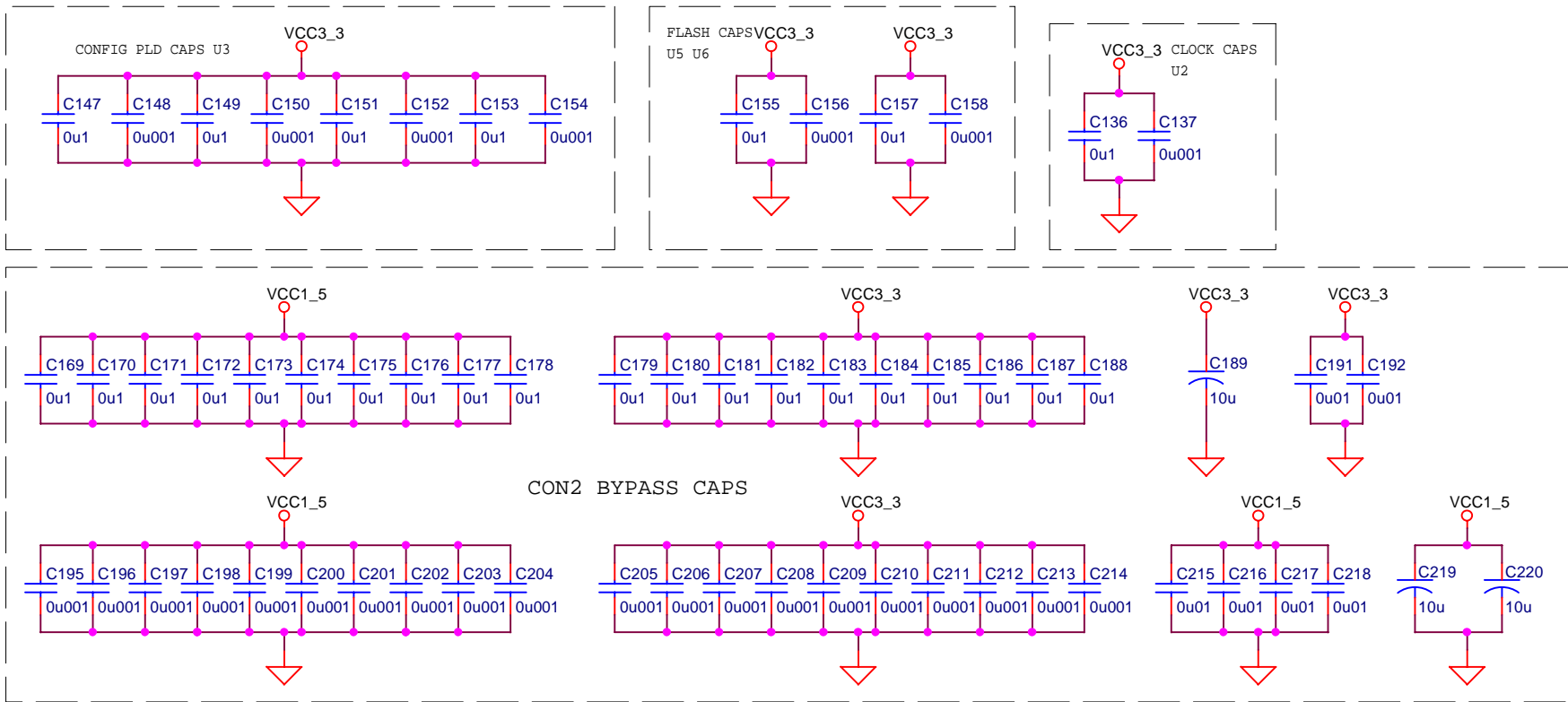
PLD Control Signals



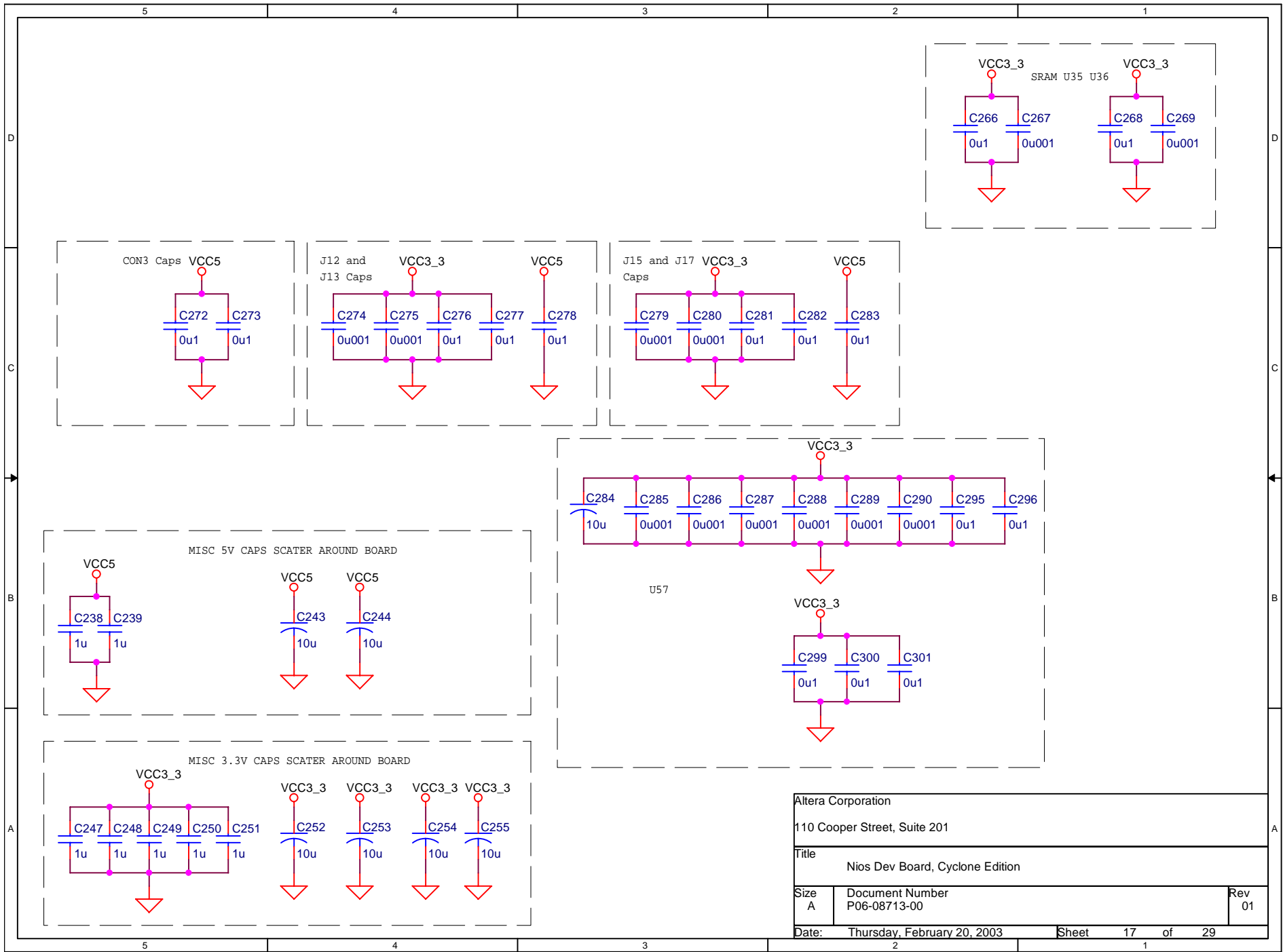


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Bypass CAPS

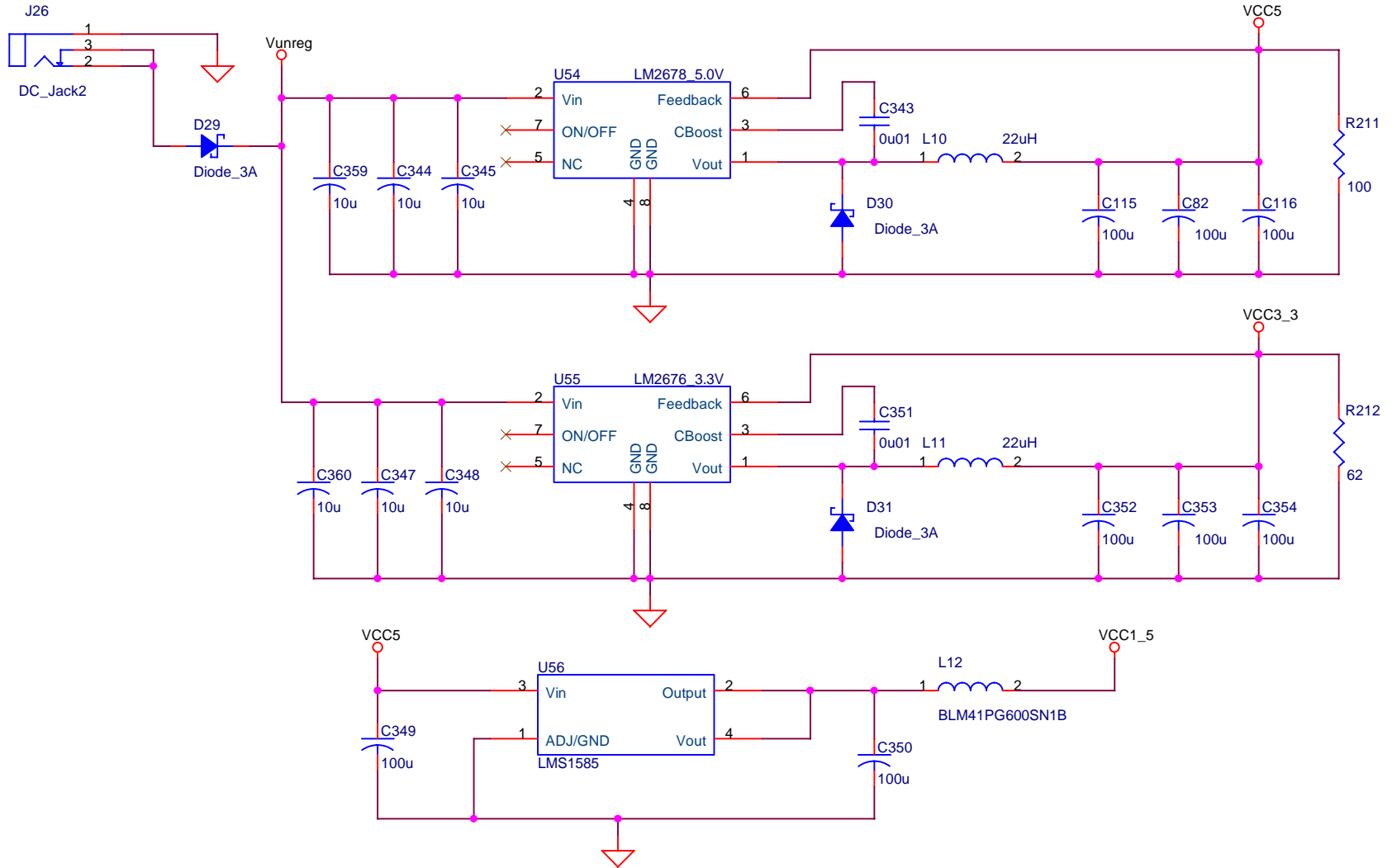


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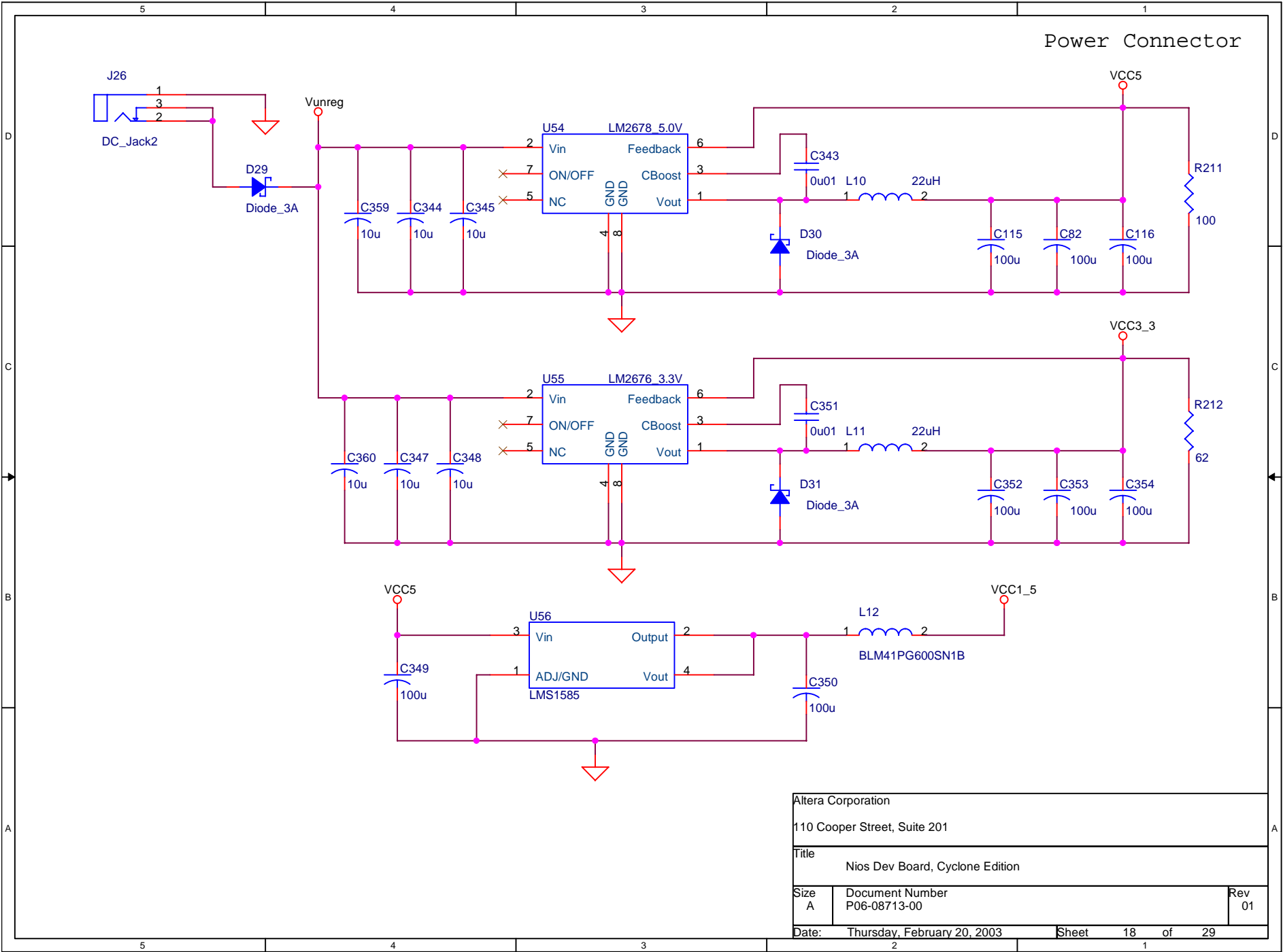


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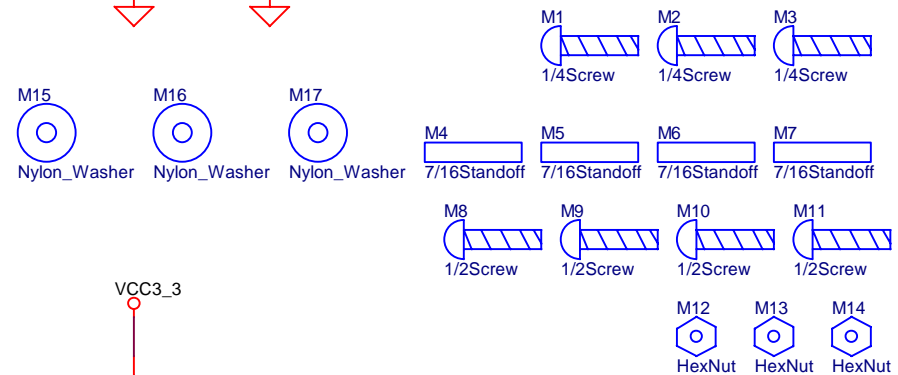
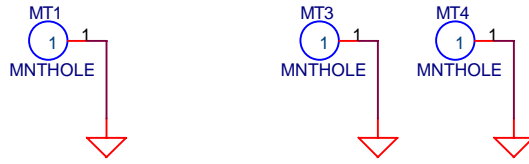
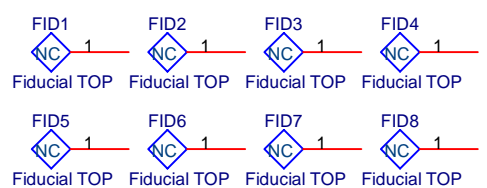
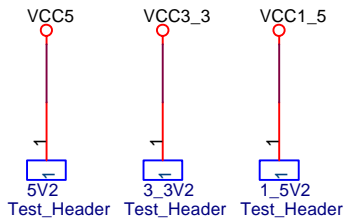
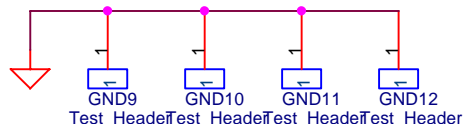
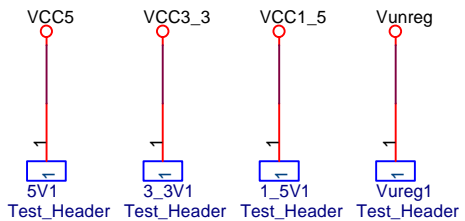
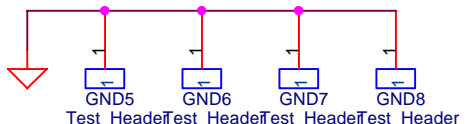
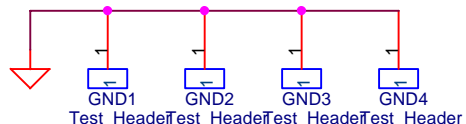
Power Connector



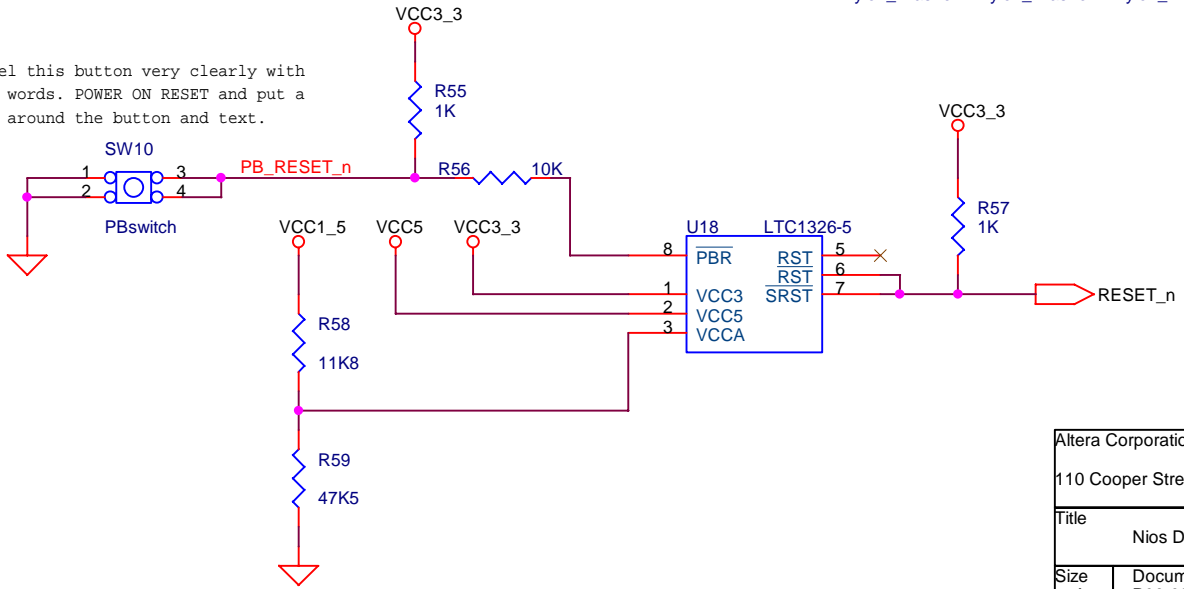
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Reset and Test headers

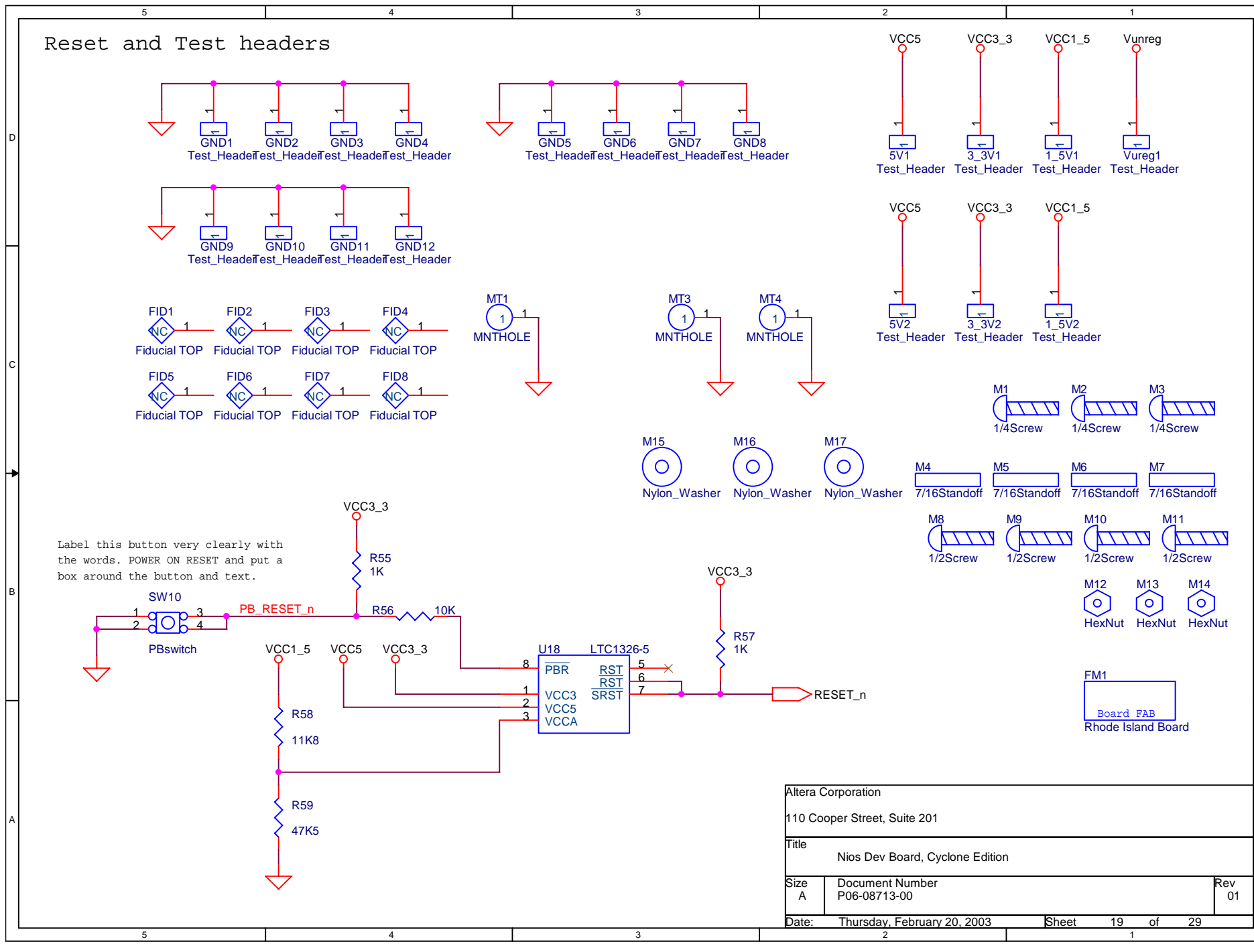


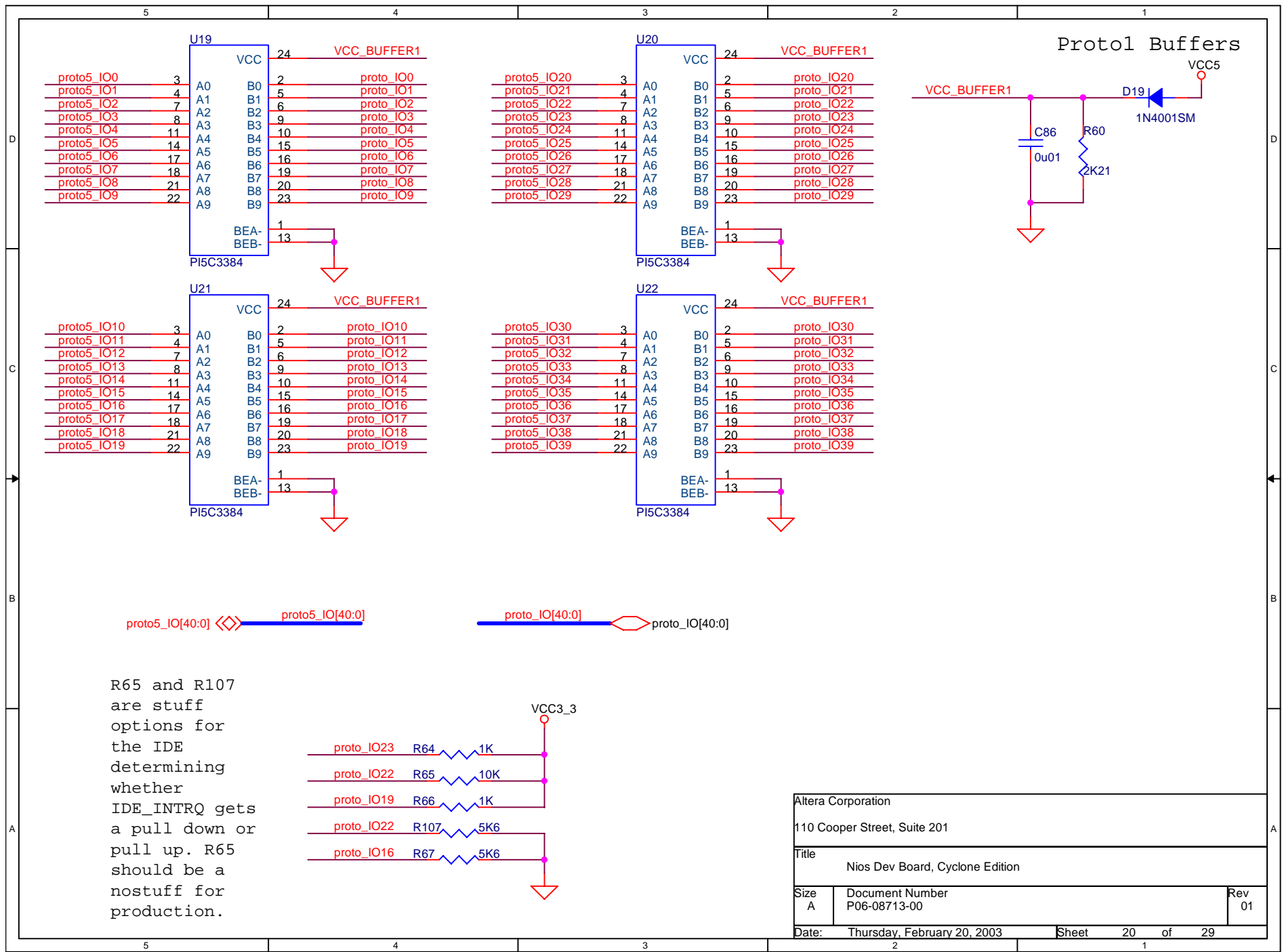
Label this button very clearly with the words. POWER ON RESET and put a box around the button and text.



FM1
Board FAB
Rhode Island Board

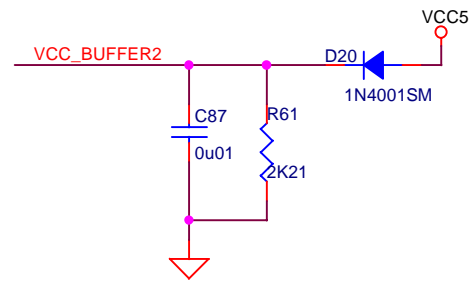
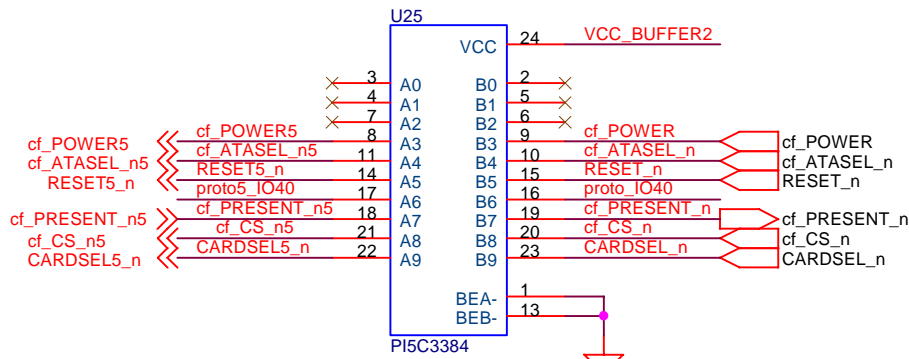
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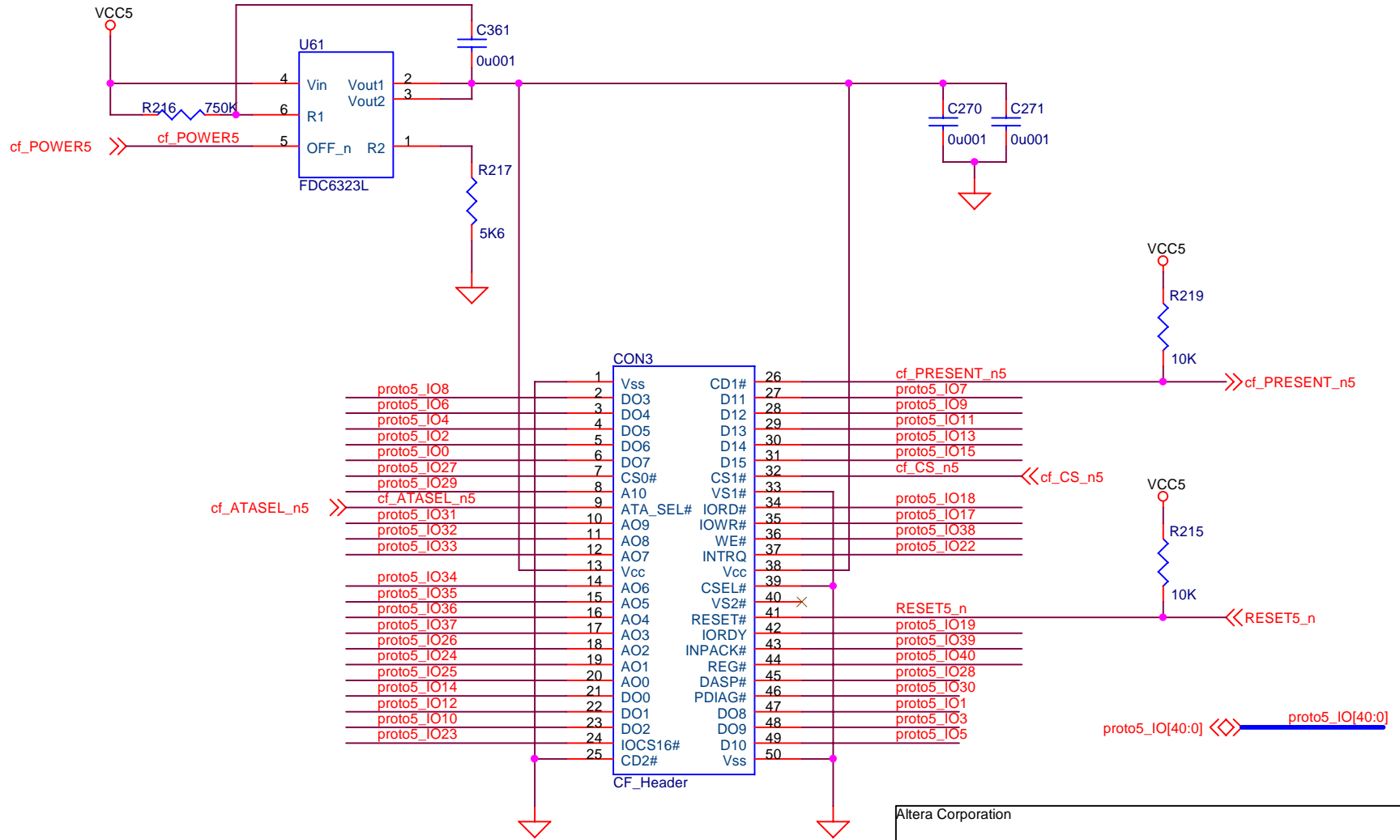
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Protol Buffers



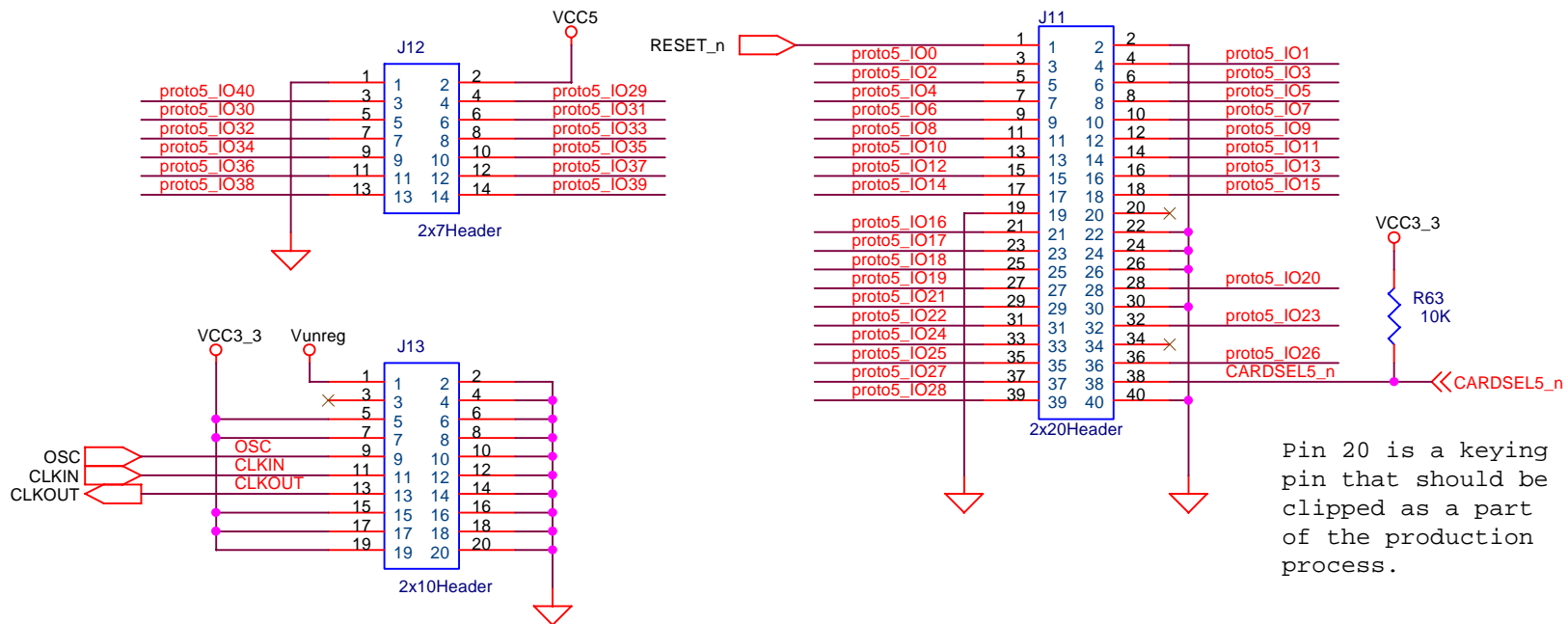
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Compaq Flash Socket



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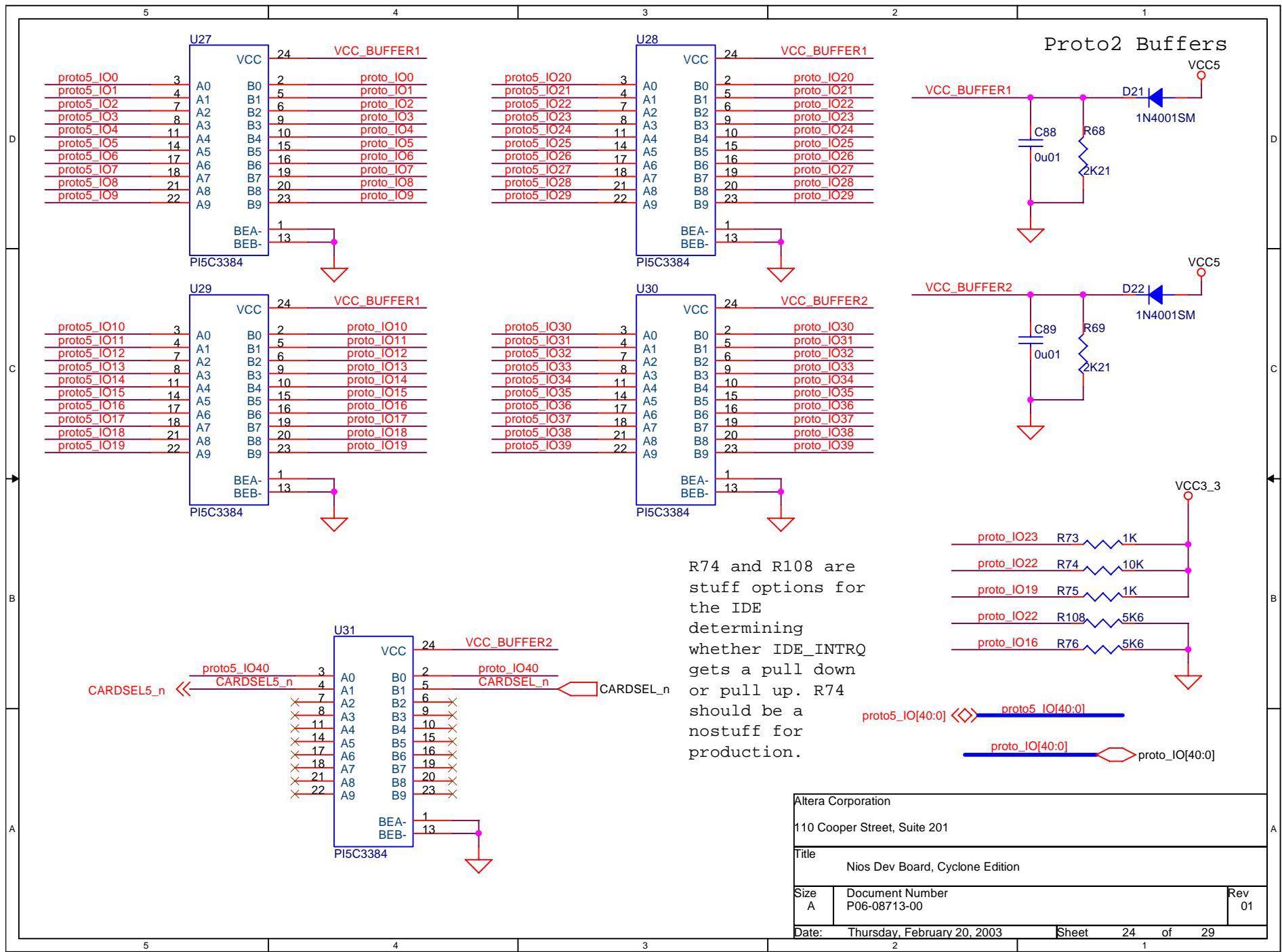
Protocard 1



proto5_IO[40:0] <<> proto5_IO[40:0]

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Pin 20 is a keying pin that should be clipped as a part of the production process.

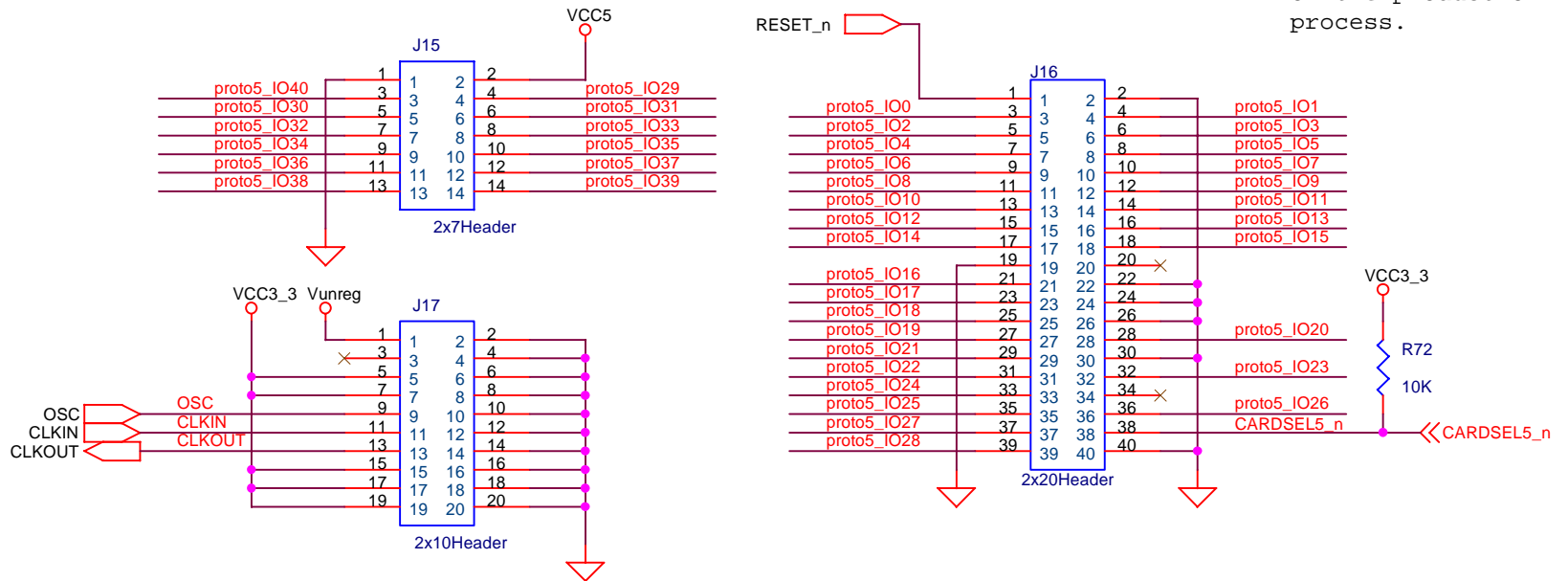


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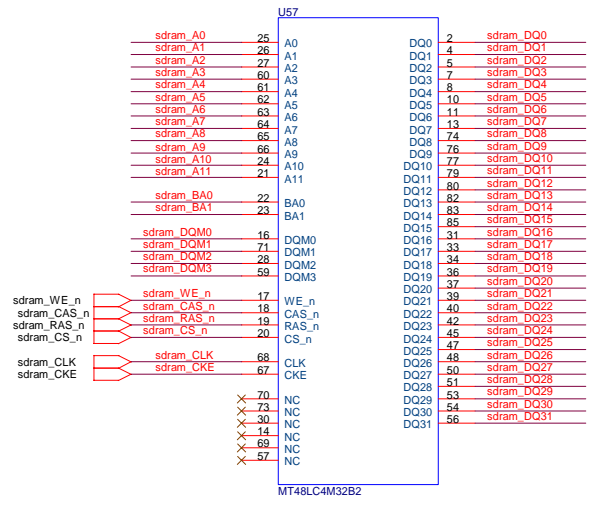
Proto2 Headers

Pin 20 is a keying pin that should be clipped as a part of the production process.

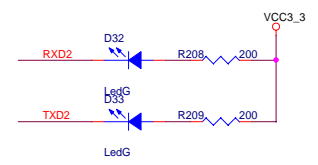
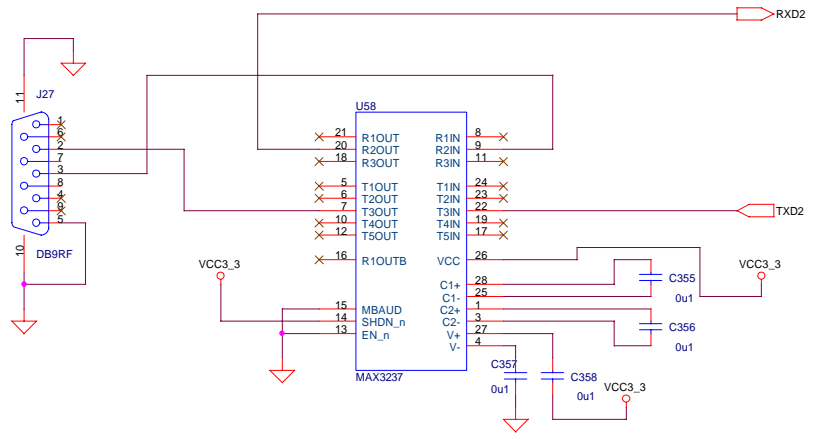
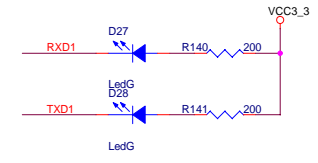
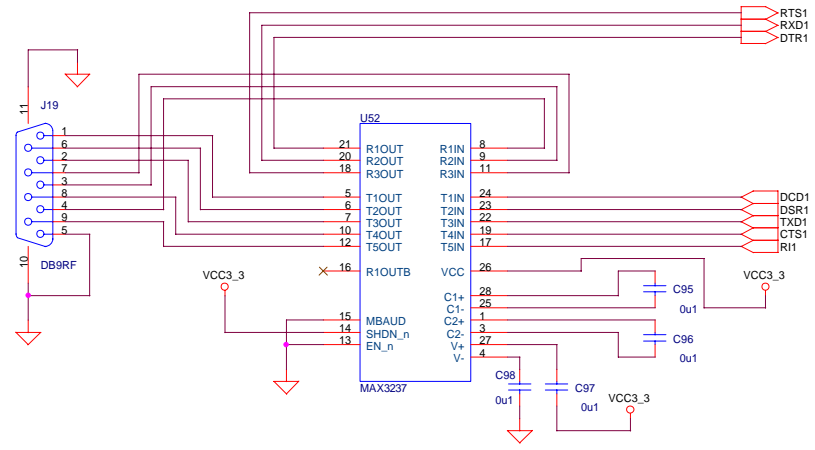
proto5_IO[40:0] <<> proto5_IO[40:0]



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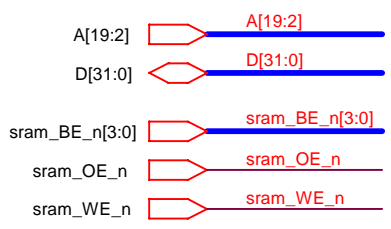
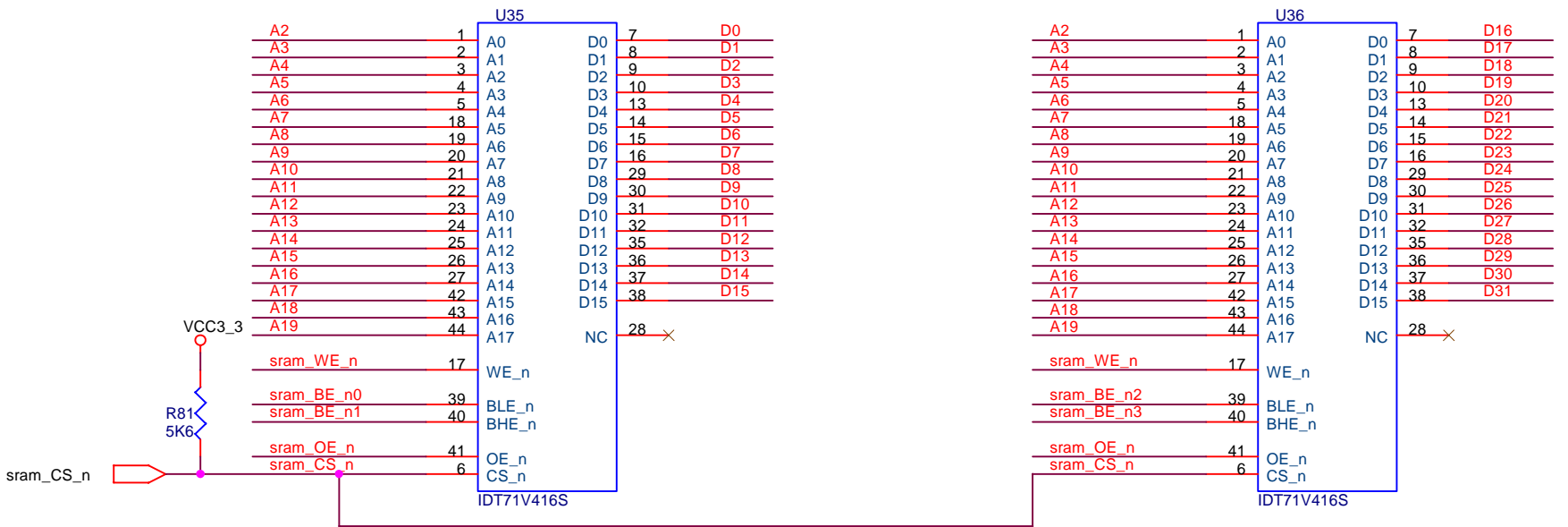


Serial Ports



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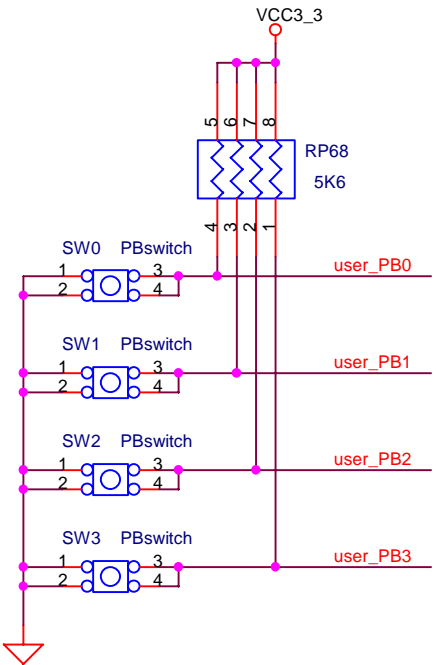
SRAM



One bank of 256K x 32 SRAM (two 256K x 16 parts in parallel) = 1Mbyte of SRAM

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Switches Buttons



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