LNA Design

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An LNA combines a low noise figure, reasonable gain, and stability without oscillation over entire useful frequency range.

The Low Noise Amplifier (LNA) always operates in Class A, typically at 15-20% of its maximum useful current. Class A is characterized by a bias point more or less at the center of maximum current and voltage capability of the device used, and by RF current and voltages that are sufficiently small relative to the bias point that the bias point does not shift.

The smallest signal that can be received by a receiver defines the receiver sensitivity. The largest signal can be received by a receiver establishes the upper power level limit of what can be handled by the system while preserving voice or data quality. The dynamic range of the receiver, the difference between the largest possible received signal and the smallest possible received signal, defines the quality of the receiver chain. The LNA function, play an important role in the receiver designs. Its main function is to amplify extremely low signals without adding noise, thus preserving the required Signal-to-Noise Ratio (SNR) of the system at extremely low power levels. Additionally, for large signal levels, the LNA amplifies the received signal without introducing any distortions, which eliminates channel interference.

- An LNA design presents a considerable challenge because of its simultaneous requirement for high gain, low noise figure, good input and output matching and unconditional stability at the lowest possible current draw from the amplifier.
- Although Gain, Noise Figure, Stability, Linearity and input and output match are all equally important, they are interdependent and do not always work in each other's favor.
- Carefully selecting a transistor and understanding parameter trade-offs can meet most of these conditions.
- Low noise figure and good input match is really simultaneously obtained without using feedback arrangements.
- Unconditional stability will always require a certain gain reduction because of either shunt or series resistive loading of the collector. High IP3 requires higher current draw, although the lowest possible noise figure is usually achieved al lower current levels.
- Envelope termination technique can be used to improve IP3 performance while operating LNA at low current levels.
- Additional improvement of IP3 can also be achieved by proper power output matching (1dB compression point match or P1dB match). The P1dB match, being different from conjugate match, reduces the gain although improving IP3 performance.
- Transistor selection is the first and most important step in an LNA design. The designer should carefully review the transistor selection, keeping the most important LNA design trade-offs in mind.

The transistor should exhibit high gain, have a low noise figure, and offer high IP3 performance at the lowest possible current consumption, while preserving relatively easy matching at frequency of operation.

Examination of a data sheet is a good starting point in a transistor evaluation for LNA design.

The transistor's S-parameters should be published at different collector/emitter voltages and different current levels for frequencies ranging from low to high values. The data sheet should also contain noise parameters, which are essential for low noise design. Spice models for the transistor and its package are also useful for IP3 and P1dB simulations.

The designer should first look at main design parameters: Noise, Gain, and IP3, and decide what Vce and Ic levels will produce optimal performance.

The forward transducer power gain represents the gain from transistor itself with its input and output presented with 50 Ω impedance.

The manufacturer of the transistor at multiple frequencies and different Vce and current levels provides the S21 values.

Additional gain can be obtained from source and load matching circuits.

Maximum Stable Gain and Maximum Power Gain (Gmax) are good indicators of additional obtainable gain from the LNA circuit.

LNA linearity is another important parameter. A figure of merit for linearity is IP3. A two-tone test is used for derivation of IP3.

As a rule of thumb for bipolar junction transistors (BJT), the Output-IP3 can be estimated from the following formula:

$$\text{OIP3[dBm]} = 10 \log (Vce * Ic * 5)$$

where Vce is in volts and Ic is in mA.

1. DC biasing
represent the first step in LNA design.
- The chosen DC bias circuit should exhibit stable thermal performance and reduce the influence of hFE spread.
- The resistive feedback arrangement is the simplest form of DC biasing that fulfills all the major requirements.
- Two bias feedback arrangements are possible: one with a combination of Rc and Rb and a second one with simple Re and Ce combination.
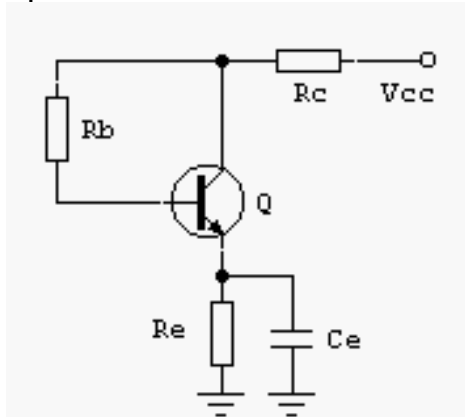
The operation of the Rc and Rb is simple: Rc and Rb will establish a biasing point. If the device current increases, the voltage drop across Rc increases, reducing the voltage seen by the base, thereby providing feedback. Because the operation of the LNA is going to be class A (constant current draw for dynamic range of power levels), a stable biasing point over different temperatures and for different lot of transistors where a small variation in hFE can be expected. For Rb to have little influence on source matching, which is crucial for noise

performance, the feedback network should be decoupled with an inductor (making biasing invisible at RF band of operation).

Another possible bias feedback can be realized with emitter resistor and capacitor. Ce should be selected carefully, because Re will also have a direct effect on RF gain of LNA. Ce should present a short at frequency of operation to limit its influence on gain and noise performance of the circuit.

Other biasing methods are suitable for class A networks. These are usually closed feedback arrangements with dynamic bias control provided by active components. Although suitable for LNA application, these active feedback bias networks increase complexity of the LNA network, introduce additional components and increase the real-estate area of the solution.

2. Stability design
should be the next step in LNA design.
- Unconditional stability of the circuit is the goal of the LNA designer.
- Unconditional stability means that with any load present to the output or output of the device, the circuit will not become unstable – will not oscillate. Instabilities are primarily caused by three phenomena: internal feedback of the transistor, external feedback around the transistor caused by external circuit, or excess gain at frequencies outside of the band of operation.
- S-parameters provided by manufacturer of the transistor will aid in stability analysis: numerical and graphical.
- Numerical analysis consists of calculating a term called Rollett Stability Factor (K-factor).
- When K-factor is greater than unity, the circuit will be unconditionally stable for any combinations of source and load impedance.
- When K-factor is less than unity, the circuit is potentially unstable and oscillation may occur with a certain combination of source and /or load impedance present to the transistor.

The K-factor represents a quick check for stability at given biasing condition. A sweep of the K-factor over frequency for a given biasing point should be performed to ensure unconditional stability outside of the band of operation.

The designer's goal is to design an LNA circuit that is unconditionally stable for the complete range of frequencies where the device has a substantial gain.

An LNA designer can use at least five methods for circuit stabilization.
- The first one consists of resistive loading of the input. This method, although capable of improving the stability of the circuit, also degrades the noise of the LNA and is almost never used.
- Output resistive loading is preferred method of circuit stabilization. This method should be carefully used because it effects are lower gain and lower P1dB point (thus IP3 point).
- The third method uses collector to base resistor-inductor-capacitor (RLC) feedback to lower the gain at the lower frequencies and hence improve the stability of the circuit.
- The fourth method consists of filter matching, usually used at the output of the transistor, to decrease the gain at a specific narrow bandwidth frequency. This method is frequently used for eliminating gain at high frequencies, much above the band of operation. Short circuit quarter wave lines designed for problematic frequencies, or simple capacitors with the same resonant frequency as the frequency of oscillation (or excessive gain) can be used to stabilize the circuit.

- The final stabilization method can be realized with a simple emitter feedback inductor. A small inductor can make the circuit more stable at higher frequencies. But if the source inductance is increased, the K-factor at higher frequencies eventually falls bellow 1. This effect limits the amount of source inductance that can safely be used.

3. Noise matching

The next step in LNA design consists of Noise Match and Input Return Loss (IRL).
- IRL defines how well the circuit is matched to 50 Ω matching of the source.
- A typical approach in LNA design is to develop an input matching circuit that terminates the transistor with conjugate of Gamma optimum (Γopt), which represents the terminating impedance of the transistor for the best noise match.

In many cases, this means that the input return loss of the LNA will be sacrificed.

The optimal IRL can be achieved only when the input-matching network terminates the device with a conjugate of S11, which in many cases is different from the conjugate of Γopt.

An emitter inductor feedback can rotate S11 closer to Γopt, which can help with obtaining close to minimum noise figure and respectable IRL simultaneously. This additional inductance at the emitter of the transistor will also reduce the overall available gain of the network and can be used in balancing trade-offs between the gain, IIP3 and stability in LNA design. Have to mention that this inductive degeneration does not seriously impact noise figure performance, as resistive degeneration does. At high frequencies this inductance will be achieved with small strip lines (stubs) connected directly to the emitters of the transistor. The inductive reactance of the stubs is usually no greater than 10 Ω and the line lengths are typically ~2mm or less with characteristic impedances 50 Ω or greater.

A typical method used in designing input matching network is to display noise circles and gain/loss circles of the input network on the same Smith chart. This provides a visual tool in establishing an input matching network for the best IRL and noise trade off.

4. Output matching

the last step in LNA design involves output matching of the transistor.

An additional resistor, either in series or parallel, has been placed on the collector of the transistor for circuit stabilization.

Conjugate matching has been exclusively used for narrow band LNA design to maximize the gain out of the circuit.

With additional IP3 requirement forced on the LNA, the trade-off between IP3 and gain must be considered.

Linearity matching is widely known by high-power amplifier designers. The so-called load pulling is used to establish IP3 and gain impedance contours. The load pulling can be realized by using the non-linear Spice model of the transistor with simulation software. Harmonic balance can be used for establishing two-tone environment. The load pulling method sweeps impedance of the whole Smith chart and plots contours of the constant gain and IP3 numbers. The optimal gain impedance does not match the optimal IP3 point, which means that the design will have to be realized by means of a trade off. Typically, the designer should design the LNA circuit at the point where the gain does not degrade as much, and the IP3is still respectable. If one were to draw a line between the optimal gain and IP3 impedance points, every point on that straight line will represent a good area of trade-off, with the ends representing the two optimal points.

The rule of thumb for 1dB gain compression point (P1dB) and IP3 is:

IP3 = P1dB +10 [dBm]

That means that by knowing the gain compression point (P1dB), can estimates the IP3 levels. The 10dB rule can further be improved with appropriate bypassing of the base and the collector. As previously indicated, the IIP3 is established by injecting two equal-in-magnitude signals with small frequency offset (S) into an active circuit.

As the active circuit approaches non-linear region, close to P1dB, the two carriers will generate distortion products, both in and out of band.

In example below we have two signals, with output levels Pout and frequencies F1 and F2.
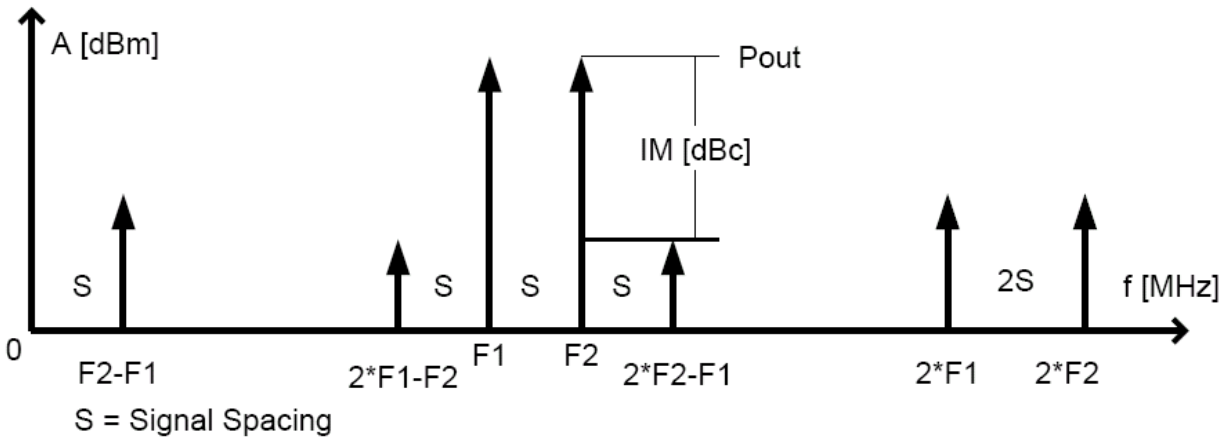

OIP3[dBm] = Pout[dBm] + dBc/2

Where dBc is the difference in amplitude between one of the two equal amplitude test tones, present at the amplifier output, and the level of the highest 3rd-order distortion product.

- For every dB increase in input power, the third order products (IM3) will increase 3dB.
- For every dB increase in input power, the second order products (IM2) will increase 2dB.

Plotting third order products versus input power predicts a 3:1 response which intersects the 1:1 response at the third order intercept point.
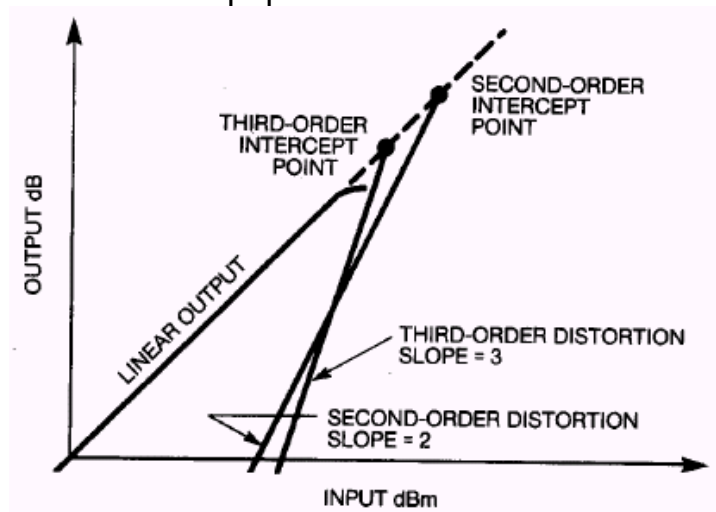
Second and Third-Order Distortion Slopes
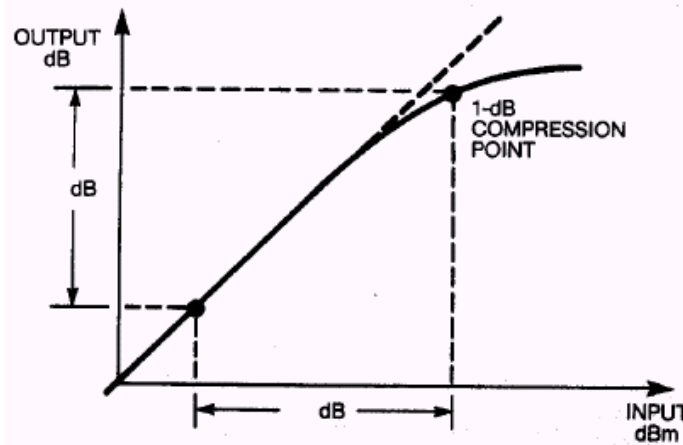
1dB Gain Compression Point (P1dB)

The relation between Input-IP3 (IIP3) and Output-IP3 (OIP3) is defined as:
IIP3[dBm] = OIP3[dBm] − Gain[dB]
The low frequency IM2 products (F2-F1), can modulate the base-emitter and collector-emitter LNA supply voltages. To improve the linearity the fluctuation of the base and the collector shall be stabilized with low impedance at so called video frequencies or baseband frequencies (between DC and usually up to 40MHz).
- The designer should exhibit caution during bypassing design. A poor selection of the by-pass capacitors could also degrade IP3 performance.
- As a rule of thumb, the impedance of bypassing circuit should be lower than 25% of the input impedance of the transistor at particular frequency spacing. Although preserving the gain performance of the LNA, the bypassing method (also known as an envelope termination technique) can improve LNA's IIP3 performance without increasing current consumption.

5. LNA components and the effect on IP3
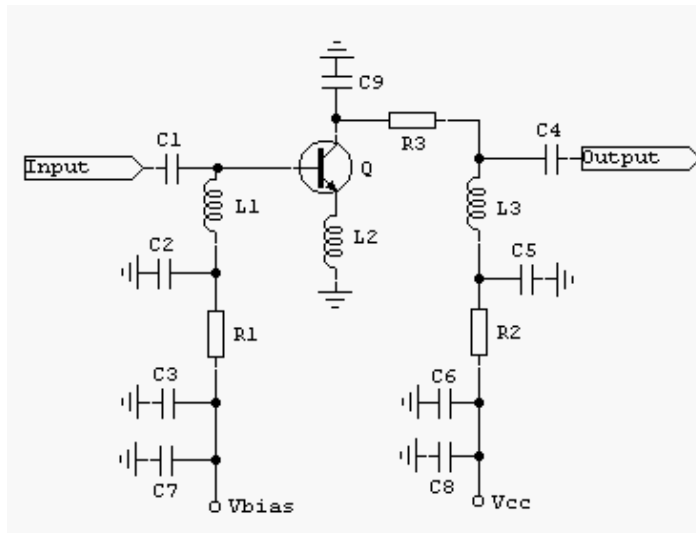
- Any mismatch due to noise matching C1/L1 improves Input-IP3.
- Increasing L2 reduces gain and improves Input-IP3, but watch for microwave oscillation with excessive inductance.
- C9 can use to improve IP3- provides gain roll-off at 2*F1 or 2*F2.
- Printed circuit board losses R3 provide Q1 stability while reducing IP3.
  R3 less than 27 Ω for about a dB reduction in IP3.

- C3 and C6 provide a HF/VHF termination for Q1. Depending on spacing of signals used to test IP3, values may not be large enough – may necessitate additional low frequency bypassing in the form of C7 and C8. Typical values are 0.01 to 0.1 uF.
- The combination of C2/C5, C3/C7 and C6/C8 must provide low impedance at F2 – F1. May have to add resistance between caps to decrease Q.
- C7 and C8 also used to minimize power supply noise from modulating the DC.
- Capacitor C2, C3 and C7 performs the low-frequency bypass function and an improvement in IP3 of approximately 5 to 10 dB can be expected by using this method. Using extra charge storage on the drain may see the same effect, but the results are not nearly as dramatic.
- The closer together the two input test tones F1 and F2 are in frequency, the lower frequency the product or beat tone (F 2 – F 1) is. Therefore, as input test tones F1 and F2 come closer together, more capacitance is needed to achieve best possible bypassing of the low frequency product (F2 – F1).

For a test tone separation of 1MHz, 0.1 uF was found to be more adequate for this application. For best results, the transistor should see a low impedance path at low frequencies between this additional bypass caps and its terminals. For this reason, a coil rather than a high value resistor is used to bring the gate bias voltage and isolate the RF from the DC bias network. For example a value of 15nH for L1, has negligible impedance up to tens of MHz, but provides enough impedance at 2 GHz to nearly isolate the gate of the transistor from the bias network within LNA's normal operating frequency range.

It is important to note that bypassing the F2 – F1 product as described here does not affect the compression point of the amplifier, but only the IP3 (3rd-order intercept point). As a results, if this bypassing used, the general rule of thumb stating that are approximately a 10 dB difference between IP3 and 1 dB gain compression point (P1dB) is no longer valid.

6. Real issues in LNA design
- An LNA is a design that minimizes the Noise Figure of the system by matching the device to its noise matching impedance, or Gamma optimum (Γopt).
- Gamma optimum (Γopt) occurs at impedance where the noise of the device is terminated.
- All devices exhibit noise energy. To minimize this noise as seen from the output port, one must match the input load to the conjugate noise impedance of the device. Otherwise the noise will be reflected back from the load to the device and amplified. While this gives a minimum noise figure, it often results in slightly reduced gain as well as possibility increasing the potential instabilities.

Noise match often comes close to S11 conjugate (S11*) under non-feedback conditions. As a result, the input impedance to the amplifier will not be matched to 50 ohms. Γopt, as presented in data sheets, is the actual measured load at which the minimum noise figure is found.

A further complication on LNA design is that the input load of the amplifier is usually less than ideal. It is either connected to an antenna, which can change its impedance with changing the environment, or to a filter, which by very physics of a reflective network will have very bad match out of band. These mismatches could cause the device to become unstable out of band and some cases in band. As the gain of the device increases, the difficulties in yielding a stable design become increasingly more challenging.

To avoid overloading the LNA, an input filter is commonly used. Since the device is not matched to S11*, the input of the LNA will not be 50 ohms. This can cause distortions in the

pass band of the filter when connected to the input of the LNA, as filter are intended to operated in their characteristic impedance, typically 50 ohms.

Printed inductors or transmission lines are free as compared to SMT inductors, which typically cost 10 to 25 times as much as resistors or capacitors in volume. Printing an inductor is easy and results in highly repeatable results. Printed inductors usually exhibit poor Q due to the lossy dielectric, and, if a ground plane exists, they are no more than a high impedance transmission line.

As shown a transmission line can replace an inductor to some degree, but inductors and high impedance transmission lines have a different trajectory on the Smith Chart. High impedance transmission line can be made to look more like printed inductors in cases where the backside of the PCB is suspended away from a grounded chassis. This is accomplished by removing the backside ground plane of the PCB directly under the printed inductor. In this case beware of digital noise coupling into the input of the LNA from circuitry on the opposite side.

- The next concern is what load impedance to match. Remember matching to the conjugate of S22* is only valid if the input is conjugate matched. Since S12 is non-zero, whatever load is present to the input will cause the output load change.
- Another issue is stability, especially if a filter is going to be used at the input. The output port can potentially give difficulties since the input is very restricted by its match.

The designer must replace the ideal sources in the bias circuit and ideal values in the matching circuit with equivalent real components. This often presents the designer with a new set of problems. First, the bias network must be robust enough to function properly over a range of power-supply voltages and temperatures. This introduces additional complexity into the bias network. The real components in the bias network the resistors and large capacitors operate at DC voltages, so frequency effects are not a problem. The matching network, however, contains real capacitors and inductors that operate at RF frequencies. Real components differ from ideal ones in several respects. First, real components have a price associated with them. There is a trade-off between price and performance of these parts. The competitiveness of today's markets often forces designers to use inexpensive components in their designs.

- Real discrete components have a finite resistance called Equivalent Series Resistance (ESR). The ESR introduces losses that result in lower gain and noise figure. Although typically only a few tenths of an ohm in value, ESR will affect the matching networks.
- Discrete components also have a Q value, measured at a particular frequency that can contribute to unwanted resonance.
- A component's Series Resonant Frequency (SRF) is the frequency where it will behave erratically. For example, if an inductor is operated at or above its SRF, it might behave as a capacitor. To avoid this, select components where the SRF is much higher than the operating frequency.
- Also, leaded through –hole parts have leads that add series inductance to a design, and surface-mount parts have pads that add shunt capacitance to a circuit.
- Another issue is that of packaging a completed design. If the circuit is to be integrated and sold as an Integrated Circuit (IC), it must be packaged. The package introduces several negative effects. In an IC, the bond wires add unwanted inductance (L) and the bond pads add unwanted capacitance (C).
- Isolation between pins in the package is also important. Lack of pin -to-pin isolation in a feedback circuit can lead to major reliability problems and stability concerns. The

additional inductance in the emitter of the collector-emitter section can severely degrade the noise figure of the circuit.
- Additionally, several grounds are usually needed to improve the performance of RF circuits, but the package has a limited number of pins. After using the input, output, and power-supply pins, there may not be enough ground pins to accommodate an adequate design.

All of these factors can degrade the circuit's performance from the ideal, and the designer must carefully take them into account.

CMOS LNA Design

- A few comparison characteristics between CMOS and BJT LNAs:
  - The DC currents of CMOS and BJT LNA's are close, therefore the transconductance (g_m) of CMOS transistor is lower than the BJT one's.
  - The g_m/I ratio of CMOS is lower than that of BJT.
  - In CMOS technologies, a high f_T is achieved through a smaller C_{gs}, while in BJT technologies the same f_T is obtained through a higher g_m.
  - Smaller C_{gs} means CMOS tuned circuits tend to have higher Q, a disadvantage in withstanding component or process variation.
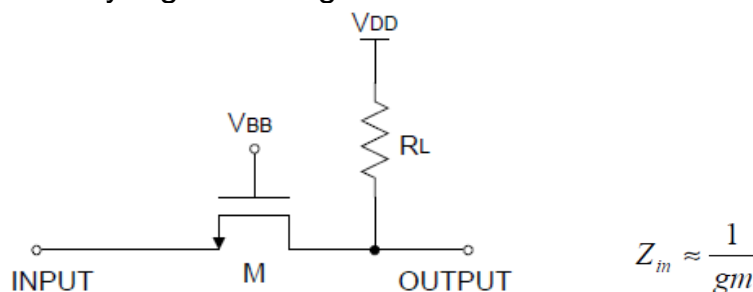
The CMOS LNA input quality factor (independent of L_s) is defined as follows:

$$Q_{gs} = \frac{1}{\omega_o C_{gs} Z_0}$$

There are two types of methods commonly used to design an LNA in CMOS circuits:
- Common-Gate
- Cascode amplifier.

While the Common-Gate stage provides a wide-band input matching and is less sensitive to parasitics, it has an inherently high noise figure.

$$Z_{in} \approx \frac{1}{gm}$$

Common-Gate CMOS LNA

- With the increasing of the operating frequency, the parasitic transistor capacitance C_{gs} starts playing roles, which degrades the amplifier performance in the high frequency. In the narrow band application, a shunt inductor is added in the input to resonate with C_{gs} to have a good impedance matching in the designed frequency.
- Due to the lower quality factor of the resonant network, Common-Gate it is more robust against the process and electrical variation.
- Due to the missing of the C_{gd} path from the input to the output, the Common-Gate LNA shows better reverse isolation and stability versus Common-Source LNA.

Therefore, in most CMOS applications where the noise figure is critical issue, a cascode LNA with inductive degeneration is preferable.
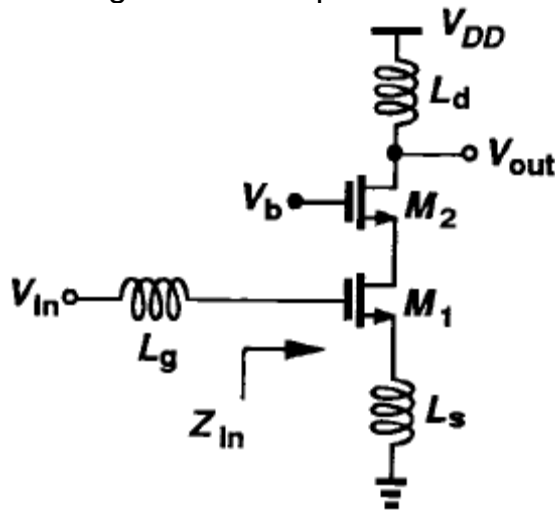
$$Z_{in}(s) = L_s \frac{g_m}{C_{gs}} + \frac{1}{C_{gs}s} + L_s s$$

Cascode CMOS LNA

- For a given unit-gain frequency as we lower the bias current, the noise figure decreases.
- For a given Q, higher g_m improves the noise figure.
- For a given source resistance of 50 ohms, as we reduce L_s, unit-gain frequency increases but the minimum value of L_s is limited by parasitic and sensitivity issues.
- By proper choice of g_m, L_s, and C_{gs}, the input resistance can be equal to 50 ohms source resistance and the input reactance (imaginary part of impedance) can be resonated out by a series inductor (L_s).
- Inductor degeneration (L_s) also improves the linearity by forming a negative series feedback.
- As we lower the bias current, while keeping unit-gain frequency constant, C_{gs} decreases, leading to higher Q.
- A high Q matching networks has several drawbacks:
  - Circuit becomes very sensitive to component variations and parasitics.
  - The input matching circuit which in this case contains a series inductor, inserts a large amount of loss at the input (even for a high-Q off-chip inductor)
- Another source of noise in the cascode topology is the noise introduced by the cascode device, M2, added to improve stability of the amplifier.
  - At high frequencies the capacitance at the drain of M1 reduces the impedance of this node, increasing the output noise, so to minimize the noise is very important to minimize this capacitance.
  - To improve the noise performance of the cascode design, the parasitic capacitance at the drain of M1 is resonated out by adding an inductor to the source of cascode.
    This inductor should be sized carefully in order to resonate the unwanted capacitances at the desired frequency of operation.

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