Si4311

315/433.92 MHz OOK/FSK Receiver

Features

- Single chip receiver with only six external components
- Selectable 315/433.92 MHz carrier frequency
- Supports OOK and FSK modulation
- High sensitivity (–112 dBm @ 2.4 kbps OOK, –113 dBm @ 1.667 kbps FSK)
- Excellent interference rejection
- Selectable IF bandwidths from 48 to 192 kHz
- Integrated squelch circuit
- Data rates up to 9.6 kbps NRZ (4.8 kbps Manchester)
- Direct battery operation with on-chip low-drop out (LDO) voltage regulator
- 16 MHz crystal oscillator support
- 3 x 3 x 0.85 mm 20L QFN package (Pb free/RoHS compliant)
- –40 to +85 ºC temperature range

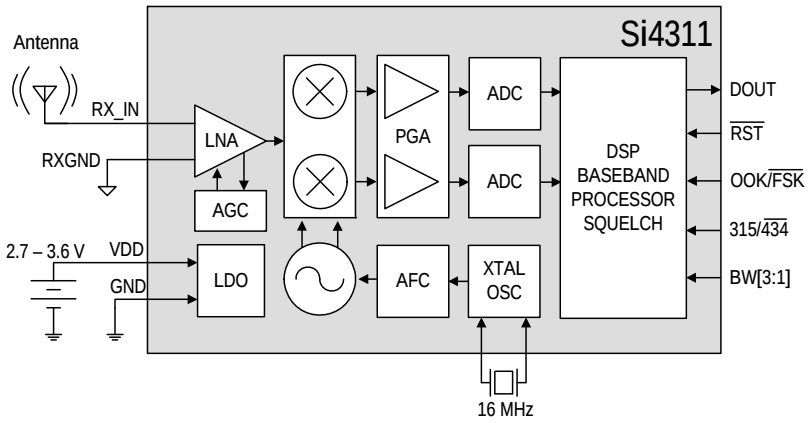
Applications

- Satellite set top box receivers
- Remote controls, IR replacement/extension
- Garage and gate door openers
- Home automation and security
- Remote keyless entry
- After market alarms
- Telemetry
- Wireless point of sale
- Toys

Description

The Si4311 is a fully integrated OOK/FSK CMOS RF receiver that operates in the unlicensed 315 and 433.92 MHz ultra-high frequency (UHF) bands. It is designed for high volume cost sensitive RF receiver applications such as set-top box RF receivers, remote controls, garage door openers, home automation, security, remote keyless entry systems, wireless POS, and telemetry. The Si4311 offers industry leading RF performance, high integration, flexibility, low BOM, small board area, and ease of design. No production alignment is necessary as all RF functions are integrated into the device.

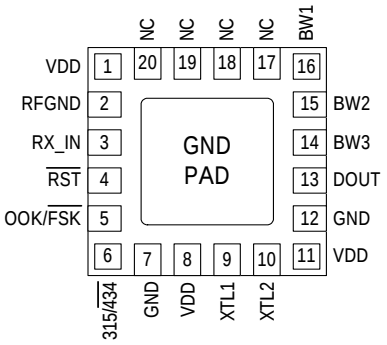
Functional Block Diagram



Ordering Information:
See page 14.

Pin Assignments

Si4311
(Top View)



Patents pending

TABLE OF CONTENTS

1. Electrical Specifications

Table 1. Recommended Operating Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Supply Voltage	V_{DD}		2.7	3.3	3.6	V
Supply Voltage Power-Up Rise Time	$V_{DD\text{-}RISE}$		10	—	—	µs
Ambient Temperature	T_A		–40	25	85	°C

Note: All minimum and maximum specifications are guaranteed and apply across the recommended operating conditions. Typical values apply at VDD = 3.3 V and 25 °C unless otherwise stated. Parameters are tested in production unless otherwise stated.

Table 2. Absolute Maximum Ratings[1,2]

Parameter	Symbol	Value	Unit
Supply Voltage	V_{DD}	–0.5 to 3.9	V
Input Current[3]	I_{IN}	10	mA
Input Voltage[3]	V_{IN}	–0.3 to (V_{DD} + 0.3)	V
Operating Temperature	T_{OP}	–45 to 95	°C
Storage Temperature	T_{STG}	–55 to 150	°C
RF Input Level[4]		0.4	V_{PK}

Notes:
1. Permanent device damage may occur if the absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as specified in the operational sections of this data sheet. Exposure beyond recommended operating conditions for extended periods may affect device reliability.
2. The Si4311 devices are high-performance RF integrated circuits with certain pins having an ESD rating of < 2 kV HBM. Handling and assembly of these devices should only be done at ESD-protected workstations.
3. For input pins OOK/$\overline{\text{FSK}}$, 315/$\overline{434}$, BW[1:3].
4. At RF input pin RX_IN.

Table 3. DC Characteristics

(T_A = 25 °C, V_{DD} = 3.3 V, R_s = 50 Ω, F_{RF} = 433.92 MHz unless otherwise noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Supply Current	I_{VDD}	Receive mode	—	19	—	mA
Reset Supply Current	R_T	Reset asserted	—	10	—	µA
High Level Input Voltage[1]	V_{IH}		0.7 x V_{DD}	—	V_{DD} + 0.3	V
Low Level Input Voltage[1]	V_{IL}		–0.3	—	0.3 x V_{DD}	V
High Level Input Current[1]	I_{IH}	V_{IN} = V_{DD} = 3.6 V	–10	—	10	µA
Low Level Input Current[1]	I_{IL}	V_{IN} = 0 V, V_{DD} = 3.6 V	–10	—	10	µA
High Level Output Voltage[2]	V_{OH}	I_{OUT} = 500 µA	0.8 x V_{DD}	—	—	V
Low Level Output Voltage[2]	V_{OL}	I_{OUT} = –500 µA	—	—	0.2 x V_{DD}	V

Notes:
1. For input pins OOK/$\overline{\text{FSK}}$, 315/$\overline{434}$, BW[1:3].
2. For output pin DOUT.

Table 4. Reset Timing Characteristics

(V_{DD} = 3.3 V, T_A = 25 °C)

Parameter	Symbol	Min	Typ	Max	Unit
$\overline{\text{RST}}$ Pulse Width	t_{SRST}	100	—	—	µs

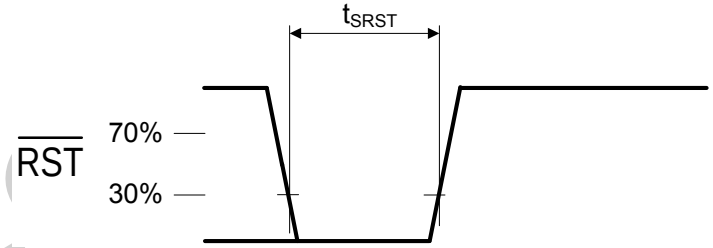


Figure 1. Reset Timing

Table 5. Si4311 Receiver Characteristics

(T_A = 25 °C, V_{DD} = 3.3 V, R_s = 50 Ω, F_{RF} = 433.92 MHz unless otherwise noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Sensitivity @ BER = 10^{-3}		OOK, 2.4 kbps, BW = 48 kHz, xtal 20 ppm	—	–112	—	dBm
		FSK, 1.667 kbps, BW = 48 kHz, Δf = 10 kHz, xtal 20 ppm	—	–113	—	dBm
Data Rate		OOK (Manchester encoded)	—	—	4.8	kbps
		FSK	—	—	9.6	kbps
Adjacent Channel Rejection ±200 kHz[1]		Desired signal is 3 dB above sensitivity (BER = 10^{-3}), unmodulated interferer is at ±100 kHz, rejection measured as difference between desired signal and interferer level in dB when BER = 10^{-3}	—	35	—	dB
Alternate Channel Rejection ±400 kHz[1]		Desired signal is 3 dB above sensitivity (BER = 10^{-3}), unmodulated interferer is at ±200 kHz, rejection measured as difference between desired signal and interferer level in dB when BER = 10^{-3}	—	55	—	dB
Image Rejection, IF = 128 kHz[1]			—	35	—	dB
Blocking[1]		±2 MHz, 2.4 kbps, desired signal is 3 dB above sensitivity, CW interferer level is increased until BER = 10^{-3}	—	65	—	dB
		±10 MHz, 2.4 kbps, desired signal is 3 dB above sensitivity, CW interferer level is increased until BER = 10^{-3}	—	70	—	dB
Maximum RF Input Power [1]			—	10	—	dBm
Input IP3[2]		$\lvert f_2 - f_1 \rvert$ = 5 MHz, high gain mode, desired signal is 3 dB above sensitivity, CW interference levels are increased until BER = 10^{-3}	—	–10	—	dBm
FSK Deviation Input Range			1	—	70	kHz
LNA Input Impedance			—	7	—	pF
RX Boot Time		From reset	—	—	9	ms

Notes:

1. Both OOK and FSK are tested. OOK: 2.4 kbps, BW = 48 kHz, xtal = ±20 ppm. FSK: 1.6 kbps, BW = 192 kHz, xtal = ±20 ppm.
2. Both OOK and FSK are tested with BW[3:1] = 111 for high gain mode. Same conditions as Note 1 but BW = 192 kHz for both OOK and FSK modes.

Table 6. Crystal Characteristics
(V_{DD} = 3.3 V, T_A = 25 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Crystal Oscillator Frequency			—	16	—	MHz
Crystal Frequency Tolerance Range*			–100	—	100	ppm
Board Capacitance			—	—	3.5	pF

***Note:** Crystal tolerance is determined by the following equation:

$$(\text{RX xtal})_{tol}\ [\text{kHz}] < \pm\left[\frac{BW}{2} - \text{VCO step size} - \Delta f - \text{data rate} - (\text{TX xtal})_{tol}\right]$$

BW = IF BW of the receiver, either 48, 64, 96, 128, or 192 kHz
VCO step size = 5 kHz
Δf = frequency deviation in kHz for FSK, 0 kHz for OOK
$(\text{TX xtal})_{tol}$ = Transmitter crystal tolerance in kHz

2. Test Circuit

2.1. Test Circuit Schematic

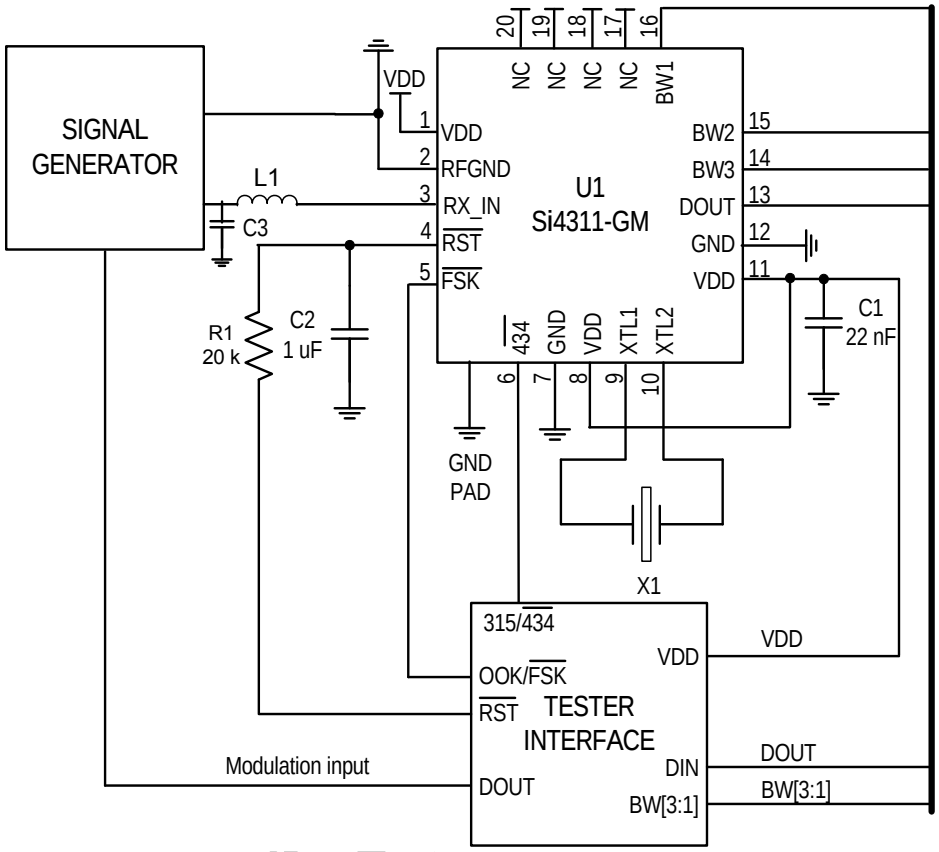


Figure 2. Test Circuit Schematic

2.2. Test Circuit Bill of Materials

Table 7. Si4311 Test Circuit Bill of Materials

Component(s)	Value/Description	Supplier(s)
C1	Supply bypass capacitor, 22 nF, 20%, Z5U/X7R	Murata
C2	Time constant capacitor, 1 µF	Murata
C3	Antenna matching capacitor, 15 pF	Murata
L1	Antenna matching inductor, 33 nH for 433.92 MHz and 62 nH for 315 MHz	Murata
R1	Time constant resistors, 20 kΩ	Murata
X1	16 MHz crystal	Hosonic
U1	Si4311 315/433.92 MHz OOK/FSK receiver	Silicon Laboratories

3. Typical Application Schematic

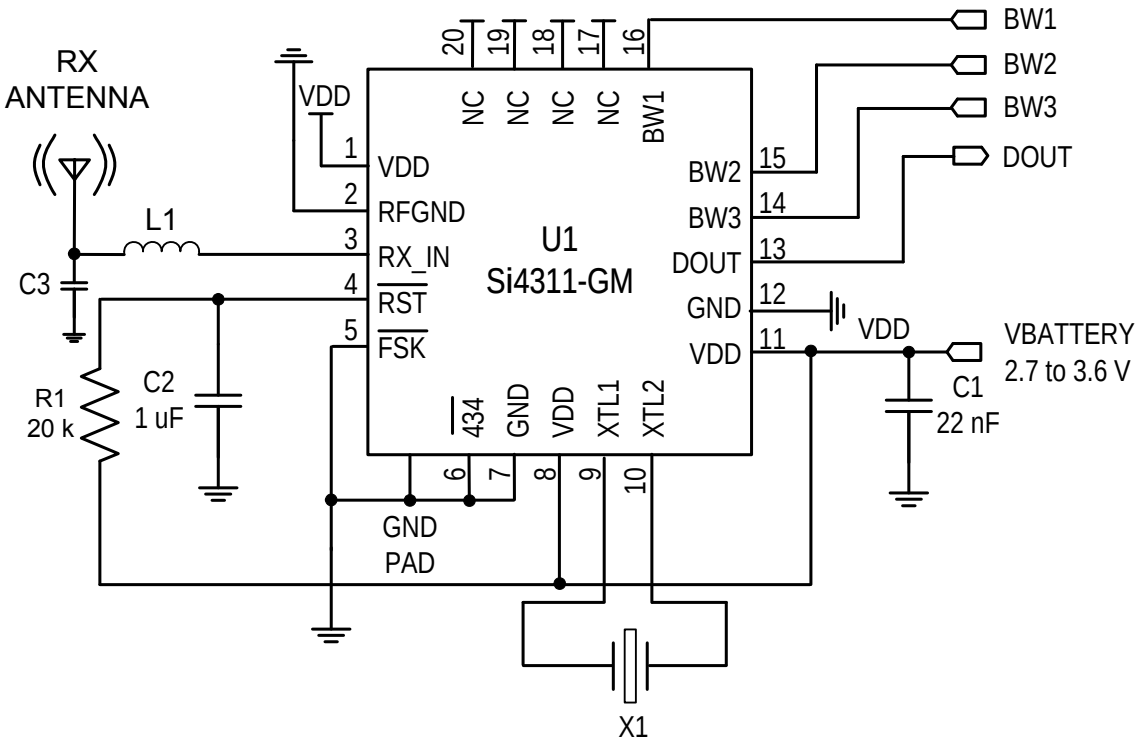


Figure 3. Si4311 FSK 433.92 MHz Application Schematic

3.1. Typical Application Bill of Materials

Table 8. Si4311 Typical Application Bill of Materials

Component(s)	Value/Description	Supplier(s)
C1	Supply bypass capacitor, 22 nF, 20%, Z5U/X7R	Murata
C2	Time constant capacitor, 1 µF	Murata
C3	Antenna matching capacitor, 15 pF	Murata
L1	Antenna matching inductor, 33 nH for 433.92 MHz and 62 nH for 315 MHz	Murata
R1	Time constant resistor, 20 kΩ	Murata
X1	16 MHz crystal	Hosonic
U1	Si4311 315/433.92 MHz OOK/FSK receiver	Silicon Laboratories

4. Functional Description

4.1. Overview

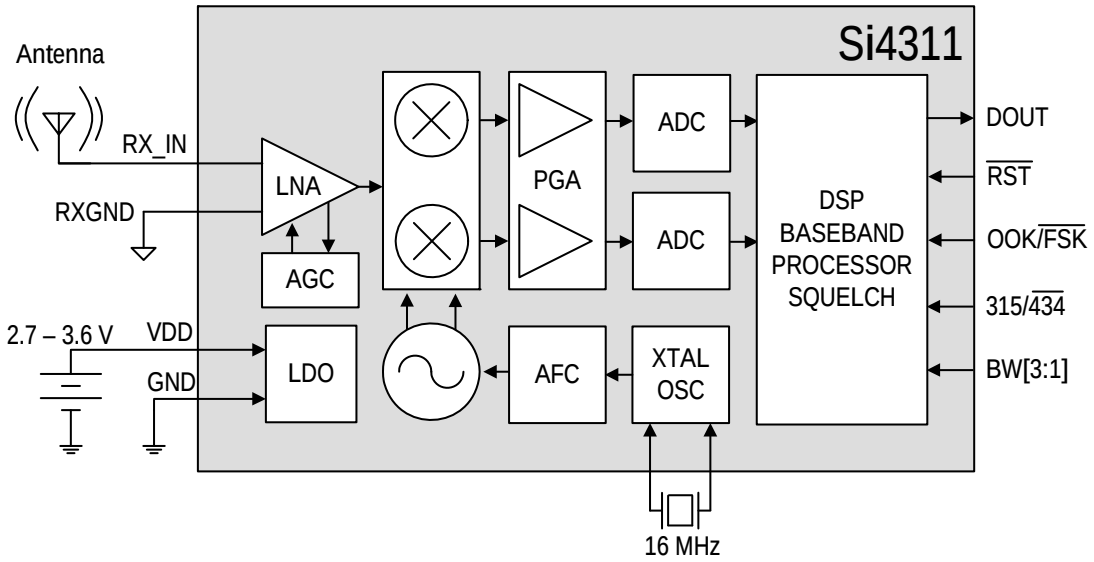


Figure 4. Functional Block Diagram

The Si4311 is a fully integrated OOK/FSK CMOS RF receiver that operates in the unlicensed 315 and 433.92 MHz ultra-high frequency (UHF) bands. It is designed for high volume cost sensitive RF receiver applications. The chip operates at a carrier frequency of 315 or 433.92 MHz and supports OOK or FSK digital modulation with data rates up to 4 kbps NRZ or 2 kbps Manchester coded. The Si4311 has selectable IF bandwidth options to optimize the sensitivity of the receiver for a given data rate. The integrated on-chip squelch circuit prevents false output data when the RF input signal is absent or below sensitivity.

The device leverages Silicon Labs' patented and proven digital low-IF architecture and offers superior sensitivity and interference rejection. The Si4311 can achieve superior sensitivity in the presence of large interference due to its high dynamic range ADCs and digital filters. The digital low-IF architecture also enables superior blocking ability and low inter-modulation distortion for robust reception in the presence of wide band interference.

Digital integration reduces the amount of required external components compared to traditional offerings, resulting in a solution that only requires a 16 MHz crystal and passive components allowing a small and compact printed circuit board (PCB) implementation area. The high integration of the Si4311 improves the system manufacturing reliability, improves quality, eases design-in, and minimizes costs.

4.2. Receiver Description

The RF input signal is amplified by a low noise amplifier (LNA) and down converts to a low intermediate frequency with a quadrature image-reject mixer. The mixer output is amplified by a programmable gain amplifier (PGA), filtered, and digitized with a high resolution analog-to-digital converter (ADC). All RF functions are integrated into the device eliminating any production alignment issues associated with external components such as SAW and ceramic IF filters.

Silicon Labs' advanced digital low-IF architecture achieves superior performance by using the DSP to perform channel filtering, demodulation, automatic gain control (AGC), automatic frequency control (AFC), and other baseband processing. DSP implementation of the channel filters provides better repeatability and control of the bandwidth and frequency response of the filter compared to analog implementations. No off-chip ceramic filters are needed with the Si4311 as all IF channel filtering is performed in the digital domain with selectable channel bandwidths.

4.3. Carrier Frequency Selection

The Si4311 can be tuned to either 315 or 433.92 MHz by driving pin 6 (315/$\overline{434}$) to VDD or GND respectively. 315 MHz operation is chosen by driving pin 6 (315/$\overline{434}$) to VDD and 433.92 MHz operation is chosen by driving pin 6 (315/$\overline{434}$) to GND.

Table 9. Carrier Frequency Selection

Pin 6 (315/$\overline{434}$)	Frequency [MHz]
0	433.92
1	315

4.4. OOK/FSK Demodulation

OOK/FSK digital demodulation is selected using pin 5 (OOK/$\overline{FSK}$). OOK demodulation is chosen by driving pin 5 (OOK/$\overline{FSK}$) to VDD and FSK demodulation is chosen by driving pin 5 (OOK/$\overline{FSK}$) to GND.

Table 10. OOK/FSK Demodulation Selection

Pin 5 (OOK/$\overline{FSK}$)	Demodulator
0	FSK
1	OOK

4.5. IF Bandwidth Selection

The Si4311 can be programmed to one of eight selectable IF bandwidths using the three bandwidth select pins, BW[3:1]. Selecting BW[3:1] = 111 puts the device in test mode where the chip is placed in high gain mode with AGC turned off and the bandwidth set to 192 kHz. This mode is useful for testing the input IP3 of the device.

Table 11. Bandwidth Selection Table Using BW[3:1] Pins

BW3	BW2	BW1	IF Bandwidth [kHz]
0	0	0	48
0	0	1	64
0	1	0	96
0	1	1	128
1	0	0	—
1	0	1	—
1	1	0	192
1	1	1	Test Mode

The IF channel bandwidth sets the noise bandwidth of the receiver and for maximum sensitivity the IF bandwidth should be chosen as small as possible while still accommodating for the data rate, RX and TX crystal tolerances, and frequency deviation for FSK systems. The ideal IF bandwidth is given by the following formula:

$$(\text{RX xtal})_{tol}\ [\text{kHz}] < \pm\left[\frac{BW}{2} - \text{VCO step size} - \Delta f - \text{data rate} - (\text{TX xtal})_{tol}\right]$$

BW = IF BW of the receiver, either 48, 64, 96, 128, or 192 kHz
VCO step size = 5 kHz
Δf = frequency deviation in kHz for FSK, 0 kHz for OOK
$(\text{TX xtal})_{tol}$ = Transmitter crystal tolerance in kHz

Frequency deviation is set to 0 Hz for OOK modulation. Since the Si4311 has five selectable IF bandwidth options to optimize the sensitivity of the receiver, the user should choose the IF bandwidth option that is just larger than the calculated Ideal IF Bandwidth given in the above equation for their system. A sample of the FSK receiver sensitivity values taken at 433.92 MHz for different channel bandwidths and frequency deviations is shown in Table 12.

Table 12. Typical Sensitivity @ 433 MHz, 2-FSK

Data Rate (kbps)	Channel BW (kHz)	Frequency Deviation (kHz)	Sensitivity (dBm)
1.667	48	10	–113
1.667	96	20	–111
1.667	192	50	–106

4.6. Low Noise Amplifier Input Circuit

The Si4311CMOS LNA is designed for voltage input and the key to maximizing the receivers' performance is to provide as large of an input voltage as possible to the LNA. Figure 3 “Si4311 FSK 433.92 MHz Application Schematic” shows the input circuit to the LNA as a series inductor L1. The input impedance of the integrated CMOS LNA is capacitive with a typical value of 7 pF. In order to maximize the input voltage to the LNA, L1 is chosen to resonate with the input capacitance of the LNA and any external parasitic board capacitance as shown in the following equation:

$$L1 = \frac{1}{(C_{LNA} + C_{PAR})(2\pi F)^2}$$

C_{LNA} = CMOS LNA input capacitance, 5 pF

C_{PAR} = External board parasitic capacitance

F = Frequency of operation, either 315 or 433.92 MHz

The Q of the input circuit is given by the following equation:

$$Q = \frac{(2\pi F)L1}{R_S}$$

R_S = Series resistance of the inductor and the antenna

Figure 3 shows the typical application circuit with 50 Ω matching. Components C3 and L1 are used to transform the input impedance of the LNA. C3 is equal to 15 pF and L1 is equal to 33 nH at 433.92 MHz and 62 nH at 315 MHz for 50 Ω matching. The criteria for choosing inductor L1 is different for maximum voltage gain and 50 Ω matching.

4.7. Squelch Circuit

The on-board DSP within the Si4311 provides a digitized receive signal strength indicator (RSSI) value which is used for a variety of tasks such as AGC, FSK/OOK demodulation, and noise squelching. When the carrier signal is absent, the input signal and the measured RSSI value will be noise and this input noise can trigger demodulation within the receiver to produce demodulated noise output bits. To avoid these noisy output bits, a squelch function is implemented. The squelch circuit gates the digital output data when the RSSI falls 1 dB below sensitivity and enables the digital output when the RSSI level is at sensitivity. A hysteresis of 6 dB is used to avoid the RSSI noise in the absence of a carrier.

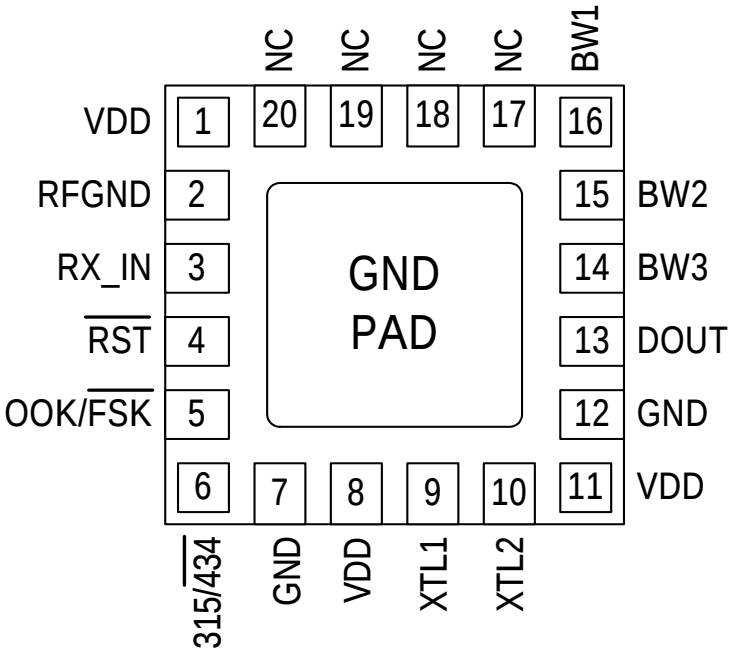
4.8. Crystal Oscillator

An on-board crystal oscillator is used to generate a 16 MHz reference clock for the Si4311. This reference clock is required for proper operation of the Si4311 and is used for calibration of the on-chip VCO and other timing references. No external load capacitors are required to set the 16 MHz reference frequency. Refer to Table 6, “Crystal Characteristics,” on page 7 for board capacitance and frequency tolerance information. The frequency tolerance of the crystal should be chosen such that the received signal is within the IF bandwidth of the Si4311 receiver. Refer to Section “4.5. IF Bandwidth Selection” to see the relationship between IF bandwidth and crystal frequency tolerance. The Si4311 can achieve better sensitivity with a tighter tolerance crystal.

4.9. Reset Pin

Driving the $\overline{\text{RST}}$ pin (pin 4) low will disable the Si4311 and place the device into reset mode. All active blocks in the device are powered off in this mode, bringing the current consumption to 10 uA. The Si4311 is enabled by driving the $\overline{\text{RST}}$ pin (pin 4) to VDD. Refer to Table 4 "Reset Timing Characteristics" for the reset timing requirements.

5. Pin Descriptions: Si4311-A10-GM



Pin Number(s)	Name	Description
1, 8, 11	VDD	Supply voltage, may connect to external battery.
2	RFGND	RF ground. Connect to ground plane on PCB.
3	RX_IN	RF receiver input.
4	$\overline{\text{RST}}$	Device reset, active low input.
5	OOK/$\overline{\text{FSK}}$	Selectable logic input for OOK or FSK modulation.
6	315/$\overline{434}$	Selectable logic input for 315 or 433.92 MHz operation.
7, 12, GND PAD	GND	Ground. Connect to ground plane on PCB.
9	XTL1	Crystal input.
10	XTL2	Crystal input.
13	DOUT	Data output.
14, 15, 16	BW[3:1]	Bandwidth selection input pins.
17, 18,19,20	NC	No connect. Leave floating.

6. Ordering Guide

Part Number*	Description	Package Type	Operating Temperature
Si4311-A10-GM	315/433.92 MHz OOK/FSK Receiver	QFN Pb-free	–40 to 85 °C
***Note:** Add an “(R)” at the end of the device part number to denote tape and reel option; 2500 quantity per reel.			

7. Package Markings (Top Marks)

7.1. Si4311 Top Mark

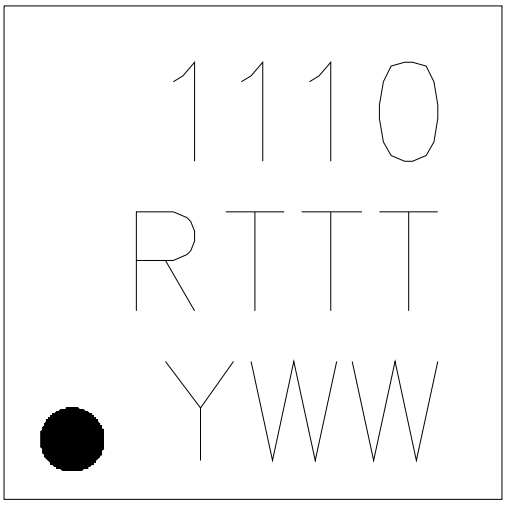


Figure 5. Si4311 Top Mark Example

7.2. Top Mark Explanation

Mark Method:	YAG Laser	
Line 1 Marking:	Part Number	11 = Si4311
	Firmware Revision	10 = Firmware Revision 1.0
Line 2 Marking:	Die Revision	A = Revision A Die
	TTT = Internal Code	Internal tracking code
Line 3 Marking:	Circle = 0.5 mm Diameter (Bottom-Left Justified)	Pin 1 Identifier
	YWW = Date Code	Assigned by the Assembly House. Corresponds to the last digit of the current year (Y) and the workweek (WW) of the mold date.

8. Package Outline: Si4311-A10-GM

Figure 6 illustrates the package details for the Si4311-A10-GM. Table 13 lists the values for the dimensions shown in the illustration.

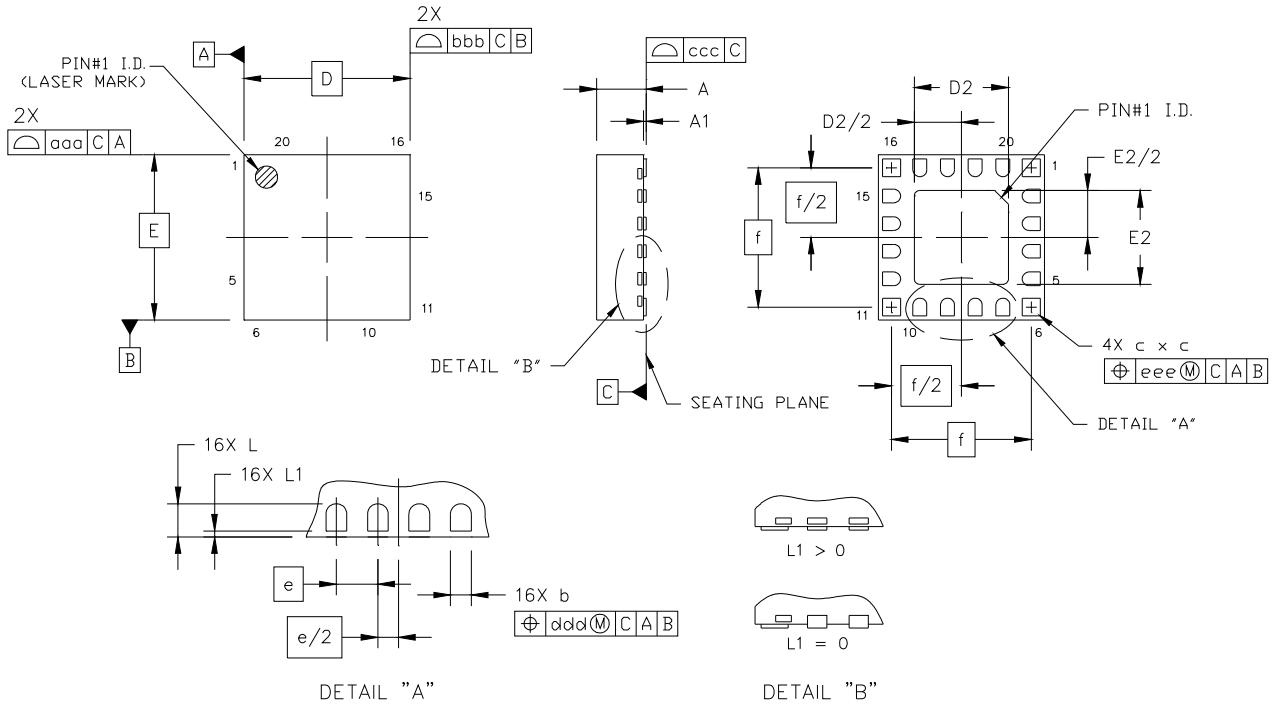


Figure 6. 20-Pin Quad Flat No-Lead (QFN)

Table 13. Package Dimensions

Symbol	Millimeters		
	Min	Nom	Max
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
b	0.20	0.25	0.30
c	0.27	0.32	0.37
D		3.00 BSC	
D2	1.65	1.70	1.75
e		0.50 BSC	
E		3.00 BSC	
E2	1.65	1.70	1.75

Symbol	Millimeters		
	Min	Nom	Max
f		2.53 BSC	
L	0.30	0.35	0.40
L1	0.00	—	0.10
aaa	—	—	0.05
bbb	—	—	0.05
ccc	—	—	0.08
ddd	—	—	0.10
eee	—	—	0.10

Notes:

1. All dimensions are shown in millimeters (mm) unless otherwise noted.
2. Dimensioning and tolerancing per ANSI Y14.5M-1994.

9. PCB Land Pattern: Si4311-A10-GM

Figure 7 illustrates the PCB land pattern details for the Si4311-A10-GM. Table 14 lists the values for the dimensions shown in the illustration.

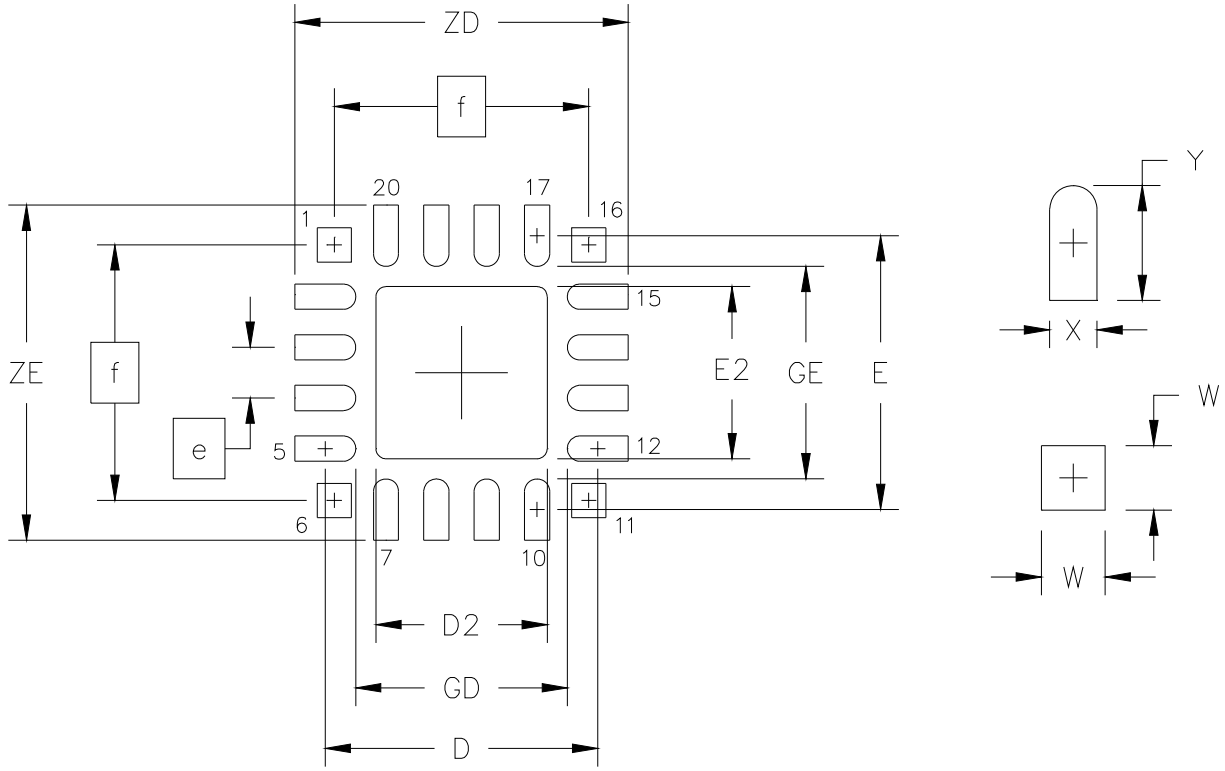


Figure 7. PCB Land Pattern

Table 14. PCB Land Pattern Dimensions

Symbol	Millimeters	
	Min	Max
D	2.71 REF	
D2	1.60	1.80
e	0.50 BSC	
E	2.71 REF	
E2	1.60	1.80
f	2.53 BSC	
GD	2.10	—

Symbol	Millimeters	
	Min	Max
GE	2.10	—
W	—	0.34
X	—	0.28
Y	0.61 REF	
ZE	—	3.31
ZD	—	3.31

Notes: General

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and tolerancing is per the ANSI Y14.5M-1994 specification.
3. This land pattern design is based on IPC-SM-782 guidelines.
4. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a fabrication allowance of 0.05 mm.

Note: Solder Mask Design

1. All metal pads are to be non-solder-mask-defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

Notes: Stencil Design

1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 1:1 for the perimeter pads.
4. A 1.45 x 1.45 mm square aperture should be used for the center pad. This provides approximately 70% solder paste coverage on the pad, which is optimum to assure correct component standoff.

Notes: Card Assembly

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for small body components.

DOCUMENT CHANGE LIST

Revision 0.1 to Revision 0.2

- Maximum data rate changed from 10 to 4 kbps for FSK and from 5 to 2 kbps for OOK with Manchester encoding.
- Maximum RF input power changed from 5 to 10 dBm.
- Changed test conditions for sensitivity measurements and added the xtal frequency tolerance of 20 ppm.
- Updated text in Section “4. Functional Description”.
- Added Ideal IF Bandwidth equation and description for choosing the IF bandwidth in Section “4.5. IF Bandwidth Selection”.
- Updated Table 12, “Typical Sensitivity @ 433 MHz, 2-FSK,” on page 11.
- Changed hysteresis level from 1 dB to 6 dB in Section “4.7. Squelch Circuit”.
- Added text in Section “4.8. Crystal Oscillator” regarding the crystal frequency tolerance and IF Bandwidth choice and sensitivity performance.

Revision 0.2 to Revision 0.3

- Updated features list
- Reduced font size in the test condition section of Table 5 "Si4311 Receiver Characteristics"
- Added crystal tolerance equation to Table 6 "Crystal Characteristics"
- Updated matching circuit and BOM to Section “2. Test Circuit” and Section “3. Typical Application Schematic”
- Modified text in Section “4. Functional Description”
- Changed bandwidth option in Table 11 "Bandwidth Selection Table Using BW[3:1] Pins" and test mode.
- Reset section updated to reflect active blocks are powered off in reset mode.

CONTACT INFORMATION

Silicon Laboratories Inc.

400 West Cesar Chavez
Austin, TX 78701
Tel: 1+(512) 416-8500
Fax: 1+(512) 416-9669
Toll Free: 1+(877) 444-3032

Email: wireless@silabs.com
Internet: www.silabs.com