UM2455

Low Power 2.4GHz Direct Sequence Spread Spectrum (DSSS) Transceiver

Datasheet

DS-2455-01

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UM2455

Low Power 2.4 GHz Direct Sequence Spread Spectrum (DSSS) Transceiver

Applications

- ❑ Baby Finder and Tracker
- ❑ Home Automation Control
- ❑ Interactive Toy
- ❑ Wireless Sensor Network
- ❑ PC Peripherals
- ❑ Medical Equipment
- ❑ Remote Controller

Introduction

The UM2455 is a low cost, highly integrated single chip 2.4GHz transceiver designed for low power wireless applications. This circuit is intended for short range communications and control operating at the ISM band (2.405 – 2.483.5GHz).The chip, which is fabricated with an advanced 0.18um RFCMOS process, integrates a receiver, a transmitter, a frequency synthesizer, a DSSS baseband, and an MAC modem on a single chip. The DSSS modem supports the O – QPSK modulation format and has a configurable data rate of 250K or 625Kbps. The chip also features extensive hardware supports of TX/RX FIFO, CSMA-CA, Security engine, MAC functions, clear channel assessment, link quality indication, and wake up trigger by an MCU or a register.
The main operating parameters and the 128 bytes transmit/receive FIFOs of the UM2455 can be controlled via the SPI/I^2C interface. In typical applications, the UM2455 will be used together with a microcontroller and few external passive components.

Features

RF/Analog

- ❑ ISM band 2.405~2.480 GHz operation
- ❑ -92 dBm sensitivity and 5 dBm maximum input level
- ❑ 0 dBm typical output power and 36 dB TX power control range
- ❑ Differential RF input/output and integrated TX/RX switch
- ❑ Integrated low phase noise VCO, frequency synthesizer and PLL loop filter
- ❑ Integrated 20 MHz oscillator driver
- ❑ Integrated 100 kHz internal oscillator circuit
- ❑ 20 MHz reference clock output
- ❑ Digital VCO and filter calibration
- ❑ Digital RSSI
- ❑ Integrated LDO
- ❑ High receiver and RSSI dynamic range
- ❑ Support power saving modes
- ❑ Low current consumption: 20 mA in RX and 23 mA in TX mode
- ❑ 2 uA deep sleep mode

- ❑ Small 32-pin leadless QFN 5x5 mm^2 package
- ❑ Few external component count
- ❑ Data rates of 250 and 625kbps respectively

MAC/Baseband

- ❑ O–QPSK modulation (DSSS baseband)
- ❑ Hardware CSMA-CA, automatic ACK response and FCS check
- ❑ Up to 8 nodes supported
- ❑ Hardware security engine(AES-128) with CTR, CCM and CBC-MAC modes
- ❑ Four low power operation modes
- ❑ Support all CCA modes and RSSI/LQI
- ❑ Simple four-wire SPI interface
- ❑ I^2C slave supported

Block Diagram

Figure 1 shows the block diagram of UM2455. UM2455 is composed of six blocks:

- ❑ Radio block
- ❑ MAC block
- ❑ Memory block
- ❑ Security engine block
- ❑ Power management block
- ❑ Interfacing block

Detailed descriptions for each block will be described in the following sections.

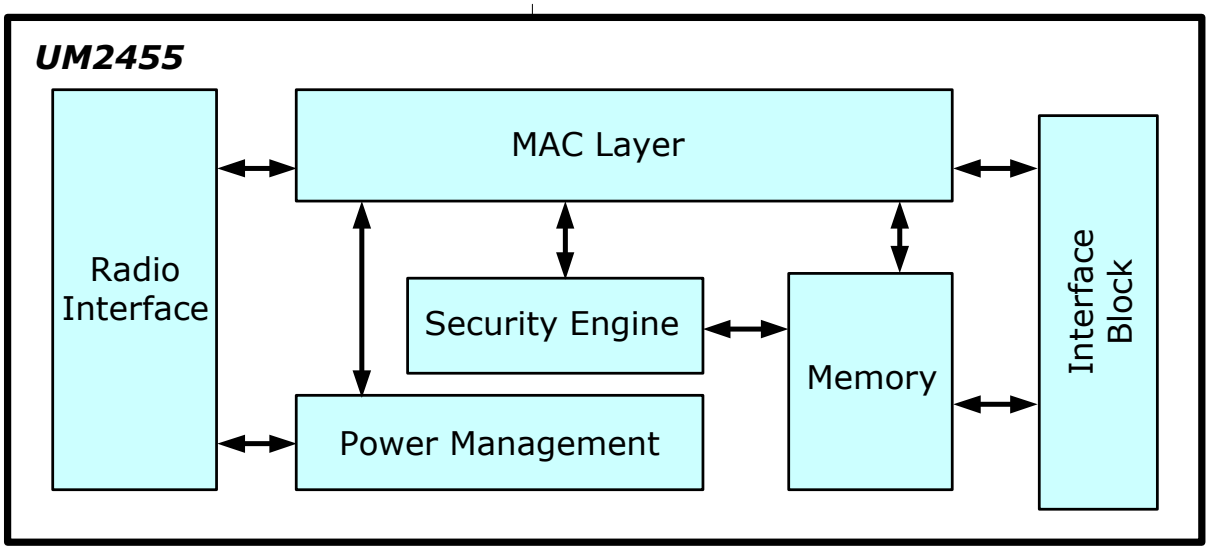

Figure 1. UM2455 Block Diagram

Table of Content

Abbreviations

ACK	Acknowledgement
ADC	Analog to Digital Converter
AES	Advanced Encryption Standard
CAP	Contention Access Period
CBC-MAC	Cipher Block Chaining Message Authentication Code
CCA	Clear Channel Assessment
CCM	Counter Channel Mode
CFP	Contention Free Period
CRC	Cyclic Redundancy Check
CTR	Counter mode + CBC
DAC	Digital Analog Converter
DSSS	Direct Sequence Spread Spectrum
ESD	Electronic Static Discharge
EVM	Error Vector Magnitude
FCF	Frame Control Field
FCS	Frame Check Sequence
FIFO	First In First Out
GTS	Guaranteed Time Slot
IEEE	Institute of Electrical and Electronics Engineers
INT	Interrupt
ISM	Industrial Scientific and Medical
Kbps	Kilo bit per second
LNA	Low Noise Amplifier
LO	Local Oscillator
LQI	Link Quality Indication
LSB	Least Significant Bit / Byte
MSB	Most Significant Bit / Byte
MAC	Medium Access Control
MIC	Message Integrity Code
MPDU	MAC Protocol Data Unit
NC	Not Connected
O-QPSK	Offset Quadrature Phase Shift Keying
PA	Power Amplifier
PHY	Physical Layer
PLL	Phase Locked Loop
QFN	Quad Flat No-lead Package
RF	Radio Frequency
RSSI	Receive Signal Strength Indicator
RX	Receive
SPI	Serial Peripheral Interface
TX	Transmit
VCO	Voltage Control Oscillator

Format Representations of Registers and Their Bits

1. SREG0xnn[m] or SREG0xnn[p:m]
   SREG: short registers
   0xnn: register number
   nn: can be numerical numbers (for example: 1, 2, or 3, etc) or alphabetical words (for example: A, b, or C, etc)
   [m]: the bit number
   [p:m]: bit m, bit n, bit o, and bit p (for example: bit [7:5] means bit 7, bit 6, bit 5, and bit 4)

2. LREG0xnn[m] or LREG0xnn[p:m]
   LREG: long registers
   0xnn: register number
   nn: can be numerical numbers (for example: 1, 2, or 3, etc) or alphabetical words (for example: A, b, or C, etc)
   [m]: the bit number
   [p:m]: bit m, bit n, bit o, and bit p (for example: bit[7:5] means bit 7, bit 6, bit 5, and bit 4)

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1. Pin Configuration

1.1. Device Pin Assignments

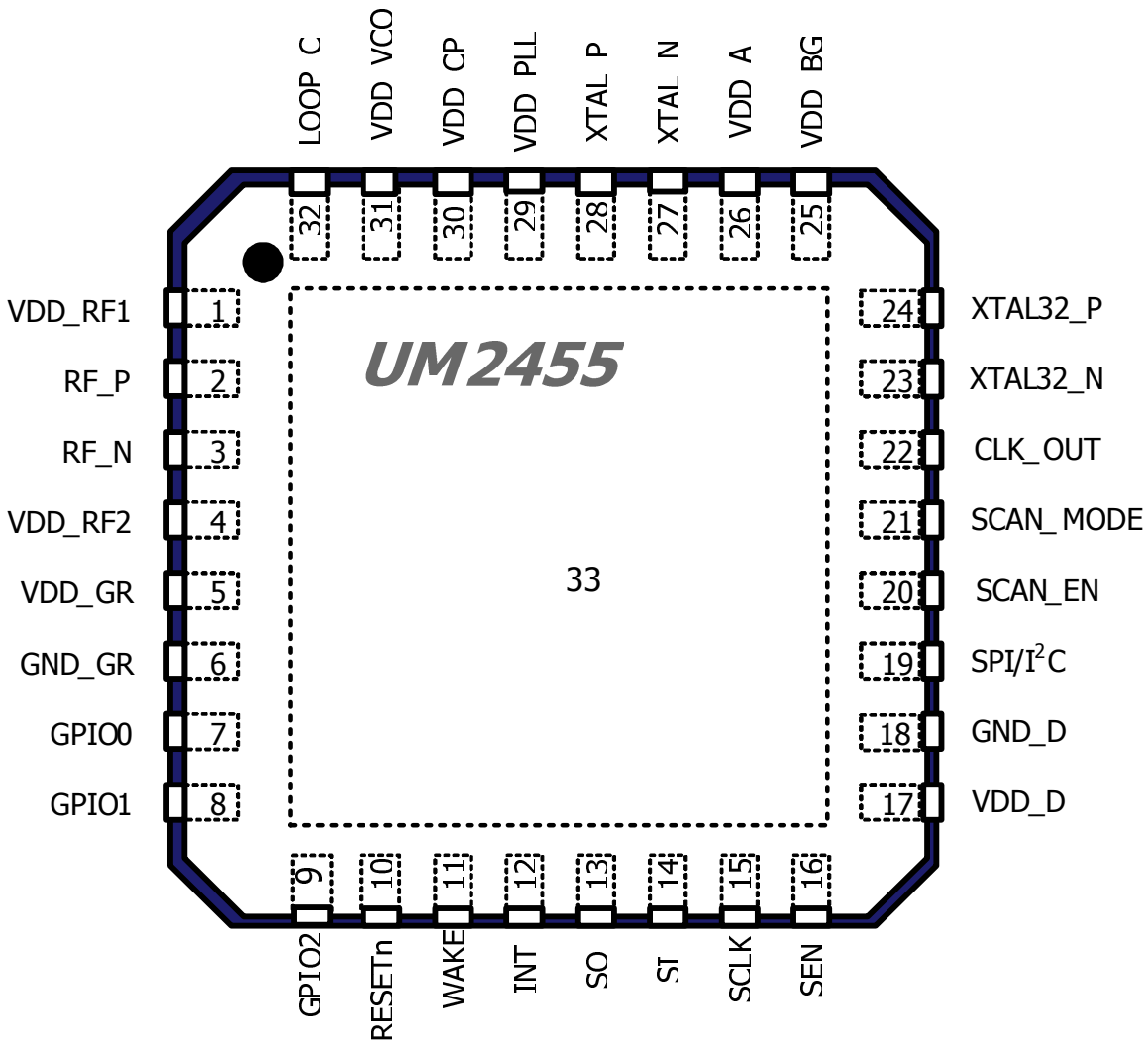


Figure 2. Pin Assignments (top view)

1.2. Device Pin Descriptions

Pin type abbreviation: A = Analog, D = Digital, I = Input, O = Output

Table 1. Pin Descriptions

Pin	Symbol	Type	Description
1	VDD_RF1	Power	The RF power supply. Bypass with a capacitor as close to the pin as possible.
2	RF_P*	AIO	The differential RF input/output (+).
3	RF_N*	AIO	The differential RF input/output (-).
4	VDD_RF2	Power	The RF power supply. Bypass with a capacitor as close to the pin as possible.
5	VDD *	Power	The power supply. Bypass with a capacitor as close to the pin as possible.
6	GND	Ground	Ground.
7	GPIO0	DIO	The general purpose digital I/O. It is also used to enable an external PA.
8	GPIO1	DIO	The general purpose digital I/O. It is also used as an external TX/RX switch control.
9	GPIO2	DIO	The general purpose digital I/O. It is also used as an external TX/RX switch control.
10	RESETn	DI	The global hardware reset pin, which is active low.
11	WAKE	DI	The external wake up trigger.
12	INT	DO	The interrupt pin to the micro-processor.
13	SO,SCL	DIO	The serial interface data output from the UM2455 or the I^2C clock.
14	SI,SDA	DIO	The serial interface data input to the UM2455 or the I^2C data in/out.
15	SCLK	DI	The clock of a serial interface.
16	SEN	DI	The enabled pin of a serial interface.
17	VDD_D	Power	The power supply of the Digital circuit.
18	GND_D	Ground	The ground for the digital circuit.
19	SPI/I2C	DI	The SPI or the I^2C interface selection.
20	SCAN_EN	DI	The scan insertion testing enables signal.

21	SCAN_MODE	DI	The digital scan/test mode enables signal for the chip testing purpose.
22	CLKL_OUT	DIO	The 20/10/5/2.5 MHz clock output.
23	NC	NC	Left Floated.
24	NC	NC	Left Floated.
25	VDD_BG	Power	The power supply for the bandgap reference circuit. Bypass with a capacitor as close to the pin as possible.
26	VDD_A	Power	The power supply for the analog circuit. Bypass with a capacitor as close to the pin as possible.
27	XTAL_N	AI	The 20 MHz crystal input (-).
28	XTAL_P	AI	The 20 MHz crystal input (+).
29	VDD_PLL	Power	The PLL power supply. Bypass with a capacitor as close to the pin as possible.
30	VDD_CP	Power	The charge pumps power supply. Bypass with a capacitor as close to the pin as possible.
31	VDD_VCO	Power	The VCO supply. Bypass with a capacitor as close to the pin as possible.
32	LOOP_C		The PLL loop filter external capacitor. Connected to the external 100 pF capacitor.
33	GND	Ground	Connect to the ground plate.

* ***Caution***: ESD sensitive. Please refer to Section 2.5 for more information.

2. Electrical Characteristics

2.1. Absolute Maximum Ratings

Table 2. Absolute Maximum Ratings

Parameters	Min	Max	Unit
Storage temperature	-40	+120	°C
Supply voltage VDD pin to ground	-0.5	+3.6	V
Voltage applied to inputs	-0.5	VDD+0.5	V
Short circuit duration, to GND, or VDD		5	sec

2.2. Recommended Operating Conditions

Table 3. Recommended Operating Conditions

Parameters	Min	Typ	Max	Units
Ambient Operating Temperature	-40		+85	°C
Supply Voltage for the RF, analog, and digital circuits	2.4	3	3.6	V
Logical high input voltage (for DI type pins)	0.5xVDD_D			V
Logical low input voltage (for DI type pins)			0.2xVDD_D	V

2.3. DC Electrical Characteristics

Test conditions: T_A = 25°C, VDD = 3 V

Table 4. DC Electrical Characteristics

Chip Mode	Condition	Min	Typ	Max	Unit
IDLE	RF in reset mode. Regulator, Oscillator, and digital circuits are on.		7.6		mA
STANDBY	All circuits are powered off; only the 100 kHz oscillator is still on.		3.5		uA
DEEP SLEEP	All circuits are powered off.		2		uA
ACTIVE: TX	At 0 dBm, the output power		23		mA
ACTIVE: RX			20		mA

2.4. Radio Frequency AC Characteristics

2.4.1. Receiver Radio Frequency AC Characteristics

Test conditions: T_A = 25°C, VDD = 3 V, LO frequency=2.445 GHz

Table 5. Receiver Radio Frequency AC Characteristics

Parameters	Condition	Min	Typ	Max	Unit
RF input frequency		2.405		2.480	GHz
RF sensitivity	At antenna input with O-QPSK signal		-92		dBm
Maximum RF input		+5			dBm
LO leakage	Measured at the balun matching the network with the input frequency at 2.4 ~ 2.5 GHz		-60		dBm
Noise figure (Including matching)			8		dB
Adjacent channel rejection	@+/-5 MHz	30			dB
Alternative channel rejection	@+/-10 MHz	40			dB
RSSI range			50		dB
RSSI error		-5		5	dB
Total RX current			20		mA

2.4.2. Transmitter Radio Frequency Characteristics

Test conditions: T_A = 25°C, VDD = 3 V, LO frequency=2.445 GHz

Table 6. Transmitter Radio Frequency AC Characteristics

Parameters	Condition	Min	Typ	Max	Unit
RF carrier frequency		2.405		2.480	GHz
Maximum RF output power			0	3	dBm
RF output power control range			36		dB
TX gain control resolution		0.5	1.25	1.4	dB
Carrier suppression			-30		dBc
TX spectrum mask for O-QPSK signal	Offset frequency > 3.5 MHz, at 0 dBm output power	-33			dBm
TX EVM			15%		
Total TX current	At 0 dBm, the output power		23		mA

2.5. ESD Notice

For the ESD HBM (Human Body Mode), all pins pass 1.5KV voltage requirement.

For the ESD MM (Machine Mode), there are 5 pins that are sensitive to the ESD, which are pin 2(RF_P), pin 3(RF_N), pin 5(VDD), pin 23(NC) and pin 24(NC). A PC board designer should take into account of the ESD sensitivity at these 5 pins.

2.6. Peripheral Characteristics

The UM2455 has both the slave mode SPI and the I^2C interfaces. They can be used by MCU host to access the UM2455 registers and FIFOs. The 4-wire SPI (SEN, SCLK, SI, SO) provides a high speed interface up to 8 MHz on the SCLK pin. Also, the 2-wire I^2C (SDA, SCL) interface provides another lower pin-count solution. The I^2C SDA pin and the SCL pin share the same pins with the SPI SI and the SO respectively.

The UM2455 has 3 GPIO pins. Each can be used for an external PA, a TX, and an RX switch. Users can use them for the control or monitoring purposes. By simply configuring the GPIODIR register for the input/output selection and the GPIO for the input/output data, users can gain a full control over all 3 GPIO pins.

2.7. Power-on and Reset Characteristics

The UM2455 has a built-in power-on reset (POR) circuit which automatically resets all digital registers when the power is turned on. The 20 MHz oscillator circuit starts to lock to the right clock frequency after power-on. The whole process takes 2 ms for the clock circuit to become stable and complete the power-on reset. It is highly recommended that the user waits at least 2 ms before starting to access the UM2455

For the external hardware reset (warm start), the external reset pin 10 (RESETn) is internally pulled high. The UM2455 will hold in the reset state for around 250 usec after the pin 10 (RESETn) is released from the low state.

2.8. Crystal Parameter Specifications

The clock system of the UM2455 can be separated into two parts; one is called main clock and the other sleep clock. The main clock is generated by the 20 MHz oscillator while the sleep clock can be selected from the on-chip 100 kHz oscillator. Among all, the 20 MHz clock utilizes an external crystal for generating the oscillation. The associated pins are XTAL_P and XTAL_N for the 20 MHz crystal. The frequency variation allowed for the 20 MHz crystal is from -60ppm to 60ppm.

3. Functional Description

3.1. Radio Block

Figure 3 shows the block diagram of the radio of the UM2455.

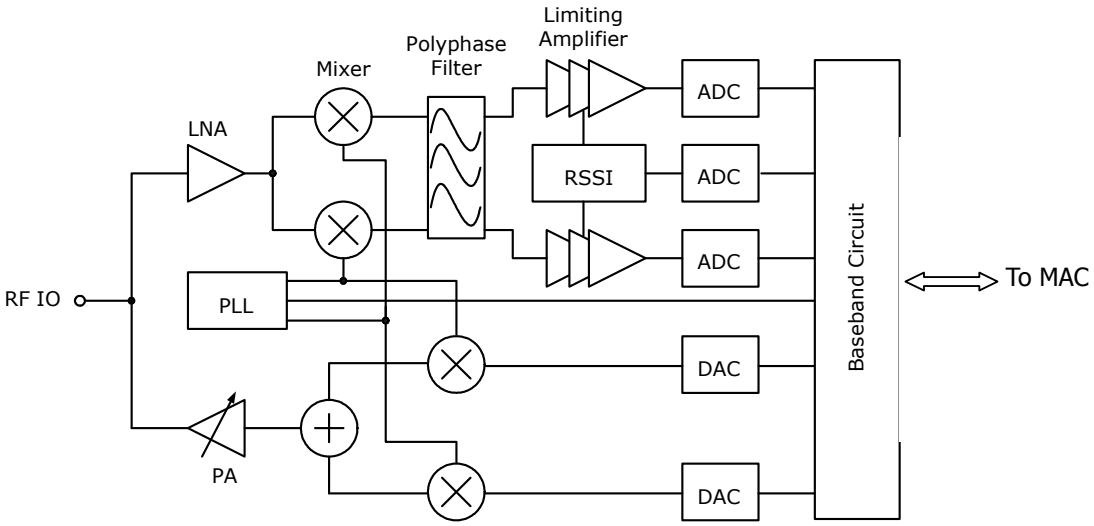


Figure 3. Radio Block Architecture

3.1.1. RSSI/ED and LQI

The RSSI is used to report the signal strength of a received packet. The UM2455 attaches the RSSI value following a received packet in the RXFIFO every time a packet is received successfully. The format of the RXFIFO is as below:

Table 7. RXFIFO Format

LSB					MSB
1 Byte	N Byte	N Bytes	2 Byte	1 Byte	1 Byte
Frame length	Header	Payload	Frame check sequence (FCS)	LQI	RSSI

Please refer to Appendix A for the RSSI mapping table.

3.2. MAC Layer

The UM2455 MAC provides plenty of hardware-assisted features to relieve the CPU/MCU power requirement. The TX-MAC performs the CSMA-CA protocol to send a packet automatically. It also generates a 16-bit FCS automatically.
The RX-MAC receives packets from the RX-Baseband. The received packet is put into the RXFIFO and checked for the FCS simultaneously. The RX-MAC performs the packet filtering by the destination address field and the PAN-ID. Note that only the lower 3 bits of either short or extended address are used by the filter in the RXMAC. Specifically, the RXMAC matches the address whenever the 3 bits are the same as the device address. If both of the address and PAN-ID match their own identity and the FCS check is passed, an interrupt is issued to the CPU/MCU. In normal mode, unqualified packets are skipped. However, in promiscuous mode, any packet passing the FCS check is accepted and an interrupt will be issued. In error mode, any packet is accepted with an interrupt issued. The RX-MAC also informs the TX-MAC to send an acknowledge packet automatically. This happens whenever a packet is successfully received and the bit 5 of the frame control field (FCF) is set to '1'. This will maintain the time requirement of the acknowledge packet.

A 16-bit MAC timer is provided to facilitate the generation of the 15.36 mini second (ms) interrupt necessary for the Simple RF application.

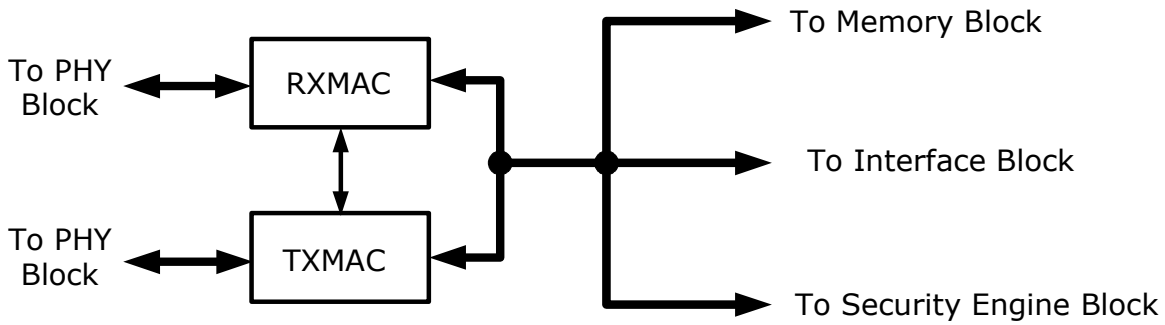


Figure 4. MAC Layer Block Diagram

3.2.1. MAC Layer Introduction

The MAC layer provides the following tasks:

- Generating a connection
- Supporting the Peripheral area network(PAN) association and disassociation
- Providing a reliable link between two peer MAC entities

The packet format of the MAC layer is given as below:

Bytes: 2	1	0 to 20	n	2
Frame Control Field (FCF)	Data Sequence Number	Address Information	Frame payload	Frame Check Sequence (FCS)
MAC Header (MHR)			MAC Payload	MAC Footer (MFR)

Figure 5. Packet Format for MAC

The frame control field (FCF) format is two bytes as the following:

Table 8. MAC Frame Control Field

Bits: 0-2	3	4	5	6	7-9	10-11	12-13	14-15
Frame Type	Security Enabled	Frame Pending	Acknowledge request	Intra PAN	Reserved	Destination address mode	Reserved	Source address mode

The frame check sequence (FCS) is CRC-16. The polynomial of degree 16 is as below:

$$G_{16}(x) = x^{16} + x^{12} + x^5 + 1$$

3.2.2. MAC Timer

The UM2455 has an internal MAC timer for the application protocol use. It is a 16-bit down-counting timer ticking with 8 us. The packet interval for the application protocol is selectable as long as it is a multiple of 15.36 ms, which is 1920 times of 8 us. Using the MAC timer can relieve the timer resource from the MCU. The MAC timer can be triggered by writing the register 'HSYMTMR1' to start downward counting. The timer generates a timer interrupt (half-symbol interrupt) when the down-counting reaches zero. The related registers are as below:

SREG0x28 HSYMTMR0

SREG0x28, HSYMTMR0							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
Low bytes of the half-symbol tick timer low byte [7:0]							
R/W-0x00							

Bit 7:0 **HSYMTMR0**: Low bytes of the 16-bit half-symbol timer.

SREG0x29 HSYMTMR1

SREG0x29, HSYMTMR1							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
low bytes of the half-symbol tick timer [15:8]							
R/W-0x00							

Bit 7:0 **HSYMTMR1**: High bytes of the 16-bit half-symbol timer.

3.2.3. RXMAC

The RXMAC block will do the CRC checking, do a parsing of the received frame type, and do the address recognition before storing the received frame in the RXFIFO which is a 128-byte dual port register file. The received frame will be stored in the RXFIFO one packet at a time. A byte indicating the frame length will be appended in the beginning of the RXFIFO before MPDU, so that the host can decode the frame correctly. There are also 9 bytes of the information attached after MPDU: the LQI, the RSSI, and the Frame Timer (4 bytes). The behavior of the RXFIFO follows a certain rule: When a received packet is not filtered or dropped out, a received interrupt/status will be issued. The interrupt is a read-to-clear type to save the host operation clock cycle. However, the RXFIFO is flushed only by the following three ways: (1) the host reads the first byte of the packet, (2) the host issues an RX flush, and (3) the software resets. Please note that once the first byte of the RXFIFO is read, the RXFIFO is ready to receive the next packet. So it is suggested that the programmer reads back all data without any interrupt or jumping to other processes.
The RXMAC recognized a valid packet. The acceptance rules are:

(1) The frame type subfields shall not contain an illegal frame type.
(2) If the frame type indicates that the frame is a TDMA frame, the source PAN identifier shall match the macPANId unless it is equal to '0xffff', in which case the TDMA frame shall be accepted regardless of the source PAN identifier. If a destination PAN identifier is included in the frame, it shall match the macPANId or shall be the broadcast PAN identifier (0xFFFF).
(3) If a short destination address is included in the frame, it shall match either the lower 3 bits of the macShort address or the broadcast address (0xFFFF). Otherwise, if an extended destination address is included in the frame, it shall match the lower 3 bits of an Extended Address.
(4) If only the source address fields are included in the data or the MAC command frame, the frame shall be accepted only if the device is a PAN coordinator and the source PAN identifier matches macPANId.

If the above conditions are met, the RXMAC will issue an RX interrupt to the host device to indicate that a valid packet is received. The UM2455 RXMAC also supports promiscuous mode and error mode. Promiscuous mode is supported to receive all FCS-ok packets. Error mode is supported to receive all packets that successfully correlate with the physical layer (PHY) level preamble and the delimiter. Under these two conditions, the RXMAC issues an RX interrupt, too.

The UM2455 RXMAC supports an automatic ACK reply. If and only if the four conditions mentioned above are met, and the AckReq bit in the frame-control field of the header of the received packet is set, an ACK packet will be sent by the TXMAC automatically in the meantime. The sequence number will be the same as the incoming packet.

When an encrypted packet is received, the RXMAC will not inform the security module directly. Instead, it issues a security interrupt. Then the host can decide whether to decrypt or ignore it.

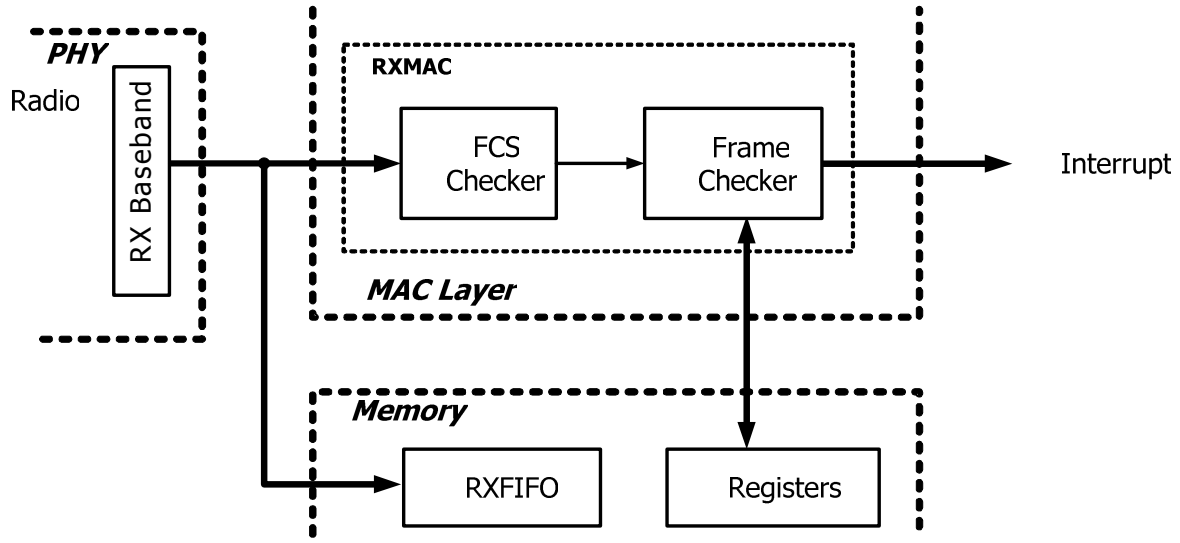


Figure 6. RXMAC Block Diagram

3.2.4. TXMAC

The block diagram of the TXMAC is shown in the Figure 7 as below. The TXMAC performs three major tasks. They are:

- TXFIFO control
- Automatic ACK
- Time alignments.

For the TXFIFO control function, the TXMAC controls one FIFO-the normal FIFO. When the normal FIFO is triggered, the TXMAC performs the automatic anti–interference algorithm sends the packet to the TX baseband at the right time, handles the retransmission if the ACK is required but not received, and generates FCS bytes automatically. The automatic anti–interference algorithm performs the time alignments such as LIFS, SIFS, and the ACK turnaround time. A user can simply program the parameters of the anti–interference algorithm, and the TXMAC will perform corresponding tasks automatically.

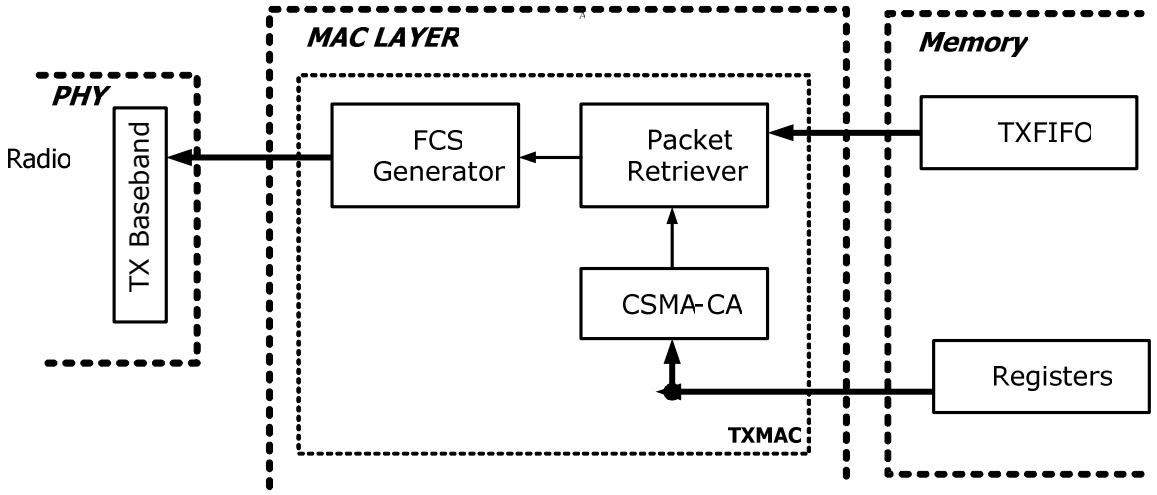


Figure 7. TXMAC Block Diagram

3.3. Memory Block

The memory block (including registers and FIFOs) of the UM2455 is implemented by the SRAM. It is composed of registers and FIFOs shown as below:

Registers

- Short register (6-bit short address mode register, total 64 bytes)
- Long register (10-bit long address mode register, total 128 bytes)

FIFOs

- TX FIFO–Normal (128 bytes)
- Security Key FIFO (64 bytes)
- RX FIFO (128 + 16 bytes)

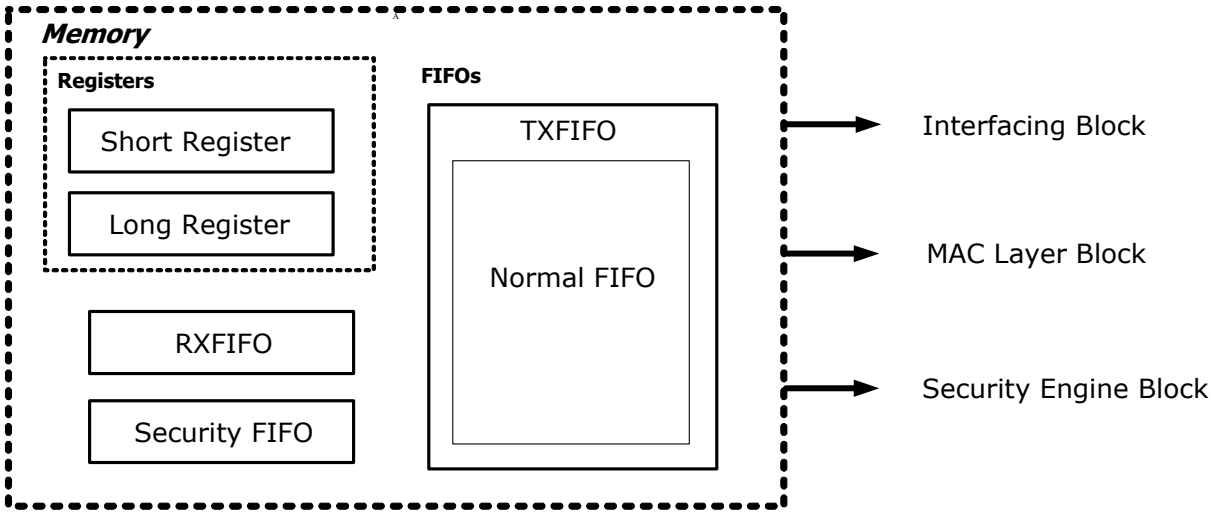


Figure 8. Memory Block Diagram

Registers provide control bits and status flags for UM2455 operations, including the transmission, the reception, the interrupt control, a timer, MAC/baseband/RF parameter settings, security, etc. Short registers are accessed by short address mode with valid addresses ranging from '0x00' to '0x3F'. Long registers are accessed by long address mode with valid addresses ranging from '0x200' to '0x27F'. The length of the address differs between the two modes. Please refer to Section 3.7.1 and 3.7.2 for detailed address rules for the SPI and the I^2C interface.

FIFOs serve as the temporary data buffers for the data transmission, the reception, and security keys. Each FIFO holds only one packet at a time. The transmission FIFO is called TXFIFO. The TXFIFO is composed of a 128-byte FIFO for different purposes, namely Normal FIFO. The receiving FIFO is called RXFIFO. The RXFIFO is composed of one 144-byte FIFO. The final part is called Security Key FIFO. The Security Key FIFO is composed of one 64-bite FIFO and is capable of holding four 16-byte security keys for secured operation. Please refer to Section 4.2 for further information about registers and FIFOs.

3.3.1. Registers

Short Registers

Short registers are accessed by short address mode with valid addresses ranging from '0x00' to '0x3F'. Together with long registers, they provide control bits and status flags for UM2455 operations, including the transmission, the reception, the interrupt control, the timer, MAC/baseband/RF parameter settings, security, etc. Short registers are accessed faster than long registers.

Long Registers

Long registers are accessed by long address mode with valid addresses ranging from '0x200' to '0x27F'. Together with short registers, they provide control bits and status flags for UM2455 operations, including the transmission, the reception, the interrupt control, the timer, MAC/baseband/RF parameter settings, security, etc. Long registers are accessed slower than short registers.

3.3.2. FIFOs

TXFIFO

The TXMAC gets data to transmit from one TXFIFO called 'normal TXFIFO'. According to different conditions, the different FIFO is selected. The normal TXFIFO is 128 bytes in length.

RXFIFO

The RXFIFO is a 144-byte FIFO memory to store the incoming packet. It's designed to store one packet at a time.

Security FIFO

A security FIFO holds the corresponding key of each FIFO. The address mapping is as below:

Address	Description
280h ~ 28Fh	TX Normal FIFO key
2B0h ~ 2BFh	RX FIFO key

3.4. Power Management Block

Almost all wireless sensor network applications require low-power consumption to lengthen the battery life. Typical power consumption of a battery-powered device is such that the deployed device could operate over years without the need to replace its battery. The UM2455 achieves the low active current consumption of both the digital and RF/analog circuits by controlling the supply voltage and using the low-power architecture. The sleep current for the UM2455 can be as low as 2uA only. During sleep mode, the data in the digital registers/FIFOs are retained. The UM2455 has four power saving modes that will be further described in Section 3.4.5.

3.4.1. Power Supply Scheme

The table below lists the recommended external bypass capacitors for each pin of the UM2455. For the two power supply pins (pin No.1 and 31), they need an extra bypass capacitor in parallel for decoupling purpose while the rest of the power supply pins require only one bypass capacitor. The length of the path from the bypass capacitors to each pin should be made as short as possible.

Table 9. Recommended External Bypass Capacitors

Pin	Symbol	Bypass Capacitor 1	Bypass Capacitor 2
1	VDD_RF1	47 pF	10 nF
4	VDD_RF2	47 pF	
5	VDD	100 nF	
17	VDD_D	10 nF	
25	VDD_BG	47 pF	10 nF
26	VDD_A	47 pF	
29	VDD_PLL	47 pF	
30	VDD_CP	10 nF	
31	VDD_VCO	1 uF	

3.4.2. Voltage Regulator

There is an individual voltage regulator for each supply voltage pin of the UM2455. No external stabilizing capacitor is needed for each of the voltage regulators. All the regulators supply a 1.8V output to internal circuit nets.

3.4.3. Battery Monitor

The UM2455 provides a function to monitor the system supplied voltage. A 4-bit voltage threshold can be configured so that when the supplied voltage is lower than the threshold, the system will be notified. For the battery monitor function, please refer to Section 3.10.4

3.4.4. Power-on Reset

The UM2455 has a built-in power-on reset (POR) circuit which automatically resets all digital registers whenever the power is turned on. The 20 MHz oscillator circuit starts to lock to the right clock frequency after power-on. The whole process takes 2 ms for the clock circuit to become stable and complete the power-on reset. It is highly recommended that the user waits at least 2 ms before starting to access the UM2455.

3.4.5. Power Modes

The power modes of the UM2455 are classified into the following four modes:

- ACTIVE : Fully turned on with two sub-modes designated as TX-ACTIVE and RX-ACTIVE
- IDLE : RF shutdown mode
- STANDBY : RF/MAC/BB shutdown while the sleep clock remains active
- DEEP_SLEEP : All power is shutdown except the power to the digital circuits; the register and the FIFO data are retained.

Sleep mode mentioned later means both STANDBY mode and DEEP_SLEEP mode. The only difference between STANDBY mode and DEEP SLEEP mode is the power status of the sleep clock. IDLE mode is rarely used because the device should at least always turn on its RX circuit onto capture the on-air RF signals.

The power management control is used for the low power operation of the MAC and the baseband modules. It manages to turn on and off the 20 MHz clock when the UM2455 goes into sleep mode. By turning off the 20 MHz clock, the MAC and the baseband circuits become inactive regardless whether their power supplies exist or not.

All the digital modules are clock-gated automatically. That means only when a module is functioning, its clock would then be turned on. For example, the clock of the security module is turned off if the security feature is disabled. This approach efficiently decreases a certain amount of the current consumption.

There are two dedicated time counters in the UM2455 for sleep mode operation. One is called main counter and the other is called remain counter. The unit of a tick differs between the two counters since the clock for the main counter is driven by the sleep clock which is 100 kHz (on-chip internal clock). The remain counter is driven by the 20 MHz clock. The sleep reference interval is calculated using the combination of the two time counts of the main counter and remain counter to achieve the time accuracy.

With the help of on-chip main and remain counters, the UM2455 is able to switch between ACTIVE and STANDBY modes. Detailed descriptions are available in Section 3.10.2. If DEEP_SLEEP mode is desired instead of STANDBY mode, MCU host has to control the timing of sleeping process counters for Power Saving Modes.

Sleep Reference Interval

The sleep reference interval is composed of three parts. In the beginning, there is a front remain clock period. In the middle, there is a main clock period which is the major component of the sleep reference interval. In the end, there is a rear remain clock period which is identical to the front clock period. The front and rear remain clock periods increase the accuracy of the sleep intervals.

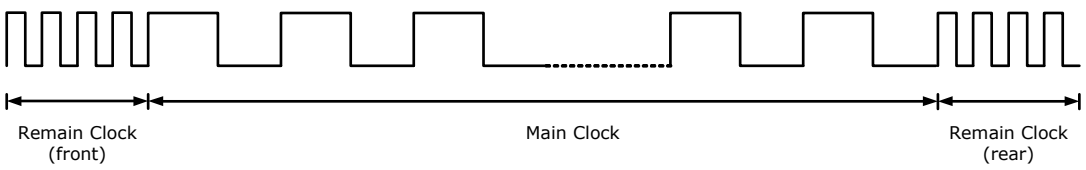


Figure 9. Composition of Sleep Reference Interval

Sleep Alert (SLPIF, SREG0x31 [7])

The sleep alert is issued by the TXMAC on the boundary between the active (composed of the CAP and the CFP) and the inactive period. Sleep alert is an interrupt event.

Sleep Acknowledgement (SLPACK, SREG0x35 [7])

The short register 'SLPACK' (SREG0x35 [7]) should be issued by MCU host to initiate the sleep process. The sleep acknowledgement also turns off the PHY block.

Start Count (StartCnt, LREG0x229 [7])

The StartCnt (LREG0x229 [7]) should be set to the value '1' to initiate the sleep process. The StartCnt also turns off the PHY block and starts the sleep reference clock.

Wake-up and Wake-up Alert (WAKEIF, SREG0x31 [6])

The UM2455 wakes up when the wake-time (waketime, LREG0x222, and LREG0x223) is reached. The 20 MHz oscillator is restarted after the wake-up signal restarts itself. Since the 20 MHz_oscillator needs 2~3 ms to become stable, the 20 MHz clock is not enabled immediately once the 20 MHz oscillator is restarted. The 20 MHz clock will be enabled only when one wake-count (SREG0x35 and SREG0x36) is reached.

Main Counter (TXMAINCNT, LREG0x226, LREG0x227, LREG0x228, LREG0x229)

The main counter uses a sleep clock to count. The sleep clock, the internal 100 kHz clock, can be selected by the long register LREG0x207 [7:6]. Accurate calibration of the clock should be performed when using the 100 kHz internal oscillator as the sleep clock. Please refer to Section 4.5.1 for detailed calibration procedures. The count is stored from the long register LREG0x226 to LREG0x229.

Remain Counter (TXREMCNT, LREG0x224, LREG0x225)

The remain counter uses a 20 MHz clock to count. The count is stored in the long registers LREG0x24 and LREG0x25.

Waketime (WAKETIME, LREG0x222, LREG0x223)

The waketime is denoted with the number 'n'. It indicates the time when the 20 MHz oscillator should wake up from the sleep status.

Wake count (WAKECNT, SREG0x35, and SREG0x36)

The WAKECNT is the time count 't' in between the restart of the 20 MHz oscillator and when it becomes stable and available. It ticks according to the chosen sleep clock.

Enter STANDBY or DEEP_SLEEP Modes

- STANDBY mode
  - STANDBY modes of the UM2455 can be activated by setting the short register SLPACK (SREG0x35 [7]) or setting the long register StartCnt (LREG0x229 [7]). When either of these two bits is set, the UM2455 turns off the voltage regulators and the RF circuits enter sleep mode. During sleep mode, both long and short registers are accessible and their contents are retained.
- DEEP_SLEEP mode
- To enter DEEP_SLEEP mode for the sleep status, a user has to disable the sleep clock to further reduce the current consumption. The sleep clock is always turned-on in STANDBY mode. Setting the short register SLPACK (SREG0x35[7]) to the value '1' will enforce the UM2455 to sleep. To further turn off sleep clock, set CLK32OFF(LREG0x21d1[0]) to '1'. Under DEEP_SLEEP mode, UM2455 can only be waken up by WAKE pin or by resetting power circuits at RSTPWR(SREG0x2A[2]).

Wake-up

The UM2455 has two wake-up modes: timed wake-up and immediate wake-up.

- Timed wake-up
  - However, if a user sets both the main counter and remain counter to zero, the UM2455 will not wake up unless an immediate wake-up is triggered.
- Immediate wake-up
  - The UM2455 can be awakened externally by WAKE (pin 15). The register SREG0x0D [5] enables the WAKE pin. The register SREG0x0D [6] controls the polarity of the WAKE pin. Be sure to set the register SREG0x22 [7] to the value '1' to enable the Immediate wake-up mode before sleeping.
  - The UM2455 can also be awakened by setting the register SREG0x22[6] to the value '1' and back to the value '0', the immediate wake-up mode is then entered.
  - Another fast way to wake up the UM2455 is to set the register SOFTRST. Setting the register SREG0x2A [2] as the value '1' resets the power management circuits, including the sleep registers.

3.4.6. Hardware Acknowledgement

Following the request for the remote acknowledgement of a transmitted packet can be enabled or disabled by setting its header field. The header format is shown as below:

Octets: 2	1	0/2	0/2/8	0/2	0/2/8	variable	2
Frame control	Sequence number	Destination PAN identifier	Destination address	Source PAN identifier	Source address	Frame payload	FCS
		Address fields					
MHR						MAC payload	MFR

Bits: 0-2	3	4	5	6	7-9	10-11	12-13	14-15
Frame type	Security enabled	Frame pending	Ack. request	Intra-PAN	Reserved	Destination Address mode	Reserved	Source Address mode

Bit 5 of the 'Frame control' field indicates whether the frame needs an acknowledgement or not. Users should prepare the header information correctly and write it into the TXFIFO. If the 'ACK request' bit-field is set to be the value '1', the receiver of this packet is required to send the ACK packet back. If the ACK frame from the remote receiver is not received, the transmitter should send the packet again and again till the maximum number of the retransmission times is reached.

The UM2455 has a built-in circuit to facilitate the acknowledgement protocol automatically. For the transmitting side, the UM2455 supports auto-retransmissions. For the receiving side, the UM2455 supports auto-acknowledgements. Each of the two sides needs to set corresponding registers correctly to utilize the functions.

Auto-retransmission on TX Side

For the TXMAC to retransmit a packet automatically when an ACK is not received, the short register 'TXNACKREQ' (SREG0x1B [2] for TX Normal FIFO) is required to set to be the value '1'.

Auto-acknowledgement on RX Side

The RXMAC of the UM2455 will automatically reply an ACK packet by default if an 'ACK request' in the frame header is set to the value '1'. This auto-acknowledgement feature can be disabled by setting the short register NOACKRSP (SREG0x00 [5]) to the value '1'.

3.5. Security Engine Block

The Security module provides the security engine for the UM2455 MAC. In addition to the security requirements of the MAC layer, the UM2455 also provides a security method called 'upper-layer security' for the network or application layer.

The followings are the features of the UM2455 Security Engine Block:

- Transmit encryption and receive decryption
- Seven modes of Security suites are provided:
  - AES-CTR
  - AES-CCM-128
  - AES-CCM-64
  - AES-CCM-32
  - AES-CRC-MAC-128
  - AES-CRC-MAC-64
  - AES-CRC-MAC-32
- Security of APL and NWK layers can be achieved using the same engine.

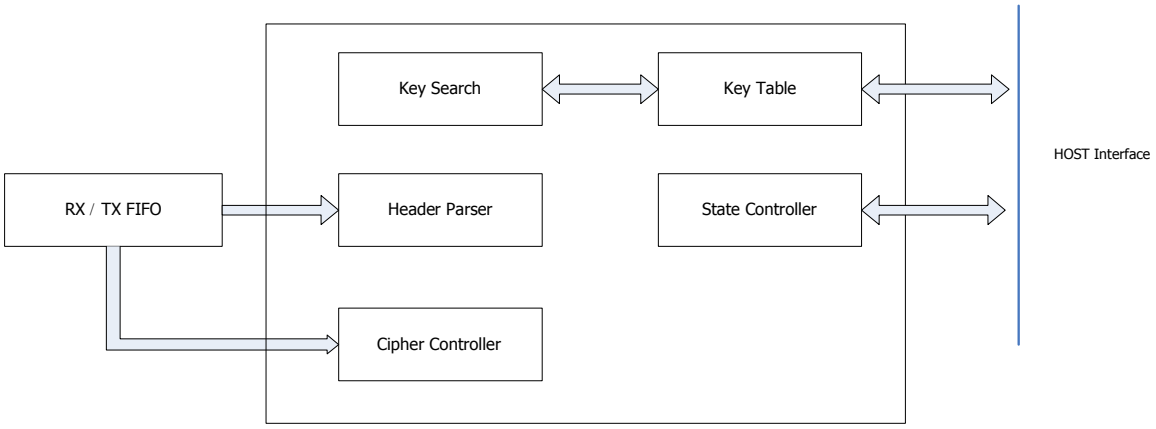


Figure 10. Security Engine Block Diagram

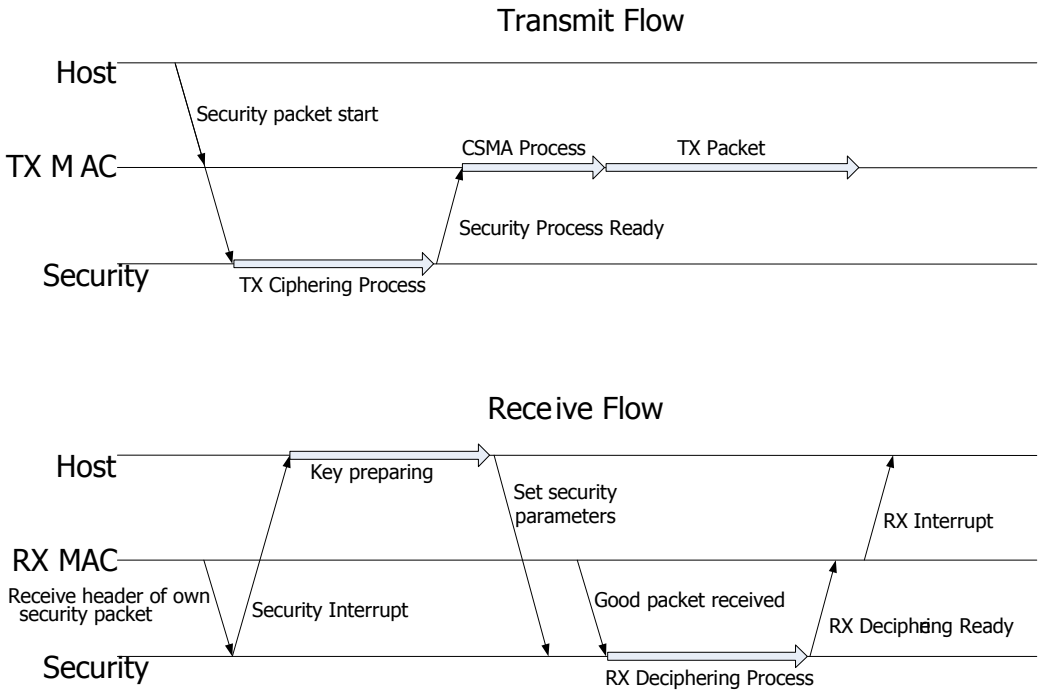


Figure 11. Security Engine Flow Chart

3.6. Analog Circuits

3.6.1. Crystal Oscillators

The table below lists the parameters of the 20 MHz crystal oscillator used in the UM2455. This clock is exportable at pin 22. Optional frequencies are selectable among 20 MHz / 10 MHz / 5 MHz / 2.5 MHz. The crystal can be shared with a MCU host.

By default, the 20 MHz crystal is suggested for most of the applications. A user has to select the 20 MHz crystal which meets the following requirements in order to operate the UM2455 properly.

Table 10. Requirements for 20 MHz Crystal

Parameter	Min	Typ	Max	Unit
Crystal Frequency		20		MHz
Frequency Offset	-60		60	ppm
Shunt Capacitance		27		pF
Start-up Time		1		msec

3.6.2. PLL Frequency Synthesizer

The loop filers of the Phase-Lock Loop (PLL) in the frequency synthesizer are integrated into the UM2455 except one external capacitor which should be connected to pin 32. The surrounding board layout between pin 32 and the ground should be carefully designed to avoid the EMI (electro magnetic interference) in order to keep the PLL stable. The recommended value of this external capacitor is 100 pF.

3.6.3. Internal 100 kHz Sleep Clock Oscillator for the Sleep Clock

There is a free-running 100 kHz sleep clock oscillator integrated into the UM2455. No external component is needed for the operation of this sleep clock. A user has to calibrate this 100 kHz sleep clock before an application starts.

3.7. Peripherals

3.7.1. SPI Interface

The SPI module provides the slave SPI interface to read/write the control registers, FIFOs, and security key table of the UM2455. The features are as below:

- Normal Mode: a simple 4-wire SPI-compatible interface (pins SCLK, SEN, SI and SO) where the UM2455 is the slave.
- Plus Mode: a 2x speed for long address read/write only. It uses the pin SI as SO1 & SO as SO0 while reading the long-address data.
- Most significant bit (MSB) of all addresses and data transfers on the SPI interface is done first.
- Mode selection: By default, the SPI is set to normal mode. To select plus and enhanced modes,

SREG0x34 [7:6] should be set (by normal SPI operation) to the value '0x1' as plus mode, and the value '0x2' as enhanced mode. Afterward, plus or enhanced modes should be used.

SPI Characteristic

Table 11. SPI Characteristics

Parameter	Symbol	Min	Max	Units	Conditions
SCLK, clock frequency	F_{SCLK}		<10 <5	MHz	10 MHz in normal/plus mode 5 MHz in turbo mode
SCLK low pulse duration	t_{CL}	50 100		ns	SCLK pin must be low in the minimum time period.
SCLK high pulse duration	t_{CH}	50 100		ns	SCLK pin must be high in the minimum time period.
SEN setup time	t_{SP}	50		ns	SEN pin must be low in the minimum time period before the first positive edge of SCLK.
SEN hold time	t_{NS}	>50 >100		ns	SEN pin must be held low in the minimum time period after the last negative edge of SCLK pin.
SI setup	t_{SD}	25		ns	Data must be ready at SI pin in the minimum time period, before the positive edge of SCLK pin
SI hold time	t_{HD}	25		ns	Data must be held at SI pin in the minimum time period, after the positive edge of SCLK pin.
Rise time	t_{RISE}		25	ns	The maximum rising time period for SCLK and SEN pins.
Fall time	t_{FALL}		25	ns	The maximum falling time period for SCLK and SEN pins.

SPI Time Diagrams

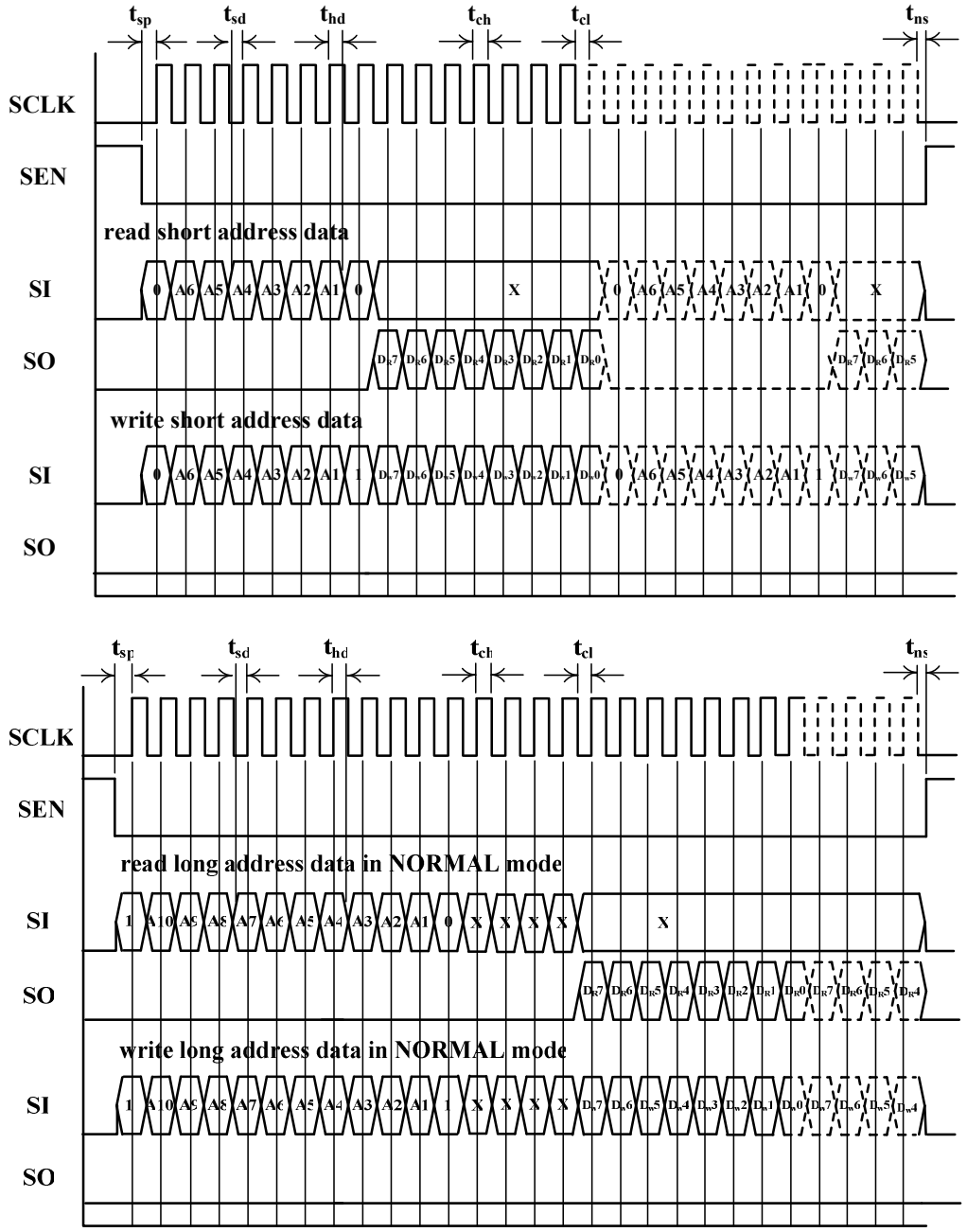


Figure 12. Time Diagram and Specification in Normal Mode

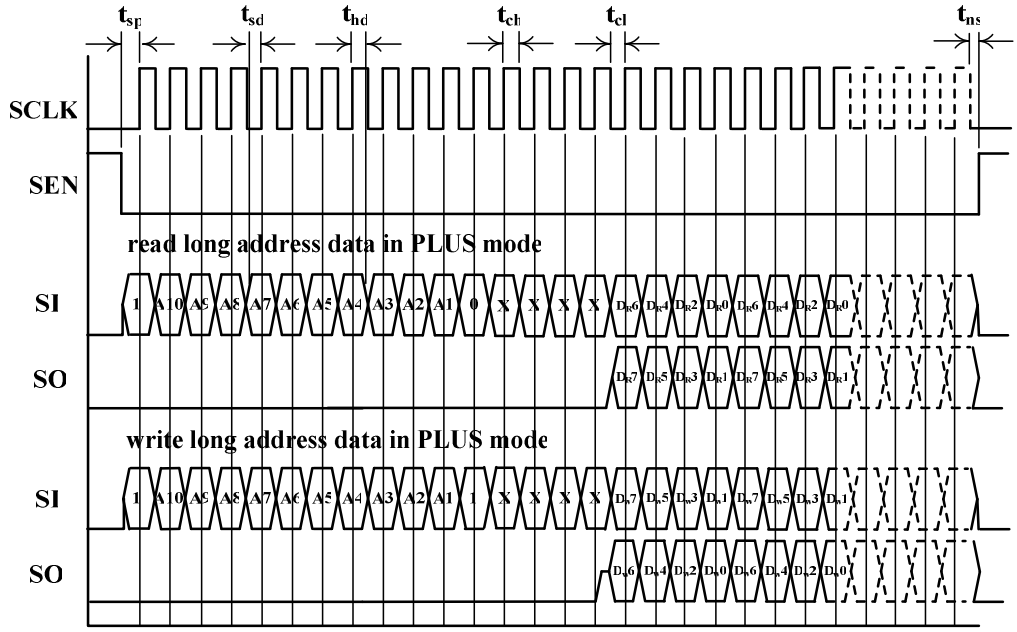


Figure 13. Time Diagram and Specification in Plus Mode (Only for Long Address Registers)

3.7.2. I²C Interface

The UM2455 provides another serial interface and I²C serial interface to access the control registers and FIFOs.

Device Operation

- CLOCK and DATA TRANSITIONS: The SDA/SCLK pin is normally pulled high with an external device. Data on the SDA pin may change only during SCLK low time periods. Data changes during SCLK high periods will indicate a start or stop condition as defined below.
- START CONDITION: A high-to-low transition of SDA with SCLK high is a start condition which must precede any other command.
- STOP CONDITION: A low-to-high transition of SDA with SCLK high is a stop condition.
- ACKNOWLEDGE: All addresses and data words are serially transmitted to and from the UM2455 in 8-bit words. The UM2455 sends a zero to acknowledge that it has received each word. This happens during the ninth clock cycle.

Device Address

The UM2455 requires 7-bit device addresses adding control bits-over the two-wire serial bus following a start condition to enable the chip for a read or write operation. The device address word consists of 11001 for the first five most significant bits as shown below. The next 2 bits are b_2 and b_1 which are selected by SCLK and SEN pins respectively. The $11001b_2b_1$ is the I²C slave address of the UM2455. The programmable part b_2b_1 of the address is defined by hardware pins SCLK and SEN respectively. The last bit b_0 is a control bit. If b_0 is LOW, it means 'Write Operation' or else 'Read Operation'.

Table 12. I²C Device Address Configuration

SCLK	SEN	Slave Address
0	0	110 0100
0	1	110 0101
1	0	110 0110
1	1	110 0111

Write Operations

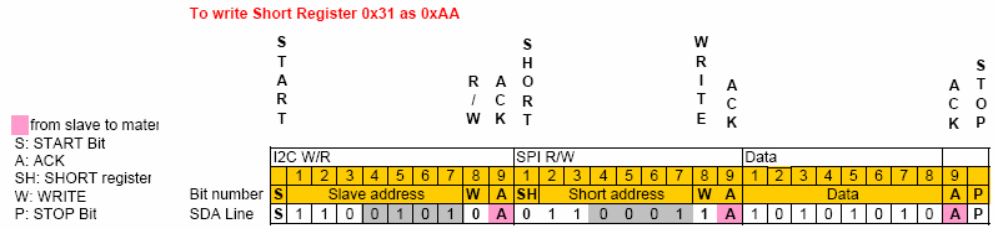
A writing operation requires an 8-bit data word address following the slave address word and acknowledgment. Upon a receipt of this address, the UM2455 will again respond with a zero and then clock in the first 8-bit register address. Following the receipt of the 8-bit data word, the UM2455 will automatically output a zero; the address device, such as a microcontroller, must terminate the write sequence with a stop condition.

Read Operations

Read operations are initiated the same way as the write operations with the exception that the read/write select bit in the slave address word is set to the value '1'. Once the slave address word and data word address are acknowledged by the UM2455, the microcontroller must generate another start condition. The microcontroller now initiates a current address read by sending a device address with the read/write select bit high. The UM2455 acknowledges the slave address and serially clocks out the data word. The microcontroller does not respond with a zero but does generate a following stop condition.

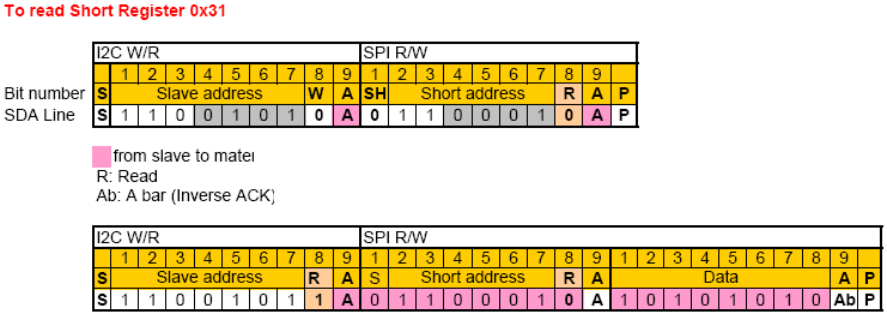
Short Register Write

Example: write short register 0x31 as 0xAA



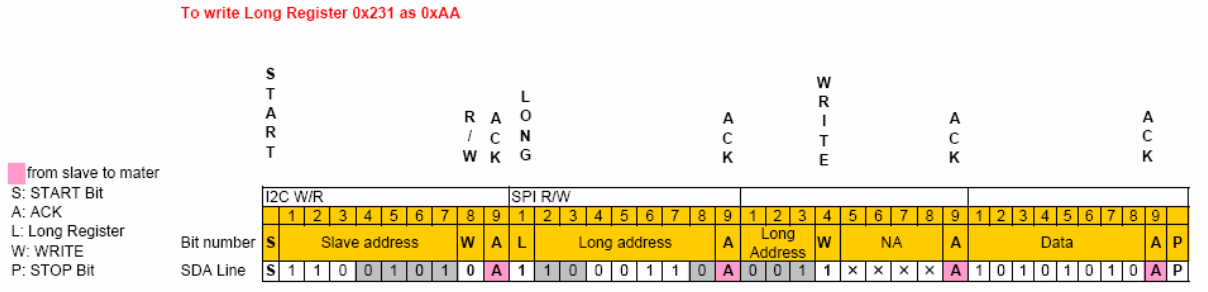
Short Register Read

Example: read short register 0x31



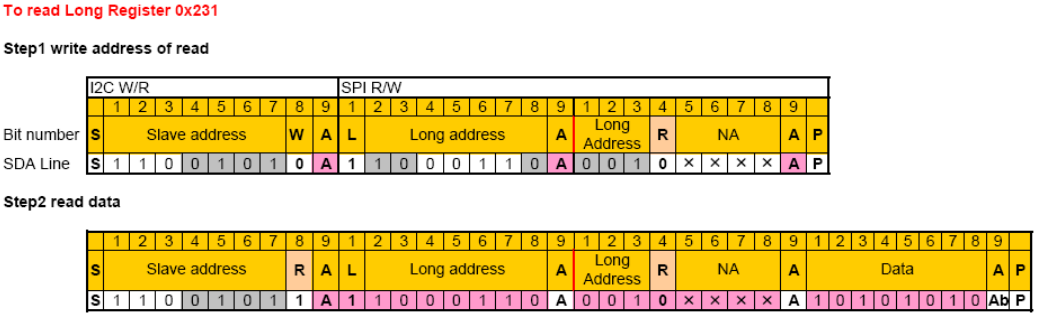
Long Register Write

Example: write long register 0x231 as 0xAA



Long Register Read

Example: read short register 0x231



3.7.3. GPIO

The UM2455 has 3 digital GPIOs. Each GPIO can be configured as input or output respectively. When being configured as an output pad, the driving capability is 4mA for GPIO0 and 1mA for GPIO1 and GPIO2. Besides, GPIO1 and GPIO2 can be configured to control an external PA, a LNA, and a switch according to the current RF state, a TX, or the RX state.

3.7.4. Interrupt Signal

The UM2455 provides an output interrupt pin (INT), and the polarity of interrupt signal is selectable. The UM2455 issues interrupts to MCU host on eight possible events (For detailed interrupt event descriptions, please see Section 4.2.5). If any event happens, the UM2455 sets the corresponding status bit in the short register SREG0x31. If the corresponding interrupt mask in the short register SREG0x32 is clear (i.e. equals '0'), an interrupt will be issued. If it is set (masked, blocked), an interrupt will not be issued, but the status is still present. An interrupt is a read-to-clear operation. Whenever the register SREG0x31 is read, the interrupt and status are cleared. This is beneficial to increase the performance.

The UM2455 issues an interrupt according to the following eight events which are described as below:

Sleep alert interrupt (SLPIF)

The UM2455 counts the active and inactive periods. When encountering the inactive period, the UM2455 will

issue a sleep alert interrupt to indicate the event, regardless whether it is set to be the coordinator or device mode.

Wake-up alert interrupt (WAKEIF)

Every time a wake-up event happens, the UM2455 issues the interrupt event.

Half symbol timer interrupt (HSYMTMRIF)

The half symbol timer (HSYMTMR) (16 bits) setting with the short registers SREG0x28 and SREG0x29 is an internal timer ticking at half-symbol rate (8 us). The interrupt is issued when HSYMTMR down counts to '0'. Note that HSYMTMR does not reload.

Security interrupts (SECIF)

On receiving a packet with 'Security enable' bit set in 'Frame control' field of the packet header, a security interrupt is issued. Normally MCU host should prepare the security key, NONCE, cipher mode, or other necessary information at that moment. Then start or ignore the decryption.

RX OK interrupts (RXIF)

This interrupt is issued when an available packet is received in the RXFIFO. An available packet means that it passes the RXMAC filter, which includes a FCS check, PANID/address filtering, packet type, or promiscuous/error mode.

TX normal FIFO release interrupts (TXNIF)

This interrupt can be issued in the two possible conditions. The conditions are when a packet in normal FIFO is triggered and sent successfully. The other condition is when the packet is triggered and the retransmission is timed out. The register SREG0x24 [0] indicates the TX normal FIFO release status.

The interrupt events are indicated in the short register SREG0x31. The register is 'read-to-clear'. Each of the eight interrupts can be masked by setting the short register SREG0x32 (INTMSK).

3.8. Registers and FIFOs

The registers and FIFOs of the UM2455 can be accessed by either the SPI or the I^2C interfaces. They are divided into two address spaces. One is the short address space, and the other is the long address space.

3.8.1. Register Summary

Short Registers

Table 13. Short Address Register List

Address	File Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR
0x00	RXMCR	--		NOACKRSP	--	PANCOORD	COORD	ERRPKT	PROMI	–0- 0000
0x01	PANIDL	PANIDL								0000 0000
0x02	PANIDH	PANIDH								0000 0000

0x03	SADRL	SADRL							0000 0000
0x04	SADRH	SADRH							0000 0000
0x05	EADR0	EADR0							0000 0000
0x06	EADR1	EADR1							0000 0000
0x07	EADR2	EADR2							0000 0000
0x08	EADR3	EADR3							0000 0000
0x09	EADR4	EADR4							0000 0000
0x0A	EADR5	EADR5							0000 0000
0x0B	EADR6	EADR6							0000 0000
0x0C	EADR7	EADR7							0000 0000
0x0D	RXFLUSH	--	WAKEPOL	WAKEPAD	--	ONLYCMD	ONLYDATA	ONLYBCN	RXFLUSH	-000 0000
0x10	ORDER	BO				SO				1111 1111
0x11	TXMCR	NOCSMA	--	SLOTTED	MACMINBE		CSMABF			0001 1100
0x18	FIFOEN	FIFOEN	--	TXONTS			TXONT			1-00 1000
0x1A	TXBCNTRIG	--						TXBCNSECEN	TXBCNTRIG	---- --00
0x1B	TXNTRIG	--			PENDACK	INDIRECT	TXNACKREQ	TXNSECEN	TXNTRIG	---- -000
0x22	WAKECTL	IMMWAKE	REGWAKE	--						00-- ----
0x24	TXSR	TXRETRY		CCAFAIL					TXNS	0000 0000
0x25	TXBCN MSK	TXBCN MSK	--							0--- ----
0x28	HSYMTMR0	HSYMTMR0								0000 0000
0x29	HSYMTMR1	HSYMTMR1								0000 0000
0x2A	SOFTRST	--					RSTPWR	RSTBB	RSTMAC	---- -0--
0x2C	SECCR0	SECIGNORE	SECSTART	RXCIPHER			TXNCIPHER			0000 0000
0x2D	SECCR1	--	TXBCIPHER			SNIFMODE	--	DISDEC	DISENC	-000 --00
0x2E	TXPEMISP	TXPET				MISP				0111 0101
0x30	RXSR	--	UPSECERR	BATIND	--					-00- ----
0x31	ISRSTS	SLPIF	WAKEIF	HSYMTMRIF	SECIF	RXIF			TXNIF	0000 0000
0x32	INT MSK	SLP MSK	WAKE MSK	HSYMTMR MSK	SEC MSK	RX MSK			TXN MSK	1111 1111
0x33	GPIO	--		GPIQ5	GPIQ4	GPIQ3	GPIQ2	GPIQ1	GPIQ0	--00 0000
0x34	SPIGPIO	SPIMODE		GPDIR5	GPDIR4	GPDIR3	GPDIR2	GPDIR1	GPDIR0	0000 0000
0x35	SLPACK	SLPACK	WAKECNT							0000 0000
0x36	RFCTL	20MOFF	--		WAKECNTEXT		RFRESET	--		0--0 00--
0x37	SECCR2	UPDEC	UPENC							0000 0000
0x38	BBREG0	--							TURBO	---- ---0
0x3A	BBREG2	CCAMODE		CCATH			--			0100 10--
0x3B	BBREG3	PREVALIDTH				PREDETTH			--	1101 100-
0x3C	BBREG2	CSTH			PRECNT			TXDACEDGE	RXADCEDGE	1001 1100
0x3E	BBREG6	RSSIMODE1	RSSIMODE2	--					RSSIRDY	00-- ---1
0x3F	BBREG7	RSSITHCCA								0000 0000

Long Registers

Table 14. Long Address Register List

Address	File Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR
0x200	RFCTRL0	CHANNEL				RFOPT				0000 0000
0x202	RFCTRL2	RFPLL	RSSIDC		RSSISLOPE		--			0000 0---
0x203	RFCTRL3	TXPOWL		TXPOWF			--			0000 0---
0x205	RFCTRL5	BATTH				--				0000 ----
0x206	RFCTRL6	TXFIL	--	20MRECVR		BATMONEN	--			0-00 0---
0x207	RFCTRL7	SLPCLK		--				CLKDIV		00-- --00
0x208	RFCTRL8	--			RFVCO	--			CLKOUTSRC	---0 ---0
0x209	SLPCAL1	SLPCAL1								0000 0000
0x20A	SLPCAL2	SLPCAL2								0000 0000
0x20B	SLPCAL3	CALRDY	--		CALEN	SLPCAL3				0--0 0000
0x211	CLKIRQCR	--						IRQPOL	CLK32KOFF	---- --00
0x220	SCLKDIV	I2CWDTEN	--	CLKOUTEN	SCLKDIV					0-00 0000
0x222	WAKETIMEL	WAKETIMEL								0000 1010
0x223	WAKETIMEH	--					WAKETIMEH			---- -000
0x224	TXREMCNTL	TXREMCNTL								0000 0000
0x225	TXREMCNTH	TXREMCNTH								0000 0000
0x226	TXMAINCNT0	TXMAINCNT0								0000 0000
0x227	TXMAINCNT1	TXMAINCNT1								0000 0000
0x228	TXMAINCNT2	TXMAINCNT2								0000 0000
0x229	TXMAINCNT3	STARTCNT	TXMAINCNT3							0000 0000
0x22F	TESTMODE	--			RSSIWAIT		TESTMODE			---0 1000
0x230	ASSOEADR0	ASSOEADR0								0000 0000
0x231	ASSOEADR1	ASSOEADR1								0000 0000
0x232	ASSOEADR2	ASSOEADR2								0000 0000
0x233	ASSOEADR3	ASSOEADR3								0000 0000
0x234	ASSOEADR4	ASSOEADR4								0000 0000
0x235	ASSOEADR5	ASSOEADR5								0000 0000
0x236	ASSOEADR6	ASSOEADR6								0000 0000
0x237	ASSOEADR7	ASSOEADR7								0000 0000
0x238	ASSOSADR0	ASSOSADR0								0000 0000
0x239	ASSOSADR1	ASSOSADR1								0000 0000
0x240 | 0x24C	UPNONCE									

3.8.2. Security Buffers

Security buffer stores the security keys. These keys will be needed for secured data packet transferring.

Table 15. Security Buffer Mapping

Address	Description
280h ~ 28Fh	TX normal FIFO key
2B0h ~ 2BFh	RX FIFO key

3.8.3. Interrupt Configuration

The UM2455 issues the hardware interrupt via pin 12 to MCU host. There are two related registers that need to be set correctly with respect to a designer's application. The interrupt status can be read from the short register SREG0x31 (ISRSTS). The interrupt is by default sent to the MCU host as a falling edge signal. The interrupt should be configured in the step 2 of the initialization procedure by setting the short register SREG0x32 (INTMSK) whose description is omitted here. All the interrupts are masked (disabled) by default.

Address mode	Addr	Register Name	Descriptions
SREG	0x31	ISRSTS	Interrupt status
SREG	0x32	INT MSK	Interrupt masks
LREG	0x211	CLKIRQCR	Interrupt polarity configuration register

SREG0x31 ISRSTS

SREG0x31, ISRSTS							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
SLPIF	WAKEIF	HSYMTMRIF	SECIF	RXIF	Reserved	Reserved	TXNIF
RC-0	RC-0	RC-0	RC-0	RC-0			RC-0

Bit 7 **SLPIF**: Sleep alert interrupt bit
0: Otherwise
1: Sleep alert interrupt occurred

Bit 6 **WAKEIF**: Wake-up alert interrupt bit
0: Otherwise
1: Wake-up interrupt occurred

Bit 5 **HSYMTMRIF**: Half symbol timer interrupt bit
0: Otherwise
1: Half symbol timer interrupt occurred

Bt 4 **SECIF**: Security key request interrupt bit
0: Otherwise
1: Security key request interrupt occurred

Bit 3 **RXIF**: RX receive interrupt bit
0: Otherwise
1: RX receive interrupt occurred

Bit 0 **TXNIF**: TX Normal FIFO transmission interrupt bit
0: Otherwise
1: TX Normal FIFO transmission interrupt occurred

LREG0x211 CLKIRQCR

LREG0x211, CLKIRQCR							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
Reserved						IRQPOL	CLK32KOFF
--						R/W-0	R/W-0

Bit 1 **IRQPOL**: Interrupt edge polarity bit
0: Falling edge
1: Rising edge

Bit 0 **CLK32KOFF**: SLPCLK disable bit
0: Enable
1: Disable

3.8.4. External Power Amplifier Configuration

Set the long register LREG0x22F to the value '0x0F' to enable the PA function. This register setting enables the PA and RF Switch Control (TX mode or RX mode) which utilizes pin GPIO0, GPIO1, and GPIO2. If the UM2455 is in TX mode, the pin GPIO0 (the external PA enable) and pin GPIO1 (TX mode enable) will be pulled HIGH, and the pin GPIO2 (RX mode enable) will be pulled LOW automatically. If the UM2455 is in RX mode, the pin GPIO0 and pin GPIO1 will be pulled LOW, and the pin GPIO2 will be pulled HIGH automatically. That is, it automatically changes the status of the external PA and the TX/RX branch corresponding to TX or RX modes of the UM2455.

- TX mode: GPIO0 HIGH, GPIO1 HIGH, GPIO2 LOW
- RX mode: GPIO0 LOW, GPIO1 LOW, GPIO2 HIGH

LREG0x22F TESTMODE

LREG0x22F, TESTMODE							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
Reserved			RSSIWAIT		TESTMODE		
			R/W-0b01		R/W-000		

Bit 4-3 **RSSIWAIT**: RSSI state machine parameter.
0b01 is the optimized value.

Bit 2-0 **TESTMODE**: the UM2455 test mode using GPIO pins
0b101: Single-tone test mode.
0b111: GPIO0, GPIO1, GPIO2 are configured to control an external PA, a LNA or a switch as discussed above.

3.8.5. Low speed and High speed Configuration

The UM2455 provides either high speed of 625kbps or low speed of 250kbps for the data transmission. To enable the UM2455 in low speed or high speed mode, the following registers need to be configured as below.

Address mode	Addr	Register Name	Descriptions	Setting Value(hex)
SREG	0x38	BBREG0	Enable high speed mode	0x01
SREG	0x3B	BBREG3	Configure baseband circuit	0x38
SREG	0x3C	BBREG4	Configure baseband circuit	0x5C

SREG0x38 BBREG0

SREG0x38, BBREG0							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
Reserved							High speed
Reserved							R/W-0

Bit 0 **Bit 0 speed select**: enable the 625kbps high speed mode of the UM2455
1: high speed mode
0: low speed mode

SREG0x3B BBREG3

SREG0x3B, BBREG3							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
PREVALIDTH				PREDETTH			Reserved
R/W-1101				R/W-100			

Bit 7-4 **PREVALIDTH**: Baseband decoder parameter
1101: Low speed mode (250kbps) optimized value
0011: High speed mode (625kbps) optimized value
Do not use other values

Bit 3-1 **PREDETTH**: Baseband decoder parameter
100 is the optimized value for both the low speed and high speed

SREG0x3C BBREG4

SREG0x3C, BBREG4							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
CSTH			PRECNT			TXDACEDGE	RXADCEDGE
R/W-100			R/W-111			R/W-0	R/W-0

Bit 7-5 **CSTH**: Baseband decoder parameter.
100: Low speed mode (250kbps) optimized value
010: High speed mode (625kbps) optimized value
Do not use other values

Bit 4-2 **PRECNT**: Baseband decoder parameter
'111' is the optimized value for both low speed and high speed mode

Bit 1 **TXDACEDGE**: Tx DAC latches time selection.

1: DAC latches I/Q data at the negative edge of the clock.
0: DAC latches I/Q data at the positive edge of the clock.

Bit 0 **RXADCEDGE**: Rx ADC latch time selection
1: ADC value is latched at the negative edge of the clock.
0: ADC value is latched at the positive edge of the clock.

3.9. TX / RX operation

3.9.1. Initialization

After the UM2455 is powered up, some registers need to be configured before the data transmission or reception. The procedure is described as below.

Step 1.
Perform software reset by writing the value '0x07' to the short register SREG0x2A.

Address mode	Addr	Register Name	Descriptions	Setting Value(hex)
SREG	0x2A	SOFTRST	Software reset	0x07

SREG0x2A SOFTRST

SREG0x2A, SOFTRST							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
Reserved					RSTPWR	RSTBB	RSTMAC
					WT-0	WT-0	WT-0

Bit 2 **RSTPWR**: Power management reset
Write the value '1' to perform reset.
Bit 1 **RSTBB**: Baseband reset
Write the value '1' to perform reset.
Bit 0 **RSTMAC**: MAC reset
Write the value '1' to perform reset.

Step 2.
Set the registers according to the following table.

Address mode	Addr	Register Name	Descriptions	Setting Value(hex)
SREG	0x3A	BBREG2	Reserved	0x80
SREG	0x3E	BBREG6	Append RSSI value in Rx packets	0x40
SREG	0x3F	RSSIYHCCA	Reserved	0x60
SREG	0x18	FIFOEN	Increase TXON time	0x98
SREG	0x2E	TXPEMISP	VCO calibration period	0x95
SREG	0x35	SLPACK	20 MHz clock recovery time	0x5F
LREG	0x202	RFCTL2	RF optimized control	0x80

LREG	0x206	RFCTL6	RF optimized control	0x90
LREG	0x207	RFCTL7	RF optimized control	0x80
LREG	0x208	RFCTL8	RF optimized control	0x10
LREG	0x220	SCLKDIV	sleep clock frequency control	0x01
SREG	0x32	INT MSK	Enable all interrupts	0x00

SREG0x3A BBREG2

SREG0x3A, BBREG2							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
CCAMODE		CCATH				Reserved	
R/W-0b01		0b0010					

Bit 7-6 **CCAMODE**: CCA mode selection
0b00: Reserved
0b01: Carrier sense (CS) mode, which detects standardized O-QPSK/DSSS signals
0b10: Energy detection (ED) mode, which detects in-band signals
0b11: Combination of carrier sense mode and energy detection mode

SREG0x3E BBREG6

SREG0x3E, BBREG6							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
RSSIMODE1	RSSIMODE2	Reserved					RSSIRDY
WT-0	R/W-0						R-1

Bit 7 **RSSIMODE1**: RSSI mode 1 enable
1: Calculate RSSI for the firmware request, and it will be clear to the value '0' when RSSI calculation is finished.

Bit 6 **RSSIMODE2**: RSSI mode 2 enable
1: Calculate RSSI for each received packet, and the RSSI value will be stored in the RXFIFO.
0: No RSSI calculation for a received packet.

Bit 0 **RSSIRDY**: RSSI ready signal for **RSSIMODE1** use
If **RSSIMODE1** is set, this bit will be cleared to the value '0' until RSSI calculation is done. When RSSI calculation is finished and the RSSI value is ready, this bit will be set to the value '1' automatically.

SREG0x3F BBREG7

SREG0x3F, BBREG7							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
RSSITHCCA							
R/W-0x0							

Bit 7-0 **RSSITHCCA**: CCA-ED threshold

Note: If the in-band signal strength is larger than the threshold, the channel is busy. The 8-bit value can be

mapped to a certain power level according to Appendix A.

SREG0x18 FIFOEN

SREG0x18, FIFOEN							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
FIFOEN	Reserved	TXONTS				TXONT	
R/W-1		R/W-0x2				R/W-0x0	

Bit 7 **FIFOEN**: The TXFIFO and RXFIFO output enables manual control
1: The TXFIFO and RXFIFO are always output enabled.
0: The enabled signal for the TXFIFO and RXFIFO output is controlled by the internal state machine.

Bit 5-2 **TXONTS**: The number of the symbols before the TX. The minimum value is '1'.

Bit 1-0 **TXONT**: The period when the counter 'rfmode1' is active before the TX.

SREG0x2E TXPEMISP

SREG0x2E, TXPEMISP							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
TXPET				MISP			
R/W-0111				R/W-0101			

Bit 7-4 **TXPET**: For VCO circuit calibration.

Bit 3-0 **MISP**: For CSMA-CA calibration.

The recommend value for the register TXPEMISP is '0x95'. Please do not use other values for this register.

SREG0x35 SLPACK

SREG0x35, SLPACK							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
SLPACK	WAKECNT						
WT-0	R/W-0000000						

Bit 7 **SLPACK**: Sleep acknowledgement. Setting this bit to the value '1' will cause the UM2455 entering sleep mode immediately. This bit will be automatically cleared to the value '0'.

Bit 3-0 **WAKECNT**: System clock (20 MHz) recovery time
Note: In the initial procedure, set **WAKECNT** to '0x5F' to optimize the performance.

LREG0x202 RFCTL2

LREG0x202, RFCTRL2							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
PLLCTL	RSSIDC		RSSISLOPE		Reserved		
R/W-0	R/W-0b00		R/W-0b00				

Bit 7 **PLLCTL**: RF Phase Lock Loop (PLL) control
1: The recommended value for the RF optimization. This needs to be set before the RF transmission and reception.

Bit 6-5 **RSSIDC**: RSSI DC level shift.
Note: The value '0b11' is not allowed.

Bit 4-3 **RSSISLOPE**: RSSI range control.
Note: The value '0b11' is not allowed.

LREG0x206 RFCTL6

LREG0x206, RFCTL6							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TXFIL	Reserved	20MRECVR		BATEN	Reserved		
R/W-0		R/W-0b00		R/W-0			

Bit 7 **TXFIL**: TX filter control
1: The recommended value for the RF optimization.

Bit 5-4 **20MRECVR**: 20 MHz clock recovery time (recovery from sleep) control
10: Less than 1 ms
Otherwise: Less than 3 ms

Bit 3 **BATEN**: Battery monitor enable
1: Battery monitor is enabled.
0: Battery monitor is disabled.

LREG0x207 RFCTL7

LREG0x207, RFCTL7							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
SLPCLK		Reserved				CLKDIV	
R/W-0b00						R/W-0b00	

Bit 7-6 **SLPCLK**: Sleep clock
10: Internal ring oscillator
Otherwise: Do not use other values.

Bit 1-0 **CLKDIV**: The UM2455 output clock frequency selection
00: 2.5 MHz
01: 5 MHz
10: 10 MHz
11: 20 MHz

LREG0x208 RFCTL8

LREG0x208, RFCTL8							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved			RFVCO	Reserved			CLKOUTSRC
			R/W-0				R/W-0

Bit 4 RFVCO: The VCO control. The recommend value is '1'.

Bit 0 CLKOUTSRC: The source of 20 MHz clock output

0: From analog module. Unstable when recovering from sleep mode.

1: From power management module. Stable when recovering from sleep mode.

LREG0x220 SCLKDIV

LREG0x220, SCLKDIV							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
I2CWDTEN	Reserved	CLKOUTEN	SCLKDIV				
R/W-0		R/W-0	R/W-0b00000				

Bit 7 **I2CWDTEN**: I^2C watchdog timer enable

1: Enable

0: Disable

Bit 5 **CLKOUTEN**: the UM2455 clock output enable

1: Enable

0: Disable

Bit 4-0 **SCLKDIV**: Sleep clock division selection.

n: The sleep clock is divided by 2^n before being fed to the logic circuit.

Note: If the internal ring oscillator is used, '0b0001' is the recommended value.

SREG0x32 INT MSK

SREG0x32, INT MSK							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SLP MSK	WAKE MSK	HSYMTMR MSK	SEC MSK	RX MSK	Reserved	Reserved	TXN MSK
R/W-1	R/W-1	R/W-1	R/W-1	R/W-1			R/W-1

Bit 7 **SLP MSK**: Sleep alert interrupt mask

Bit 6 **WAKE MSK**: Wake-up alert interrupt mask

Bit 5 **HSYMTMR MSK**: Half symbol timer interrupt mask

Bit 4 **SEC MSK**: Security interrupt mask

Bit 3 **RX MSK**: RX receive interrupt mask

Bit 0 **TXN MSK**: TX Normal FIFO transmission interrupt mask

1: The interrupt is masked, and hence the INT pin will not change even if an interrupt occurs.

0: The interrupt is not masked.

Step 3.

Reset the RF state machine by setting the short register SREG0x36 (RFCTL) to the value '0x04' and then setting it (RFCTL) to the value '0x00'

Address mode	Addr	Register Name	Descriptions	Setting Value(hex)
SREG	0x36	RFCTL	Reset the RF state machine	0x04
SREG	0x36	RFCTL	Reset the RF state machine	0x00

SREG0x36 RFCTL

SREG0x36, RFCTL							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
20MOFF	Reserved		WAKECNTEXT		RFRST	RFTXMODE	RFRXMODE
R/W-0			R/W-00		R/W-0	R/W-0	R/W-0

Bit 7 **20MOFF**: 20 MHz clock mask off in external wake-up mode without a sleep clock, turn the 20 MHz clock mask off by software. This bit will be cleared automatically.

Bit 4 -3 **WAKECNTEXT**: 20 MHz clock recovery time extension bits

Bit 2 **RFRST**: RF state reset.
Reset RF state. The RF state must be reset in order to change the RF channels.
Write the value '1', and then write the value '0' to accomplish the reset operation.

Bit 1 **RFTXMODE**: An RF is forced into TX mode.

Bit 0 **RFRXMODE**: An RF is forced into RX mode.

Step 4.

Set the RF operation channel. The UM2455 operates in the 2.4 GHz Industry, Scientific, and Medical (ISM) unlicensed band. The operating frequency is divided into 16 channels. If a user wants to select any operating channel, the long register LREG0x200 (RFCTL0) should be configured as the following table.

Address mode	Addr	Register Name	Descriptions	Setting Value(hex)
LREG	0x200	RFCTL0	Set RF operation channel	List as Table 14.

Table 14. RF operation channel settings

Channel Name	Frequency	Register Address	Set Value(hex)
Channel 1	2405 MHz	0x200	02
Channel 2	2410 MHz	0x200	12
Channel 3	2415 MHz	0x200	22
Channel 4	2420 MHz	0x200	32
Channel 5	2425 MHz	0x200	42
Channel 6	2430 MHz	0x200	52
Channel 7	2435 MHz	0x200	62
Channel 8	2440 MHz	0x200	72
Channel 9	2445 MHz	0x200	82
Channel 10	2450 MHz	0x200	92
Channel 11	2455 MHz	0x200	A2
Channel 12	2460 MHz	0x200	B2
Channel 13	2465 MHz	0x200	C2
Channel 14	2470 MHz	0x200	D2
Channel 15	2475 MHz	0x200	E2
Channel 16	2480 MHz	0x200	F2

LREG0x200 RFCTRL0

LREG0x200, RFCTRL0							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
CHANNEL				RFOPT			
R/W-0b0000				R-0b0000			

Bit 7-4 **CHANNEL**: RF channel number.
0b0000: channel 1 (2405 MHz)
0b0001: channel 2 (2410 MHz)
0b0010: channel 3 (2415 MHz)
0b1111: channel 16 (2480 MHz)

Bit 3-0 **RFOPT**: Optimize an RF control.
'0b0010' is the recommended value for the RF optimization.

Step 5.

After the operation channel is set, the RF state machine should be reset by setting the short register SREG0x36 (RFCTL) to the value '0x04' and then setting the short register SREG0x36 (RFCTL) to the value '0x00'.

Address mode	Addr	Register Name	Descriptions	Setting Value(hex)
SREG	0x36	RFCTL	Reset RF state machine	0x04
SREG	0x36	RFCTL	Reset RF state machine	0x00

By finishing all the above five steps, a basic initialization procedure is done. This configuration procedure is valid for most of the application conditions.

3.9.2. Typical TX Operations

The TXMAC inside the UM2455 will automatically generate the preamble and Start-of-Frame delimiter fields when transmitting. Additionally, the TXMAC can generate any padding (if needed) and the CRC, if configured to do so. The MCU host must generate and write all other frame fields into the buffer memory for transmission described as the followings.

3.9.2.1. Transmit Packet in Normal FIFO

To send a packet in normal FIFO, there are several steps to follow:

Step 1.

Fill in Normal FIFO with the packet to send. The FCS or MIC is not necessary. The format is as the following.

Table 17. Normal FIFO Format

LSB			MSB
1 Byte	1 Bytes	N Bytes	N Bytes
Header length	Frame length	Header	Payload

Step 2.

Set an ACKREQ (SREG0x1B [2]) if an acknowledgement from the receiver is required. If the ACKREQ is set, the UM2455 automatically retransmits the packet if there is no acknowledgement sent back. The UM2455 will retransmit the packet till the maximum number of trial times is reached.

Step 3.

Set the trigger bit (SREG0x1B [0]) to send a packet. This bit will be automatically cleared. At this time, the TXMAC will perform an anti-interference mechanism and send the packet at the right moment.

Step 4.

Wait for the interrupt/status (SREG0x31 [0])

Step 5.

If a retransmit is required, check SREG0x24 [0] to see if it is successful. 'Successful' means that the ACK was received. If no retransmission is required, SREG0x31 [0] indicates the packet is transmitted. The number of the retransmission times can be read at SREG0x24 [7:6].

SREG0x1B TXNTRIG

SREG0x1B, TXNTRIG							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
Reserved			PENDACK	INDIRECT	TXNACKREQ	TXNSECEN	TXNTRIG
-			R-0	R/W-0	R/W-0	R/W-0	WT-0

Bit 4 **PENDACK**: Indication of the incoming ACK packet with a pending-bit is set to the value '1'.
Bit 3 **INDIRECT**: Activate indirect transmission – coordinator only.
Bit 2 **TXNACKREQ**: Transmit a packet with an ACK packet expected. If an ACK is not received, the UM2455 will retransmit automatically.
Bit 1 **TXNSECEN**: Transmit a packet which needs to be encrypted.
Bit 0 **TXNTRIG**: Trigger a TXMAC to transmit the packet inside a TX normal FIFO.

SREG0x24 TXSR

SREG0x24, TXSR							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
TXRETRY		Reserved					TXNS
R-0b00							R-0

Bit 7-6 **TXRETRY**: Retry times of the most recent TXNFIFO transmission.
Bit 0 **TXNS**: Normal FIFO release status
1: Fail (retry counts exceed)
0: OK

3.9.2.2. Transmit Packet with Security Encryption

To send a secured packet with a TXFIFO, there are several steps to follow:

Step 1.

Fill in one TXFIFO that you want to send with encryption. The format is the same as the normal FIFO.

Step 2.

Fill in the corresponding key into the memory of the key table.

Normal FIFO key	LREG: 0x280 – 0x28F

Step 3.

Fill in cipher mode.

Normal FIFO cipher mode	SREG0x2C[2:0]

Step 4.

Trigger to encrypt the content in the FIFO and send it.

Normal FIFO:	SREG0x1B[1:0] = '11'

Wait for the FIFO to release the interrupt/status as a plaintext packet does.

SREG0x2C SECCR0

SREG0x2C, SECCR0							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
SECIGNORE	SECSTART	RXCIPHER			TXNCIPHER		
WT-0	WT-0	R/W-0b000			R/W-0b000		

Bit 7 **SECIGNORE**: Set this bit to ignore the decryption process when there is no matching key for the incoming packet.

Bit 6 **SECSTART**: Set this bit to start the decryption process when a matching key is found and written into the security key FIFO.

Bit 5-3 **RXCIPHER**: Select one of the seven cipher modes below for an RX packet in the RXFIFO.

0b000: None
0b001: AES-CTR
0b010: AES-CCM-128
0b011: AES-CCM-64
0b100: AES-CCM-32
0b101: AES-CBC-MAC-128
0b110: AES-CBC-MAC-64
0b111: AES-CBC-MAC-32

Bit 2-0 **TXNCIPHER**: Select one of the seven cipher modes above for a TX packet in the TX normal FIFO. The mode settings are the same as the RXCIPHER.

SREG0x2D SECCR1

SREG0x2D, SECCR1							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
Reserved	Reserve			SNIFMODE	Reserved	DISDEC	DISENC
				R/W-0		R/W-0	R/W-0

Bit 3 **SNIFMODE**: Sniffer mode. Note: Set this bit the value '0' when using the 16-bit half-symbol timer.

Bit 1 **DISDEC**: Disable the decryption process. Even if the 'security' bit in MAC header is detected, the UM2455 does not generate a security interrupt.

Bit 0 **DISENC**: Disable the encryption process. Even if the TX security is enabled, the UM2455 does not encrypt.

SREG0x37 SECCR2

SREG0x37, SECCR2							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
UPDEC	UPENC	Reserved			Reserved		
WT-0	WT-0						

Bit 7 **UPDEC**: Upper security decryption mode. Set this bit when doing the upper decryption using a TX normal FIFO.

Bit 6 **UPENC**: Upper security encryption mode. Set this bit when doing the upper encryption using a TX normal FIFO.

3.9.3. Typical RX Operations

The UM2455 RX PHY filters all incoming signals and tracks the synchronization symbols. When the preamble of a UM2455 packet is found, the packet is demodulated and stored in the RXFIFO. At the same time, the RXMAC starts calculating the frame FCS byte by byte and checking after having received a whole packet.

In normal mode, the RXMAC filters the MAC header and skips those packets not being sent to the device addresses. Note only the lowest 3 bits are used in the filter. Specifically, the address matching the lowest 3 bits will be accepted during the RX process. If the packet is acceptable and needs an acknowledgement, the RXMAC will inform the TXMAC to send an ACK packet automatically. In promiscuous mode, the RXMAC receives all packets with the correct FCS. In error mode, the RXMAC will receive all packets.

3.9.3.1. Receive Packet in RXFIFO

LSB					MSB
1 Byte	N Byte	N Bytes	2 Byte	1 Byte	1 Byte
Frame length	Header	Payload	FCS	LQI	RSSI

In the above table, the field 'Frame length' (in bytes) includes the lengths of the header, the payload, and FCS (2 bytes), but it does not include LQI (1 byte) and RSSI (1 byte). When a packet passes the baseband filtering (preamble and delimiter), it goes into the RXMAC. The RXMAC performs several levels of the packet filtering. Default mode is address-recognition mode, which can filter those packets not being sent to this device and/or others. Promiscuous mode will receive all packets with a successful FCS. Error mode will receive all packets passing the baseband filtering (the register SREG0x00 [1:0]). The RXMAC can further filter 'Command Only' and 'Data Only' packets at the register SREG0x0D [3:1]. When a received packet passes the filters discussed

above and has the correct FCS, an 'RXOK interrupt' is issued at SREG0x31 [3]. MCU host can read the whole packet inside the RXFIFO. The RXFIFO is flushed when the first and the last byte of the received packet are read or the host triggers an 'RX flush' at the register SREG0x0D [0].

3.9.3.2. Receive Packet with Security Decryption

Configuring the UM2455 to receive and decrypting a ciphered packet can be done by the following steps:

Step 1.

When a packet comes with the security enabled bit set in the frame control field of the packet header, a security interrupt (the register SREG0x31 [4]) is issued right after the complete packet header is received. The security interrupt indicates MCU host that the coming packet needs to be properly deciphered. Then MCU host should perform the key searching and fill in the key table in the RXFIFO register.

RXFIFO key	LREG: 0x2B0 – 0x2BF

Besides setting the RXFIFO key, MCU host should also perform the cipher mode decision and set the corresponding cipher mode in the register SREG0x2C [5:3].

Step 2.

After both key and cipher modes are set, the security engine should be configured and enabled by properly setting SREG0x2C. If the RXFIFO key does not match with the received packet, the following decryption process should be disabled by setting the short register SREG0x2C [7] (SECIGNORE). Security engine can be enabled by setting the short register SREG0x2C [6] (SECSTART).

Step 3.

After the packet is successfully decrypted, an RX interrupt is issued to MCU host to notify that the whole process of receiving and decryption has been done correctly.

SREG0x2C SECCR0

SREG0x2C, SECCR0							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
SECIGNORE	SECSTART	RXCIPHER			TXNCIPHER		
WT-0	WT-0	R/W-0			R/W-0		

Bit 7 **SECIGNORE**: Set this bit to ignore the decryption process when there is no matching key that can be found for the incoming packet.

Bit 6 **SECSTART**: Set this bit to start the decryption process when a matching key is found and write into the security key FIFO.

Bit 5-3 **RXCIPHER**: Select one of the seven cipher modes below for an RX packet in the RXFIFO.
0x0: None
0x1: AES-CTR
0x2: AES-CCM-128
0x3: AES-CCM-64

0x4: AES-CCM-32
0x5: AES-CBC-MAC-128
0x6: AES-CBC-MAC-64
0x7: AES-CBC-MAC-32

Bit 2-0 **TXNCIPHER**: Select one of the seven cipher modes for a TX packet in the TX normal FIFO. The mode settings are the same as those for RXCIPHER.

3.10. Option

3.10.1. Power Saving Mode Operations

Please refer to Section 3.4 Power Management for detailed descriptions. The following provides an example setting for normal modes:

3.10.2. Power Saving for normal mode

For a coordinator or device to sleep for 5 ms and then wake-up:

5(ms) = 163 * 30.517(us) (when sleep clock = 32.768K) + 515*50(ns) (System clock = 20 MHz)
So we have the Main-counter = 163(0xA3), Remain-counter = 515(0x203).

Step 1.
Set main counter, remain counter, and WAKECNT

- LREG0x224 = 0x03: remain counter[7:0]
- LREG0x225 = 0x02: remain counter[9:8]
- LREG0x226 = 0xA3: main counter[7:0]
- LREG0x227 = 0x00: main counter[15:8]
- LREG0x228 = 0x00: main counter[23:16]
- {SREG0x36[4:3], SREG0x35[6:0]} = 0x41: WAKECNT (For the main clock to wake-up and be stable, set to 2 ms in this case)

Step 2.
Set SLPACK to put a coordinator/device to sleep.

- LREG0x229[7] = 1: put a device/coordinator to sleep

3.10.3. External Wake-up Mode

There are three modes for external wake-up. One is waken by the external pin triggering, another is waken by the register triggering, and the other is by the software reset.
The register SREG0x22 [7] controls the mode switch: '1' (external pin), '0' (register).

SREG0x22 WAKECTL

SREG0x22, WAKECTL							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
IMMWAKE	REGWAKE	Reserved					

R/W-0	R/W-0	

Bit 7 **IMMWAKE**: Immediate wake-up mode enable.

Bit 6 **REGWAKE**: Register-triggered wake-up signal. It should be cleared to the value '0' by MCU host.

Waken by External Pin

Step 1.

Configure pin 15 (WAKE),

- SREG0x22 [7] = 0x1: set to wake-up mode of an external pin.
- SREG0x0D [6] = 0x1: set the polarity of WAKE signal.
- SREG0x0D [5] = 0x1: turn on the pad of WAKE pin.

Step 2.

<Put a device to sleep according to Section 3.10.3

Waken by Register

Step 1.

Configure the register.

- SREG0x22 [7] = 0x0: set the register to wake up mode.

Step 2.

<Put device to sleep according to Section 3.10.3

Step 3.

- SREG0x22 [6] = 0x1: wake up device. Note that the short address can be accessed during sleep mode.
- SREG0x22 [6] = 0x0: clear the value of this bit to release a wake-up event.

Waken by Software Reset

Step 1.

Set wake-up mode.

- SREG0x22 [7] = 0x0: set the register to wake up mode.

Step 2.

<Put a device to sleep according to Section 3.10.3

Step 3.

- SREG0x2A[2] = 0x1; No need for the SW release

3.10.4. Battery Monitor Operations

Step 1.

Set the threshold value of the battery monitor at the register LREG0x205 [7:4].

Step 2.

Enable the battery monitor by setting the register LREG0x206 [3] to the value '1'.

Step 3.

Read the battery-low indicator at the register SREG0x30 [5]. If this bit is set, it means that the supply voltage is lower than the threshold.

LREG0x205 RFCTRL5

LREG0x205, RFCTRL5							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
BATTH				Reserved			
R/W-0b000				-			

Bit 7-4 **BATTH**: Battery monitor threshold value corresponding to the voltage supply

0b1110: 3.5V
0b1101: 3.3V
0b1100: 3.2V
0b1011: 3.1V
0b1010: 2.8V
0b1001: 2.7V
0b1000: 2.6V
0b0111: 2.5V
Other: out of the operation voltage

3.11. Upper Cipher Encryption and Decryption Operations

3.11.1. Upper Cipher Encryption

User the TXNFIFO to perform the upper cipher encryption:

Step 1.

Fill in the TXNFIFO with the following format:

LSB			MSB
1 Byte	1 Bytes	N Bytes	N Bytes
Header length	Frame length	Header	Payload

Step 2. Write NONCE (13 bytes) at LREG0x240~0x24C.

Step 3.

Set the register SREG0x37 [6] = '1'.

Step 4.

Set TXNFIFO security key.

Step 5.

Set the cipher mode of TXNFIFO at the register SREG0x2C [2:0].

Step 6.

Trigger TXNFIFO to send by setting the register SREG0x1B [0].

Step 7

Check ISRSTS (SREG0x31 [0] ='1') and TXSR (SREG0x24 [0] ='0'), which means the ciphering is done.

Step 8.

Read back TXNFIFO to get the result.

3.11.2. Upper Cipher Decryption

Use TXNFIFO to perform the upper cipher decryption:

Step 1.

Fill in TXNFIFO with the following format

LSB			MSB
1 Byte	1 Bytes	N Bytes	N Bytes
Header length	Frame length	Header	Payload

Step 2.

Write NONCE (13 bytes) at LREG0x240~0x24C.

Step 3.

Set the register SREG0x37 [7] = '1'.

Step 4.

Set TXNFIFO security key.

Step 5.

Set the cipher mode of TXNFIFO at the register SREG0x2C [2:0].

Step 6.

Trigger TXNFIFO to send by setting the register SREG0x1B [0].

Step 7.

Check ISRSTS (SREG0x31 [0] ='1') and TXSR (SREG0x24 [0] ='0'), which means the ciphering is done.

Step 8.

Read back TXNFIFO to get the result.

Step 9.

Check the value of the short register SREG0x30 [6] (RXSR) for the MIC check error. If the value is '0', then it's ok.

SREG0x37 SECCR2

SREG0x37, SECCR2							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
UPDEC	UPENC	Reserved			Reserved		
WT-0	WT-0						

Bit 7 **UPDEC**: Upper security decryption mode. Set this bit when doing the upper decryption using TX normal FIFO.

Bit 6 **UPENC**: Upper security encryption mode. Set this bit when doing the upper encryption using TX normal FIFO.

SREG0x2C SECCR0

SREG0x2C, SECCR0							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
SECIGNORE	SECSTART	RXCIPHER			TXNCIPHER		
WT-0	WT-0	R/W-0			R/W-0		

Bit 7 **SECIGNORE**: Set this bit to ignore the decryption process when there is no matching key for the incoming packet.

Bit 6 **SECSTART**: Set this bit to start the decryption process when a matching key is found and write into a security key FIFO.

Bit 5-3 **RXCIPHER**: Select one of the seven cipher modes below for an RX packet in the RXFIFO.
0x0: None
0x1: AES-CTR
0x2: AES-CCM-128
0x3: AES-CCM-64
0x4: AES-CCM-32
0x5: AES-CBC-MAC-128
0x6: AES-CBC-MAC-64
0x7: AES-CBC-MAC-32

Bit 2-0 **TXNCIPHER**: Select one of the seven cipher modes for a TX packet in a TX normal FIFO. The mode settings are the same as RXCIPHER.

LREG0x240-0x24C Upper Nonce

LREG0x240-0x24C, Upper Nonce							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
UPNONCE – 13 bytes							
R/W-0							

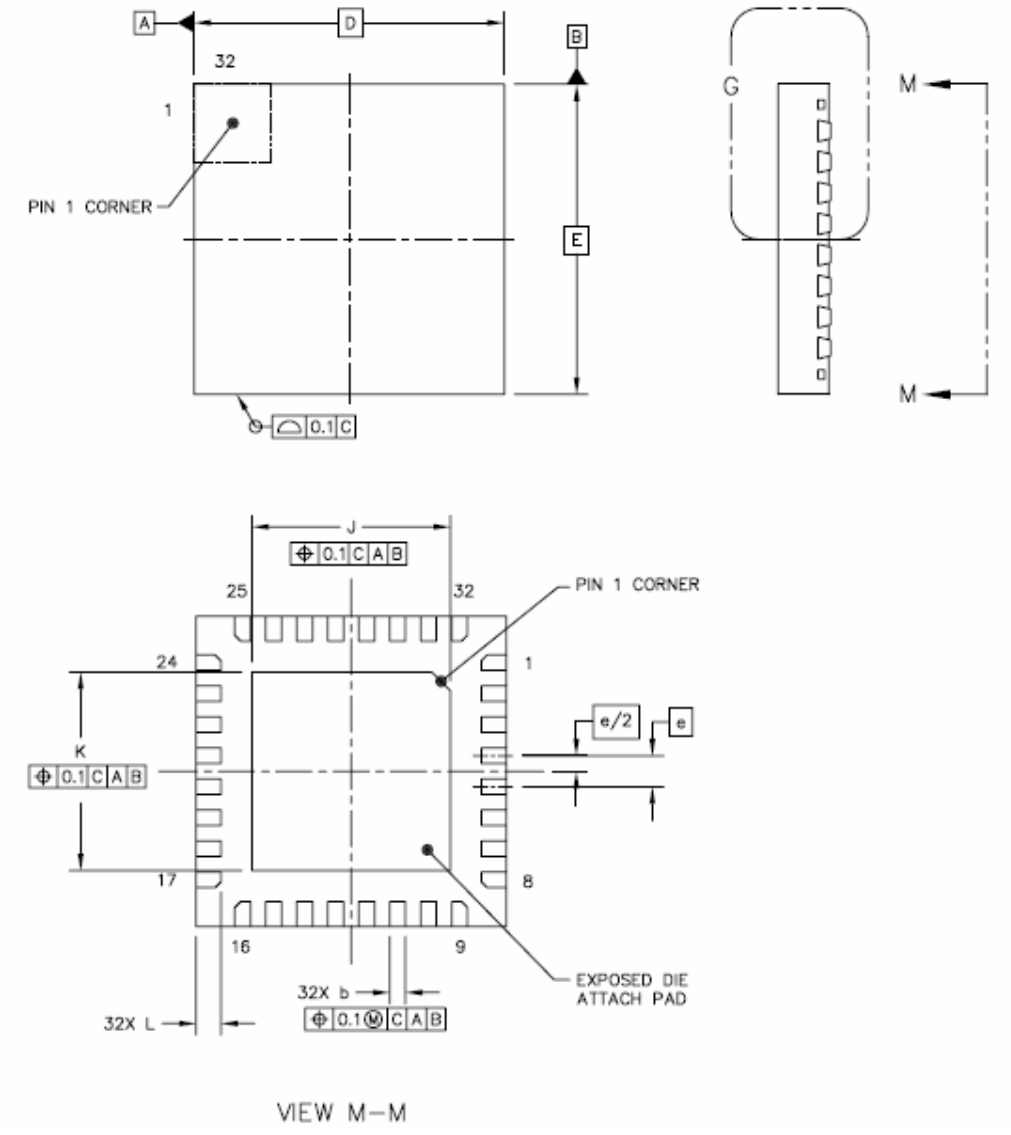
Bit 7-0 **UPNONCE**: Set the 13-byte NONCE field of CCM/CCM* protocol. Generally speaking, these fields should be provided by a key management protocol of the upper layer (i.e. network/application).

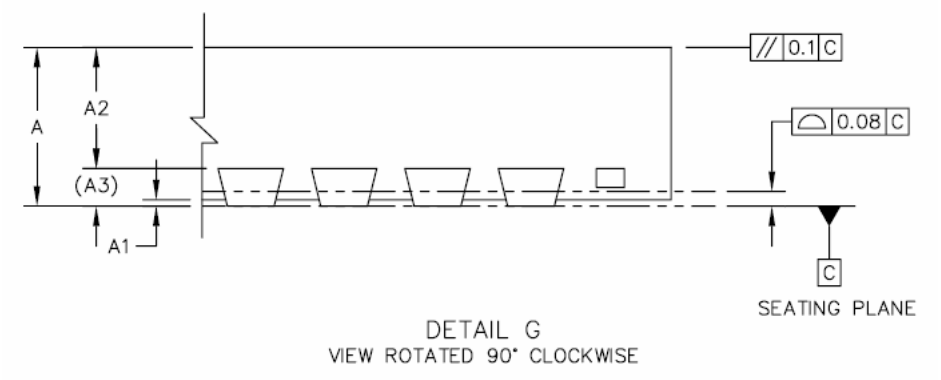
4. Package Information

4.1. Package Drawing

The QFN-32 package outline is given below.

QFN-32, 5x5mm²





DIM	MIN	NOM	MAX	NOTES
A	0.8	0.85	0.9	1.0 Coplanarity applies to Leads,
A1	0	0.035	0.05	corner leads, and die attach pad.
A2	---	0.65	0.67	
A3		0.203 REF		
b	0.2	0.25	0.3	
D		5 BSC		
E		5 BSC		
e		0.5 BSC		
J	3.1	3.2	3.3	
K	3.1	3.2	3.3	
L	0.35	0.4	0.45	

4.2. Package Soldering

4.2.1. Background

The UM2455 is housed in a small 32-pin lead-free QFN 5x5mm^2 package. The packaged part passed the Level 3 pre-condition testing.

4.2.2. Reference Reflow Temperature Curve

Figure 15 is a reference temperature curve for the SMD package IR reflow. Different equipment may have different optimized reflow conditions. The user may need to modify the reflow profile to suit the particular equipment used in order to maximize the yield.

Pb-free SMD Package IR Reflow Profile

Step#	Profile Feature	Condition / Duration
Step 1	Ramp-up rate	1.5-3℃ /sec
Step 2	Preheat : 150~ 200℃ (Ta-Tb)	t1-t2: 60~80 sec
Step 3	Ramp-up rate (T_L to T_P)	1.5-3℃ /sec
	Temperature maintained above 220℃ (T_L)	t_L : 80~150 sec
Step 4	Peak temperature (T_P)	260+0/-5℃
	Time within 5℃ of the actual peak temperature	30±10 sec
Step 5	Ramp-down rate	6℃/sec. Max.
Note1 Subject the samples to 3 cycles of the above defined reflow conditions. Note2 Time 25℃ to peak temperature: 8 minutes maximum. Note3 The time between reflows shall be 5 minutes minimum and 60 minutes maximum.		

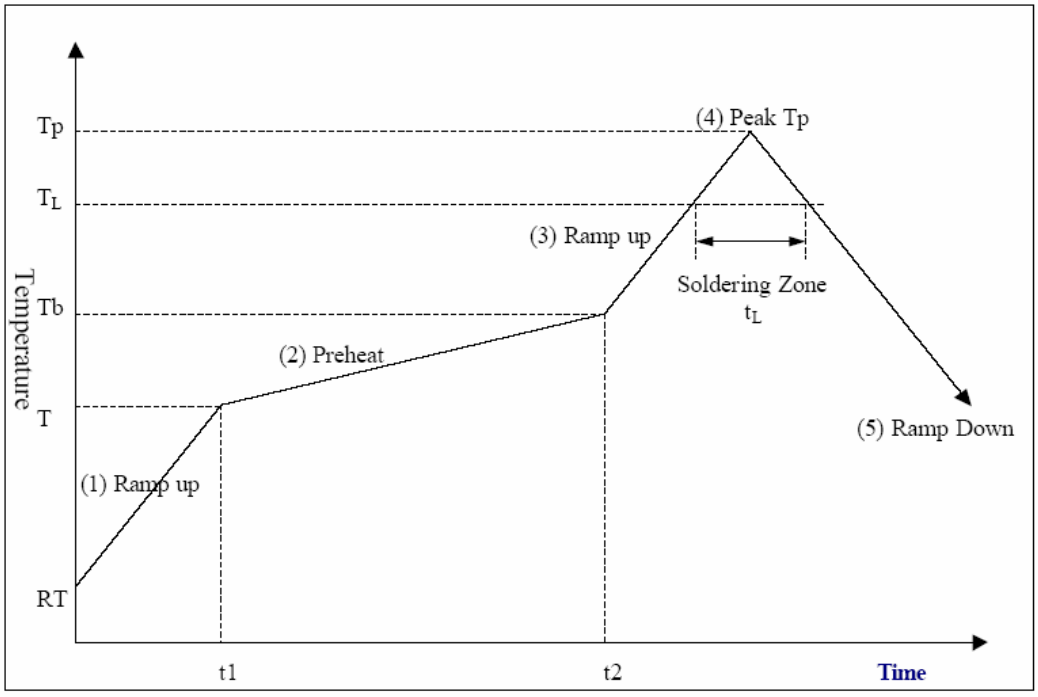


Figure 15. Reference SMD Package IR Reflow Profile

Appendix A. RSSI mapping table

RSSI Vs. Input Power

Input Power (dBm)	RSSI(hex)	Input Power (dBm)	RSSI(hex)	Input Power (dBm)	RSSI(hex)
-100	00	-73	49	-46	D4
-99	00	-72	4E	-45	D8
-98	00	-71	53	-44	DD
-97	00	-70	59	-43	E1
-96	00	-69	5F	-42	E4
-95	00	-68	64	-41	E9
-94	00	-67	6B	-40	EF
-93	00	-66	6F	-39	F5
-92	00	-65	75	-38	FA
-91	00	-64	79	-37	FD
-90	00	-63	7D	-36	FE
-89	01	-62	81	-35	FF
-88	02	-61	85	-34	FF
-87	05	-60	8A	-33	FF
-86	09	-59	8F	-32	FF
-85	0D	-58	94	-31	FF
-84	12	-57	99	-30	FF
-83	17	-56	9F	-29	FF
-82	1B	-55	A5	-28	FF
-81	20	-54	AA	-27	FF
-80	25	-53	B0	-26	FF
-79	2B	-52	B7	-25	FF
-78	30	-51	BC	-24	FF
-77	35	-50	C1	-23	FF
-76	3A	-49	C6	-22	FF
-75	3F	-48	CB	-21	FF
-74	44	-47	CF	-20	FF

RSSI is used to report the signal strength of a received packet. The UM2455 attaches RSSI value following a received packet in the RXFIFO every time a packet is received successfully.

Appendix B. TX Power Configuration

Default output power is 0dBm. Summation of 'large' and 'small' tuning decreases the output power.

LREG0x203 RFCTL3

LREG0x203, RFCTRL3							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
TXPOWL		TXPOWF			Reserved		
R/W-0b00		R/W-0b000					

Bit 7-6 **TXPOWL**: Large scale control for TX power in dB
0b00: 0 dB
0b01: -10 dB
0b10: -20 dB
0b11: -30 dB

Bit 5-3 **TXPOWF**: Fine scale control for the TX power in dB
0b000: 0 dB
0b001: -0.5 dB
0b010: -1.2 dB
0b011: -1.9 dB
0b100: -2.8 dB
0b101: -3.7 dB
0b110: -4.9 dB
0b111: -6.3 dB

Appendix C. Register Descriptions

Register Types

Register Type	Description
R/W	Read/Write register
WT	Write to trigger register, automatically cleared by hardware
RC	Read to clear register
R	Read-only register
R/W1C	Read/Write '1' to clear register

C.1 Short Registers (SREG0x00~SREG0x3F)

SREG0x00 RXMCR

SREG0x00, RXMCR							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
Reserved		NOACKRSP	Reserved	PANCOORD	COORD	ERRPKT	PROMI
		R/W-0		R/W-0	R/W-0	R/W-0	R/W-0

Bit 5 **NOACKRSP**: Disable automatic acknowledgement response.
0: Otherwise
1: Disable automatic acknowledgement
Bit 3 **PANCOORD**: Set the device as a PAN Coordinator.
Bit 2 **COORD**: Set the device as a Coordinator.
Bit 1 **ERRPKT**: Accept all kinds of packets including CRC errors.
Bit 0 **PROMI**: Accept all kinds of packets with CRC OKs.

SREG0x01 PANIDL

SREG0x01, PANIDL							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
PANIDL							
R/W-0x00							

Bit 7-0 **PANIDL**: PAN address [7:0] of the device.

SREG0x02 PANIDH

SREG0x02, PANIDH							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
PANIDH							
R/W-0x00							

Bit 7-0 **PANIDH**: PAN address [15:8] of the device.

SREG0x03 SADRL

SREG0x03, SADRL							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
SADRL							
R/W-0x00							

Bit 7-0 **SADRL**: The 16-bit short address [7:0] of the device. The RXMAC only matches the lower 3 bits.

SREG0x04 SADRH

SREG0x04, SADRH							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
SADRH							
R/W-0x00							

Bit 7-0 **SADRH**: The 16-bit short address [15:8] of the device. The RXMAC does not filter according to this register.

SREG0x05 EADR0

SREG0x05, EADR0							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
EADR0							
R/W-0x00							

Bit 7-0 **EADR0**: The 64-bit extended address [7:0] of the device. The RXMAC only matches the lower 3 bits.

SREG0x06 EADR1

SREG0x06, EADR1							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
EADR1							
R/W-0x00							

Bit 7-0 **EADR1**: The 64-bit extended address [15:8] of the device. The RXMAC does not filter according to this register.

SREG0x07 EADR2

SREG0x07, EADR2							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
EADR2							
R/W-0x00							

Bit 7-0 **EADR2**: The 64-bit extended address [23:16] of the device. The RXMAC does not filter according

to this register.

SREG0x08 EADR3

SREG0x08, EADR3							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
EADR3							
R/W-0x00							

Bit 7-0 **EADR3**: The 64-bit extended address [31:24] of the device. The RXMAC does not filter according to this register.

SREG0x09 EADR4

SREG0x09, EADR4							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
EADR4							
R/W-0x00							

Bit 7-0 **EADR4**: The 64-bit extended address [39:32] of the device. The RXMAC does not filter according to this register.

SREG0x0A EADR5

SREG0x0A, EADR5							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
EADR5							
R/W-0x00							

Bit 7-0 **EADR5**: The 64-bit extended address [47:40] of the device. The RXMAC does not filter according to this register. The RXMAC does not filter according to this register.

SREG0x0B EADR6

SREG0x0B, EADR6							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
EADR6							
R/W-0x00							

Bit 7-0 **EADR6**: The 64-bit extended address [55:48] of the device. The RXMAC does not filter according to this register.

SREG0x0C EADR7

SREG0x0C, EADR7							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
EADR7							
R/W-0x00							

Bit 7-0 **EADR7**: The 64-bit extended address [63:56] of the device. The RXMAC does not filter according to this register.

SREG0x0D RXFLUSH

SREG0x0D, RXFLUSH							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
Reserved	WAKEPOL	WAKEPAD	Reserved	ONLYCMD	ONLYDATA	Reserved	RXFLUSH
	R/W-0	R/W-0		R/W-0	R/W-0	Reserved	WT-0

Bit 6 **WAKEPOL**: Set the polarity of WAKE signal.
0: Active low
1: Active high
Bit 5 **WAKEPAD**: Turn on the pad of WAKE pin (pin 11).
Bit 3 **ONLYCMD**: Only a command packet is allowed to receive.
Bit 2 **ONLYDATA**: Only a data packet is allowed to receive.
Bit 1, 4 **Reserved:**
Bit 0 **RXFLUSH**: Flush the RXFIFO. This will not modify the data in the RXFIFO but return pointers to zero. This bit is written to clear.

SREG0x11 TXMCR

SREG0x11, TXMCR							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
NOCSMA	Reserved	SLOTTED	MACMINBE		CSMABF		
R/W-0		R/W-0	0x3		0x4		

Bit 7 **NOCSMA**: No CSMA-CA algorithm when transmitting in non-slotted mode with SREG0x21 [1] set.
Bit 5 **SLOTTED**: Enable slotted mode.
Bit 4-3 **MACMINBE**: The minimum value of a back-off exponent of the anti-interference algorithm
Bit 2-0 **CSMABF**: The maximum number of the back-offs.

SREG0x18 FIFOEN

SREG0x18, FIFOEN							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
FIFOEN	Reserved	TXONTS				TXONT	
R/W-1		R/W-0x2				R/W-0x0	

Bit 7 **FIFOEN**: The TXFIFO and the RXFIFO output enable the manual control.
1: The TXFIFO and RXFIFO are always output enabled.
0: The enabled signal for the TXFIFO and RXFIFO output is controlled by the internal state machine.
Bit 5-2 **TXONTS**: The number of the symbols before the TX. The minimum value is '1'.
Bit 1-0 **TXONT**: The period when the counter 'rfmode1' is active before the TX.

SREG0x1A TXTRIG

SREG0x1A, TXTRIG							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
Reserved						TXBCNSECEN	TXBCNTRIG
						R/W-0	WT-0

Bit 1 **TXSECEN**: Security enable
0: Otherwise
1: Enable
Bit 0 **TXTRIG**: Trigger the TXMAC to send the packet in the TX FIFO.

SREG0x1B TXNTRIG

SREG0x1B, TXNTRIG							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
Reserved			PENDACK	INDIRECT	TXNACKREQ	TXNSECEN	TXNTRIG
-			R-0	R/W-0	R/W-0	R/W-0	WT-0

Bit 4 **PENDACK**: Indication of the incoming ACK packet with the pending-bit set to the value '1'.
Bit 3 **INDIRECT**: Activate indirect transmission.
Bit 2 **TXNACKREQ**: Transmit a packet with an ACK request. If the ACK is not received, the UM2455 retransmits.
Bit 1 **TXNSECEN**: Transmit a packet which needs to be encrypted.
Bit 0 **TXNTRIG**: Trigger the TXMAC to transmit the packet inside the TX normal FIFO.

SREG0x22 WAKECTL

SREG0x22, WAKECTL							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
IMMWAKE	REGWAKE	Reserved					
R/W-0	R/W-0						

Bit 7 **IMMWAKE**: Enable immediate wake-up mode.
Bit 6 **REGWAKE**: Register-triggered wake-up signal. It should be cleared to the value '0' by MCU host.

SREG0x24 TXSR

SREG0x24, TXSR							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
TXRETRY		Reserved	Reserved				TXNS
R-0b00		Reserved					R-0

Bit 7-6 **TXRETRY**: Retry times of the most recent TXNFIFO transmission.
Bit 0 **TXNS**: Normal FIFO release status
1: Fail (retry count exceed)
0: OK

SREG0x25 TXBCN MSK

SREG0x25, TXBCN MSK							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
TXBCN MSK	Reserved						
R/W-0							

Bit 7 **TXBCN MSK**: The TX FIFO interrupt mask
1: The interrupt is masked, and hence INT pin will not change even if an interrupt occurs.
0: The interrupt is not masked.

SREG0x2A SOFTRST

SREG0x2A, SOFTRST							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
Reserved					RSTPWR	RSTBB	RSTMAC
					WT-0	WT-0	WT-0

Bit 2 **RSTPWR**: Power management reset
Write the value '1' to perform reset.
Bit 1 **RSTBB**: Baseband reset
Write the value '1' to perform reset.
Bit 0 **RSTMAC**: MAC reset
Write the value '1' to perform reset.

SREG0x2C SECCR0

SREG0x2C, SECCR0							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
SECIGNORE	SECSTART	RXCIPHER			TXNCIPHER		
WT-0	WT-0	R/W-0b000			R/W-0b000		

Bit 7 **SECIGNORE**: Set this bit to ignore the decryption process when there is no matching key for the incoming packet.
Bit 6 **SECSTART**: Set this bit to start the decryption process when a matching key is found and written into the security key FIFO.
Bit 5-3 **RXCIPHER**: Select one of the seven cipher modes below for an RX packet in the RXFIFO.
0b000: None
0b001: AES-CTR
0b010: AES-CCM-128
0b011: AES-CCM-64
0b100: AES-CCM-32
0b101: AES-CBC-MAC-128
0b110: AES-CBC-MAC-64
0b111: AES-CBC-MAC-32

Bit 2-0 **TXNCIPHER**: Select one of the seven cipher modes above for a TX packet in TX normal FIFO. The mode settings are the same as those of the RXCIPHER.

SREG0x2D SECCR1

SREG0x2D, SECCR1							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
Reserved	TXBCIPHER			SNIFMODE	Reserved	DISDEC	DISENC
	R/W-0b000			R/W-0		R/W-0	R/W-0

Bit 6-4 **TXBCIPHER**: TX cipher mode selection of the FIFO.
0b000: None
0b001: AES-CTR
0b010: AES-CCM-128
0b011: AES-CCM-64
0b100: AES-CCM-32
0b101: AES-CBC-MAC-128
0b110: AES-CBC-MAC-64
0b111: AES-CBC-MAC-32

Bit 3 **SNIFMODE**: Sniffer mode. Note: Set this bit to the value '0' when using the 16-bit half-symbol timer.

Bit 1 **DISDEC**: Disable the decryption process. Even if the 'security' bit in the MAC header is detected, the UM2455 does not generate a security interrupt.

Bit 0 **DISENC**: Disable the encryption process. Even if the TX security is enabled, the UM2455 does not encrypt.

SREG0x2E TXPEMISP

SREG0x2E, TXPEMISP							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
TXPET				Reserved			
R/W-0111							

Bit 7-4 **TXPET**: For VCO circuit calibration.
The recommend value for TXPEMISP is '0x95'. Please do not use other values for this register.

SREG0x30 RXSR

SREG0x30, RXSR							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
Reserved	UPSECERR	BATIND	Reserved				
	R/W1C-0	R-0					

Bit 6 **UPSECERR**: The MIC error in upper layer security mode.

Bit 5 **BATIND**: Low-battery indicator.

SREG0x31 ISRSTS

SREG0x31, ISRSTS							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
SLPIF	WAKEIF	HSYMTMRIF	SECIF	RXIF	Reserved	Reserved	TXNIF
RC-0	RC-0	RC-0	RC-0	RC-0			RC-0

Bit 7 **SLPIF**: Sleep alert interrupt bit
0: Otherwise
1: Sleep alert interrupt occurred

Bit 6 **WAKEIF**: Wake-up alert interrupt bit
0: Otherwise
1: Wake-up interrupt occurred

Bit 5 **HSYMTMRIF**: Half symbol timer interrupt bit
0: Otherwise
1: Half symbol timer interrupt occurred

Bit 4 **SECIF**: Security key request interrupt bit
0: Otherwise
1: Security key request interrupt occurred

Bit 3 **RXIF**: RX receive interrupt bit
0: Otherwise
1: RX receive interrupt occurred

Bit 0 **TXNIF**: TX Normal FIFO transmission interrupt bit
0: Otherwise
1: TX Normal FIFO transmission interrupt occurred

SREG0x32 INT MSK

SREG0x32, INT MSK							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SLP MSK	WAKE MSK	HSYMTMR MSK	SEC MSK	RX MSK	Reserved		TXN MSK
R/W-1	R/W-1	R/W-1	R/W-1	R/W-1			R/W-1

Bit 7 **SLP MSK**: Sleep alert interrupt mask
Bit 6 **WAKE MSK**: Wake-up alert interrupt mask
Bit 5 **HSYMTMR MSK**: Half symbol timer interrupt mask
Bit 4 **SEC MSK**: security interrupt mask
Bit 3 **RX MSK**: RX receive interrupt mask
Bit 2 **Reserved**
Bit 1 **Reserved**
Bit 0 **TXN MSK**: TX Normal FIFO transmission interrupt mask
1: the interrupt is masked, and hence INT pin will not change even if an interrupt occurs.
0: the interrupt is not masked.

SREG0x33 GPIO

SREG0x33, GPIO							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
Reserved					GPIO2	GPIO1	GPIO0
					R/W-0	R/W-0	R/W-0

Bit 2 **GPIO2**: The status of GPIO2. Both read and write operations are allowed.
Bit 1 **GPIO1**: The status of GPIO1. Both read and write operations are allowed.
Bit 0 **GPIO0**: The status of GPIO0. Both read and write operations are allowed.

SREG0x34 SPIGPIO

SREG0x34, SPIGPIO							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
SPIMODE		Reserved			GPDIR2	GPDIR1	GPDIR0
R/W-0b00					R/W-0	R/W-0	R/W-0

Bit 7-6 **SPIMODE**: Select the mode for the SPI interface.
0b00: Normal SPI mode
0b01: PLUS SPI mode

Bit 2 **GPDIR2**: The direction of GPIO2.
Bit 1 **GPDIR1**: The direction of GPIO1.
Bit 0 **GPDIR0**: The direction of GPIO0.
0: Input direction
1: Output direction

SREG0x35 SLPACK

SREG0x35, SLPACK							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
SLPACK	WAKECNT						
WT-0	R/W-0000000						

Bit 7 **SLPACK**: Sleep acknowledgement. Setting this bit to '1' will cause the UM2455 to enter sleep mode immediately. This bit will be automatically cleared to the value '0'.
Bit 3-0 **WAKECNT**: System clock (20 MHz) recovery time
Note: In the initial procedure, set **WAKECNT** to the value '0x5F' to optimize the performance.

SREG0x36 RFCTL

SREG0x36, RFCTL							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
Reserved			WAKECNTEXT		RFRST	RFTXMODE	RFRXMODE
			R/W-00		R/W-0	R/W-0	R/W-0

Bit 4 -3 **WAKECNTEXT**: The 20 MHz clock recovery time extension bits

Bit 2 **RFRST**: RF state reset.
Reset the RF state. The RF state must be reset in order to change the RF channels.
Write the value '1', and then write the value '0' to accomplish the reset operation.

Bit 1 **RFTXMODE**: The RF is forced into TX mode.

Bit 0 **RFRXMODE**: The RF is forced into RX mode.

SREG0x37 SECCR2

SREG0x37, SECCR2							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
UPDEC	UPENC	Reserved					
WT-0	WT-0						

Bit 7 **UPDEC**: Upper security decryption mode. Set this bit when doing an upper decryption using TX normal FIFO.

Bit 6 **UPENC**: Upper security encryption mode. Set this bit when doing an upper encryption using TX normal FIFO.

SREG0x38 BBREG0

SREG0x38, BBREG0							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
Reserved							TURBO
Reserved							R/W-0

Bit 0 **TURBO**: enable high speed mode
1: High speed mode
0: Low speed mode

SREG0x3B BBREG3

SREG0x3B, BBREG3							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
PREVALIDTH				PREDETTH			Reserved
R/W-0b1101				R/W-0b100			

Bit 7-4 **PREVALIDTH**: Baseband decoder parameter
0b1101: Low speed mode (250kbps) optimized value
0b0011: High speed mode (625kbps) optimized value
Do not use other values.

Bit 3-1 **PREDETTH**: Baseband decoder parameter
0b100 is the optimized value for both Low speed and high speed modes.

SREG0x3C BBREG4

SREG0x3C, BBREG4							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
CSTH			PRECNT			TXDACEDGE	RXADCEDGE
R/W-100			R/W-111			R/W-0	R/W-0

Bit 7-5 **CSTH**: Baseband decoder parameter.
100: Low speed mode (250kbps) optimized value
010: High speed mode (625kbps) optimized value
Do not use other values.

Bit 4-2 **PRECNT**: Baseband decoder parameter
'111' is the optimized value for both normal and turbo modes.

Bit 1 **TXDACEDGE**: Tx DAC latches time selection.
1: DAC latch the I/Q data at the negative clock edge
0: DAC latch the I/Q data at the positive clock edge

Bit 0 **RXADCEDGE**: Rx ADC latch time selection
1: ADC value is latched at the negative clock edge
0: ADC value is latched at the positive clock edge

SREG0x3E BBREG6

SREG0x3E, BBREG6							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
RSSIMODE1	RSSIMODE2	Reserved					RSSIRDY
WT-0	R/W-0						R-1

Bit 7 **RSSIMODE1**: RSSI mode 1 enable
1: calculate RSSI for a firmware request, and it will be clear to the value '0' when RSSI calculation is finished.

Bit 6 **RSSIMODE2**: RSSI mode 2 enable
1: calculate RSSI for each received packet, and the RSSI value will be stored in the RXFIFO.
0: no RSSI calculation for a received packet.

Bit 0 **RSSIRDY**: RSSI ready signal for **RSSIMODE1** use
If **RSSIMODE1** is set, this bit will be cleared to the value '0' until RSSI calculation is done. When RSSI calculation is finished and the RSSI value is ready, this bit will be set to the value '1' automatically.

SREG0x3F BBREG7

SREG0x3F, BBREG7							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
RSSITHCCA							
R/W-0x0							

Note: If the in-band signal strength is larger than the threshold, the channel is busy. The 8-bit value can be mapped to a certain power level according to Appendix A.

C.2 Long Registers (LREG0x200~LREG0x27F)

LREG0x200 RFCTRL0

LREG0x200, RFCTRL0							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
CHANNEL				RFOPT			
R/W-0b0000				R-0b0000			

Bit 7-4 **CHANNEL**: RF channel number.
0b0000: channel 1 (2405 MHz)
0b0001: channel 2 (2410 MHz)
0b0010: channel 3 (2415 MHz)
0b1111: channel 16 (2480 MHz)

Bit 3-0 **RFOPT**: Optimize the RF control
0b0010 is the recommended value for the RF optimization.

LREG0x202 RFCTL2

LREG0x202, RFCTRL2							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
PLLCTL	RSSIDC		RSSISLOPE		Reserved		
R/W-0	R/W-0b00		R/W-0b00				

Bit 7 **PLLCTL**: RF Phase Lock Loop (PLL) control
1: The recommended value for the RF optimization. This needs to be set before the RF transmission and reception.

Bit 6-5 **RSSIDC**: RSSI DC level shift.
Note: 0b11 is not allowed.

Bit 4-3 **RSSISLOPE**: RSSI range control.
Note: 0b11 is not allowed.

LREG0x203 RFCTL3

LREG0x203, RFCTRL3							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
TXPOWL		TXPOWF			Reserved		
R/W-0b00		R/W-0b000					

Bit 7-6 **TXPOWL**: Large scale control for the TX power in dB
0b00: 0 dB
0b01: -10 dB
0b10: -20 dB
0b11: -30 dB

Bit 5-3 **TXPOWF**: Fine scale control for the TX power in dB
0b000: 0 dB

0b001: -0.5 dB
0b010: -1.2 dB
0b011: -1.9 dB
0b100: -2.8 dB
0b101: -3.7 dB
0b110: -4.9 dB
0b111: -6.3 dB

LREG0x205 RFCTRL5

LREG0x205, RFCTRL5							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
BATTH				Reserved			
R/W-0b000				-			

Bit 7-4 **BATTH**: Battery monitor threshold value corresponding to the voltage supply
0b1110: 3.5V
0b1101: 3.3V
0b1100: 3.2V
0b1011: 3.1V
0b1010: 2.8V
0b1001: 2.7V
0b1000: 2.6V
0b0111: 2.5V
Other: out of the operation voltage

LREG0x206 RFCTL6

LREG0x206, RFCTL6							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TXFIL	Reserved	20MRECVR		BATEN	Reserved		
R/W-0		R/W-0b00		R/W-0			

Bit 7 **TXFIL**: TX filter control
1: The recommended value for the RF optimization.
Bit 5-4 **20MRECVR**: 20 MHz clock recovery time (recovery from sleep) control
10: Less than 1 ms
Otherwise: less than 3 ms
Bit 3 **BATEN**: Battery monitor enable
1: A battery monitor is enabled.
0: A battery monitor is disabled.

LREG0x208 RFCTL8

LREG0x208, RFCTL8							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
Reserved			RFVCO	Reserved			CLKOUTSRC
			R/W-0				R/W-0

Bit 4 **RFVCO**: The VCO control. The recommend value is '1'.

Bit 0 **CLKOUTSRC**: The source of the 20 MHz clock output

0: From an analog module. Unstable when recovering from sleep mode.

1: From a power management module. Stable when recovering from sleep mode.

LREG0x209 SLPCAL1

LREG0x209, SLPCAL1							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
SLPCAL1							
R-0x0							

Bit 7-0 **SLPCAL1**: SLPCAL[7:0]. The calibration counter which calibrates a sleep clock. SLPCAL [19:0] indicates the time period of 16 sleep clock cycles. The unit is 50ns, and it is counted by 20 MHz.

LREG0x20A SLPCAL2

LREG0x20A, SLPCAL2							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
SLPCAL2							
R-0x0							

Bit 7-0 **SLPCAL2**: SLPCAL [15:8]. The calibration counter which calibrates a sleep clock. SLPCAL [19:0] indicates the time period of 16 sleep clock cycles. The counting unit is 50ns, and it is counted by 20 MHz.

LREG0x20B SLPCAL3

LREG0x20B, SLPCAL3							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
CALRDY	Reserved		CALEN	SLPCAL3			
R-0			WT-0	R-0b0000			

Bit 7 **CALRDY**: SLPCAL status indicator.

0: Not ready

1: A calibration counter finished the counting for 16 cycles of a sleep clock. SLPCAL [19:0] is ready to be read.

Bit 4 **CALEN**: Set this bit to be the value '1' to start a calibration counter.

Bit 3-0 **SLPCAL3**: SLPCAL [19:16]. The calibration counter which calibrates a sleep clock. SLPCAL [19:0] indicates the time period of 16 sleep clock cycles. The unit is 50 ns, and it is counted by 20 MHz.

LREG0x211 CLKIRQCR

LREG0x211, CLKIRQCR							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
Reserved						IRQPOL	CLK32KOFF
--						R/W-0	R/W-0

Bit 1 **IRQPOL**: Interrupt edge polarity bit
0: Falling edge
1: Rising edge

Bit 0 **CLK32KOFF**: SLPCLK disable bit
0: Enable
1: Disable

LREG0x220 SCLKDIV

LREG0x220, SCLKDIV							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
I2CWDTEN	Reserved	CLKOUTEN	SCLKDIV				
R/W-0		R/W-0	R/W-0b00000				

Bit 7 **I2CWDTEN**: I^2C watchdog timer enable
1: Enable
0: Disable

Bit 5 **CLKOUTEN**: the UM2455 clock output enable
1: Enable
0: Disable

Bit 4-0 **SCLKDIV**: Sleep clock division selection.
n: The sleep clock is divided by 2^n before being fed to the logic circuit.
Note: If internal ring oscillator is used, '0b0001' is the recommended value.

LREG0x222 WAKETIMEL

LREG0x222, WAKETIMEL							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
WAKETIMEL							
R/W-0xA							

Bit 7 **WAKETIMEL**: WAKETIME [7:0]. WAKETIME is a down counter which is counted by a sleep clock. WAKETIME should be larger than WAKECNT (SREG0x35 [6:0]). WAKETIME must be larger than the value '1' in any case.

LREG0x223 WAKETIMEH

LREG0x223, WAKETIMEH							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
Reserved					WAKETIMEH		
					R/W-0b000		

Bit 2-0 **WAKETIMEH**: WAKETIME [10:8]. WAKETIME is a down counter which is counted by the sleep clock. WAKETIME should be larger than WAKECNT (SREG0x35 [6:0]). WAKETIME must be larger than the value '1' in any case.

LREG0x224 TXREMCNTL

LREG0x224, TXREMCNTL							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
TXREMCNTL							
R/W-0x0							

Bit 7-0 **TXREMCNTL**: TXREMCNT [7:0]. The lower byte of the remain counter.

LREG0x225 TXREMCNTH

LREG0x225, TXREMCNTH							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
TXREMCNTH							
R/W-0x0							

Bit 7-0 **TXREMCNTH**: TXREMCNT [15:8]. The higher byte of the remain counter.

LREG0x226 TXMAINCNT0

LREG0x226, TXMAINCNT0							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
TXMAINCNT0							
R/W-0x0							

Bit 7-0 **TXMAINCNT0**: TXMAINCNT [7:0]. Bit 0 to bit 7 of the main counter.

LREG0x227 TXMAINCNT1

LREG0x227, TXMAINCNT1							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
TXMAINCNT1							
R/W-0x0							

Bit 7-0 **TXMAINCNT1**: TXMAINCNT[15:8]. Bit 8 to bit 15 of the main counter.

LREG0x228 TXMAINCNT2

LREG0x228, TXMAINCNT2							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
TXMAINCNT2							
R/W-0x0							

Bit 7-0 **TXMAINCNT2**: TXMAINCNT [23:16]. Bit 16 to bit 23 of the main counter.

LREG0x229 TXMAINCNT3

LREG0x229, TXMAINCNT3							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
STARTCNT	Reserved				TXMAINCNT3		
WT-0					R/W-0b000		

Bit 7 **STARTCNT**: Trigger sleep mode in un-slotted mode (**BO** = 0xF and **SLOTTED** = 0b0). Will return to 0 when wake-up.

Bit 2-0 **TXMAINCNT3**: TXMAINCNT [25:24]. Bit 24 and bit 25 of the main counter.

LREG0x22F TESTMODE

LREG0x22F, TESTMODE							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
Reserved			RSSIWAIT		TESTMODE		
			R/W-0b01		R/W-000		

Bit 4-3 **RSSIWAIT**: RSSI state machine parameter.
'0b01' is the optimized value.

Bit 2-0 **TESTMODE**: the UM2455 test mode using GPIO pins
0b101: Single-tone test mode.
0b111: GPIO0, GPIO1, GPIO2 are configured to control an external PA, a LNA or a switch as discussed above.

LREG0x230 ASSOEADR0

LREG0x230, ASSOEADR0							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
ASSOEADR0							
R/W-0x0							

Bit 7-0 **ASSOEADR0**: ASSOEADR [7:0]. Bit 7 to bit 0 of a 64-bit long address of the associated Host.

LREG0x231 ASSOEADR1

LREG0x231, ASSOEADR1							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
ASSOEADR1							
R/W-0x0							

Bit 7-0 **ASSOEADR1**: ASSOEADR [15:8]. Bit 8 to bit 15 of a 64-bit long address of the associated Host.

LREG0x232 ASSOEADR2

LREG0x232, ASSOEADR2							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
ASSOEADR2							
R/W-0x0							

Bit 7-0 **ASSOEADR2**: ASSOEADR [23:16]. Bit 16 to bit 23 of a 64-bit long address of the associated Host.

LREG0x233 ASSOEADR3

LREG0x233, ASSOEADR3							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
ASSOEADR3							
R/W-0x0							

Bit 7-0 **ASSOEADR3**: ASSOEADR [31:24]. Bit 24 to bit 31 of a 64-bit long address of the associated Host.

LREG0x234 ASSOEADR4

LREG0x234, ASSOEADR4							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
ASSOEADR4							
R/W-0x0							

Bit 7-0 **ASSOEADR4**: ASSOEADR [39:32]. Bit 32 to bit 39 of a 64-bit long address of the associated Host.

LREG0x235 ASSOEADR5

LREG0x235, ASSOEADR5							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
ASSOEADR5							
R/W-0x0							

Bit 7-0 **ASSOEADR5**: ASSOEADR [47:40]. Bit 40 to bit 47 of a 64-bit long address of the associated Host.

LREG0x236 ASSOEADR6

LREG0x236, ASSOEADR6							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
ASSOEADR6							
R/W-0x0							

Bit 7-0 **ASSOEADR6**: ASSOEADR [55:48]. Bit 48 to bit 55 of a 64-bit long address of the associated coordinator.

LREG0x237 ASSOEADR7

LREG0x237, ASSOEADR7							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
ASSOEADR7							
R/W-0x0							

Bit 7-0 **ASSOEADR7**: ASSOEADR [63:56]. Bit 56 to bit 63 of a 64-bit long address of the associated Host.

LREG0x238 ASSOSADR0

LREG0x238, ASSOSADR0							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
ASSOSADR0							
R/W-0x0							

Bit 7-0 **ASSOSADR0**: ASSOSADR [7:0]. Bit 0 to bit 7 of a 16-bit short address of the associated Host.

LREG0x239 ASSOSADR1

LREG0x239, ASSOSADR1							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
ASSOSADR1							
R/W-0x0							

Bit 7-0 **ASSOSADR1**: ASSOSADR [15:8]. Bit 8 to bit 15 of a 16-bit short address of the associated Host.

LREG0x240 ~ LREG0x24C UPNONCE

LREG0x240 ~ LREG 0x24C, UPNONCE							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
UPNONCE							
R/W-0x0							

Bit 7-0 **UPNONCE**: **UPNONCE** is 13-byte data. The lease significant byte is stored in the long register LREG0x240 while the most significant byte is stored in the long register LREG0x24C.

Revision History

Revision	Date	Description of Change
1.0	2008/01/02	Version 1.0 released.
1.1	2008/01/08	Version 1.1 released.

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