

DATA SHEET



SPY0030A

Audio Driver

Preliminary

OCT. 02, 2002

Version 0.2

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AUDIO DRIVER

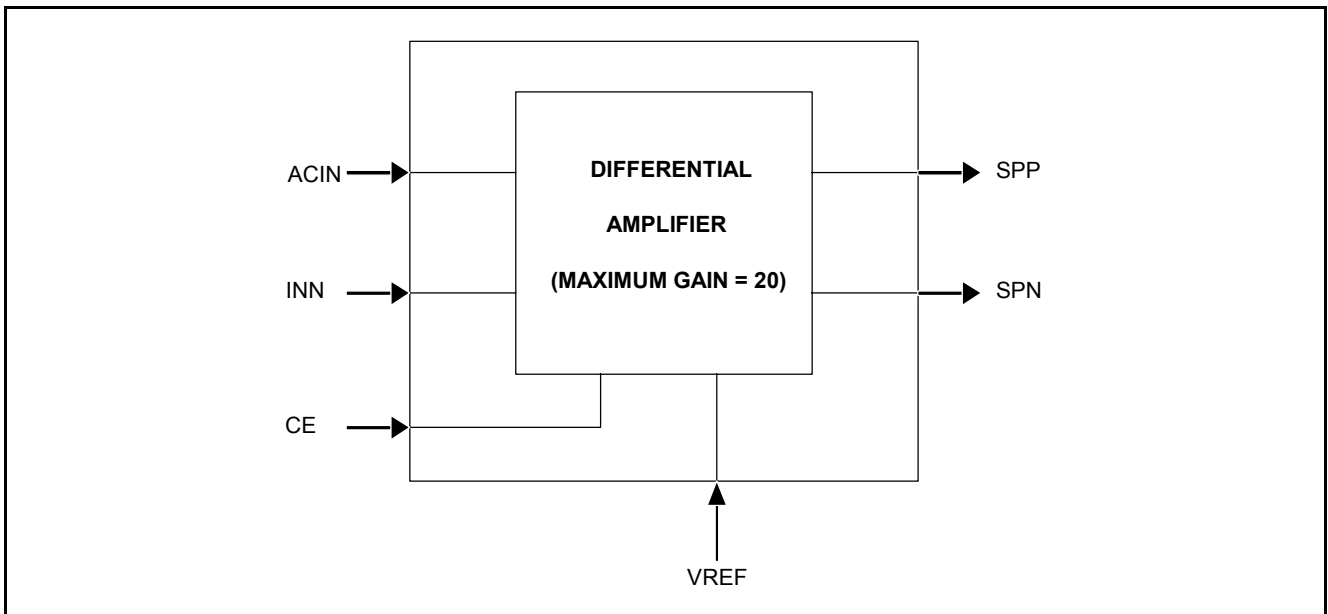
1. GENERAL DESCRIPTION

The SPY0030A is an audio driver whose gain can be adjusted by external resistor. (Maximum gain is 20) Normally, it is applied for SPC series, SPF series, SPL series and other SUNPLUS products. The SPY0030A is easily to be used in various applications and products.

2. FEATURES

- Wide operation range: 2.4V - 6.0V
- Dual-end output mode
- Low distortion: THD+N = 0.55% (Typ.)
(For VDD = 5.0V, $R_L = 8\Omega$ & $P_{out} = 500mW$)
- High output power: $P_{OUT} = 825mW$
(For VDD = 5.0V, THD+N = 10%, $f = 1.0KHz$ & $R_L = 8.0\Omega$)
- Low standby current: 1.0 μ A

3. BLOCK DIAGRAM



4. SIGNAL DESCRIPTIONS

Mnemonic	PIN No.	Type	Description	Electrical Characteristics
VDD	8	I	Power VDD	2.4V - 6.0V
VSS	3	I	Power VSS	
SPP	2	O	Audio output positive	
SPN	1	O	Audio output negative	
ACIN	5	I	Signal input positive	
INN	4	I	Signal input negative	
CE	7	I	Chip enable	
VREF	6	O	Reference voltage	VDD/2

5. ELECTRICAL SPECIFICATIONS

5.1. Absolute Maximum Ratings

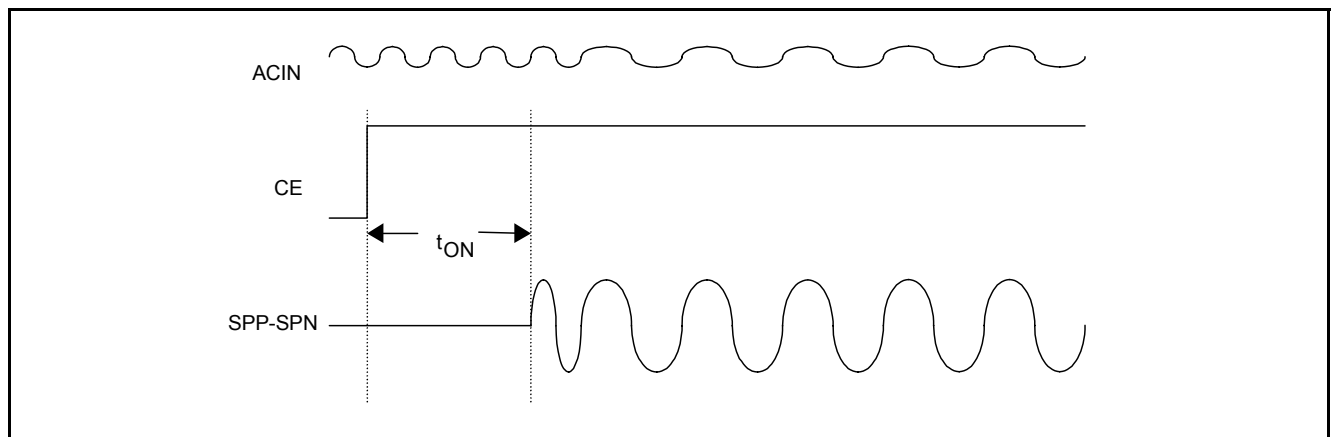
Characteristics	Symbol	Ratings
DC Supply Voltage	V_+	< 7.0V
Input Voltage Range	V_{IN}	-0.5V to $V_+ + 0.5V$
Operating Temperature	T_A	0°C to +60°C
Storage Temperature	T_{STO}	-50°C to +150°C

Note: Stresses beyond those given in the Absolute Maximum Rating table may cause operational errors or damage to the device. For normal operational conditions see AC/DC Electrical Characteristics.

5.2. DC Characteristics ($T_A = 25^\circ\text{C}$)

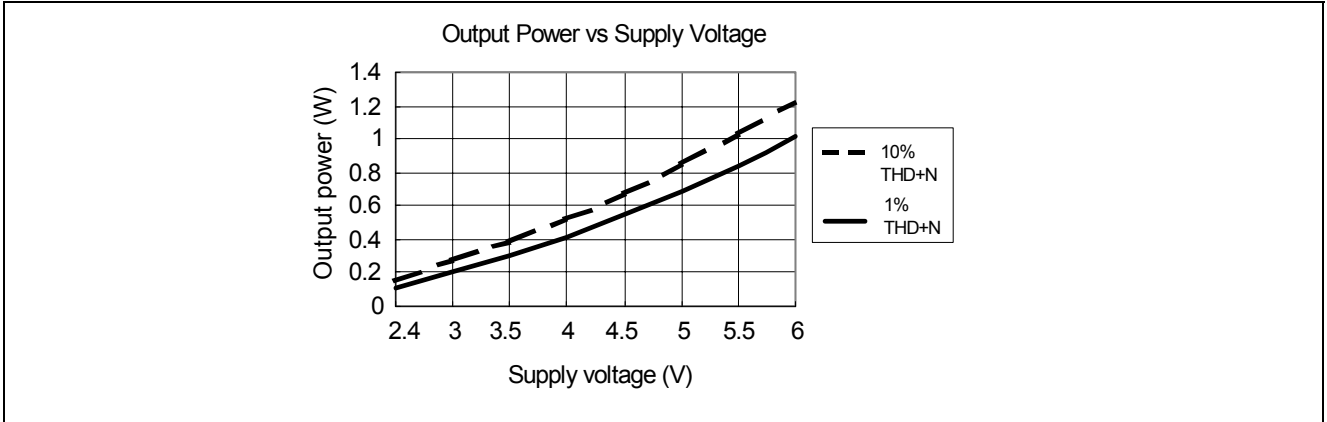
Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Operating Voltage	VDD	2.4	-	6.0	V	For 2- or 3-battery application
Standby Current	I_{STBY}	-	-	1.0	μA	CE low
Reference Voltage	V_{VREF}	-	VDD/2	-	V	CE high, the voltage of VREF (PIN 6)
Total Harmonic Distortion + Noise	THD+N	-	0.55	1.0	%	VDD = 5.0V, $R_L = 8\Omega$, $P_{OUT} = 500\text{mW}$
Input resistor (CE)	R_{CE}	-	20	-	$\text{K}\Omega$	$V_{IH} = VDD$, Pull-low
Input current (CE)	I_{CE}	200	-	-	μA	$V_{IH} = 2.3V$ at VDD = 5.0V
Operating Current	I_{OC}	-	3.0	6.0	mA	CE high, no load & ACIN floating
Output power	P_{OUT}	500	675	-	mW	VDD = 5.0V, THD+N = 1%, $f = 1.0\text{KHz}$ & $R_L = 8.0\Omega$
		-	825	-	mW	VDD = 5.0V, THD+N = 10%, $f = 1.0\text{KHz}$ & $R_L = 8.0\Omega$
Enable time (See Note 1)	T_{ON}	-	15	-	ms	VDD = 5.0V
		-	30	-	ms	VDD = 3.0V

Note: t_{ON} is the time from CE high (chip enable) to SPP or SPN output.

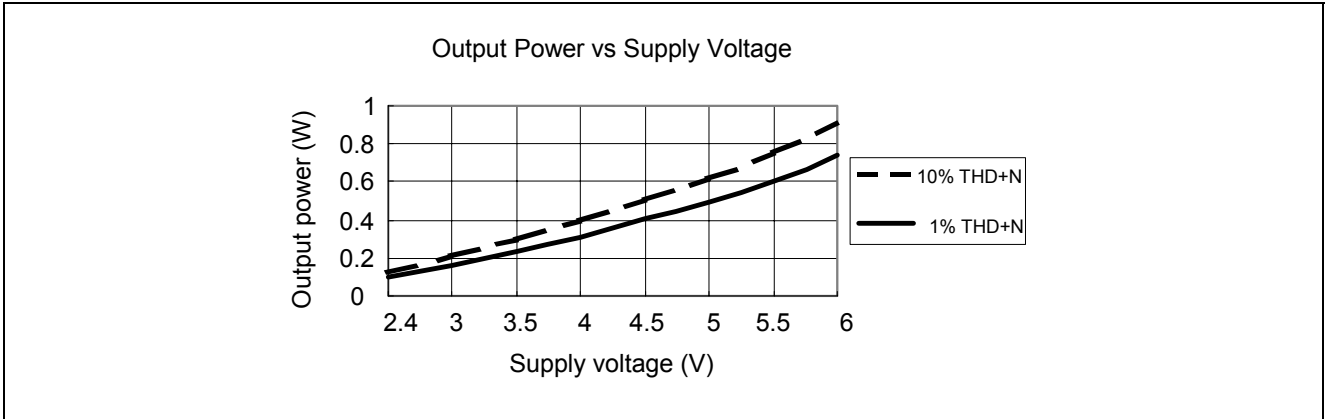


5.3. Typical Performance Characteristics

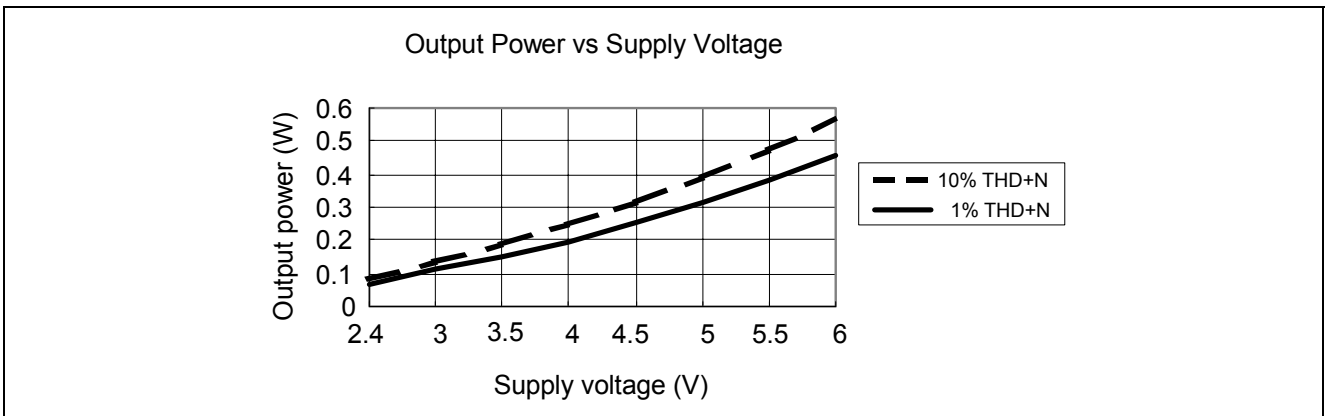
5.3.1. Output power vs. supply voltage ($f_{IN} = 1.0\text{KHz}$, $R_L = 8.0\Omega$, $20\text{Hz} < \text{BW} < 22\text{KHz}$)



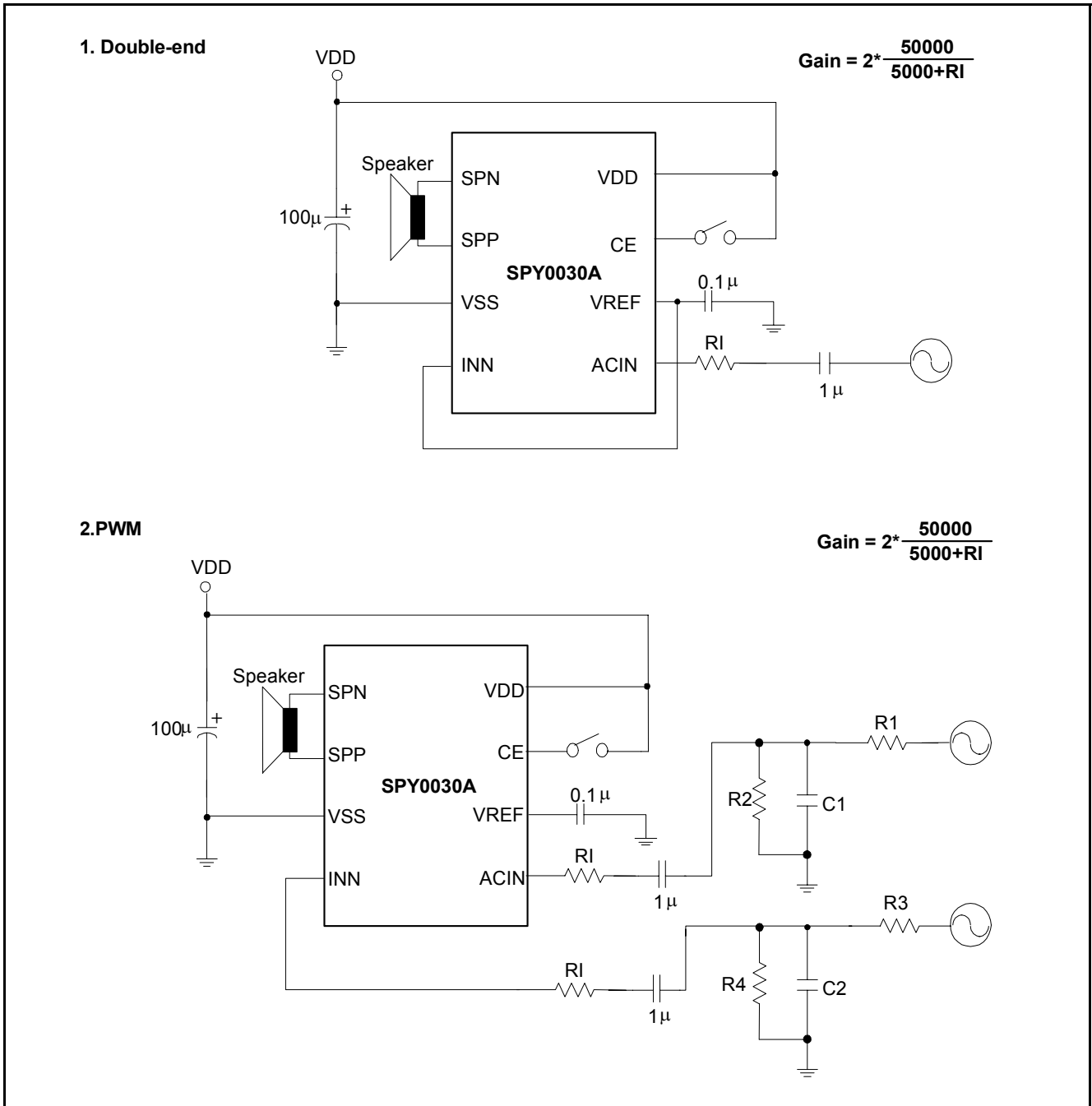
5.3.2. Output power vs. supply voltage ($f_{IN} = 1.0\text{KHz}$, $R_L = 16\Omega$, $20\text{Hz} < \text{BW} < 22\text{KHz}$)



5.3.3. Output power vs. supply voltage ($f_{IN} = 1.0\text{KHz}$, $R_L = 32\Omega$, $20\text{Hz} < \text{BW} < 22\text{KHz}$)

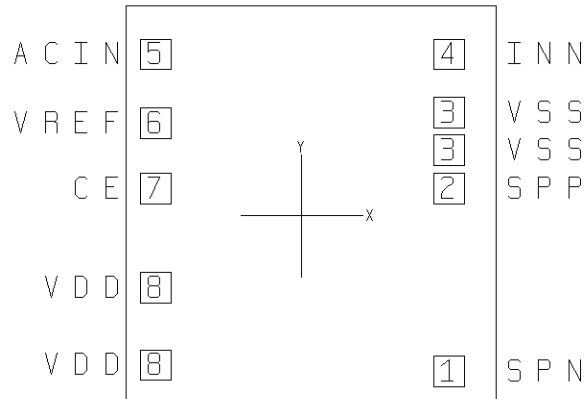


6. APPLICATION CIRCUIT



7. PACKAGE/PAD LOCATIONS

7.1. PAD Assignment



Chip Size: 1320 μ m × 1400 μ m

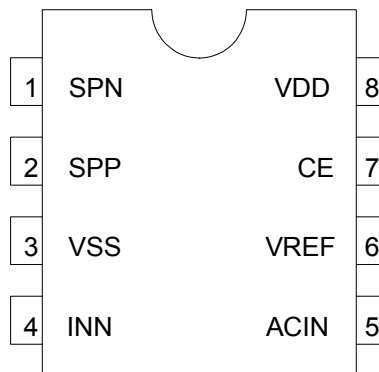
This IC substrate should be connected to VSS

Note1: Chip size included scribe line.

Note2: To ensure the IC functions properly, please bond all of VDD and VSS pins.

Note3: The 0.1 μ F capacitor between VDD and VSS should be placed to IC as close as possible.

7.2. PIN Assignment



7.3. Ordering Information

Product Number	Package Type
SPY0030A - C	Chip form
SPY0030A - PS01	Package form - SOP8 (150mil)
SPY0030A - PD01	Package form - PDIP 8 (300mil)

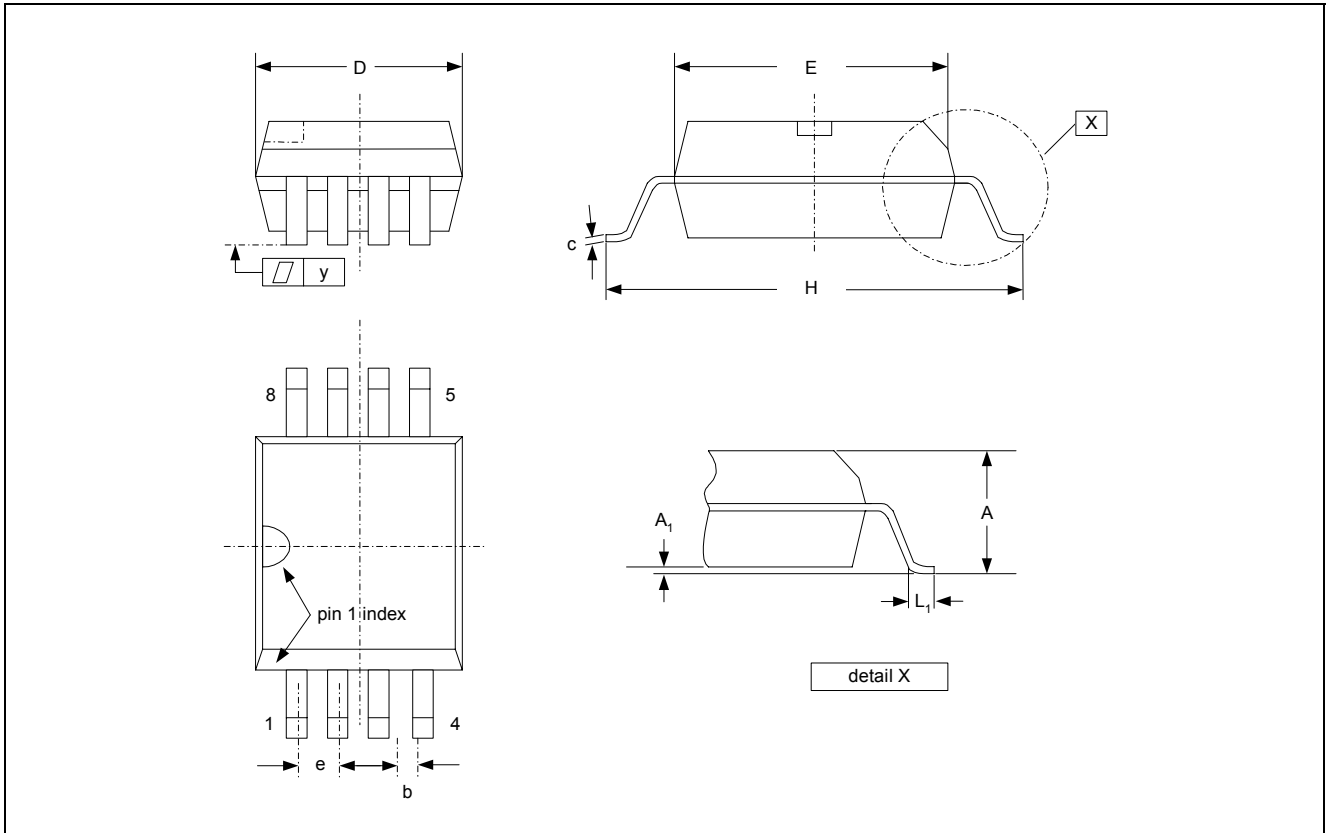
7.4. PAD Locations

PAD No.	PAD Name	X	Y
1	SPN	1064	100
2	SPP	1064	701.85
3	VSS	1064	826.85
3	VSS	1064	951.85
4	INN	1107.95	1142.2
5	ACIN	100.05	1141.45
6	VREF	100.05	915.85
7	CE	100.05	696.25
8	VDD	100.05	117.3
8	VDD	100.05	373.3

Note: VDD and VSS should be double bonding.

7.5. Package Information

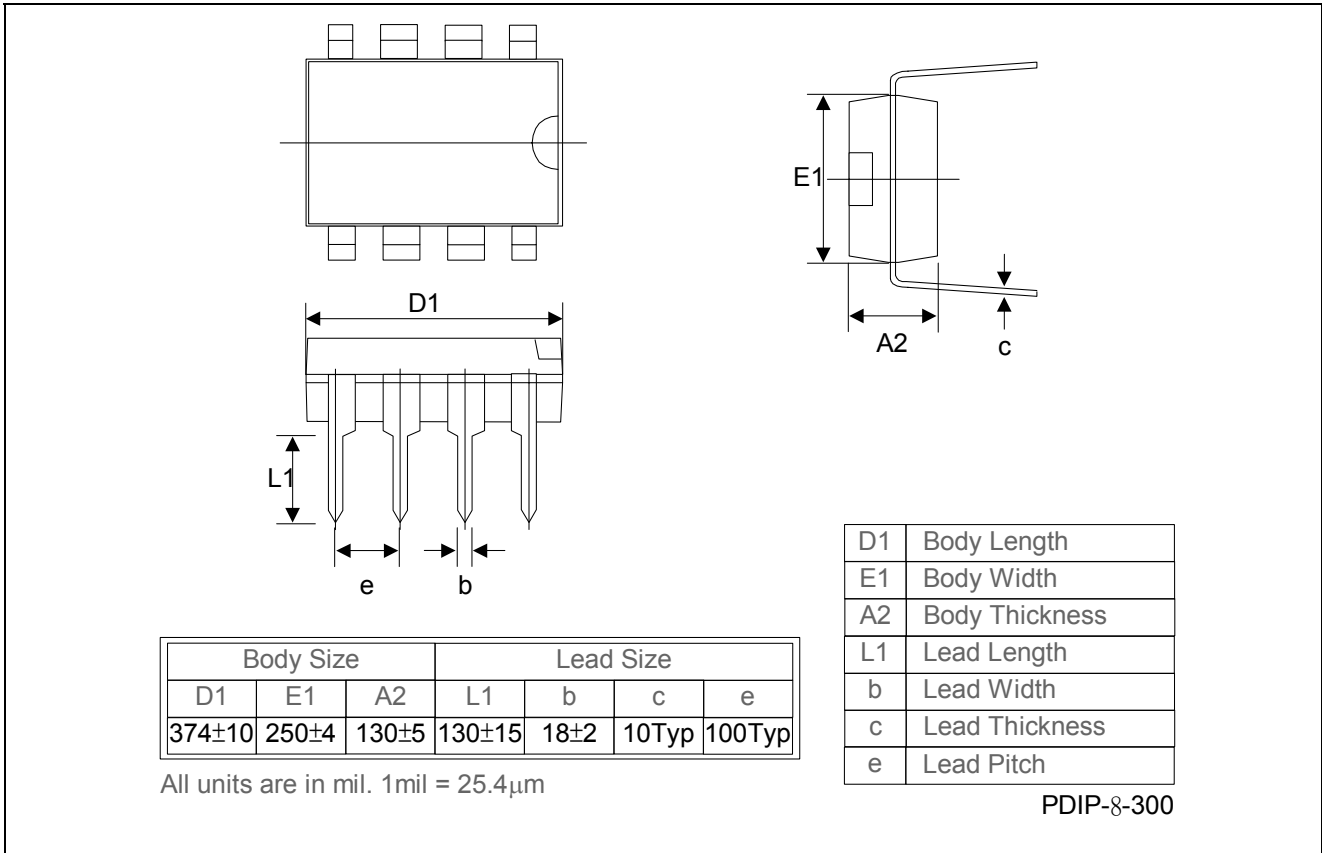
7.5.1. SOP 8



Symbol	Dimension in mm		
	Min.	Typ.	Max.
A	0.053	-	0.069
A ₁	0.004	-	0.010
b	-	0.016	-
D	0.189	-	0.196
E	0.150	-	0.157
e	-	0.050	-
H	0.228	-	0.244
L ₁	0.016	-	0.050
y	-	-	0.004



7.5.2. PDIP 8



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9. REVISION HISTORY

Date	Revision #	Description	Page
JUN. 26, 2001	0.1	Original	11
OCT. 02, 2002	0.2	1. VDD Power: 5.5V to 6.0V	
		2. Add " <i>5.3 Typical Performance Characteristics</i> "	5
		3. Modify " <i>7.3 Ordering Information</i> "	7
		4. Add " <i>7.5 Package Information</i> "	9 - 10