OCM12864-9 图形点阵液晶显示模块

使用说明书

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1、 产品简介

主要工艺：COG
显示内容：128X64 点阵
显示模式：STN，POSITIVE
驱动条件：**1/64Duty,1/9Bias**
视向：6：00
背光：LED，白色
工作温度：-20℃-+70℃
储存温度：-30℃-+80℃
驱动 **IC**：**ST7920P**

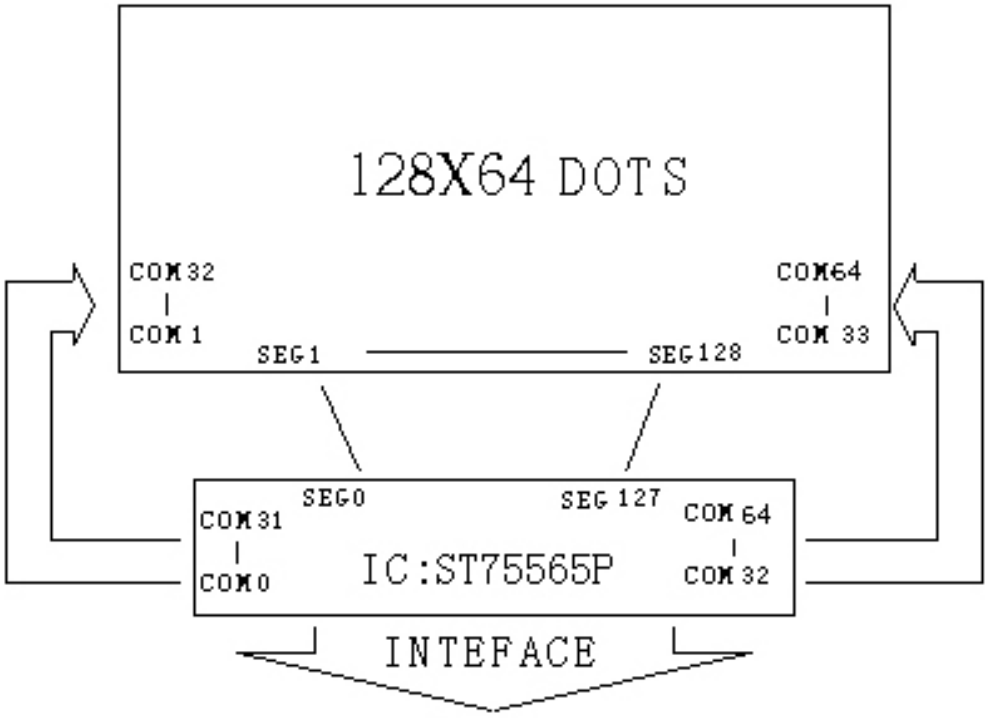
2、 引用文件

ST7565P 规格书

3、机械特性

类别	标准值	单位
模块	42.00（w）X37.00(h)X7.0(t)Max	mm
有效显示区	30(w)X22(h)	mm
点大小	0.2(w)X0.28(h)	mm
点间隙	0.018(w)X0.018(h)	mm

4、产品框图



5、光电特性

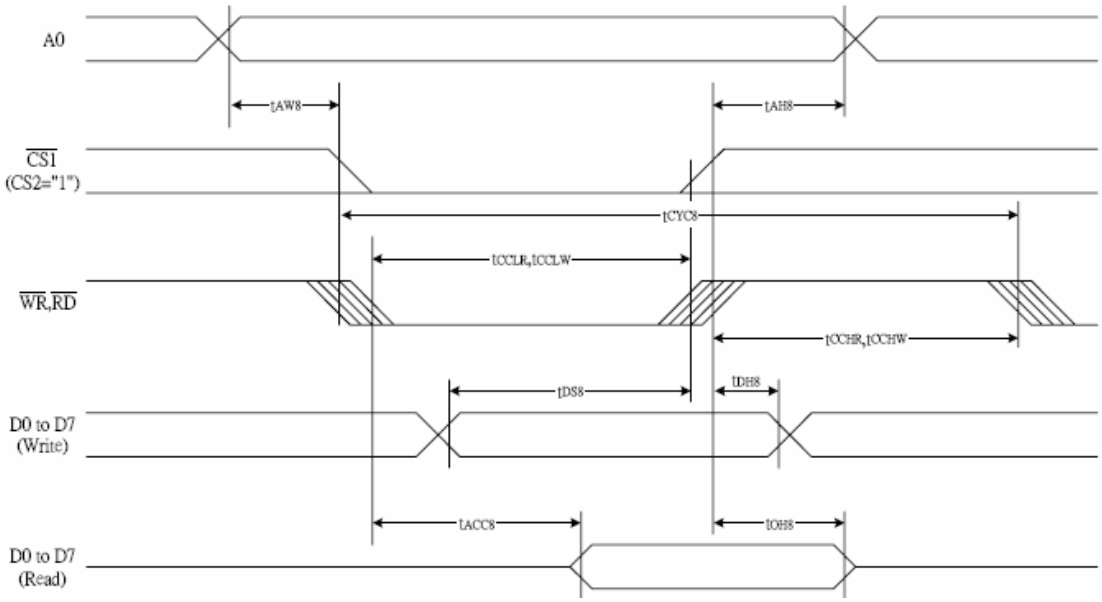
类别	符号	条件	最小值	TYP	最大值	单位
驱动电压	Vop.	25℃	8.8	9.0	9.2	V
响应时间	Ton	25℃	—	127	400	Ms
对比度	Toff	25℃	—	263	400	Ms
	CR	25℃	—	9	—	—
视角范围		25℃	—	88	—	DEG
交叉效应		25℃	—	1.2	—	—

6、极限参数

参数	符号	最小值	最大值	单位
逻辑电压	Vdd	-0.3	+3.30	V
驱动电压	Vout,VO	-0.3	+12.0	V
工作温度	Top	-20	+70	℃
存储温度	Tst	-30	+80	℃

7、接口时序

System Bus Read/Write Characteristics 1 (For the 8080 Series MPU)



(VDD = 3.3V , Ta =25°C)

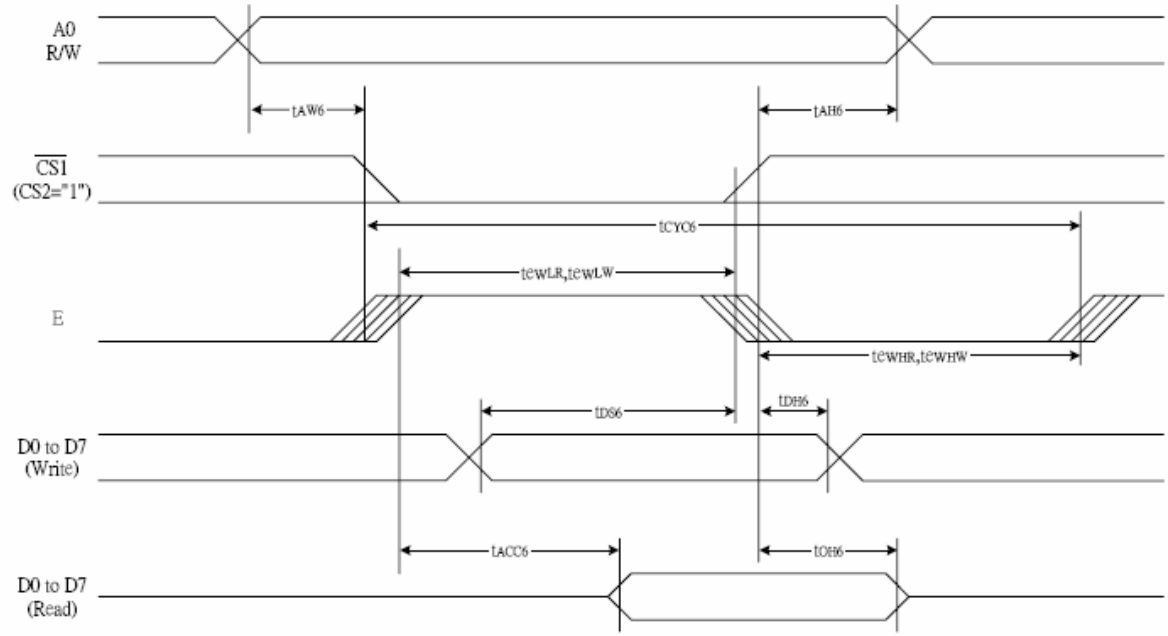
Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	t_{AH8}		0	—	Ns
Address setup time		t_{AW8}		0	—	
System cycle time		t_{CYC8}		240	—	
Enable L pulse width (WRITE)	WR	t_{CCLW}		80	—	
Enable H pulse width (WRITE)		t_{CCHW}		80	—	
Enable L pulse width (READ)	RD	t_{CCLR}		140	—	
Enable H pulse width (READ)		t_{CCHR}		80		
WRITE Data setup time	D0 to D7	t_{DS8}		40	—	
WRITE Address hold time		t_{DH8}		0	—	
READ access time		t_{ACC8}	C_L = 100 pF	—	70	
READ Output disable time		t_{OH8}	C_L = 100 pF	5	50	

(VDD = 2.7 V , Ta = 25°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	t_{AH8}		0	—	ns
Address setup time		t_{AW8}		0	—	
System cycle time		t_{CYC8}		400	—	
Enable L pulse width (WRITE)	WR	t_{CCLW}		220	—	
Enable H pulse width (WRITE)		t_{CCHW}		180	—	
Enable L pulse width (READ)	RD	t_{CCLR}		220	—	
Enable H pulse width (READ)		t_{CCHR}		180	—	
WRITE Data setup time	D0 to D7	t_{DS8}		40	—	
WRITE Address hold time		t_{DH8}		0	—	
READ access time		t_{ACC8}	C_L = 100 pF	—	140	
READ Output disable time		t_{OH8}	C_L = 100 pF	10	100	

(V_{DD} = 1.8V , Ta = 25°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	t_{AH8}		0	—	ns
Address setup time		t_{AW8}		0	—	
System cycle time		t_{CYC8}		640	—	
Enable L pulse width (WRITE)	WR	t_{CCLW}		360	—	
Enable H pulse width (WRITE)		t_{CCHW}		280	—	
Enable L pulse width (READ)	RD	t_{CCLR}		360	—	
Enable H pulse width (READ)		t_{CCHR}		280		
WRITE Data setup time	D0 to D7	t_{DS8}		80	—	
WRITE Address hold time		t_{DH8}		0	—	
READ access time		t_{ACC8}	C_L = 100 pF	—	240	
READ Output disable time		t_{OH8}	C_L = 100 pF	10	200	



System Bus Read/Write Characteristics 2 (For the 6800 Series MPU)

(V_{DD} = 3.3 V , Ta = 25°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	t_{AH6}		0	—	ns
Address setup time		t_{AW6}		0	—	
System cycle time		t_{CYC6}		240	—	
Enable L pulse width (WRITE)	WR	t_{EWLW}		80	—	
Enable H pulse width (WRITE)		t_{EWHW}		80	—	
Enable L pulse width (READ)	RD	t_{EWLR}		80	—	
Enable H pulse width (READ)		t_{EWHR}		140		
WRITE Data setup time	D0 to D7	t_{DS6}		40	—	
WRITE Address hold time		t_{DH6}		0	—	
READ access time		t_{ACC6}	C_L = 100 pF	—	70	
READ Output disable time		t_{OH6}	C_L = 100 pF	5	50	

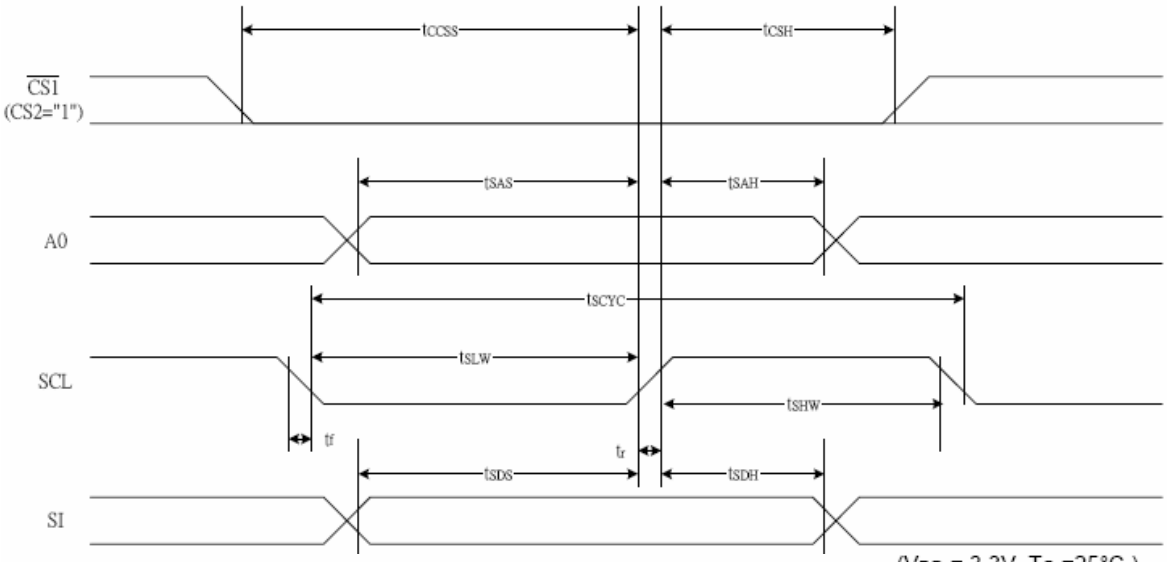
(V_{DD} = 2.7V , Ta =25°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	t_{AH6}		0	—	ns
Address setup time		t_{AW6}		0	—	
System cycle time		t_{CYC6}		400	—	
Enable L pulse width (WRITE)	WR	t_{EWLW}		220	—	
Enable H pulse width (WRITE)		t_{EWHW}		180	—	
Enable L pulse width (READ)	RD	t_{EWLR}		220	—	
Enable H pulse width (READ)		t_{EWHR}		180	—	
WRITE Data setup time	D0 to D7	t_{DS6}		40	—	
WRITE Address hold time		t_{DH6}		0	—	
READ access time		t_{ACC6}	C_L = 100 pF	—	140	
READ Output disable time		t_{OH6}	C_L = 100 pF	10	100	

(V_{DD} =1.8V , Ta =25°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	t_{AH6}		0	—	ns
Address setup time		t_{AW6}		0	—	
System cycle time		t_{CYC6}		640	—	
Enable L pulse width (WRITE)	WR	t_{EWLW}		360	—	
Enable H pulse width (WRITE)		t_{EWHW}		280	—	
Enable L pulse width (READ)	RD	t_{EWLR}		360	—	
Enable H pulse width (READ)		t_{EWHR}		280	—	
WRITE Data setup time	D0 to D7	t_{DS6}		80	—	
WRITE Address hold time		t_{DH6}		0	—	
READ access time		t_{ACC6}	C_L = 100 pF	—	240	
READ Output disable time		t_{OH6}	C_L = 100 pF	10	200	

The Serial Interface



(V_{DD} = 3.3V, Ta =25°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Serial Clock Period	SCL	T_{scyc}		100	—	ns
SCL "H" pulse width		T_{shw}		50	—	
SCL "L" pulse width		T_{SLW}		50	—	
Address setup time	A0	T_{SAS}		20	—	
Address hold time		T_{sah}		10	—	
Data setup time	SI	T_{sds}		20	—	
Data hold time		T_{SDH}		10	—	
CS-SCL time	CS	T_{css}		20	—	
CS-SCL time		T_{csh}		40	—	

(V_{DD} =2.7V , Ta =25°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Serial Clock Period	SCL	T_{scyc}		120	—	ns
SCL "H" pulse width		T_{SHW}		60	—	
SCL "L" pulse width		T_{SLW}		60	—	
Address setup time	A0	T_{SAS}		30	—	
Address hold time		T_{SAH}		20	—	
Data setup time	SI	T_{SDS}		30	—	
Data hold time		T_{SDH}		20	—	
CS-SCL time	CS	T_{CSS}		30	—	
CS-SCL time		T_{CSH}		60	—	

(V_{DD} = 1.8V , Ta = 25°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Serial Clock Period	SCL	T_{SCYC}		200	—	ns
SCL "H" pulse width		T_{SHW}		80	—	
SCL "L" pulse width		T_{SLW}		80	—	
Address setup time	A0	T_{SAS}		60	—	
Address hold time		T_{SAH}		40	—	
Data setup time	SI	T_{SDS}		60	—	
Data hold time		T_{SDH}		30	—	
CS-SCL time	CS	T_{CSS}		40	—	
CS-SCL time		T_{CSH}		100	—	

Reset Timing

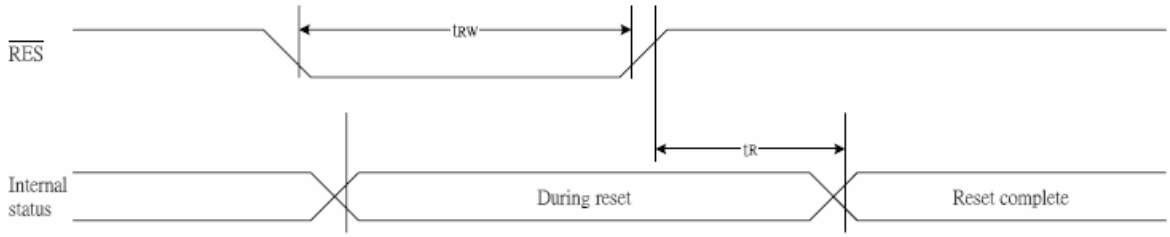


Figure 41

(V_{DD} = 3.3V , Ta = –40 to 85°C)

Item	Signal	Symbol	Condition	Rating			Units
				Min.	Typ.	Max.	
Reset time		t_R		—	—	1.0	us
Reset "L" pulse width	/RES	t_{RW}		1.0	—	—	us

(V_{DD} = 2.7V , Ta = –40 to 85°C)

Item	Signal	Symbol	Condition	Rating			Units
				Min.	Typ.	Max.	
Reset time		t_R		—	—	2.0	us
Reset "L" pulse width	/RES	t_{RW}		2.0	—	—	us

(V_{DD} = 1.8V , Ta = –40 to 85°C)

Item	Signal	Symbol	Condition	Rating			Units
				Min.	Typ.	Max.	
Reset time		t_R		—	—	3.0	us
Reset "L" pulse width	/RES	t_{RW}		3.0	—	—	us

8、直流特性（VDD=2.84V）

Unless otherwise specified, Vss = 0 V, VDD = 3.0 V ± 10%, Ta = –40 to 85°C

Item		Symbol	Condition	Rating Min.	Rating Typ.	Rating Max.	Units	Applicable Pin
Operating Voltage (1)		VDD		1.8	—	3.3	V	Vss*1
Operating Voltage (2)		VDD2	(Relative to Vss)	2.4	—	3.3	V	Vss
High-level Input Voltage		VIHC		0.8 x VDD	—	VDD	V	*3
Low-level Input Voltage		VILC		Vss	—	0.2 x VDD	V	*3
High-level Output Voltage		VOHC	IOH = –0.5 mA	0.8 x VDD	—	VDD	V	*4
Low-level Output Voltage		VOLC	IOL = 0.5 mA	Vss	—	0.2 x VDD	V	*4
Input leakage current		ILI	VIN = VDD or Vss	–1.0	—	1.0	μA	*5
Output leakage current		ILO	VIN = VDD or Vss	–3.0	—	3.0	μA	*6
Liquid Crystal Driver ON Resistance		RON	Ta = 25°C (Relative To VDD), V0 = 13.0 V	—	2.0	3.5	KΩ	SEGn COMn *7
			Ta = 25°C (Relative To VDD), V0 = 8.0 V	—	3.2	5.4	KΩ	SEGn COMn *7
Static Consumption Current		ISSQ	V0 = 13.0 V(Relative To VDD)	—	0.01	2	μA	VDD, VDD2
Output Leakage Current		ISQ	V0 = 13.0 V(Relative To VDD)	—	0.01	10	μA	V0
Input Terminal Capacitance		CIN	Ta = 25°C , f = 1 MHz	—	5.0	8.0	pF	
Oscillator Frequency	Internal Oscillator	fOSC	1/65 duty 1/33 duty Ta = 25°C	17	20	24	kHz	*8
	External Input	fCL	1/65 duty 1/33 duty Ta = 25°C	17	20	24	kHz	CL
	Internal Oscillator	fOSC	1/49 duty 1/53 duty 1/55 duty Ta = 25°C	25	30	35	kHz	*8
	External Input	fCL	1/49 duty 1/53 duty 1/55 duty Ta = 25°C	25	30	35	kHz	CL

Item		Symbol	Condition	Rating Min.	Rating Typ.	Rating Max.	Units	Applicable Pin
Internal Power	Input voltage	VDD2	(Relative To Vss)	2.4	—	3.3	V	Vss
	Supply Step-up output voltage Circuit	VOUT	(Relative To Vss)	—	—	16.0	V	VOUT
	Voltage regulator Circuit Operating Voltage	VOUT	(Relative To Vss)	6.0	—	16.0	V	VOUT
	Voltage Follower Circuit Operating Voltage	V0	(Relative To Vss)	4.0	—	13.0	V	V0 * 9
	Base Voltage	VR	Ta = 25°C , (Relative To Vss) –0.01%/°C	2.07	2.10	2.13	V	*10

9、引脚描述

接口定义：

引脚编号	引脚名称	方向	引脚功能描述
1	VSS	I	逻辑电源地 0V
2	VDD	I	逻辑电源正 3.3V
3	NC（V0）	I	悬空
4	A0	-	数据/指令选择：高电平：DB0-DB7 为显示数据 低电平：DB0-DB7 为操作指令
5	R/W（/WR）	I	读/写控制脚：当接口定义为 6800 接口时，R/W=H：读操作 R/W=L：写操作 当接口定义为 8080 接口时，/WR 为写入控制脚
6	E（/RD）	I	当接口定义为 6800 接口时，为使能控制脚，E=H 有效 当接口定义为 8080 接口时，/RD 为读控制脚，低有效
7	DB0	I/O	数据输入输出引脚
8	DB1	I/O	数据输入输出引脚
9	DB2	I/O	数据输入输出引脚
10	DB3	I/O	数据输入输出引脚
11	DB4	I/O	数据输入输出引脚
12	DB5	I/O	数据输入输出引脚
13	DB6	I/O	数据输入输出引脚
14	DB7	I/O	数据输入输出引脚
15	/CS1	I	片选择信号，低电平时有
16	NC	-	悬空
17	/RST	-	复位信号，低电平有效
18	NC（VEE）	O	悬空
19	LED+	I	背光电源,LED+（3.3V）
20	LED-	I	背光电源,LED-（0V）

10、命令描述

指令表：

Command	Command Code										Function
	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	
(1) Display ON/OFF	0	1	0	1	0	1	0	1	1	1	0 1	LCD display ON/OFF 0: OFF, 1: ON
(2) Display start line set	0	1	0	0	1	Display start address						Sets the display RAM display start line address
(3) Page address set	0	1	0	1	0	1	1	Page address				Sets the display RAM page address
(4) Column address set upper bit Column address set lower bit	0 0	1 1	0 0	0 0	0 0	0 0	1 0	Most significant column address Least significant column address				Sets the most significant 4 bits of the display RAM column address. Sets the least significant 4 bits of the display RAM column address.
(5) Status read	0	0	1	Status				0	0	0	0	Reads the status data
(6) Display data write	1	1	0	Write data								Writes to the display RAM
(7) Display data read	1	0	1	Read data								Reads from the display RAM
(8) ADC select	0	1	0	1	0	1	0	0	0	0	0 1	Sets the display RAM address SEG output correspondence 0: normal, 1: reverse
(9) Display normal/ reverse	0	1	0	1	0	1	0	0	1	1	0 1	Sets the LCD display normal/ reverse 0: normal, 1: reverse
(10) Display all points ON/OFF	0	1	0	1	0	1	0	0	1	0	0 1	Display all points 0: normal display 1: all points ON
(11) LCD bias set	0	1	0	1	0	1	0	0	0	1	0 1	Sets the LCD drive voltage bias ratio 0: 1/9 bias, 1: 1/7 bias (ST7565P)
(12) Read/modify/write	0	1	0	1	1	1	0	0	0	0	0	Column address increment At write: +1 At read: 0
(13) End	0	1	0	1	1	1	0	1	1	1	0	Clear read/modify/write
(14) Reset	0	1	0	1	1	1	0	0	0	1	0	Internal reset
(15) Common output mode select	0	1	0	1	1	0	0	0 1	*	*	*	Select COM output scan direction 0: normal direction 1: reverse direction
(16) Power control set	0	1	0	0	0	1	0	1	Operating mode			Select internal power supply operating mode
(17) V_0 voltage regulator internal resistor ratio set	0	1	0	0	0	1	0	0	Resistor ratio			Select internal resistor ratio(Rb/Ra) mode
(18) Electronic volume mode set Electronic volume register set	0	1	0	1 0	0 0	0 Electronic volume value	0	0	0	0	1	Set the V_0 output voltage electronic volume register
(19) Static indicator ON/OFF Static indicator register set	0	1	0	1 0	0 0	1 0	0 0	1 0	1 0	0 0	0 1 Mode	0: OFF, 1: ON Set the flashing mode
(20) Booster ratio set	0	1	0	1 0	1 0	1 0	1 0	1 0	0 0	0 step-up value	0	select booster ratio 00: 2x,3x,4x 01: 5x 11: 6x
(21) Power saver												Display OFF and display all points ON compound command
(22) NOP	0	1	0	1	1	1	0	0	0	1	1	Command for non-operation
(23) Test	0	1	0	1	1	1	1	*	*	*	*	Command for IC test. Do not use this command

指令介绍：

Display ON/OFF

This command turns the display ON and OFF.

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0	Setting
0	1	0	1	0	1	0	1	1	1	1	Display ON
										0	Display OFF

When the display OFF command is executed when in the display all points ON mode, power saver mode is entered. See the section on the power saver for details.

Display Start Line Set

This command is used to specify the display start line address of the display data RAM shown in Figure 4. For further details see the explanation of this function in "The Line Address Circuit".

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0	Line address
0	1	0	0	1	0	0	0	0	0	0	0
					0	0	0	0	0	1	1
					0	0	0	0	1	0	2
								↓			↓
					1	1	1	1	1	0	62
					1	1	1	1	1	1	63

Page Address Set

This command specifies the page address corresponding to the low address when the MPU accesses the display data RAM (see Figure 4). Specifying the page address and column address enables to access a desired bit of the display data RAM. Changing the page address does not accompany a change in the status display.

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0	Page address
0	1	0	1	0	1	1	0	0	0	0	0
							0	0	0	1	1
							0	0	1	0	2
								↓			↓
							0	1	1	1	7
							1	0	0	0	8

Column Address Set

This command specifies the column address of the display data RAM shown in Figure 4. The column address is split into two sections (the higher 4 bits and the lower 4 bits) when it is set (fundamentally, set continuously). Each time the display data RAM is accessed, the column address automatically increments (+1), making it possible for the MPU to continuously read from/write to the display data. The column address increment is topped at 83H. This does not change the page address continuously. See the function explanation in "The Column Address Circuit," for details.

	A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0	A7	A6	A5	A4	A3	A2	A1	A0	Column address
High bits →	0	1	0	0	0	0	1	A7	A6	A5	A4	0	0	0	0	0	0	0	0	0
Low bits →							0	A3	A2	A1	A0	0	0	0	0	0	0	0	1	1
												0	0	0	0	0	0	1	0	2
																↓				↓
												1	0	0	0	0	0	1	0	130
												1	0	0	0	0	0	1	1	131

Status Read

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	BUSY	ADC	ON/OFF	RESET	0	0	0	0

BUSY	BUSY = 1: it indicates that either processing is occurring internally or a reset condition is in process. BUSY = 0: A new command can be accepted . if the cycle time can be satisfied, there is no need to check for BUSY conditions.
ADC	This shows the relationship between the column address and the segment driver. 0: Normal (column address n ↔ SEG n) 1: Reverse (column address 131-n ↔ SEG n) (The ADC command switches the polarity.)
ON/OFF	ON/OFF: indicates the display ON/OFF state. 0: Display ON 1: Display OFF (This display ON/OFF command switches the polarity.)
RESET	This indicates that the chip is in the process of initialization either because of a /RES signal or because of a reset command. 0: Operating state 1: Reset in progress

Display Data Write

This command writes 8-bit data to the specified display data RAM address. Since the column address is automatically incremented by "1" after the write, the MPU can write the display data.

	E	R/W	
A0	/RD	/WR	D7 D6 D5 D4 D3 D2 D1 D0
1	1	0	Write data

Display Data Read

This command reads 8-bit data from the specified display data RAM address. Since the column address is automatically incremented by "1" after the read, the CPU can continuously read multiple-word data. One dummy read is required immediately after the column address has been set. See the function explanation in "Display Data RAM" for the explanation of accessing the internal registers. When the serial interface is used, reading of the display data becomes unavailable.

	E	R/W	
A0	/RD	/WR	D7 D6 D5 D4 D3 D2 D1 D0
1	0	1	Read data

ADC Select (Segment Driver Direction Select)

This command can reverse the correspondence between the display RAM data column address and the segment driver output. Thus, sequence of the segment driver output pins may be reversed by the command. See the column address circuit for the detail. Increment of the column address (by "1") accompanying the reading or writing the display data is done according to the column address indicated in Figure 4.

	E	R/W								
A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Setting
0	1	0	1	0	1	0	0	0	0	0	Normal
										1	Reverse

Display Normal/Reverse

This command can reverse the lit and unlit display without overwriting the contents of the display data RAM. When this is done the display data RAM contents are maintained.

	E	R/W								
A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Setting
0	1	0	1	0	1	0	0	1	1	0	RAM Data "H" LCD ON voltage (normal)
										1	RAM Data "L" LCD ON voltage (reverse)

When the display is in an OFF mode, executing the display all points ON command will place the display in power save mode. For details, see the Power Save section.

LCD Bias Set

This command selects the voltage bias ratio required for the liquid crystal display.

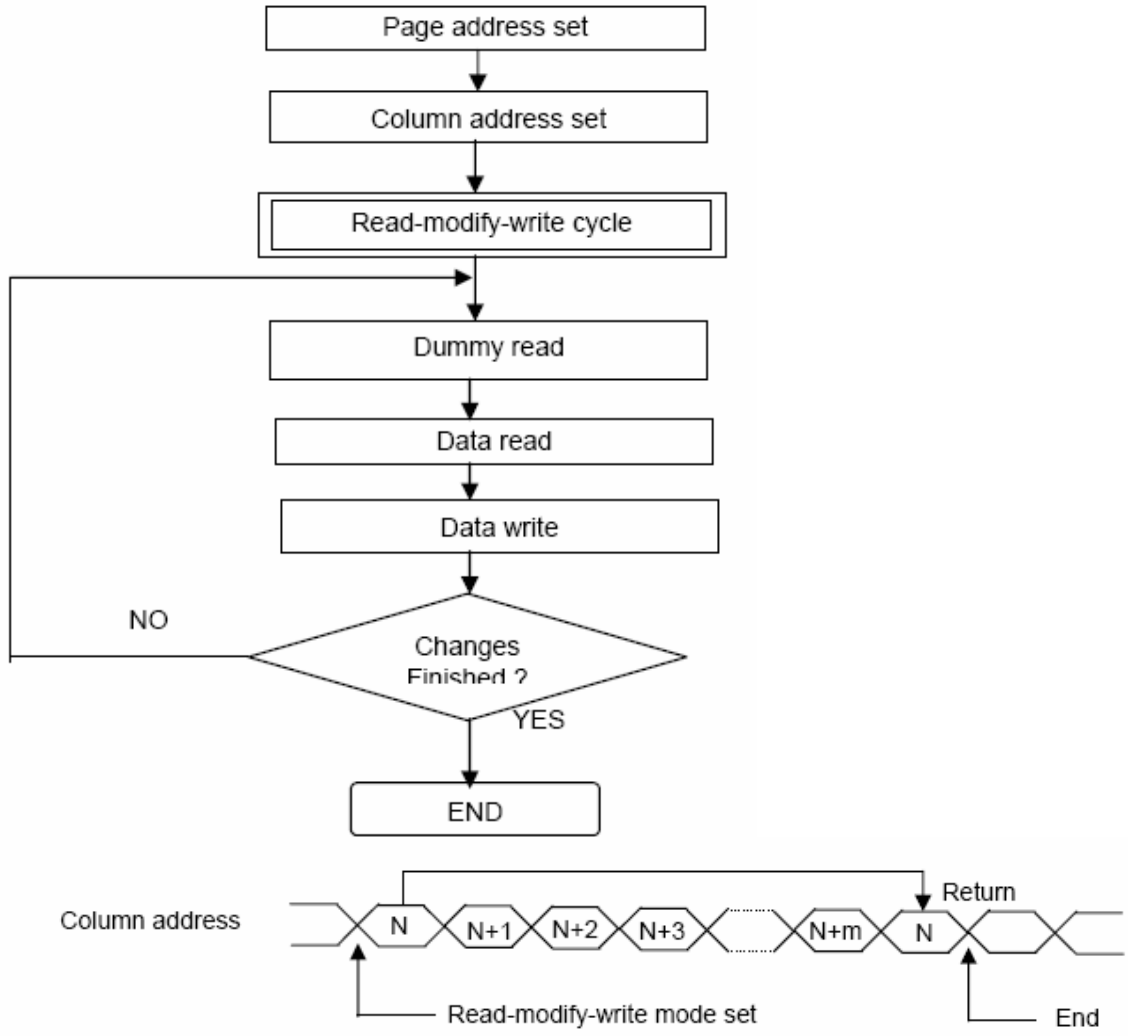
A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0	Select Status 1/65duty	1/49duty	1/33duty	1/55duty	1/53duty
0	1	0	1	0	1	0	0	0	1	0	1/9 bias	1/8 bias	1/6 bias	1/8 bias	1/8 bias
										1	1/7 bias	1/6 bias	1/5 bias	1/6 bias	1/6 bias

Read/Modify/Write

This command is used paired with the "END" command. Once this command has been input, the display data read command does not change the column address, but only the display data write command increments (+1) the column address. This mode is maintained until the END command is input. When the END command is input, the column address returns to the address it was at when the read/modify/write command was entered. This function makes it possible to reduce the load on the MPU when there are repeating data changes in a specified display region, such as when there is a blanking cursor.

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	0	0

* Even in read/modify/write mode, other commands aside from display data read/write commands can also be used.



End

This command releases the read/modify/write mode, and returns the column address to the address it was at when the mode was entered.

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	1	1	1	0

Reset

This command initializes the display start line, the column address, the page address, the common output mode, the Vo voltage regulator internal resistor ratio, the electronic volume, and the static indicator are reset, and the read/modify/write mode and test mode are released. There is no impact on the display data RAM. See the function explanation in "Reset" for details.
The reset operation is performed after the reset command is entered.

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	1	0

The initialization when the power supply is applied must be done through applying a reset signal to the /RES terminal. The reset command must not be used instead.

Common Output Mode Select

This command can select the scan direction of the COM output terminal. For details, see the function explanation in "Common Output Mode Select Circuit."

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0	Selected Mode	1/65duty	1/49duty	1/33duty	1/55duty	1/53duty
0	1	0	1	1	0	0	0	*	*	*	Normal	COM0→COM63	COM0→COM47	COM0→COM31	COM0→COM53	COM0→COM51
							1				Reverse	COM63→COM0	COM47→COM0	COM31→COM0	COM53→COM0	COM51→COM0

* Disabled bit

Power Controller Set

This command sets the power supply circuit functions. See the function explanation in "The Power Supply Circuit," for details

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0	Selected Mode
0	1	0	0	0	1	0	1	0			Booster circuit: OFF
								1			Booster circuit: ON
									0		Voltage regulator circuit: OFF
									1		Voltage regulator circuit: ON
										0	Voltage follower circuit: OFF
										1	Voltage follower circuit: ON

V0 Voltage Regulator Internal Resistor Ratio Set

This command sets the Vo voltage regulator internal resistor ratio. For details, see the function explanation is "The Voltage Regulator circuit " and table 11 .

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0	Rb/Ra Ratio
0	1	0	0	0	1	0	0	0	0	0	Small
								0	0	1	
								0	1	0	
									↓		↓
								1	1	1	
								1	1	1	Large

The Electronic Volume (Double Byte Command)

This command makes it possible to adjust the brightness of the liquid crystal display by controlling the LCD drive voltage V0 through the output from the voltage regulator circuits of the internal liquid crystal power supply. This command is a two byte command used as a pair with the electronic volume mode set command and the electronic volume register set command, and both commands must be issued one after the other.

The Electronic Volume Mode Set

When this command is input, the electronic volume register set command becomes enabled. Once the electronic volume mode has been set, no other command except for the electronic volume register command can be used. Once the electronic volume register set command has been used to set data into the register, then the electronic volume mode is released.

	E	R/W							
A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	0	0	0	0	0	1

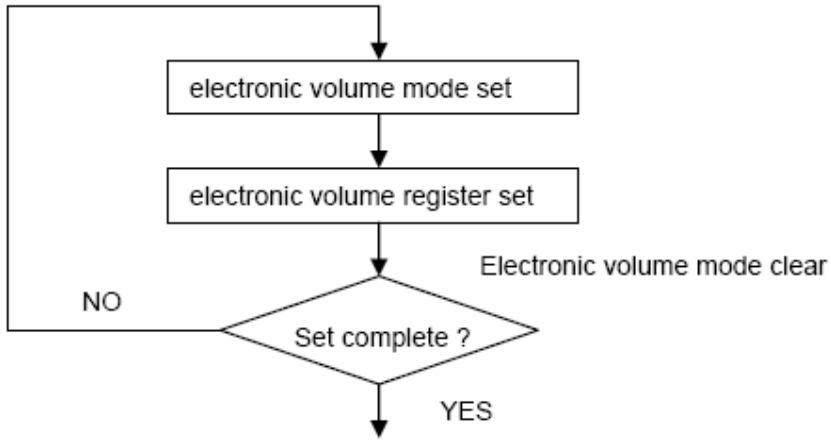
Electronic Volume Register Set

By using this command to set six bits of data to the electronic volume register, the liquid crystal drive voltage V0 assumes one of the 64 voltage levels.
When this command is input, the electronic volume mode is released after the electronic volume register has been set.

	E	R/W								
A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	| V0 |
0	1	0	*	*	0	0	0	0	0	1	Small
			*	*	0	0	0	0	1	0	
			*	*	0	0	0	0	1	1	
							↓				↓
			*	*	1	1	1	1	1	0	
			*	*	1	1	1	1	1	1	Large

* Inactive bit (set "0")
When the electronic volume function is not used, set this to (1, 0, 0, 0, 0, 0)

The Electronic Volume Register Set Sequence



Static Indicator (Double Byte Command)

This command controls the static drive system indicator display. The static indicator display is controlled by this command only, and is independent of other display control commands.
This is used when one of the static indicator liquid crystal drive electrodes is connected to the FR terminal, and the other is connected to the FRS terminal. A different pattern is recommended for the static indicator electrodes than for the dynamic drive electrodes. If the pattern is too close, it can result in deterioration of the liquid crystal and of the electrodes.
The static indicator ON command is a double byte command paired with the static indicator register set command, and thus one must execute one after the other. (The static indicator OFF command is a single byte command.)

Static Indicator ON/OFF

When the static indicator ON command is entered, the static indicator register set command is enabled. Once the static indicator ON command has been entered, no other command aside from the static indicator register set command can be used. This mode is cleared when data is set in the register by the static indicator register set command.

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0	Static Indicator
0	1	0	1	0	1	0	1	1	0	0	OFF
										1	ON

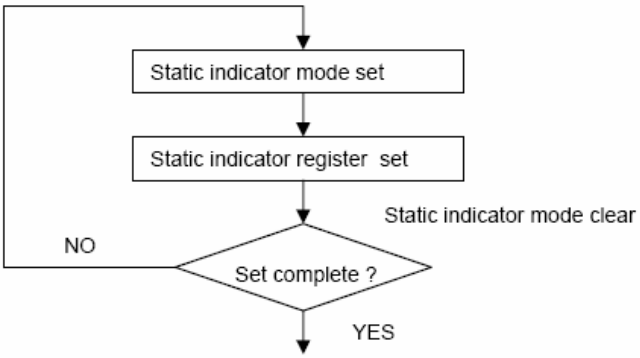
Static Indicator Register Set

This command sets two bits of data into the static indicator register, and is used to set the static indicator into a blinking mode

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0	Indicator Display State
0	1	0	*	*	*	*	*	*	0	0	OFF
									0	1	ON (blinking at approximately one second intervals)
									1	0	ON (blinking at approximately 0.5 second intervals)
									1	1	ON (constantly on)

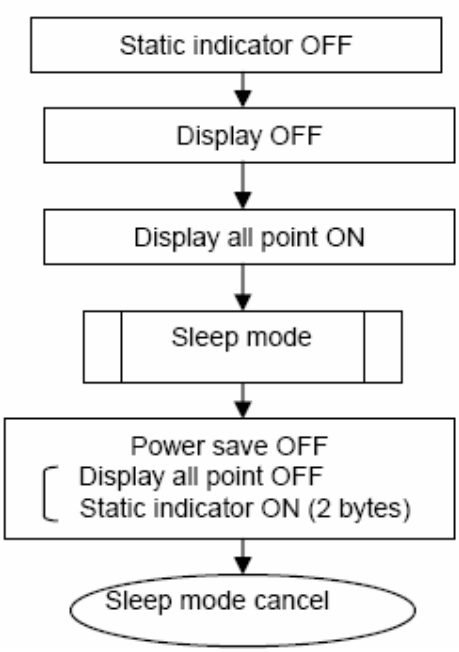
* Disabled bit (set "0")

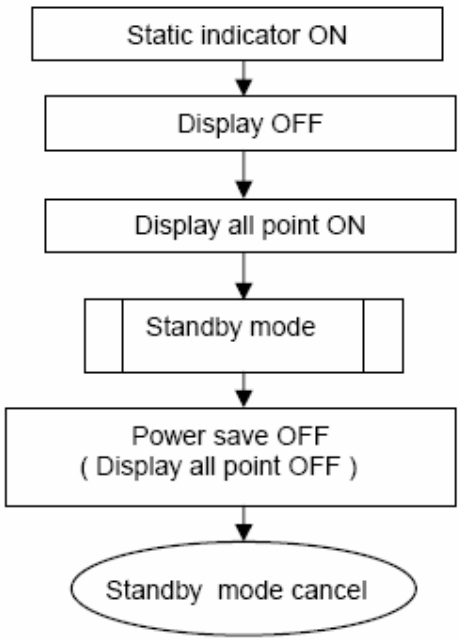
Static Indicator Register Set Sequence



Power Save (Compound Command)

When the display all points ON is performed while the display is in the OFF mode, the power saver mode is entered, thus greatly reducing power consumption.
The power saver mode has two different modes: the sleep mode and the standby mode. When the static indicator is OFF, it is the sleep mode that is entered. When the static indicator is ON, it is the standby mode that is entered.
In the sleep mode and in the standby mode, the display data is saved as is the operating mode that was in effect before the power saver mode was initiated, and the MPU is still able to access the display data RAM.
Refer to figure 28 for power save off sequence.





Sleep Mode

This stops all operations in the LCD display system, and as long as there are no accesses from the MPU, the consumption current is reduced to a value near the static current. The internal modes during sleep mode are as follows:
1. The oscillator circuit and the LCD power supply circuit are halted.
2. All liquid crystal drive circuits are halted, and the segment in common drive outputs output a Vss level.

Standby Mode

The duty LCD display system operations are halted and only the static drive system for the indicator continues to operate, providing the minimum required consumption current for the static drive. The internal modes are in the following states during standby mode.
1 The LCD power supply circuits are halted. The oscillator circuit continues to operate.
2 The duty drive system liquid crystal drive circuits are halted and the segment and common driver outputs output a Vss level. The static drive system does not operate.
When a reset command is performed while in standby mode, the system enters sleep mode.
* When an external power supply is used, it is recommended that the functions of the external power supply circuit be stopped when the power saver mode is started. For example, when the various levels of liquid crystal drive voltage are provided by external resistive voltage dividers, it is recommended that a circuit be added in order to cut the electrical current flowing through the resistive voltage divider circuit when the power saver mode is in effect. The ST7565P series chips have a liquid crystal display blanking control terminal /DOF. This terminal enters an "L" state when the power saver mode is launched. Using the output of /DOF, it is possible to stop the function of an external power supply circuit.
* When the master is turned on, the oscillator circuit is operable immediately after the powering on.

The Booster Ratio (Double Byte Command)

This command makes it possible to select step-up ratio. It is used when the power control set have turn on the internal booster circuit. This command is a two byte command used as a pair with the booster ratio select mode set command and the booster ratio register set command, and both commands must be issued one after the other.

Booster Ratio Select Mode Set

When this command is input, the Booster ratio register set command becomes enabled. Once the booster ratio select mode has been set, no other command except for the booster ratio register command can be used. Once the booster ratio register set command has been used to set data into the register, then the booster ratio select mode is released.

	E	R/W							
A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	1	1	0	0	0

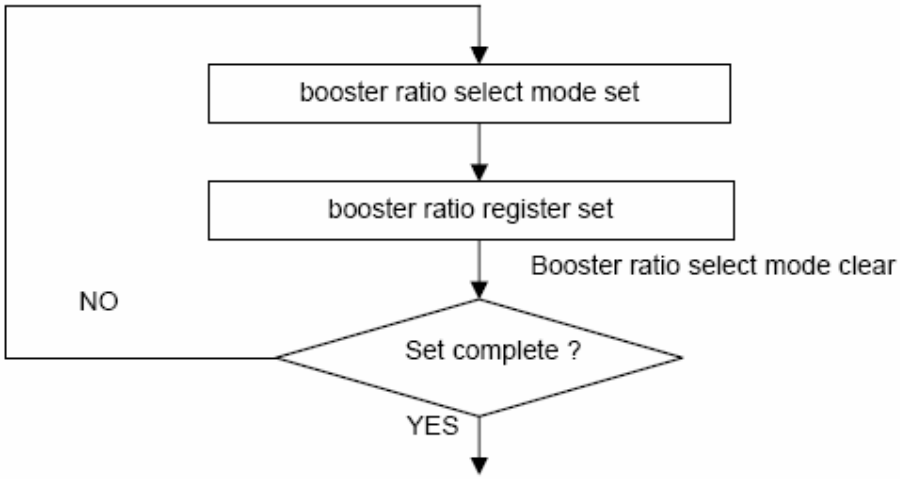
Booset Ratio Register Set

By using this command to set two bits of data to the booster ratio register, it can be select what kind of the booster ratio can be used.
When this command is input, the booster ratio select mode is released after the booster ratio register has been set.

	E	R/W								
A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Booster ratio select
0	1	0	*	*	*	*	*	*	0	0	2x,3x,4x
			*	*	*	*	*	*	0	1	5x
			*	*	*	*	*	*	1	1	6x

* Inactive bit (set "0")
When the booster ratio select function is not used, set this to (0, 0) 2x,3x,4x step-up mode

The booster ratio Register Set Sequence



NOP

Non-Operation Command

	E	R/W							
A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	1	1

Test

This is a command for IC chip testing. Please do not use it. If the test command is used by accident, it can be cleared by applying a "L" signal to the /RES input by the reset command or by using an NOP.

	E	R/W							
A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	1	1	1	*	*

* Inactive bit

Note: The ST7565P maintain their operating modes until something happens to change them. Consequently, excessive external noise, etc., can change the internal modes of the ST7565P . Thus in the packaging and system design it is necessary to suppress the noise or take measure to prevent the noise from influencing the chip. Moreover, it is recommended that the operating modes be refreshed periodically to prevent the effects of unanticipated noise.

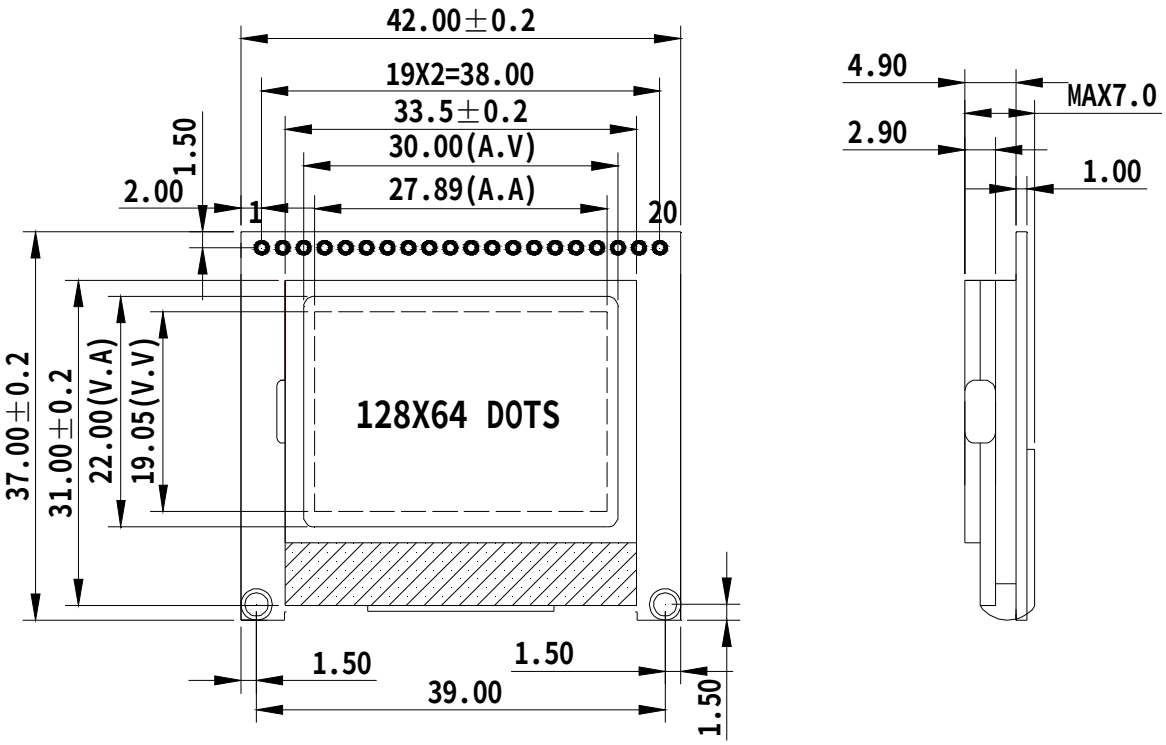
11、附录

初始化程序参考：

```
//忙检测
void check_busy(void)
{
uchar read_data=0xff;
data_bus=0xff;
LCD_RS=0;
LCD_RW=1;                //读命令
LCD_CS1=0;               //片使能
   while(read_data&0x80)
   {
      LCD_E=1;
      _nop_();
      _nop_();
      read_data=data_bus;
      LCD_E=0;
   }
   LCD_E=0;
   LCD_CS1=1;                //片禁能
}

//写命令到寄存器
void send_cmd(uchar cmd) small
{
   check_busy();
   LCD_RS=0;
   LCD_RW=0;                //写命令
   LCD_CS1=0;               //片使能
   data_bus=cmd;
   LCD_E=1;
   _nop_();
   _nop_();
   LCD_E=0;
   _nop_();
   _nop_();
   LCD_CS1=1;                //片禁能
}

//写数据到 DDRAM
void send_dat(uchar dat) small
{
   check_busy();
   LCD_RS=1;
   LCD_RW=0;                //写数据
```

```
    LCD_CS1=0;              //片使能
    data_bus=dat;
    LCD_E=1;
    _nop_();
    _nop_();
    LCD_E=0;
    _nop_();
    _nop_();
    LCD_CS1=1;              //片禁能
}

//初始化
void lcd_initial(void)
{
    LCD_RES=1;
    delay_nms(50);
    send_cmd(0xE2);
    send_cmd(0xA3);
    send_cmd(0xA0);
    send_cmd(0xC8);
    send_cmd(0x24);
    send_cmd(0x81);
    send_cmd(0x14);
    send_cmd(0x2C);
    send_cmd(0x2E);
    send_cmd(0x2F);
    send_cmd(0x40);
    send_cmd(0xB0);
    send_cmd(0x10);
    send_cmd(0x00);
    send_cmd(0xAF);
}
```

模块外形图



J1 接口定义

1	2	3	4	5	6	7	8	9	10
VSS	VDD	NC（V0）	A0	R/（/WR）	E（/RD）	DB0	DB1	DB2	DB3
11	12	13	14	15	16	17	18	19	20
DB4	DB5	DB6	DB7	/CS1	NC	/RST	NC（VEE）	LED+	LED-