STM8S208xx/STM8S207xx Errata sheet

STM8S performance line revision X device limitations

Silicon identification

This errata sheet applies to the revision X of the STMicroelectronics STM8S performance line products.

The full list of root part numbers is shown in *Table 2*.

The products are identifiable as shown in *Table 1*:

- by the Revision code marked below the Sales Type on the device package
- by the last three digits of the Internal Sales Type printed on the box label

Table 1. Device identification

Sales type	Revision code(1) marked on device
STM8S207xxxx	X
STM8S208xxxx	X

1. Refer to *Appendix A: Revision code on device marking* for details on how to identify the Revision code on the different packages.

Table 2. Device summary

Reference	Part number
STM8S207xx	STM8S207MB, STM8S207RB, STM8S207R8, STM8S207R6, STM8S207CB, STM8S207C8, STM8S207S8, STM8S207K6
STM8S208xx	STM8S208MB, STM8S208RB

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1 Product evolution

This table summarizes the fix status.

Table 3. Product evolution summary

Section	Limitation	Status
Section 2.1	*HSI RC oscillator cannot be switched off in RUN mode*	No fix planned
Section 2.2	*LSI oscillator remains ON during Active Halt mode (MVR ON) when AWU uses HSE/Div as input clock*	
Section 2.3	*TIM1_CH4 mapped on PC4 and PD7 ports by AFR4 option*	
Section 2.4	*UART PE flag cannot be cleared during reception of first half of Stop bit*	Workaround available

2 Silicon limitations

2.1 HSI RC oscillator cannot be switched off in RUN mode

Description

The HSI RC oscillator cannot be switched off in Run mode. This causes negligible extra power consumption compared to the total consumption of the MCU in Run mode.

Workaround

No workaround available.

2.2 LSI oscillator remains ON during Active Halt mode (MVR ON) when AWU uses HSE/Div as input clock

Description

The LSI RC oscillator is not switched off in Active Halt mode with main voltage regulator (MVR) on, when the AWU uses high speed external clock divided by prescaler (HSE/Div) (clock source option enabled by CKAWUSEL option bit). This causes negligible extra power consumption compared to the total consumption of the MCU in Active Halt mode with main voltage regulator (MVR) on.

Workaround

No workaround available.

2.3 TIM1_CH4 mapped on PC4 and PD7 ports by AFR4 option

Description

Timer 1 channel 4 (TIM1_CH4) is available both on pin PC4 and PD7 when the alternate function remapping AFR4 option bit is set.

Workaround

No workaround available. It is recommended to only use the AFR4 Alternate function remapping option for the 44-pin package where PC4 is not present.

2.4 UART PE flag cannot be cleared during reception of first half of Stop bit

Description

When the UART is in reception mode and a parity error (PE) occurs, the PE flag is set by hardware. This flag cannot be cleared during the first half of the Stop bit period. If software tries to clear the PE flag at this time, the flag is set again by hardware, generating an unwanted interrrupt if the PIEN bit is set in the UART_CR1 register.

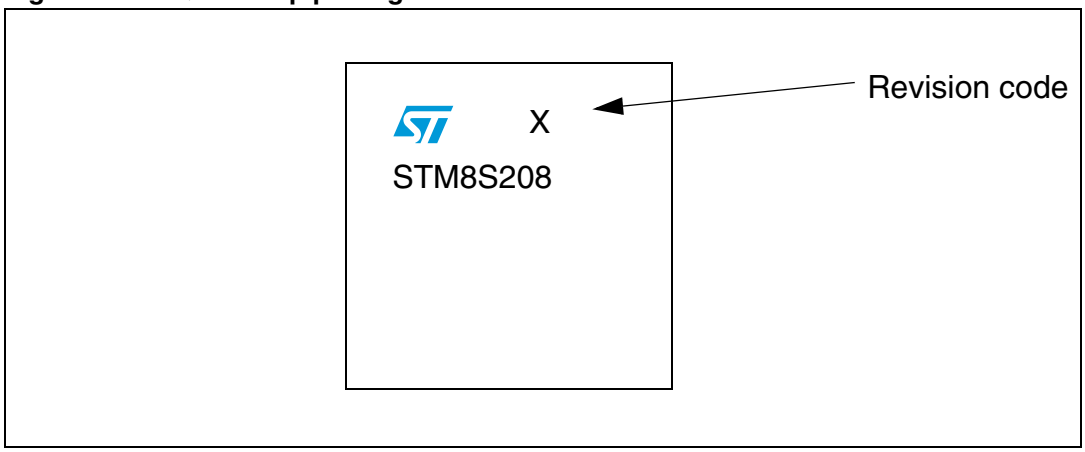
Workaround

Disable PE interrupts and, after the RXNE bit is set, use polling to manage the PE flag. For example, this could be done in the RXNE interrupt service routine.

Appendix A Revision code on device marking

Figure 1 shows the marking compositions for the LQFP80 package.

Figure 1. LQFP80 top package view



Revision history

Table 4. Document revision history

Date	Revision	Changes
04-Dec-2008	1	Initial revision

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