Analog - Voltage-to-Frequency Converter

AN2161

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Associated Project: Yes
Associated Part Family: CY8C24xxx, CY8C27xxx
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Software Version: PSoC Designer™ 4.0
Associated Application Notes: AN2041, AN2044

Application Note Abstract

This Application Note demonstrates how to build a voltage-to-frequency converter using one continuous time PSoC® block and one switched capacitor PSoC block. The converter does not utilize the CPU during operation.

Introduction

Voltage-to-frequency (V/F) converters are widely used in industrial electronics, frequency-shift keying modulators, phase-locked loop systems, analog-to-digital converters, isolation amplifiers, etc. Even though these converters are produced as standalone devices, they still require several external components and are relatively expensive compared to modern low-cost analog integrated circuits.

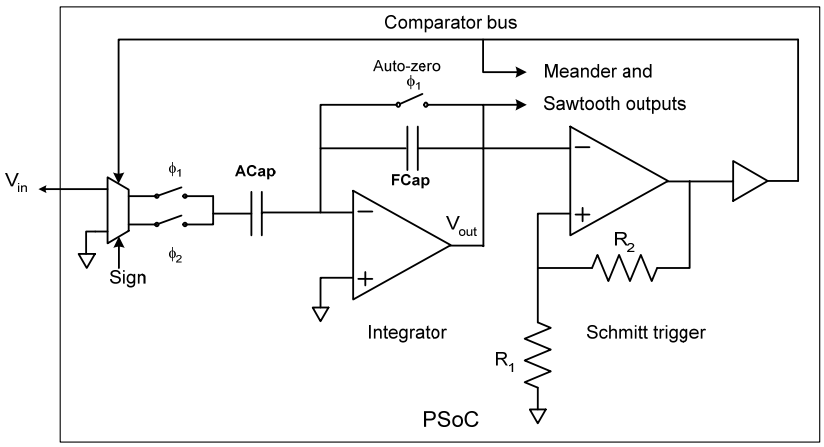
PSoC allows the designer to build the V/F using only one continuous time (CT) analog block and one switched capacitor (SC) analog block without any external analog components. All digital blocks, and the CPU, are at user disposal. The designer will get a useful device function with virtually no additional cost or extra components.

Moreover, the proposed V/F converter produces both meander and symmetric sawtooth signals, which are useful for applications such as analog PWM modulators and capacitance meters.

Converter Operation Theory

The converter, shown in the block diagram of Figure 1, consists of a reversible integrator and a Schmitt trigger. The integrator has been built around a type C SC block with an analog modulator. The Schmitt trigger has been built using a CT block with internal resistors. For more details about SC block operation, please refer to Application Notes AN2041 “Understanding Switched Capacitor Analog Blocks” and AN2044 “Signal Rectification, Using Switched Capacitor Modulators.”

Figure 1. Converter Block Diagram



The integrator output voltage is determined by its output voltage from the previous sample and the state of the Schmitt trigger. The sign bit in the SC block is set to 1, which makes the integrator gain negative. The output state of the Schmitt trigger follows the polarity of the integrator output. When the Schmitt trigger output is negative, each column sample clock period decreases the integrator output voltage, V_{out}, by ΔV. This increment is determined by the input voltage, V_{in}, and the block Acap-to-Fcap ratio:

$$\Delta V = V_{in} \frac{ACap}{FCap} \qquad \text{Equation 1}$$

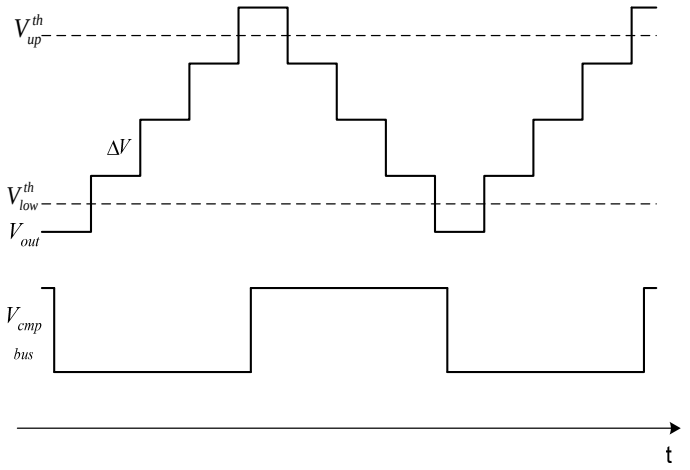
When V_{out} reaches the lower Schmitt trigger threshold, V^{th}_{low}, the trigger switches to the opposite state, driving the comparator bus high. This changes the integrator input voltage sign, causing the integrator signal to rise with the same ΔV at each column sample clock period. This process will continue until the integrator signal reaches the Schmitt trigger upper threshold value, V^{th}_{up}. At this point, the trigger drives the comparator bus low again, and the process repeats.

The Schmitt trigger thresholds are determined by supply voltage, selected analog ground and the ratio of the internal resistors. The Schmitt trigger thresholds, V^{th}_{low} and V^{th}_{up}, are calculated easily using Equation 2 (all voltages are AGND related).

$$V^{th}_{low} = \frac{R_1}{R_1 + R_2} - V_{AGND};$$
$$V^{th}_{up} = \frac{R_1}{R_1 + R_2}\left(V_{dd} - V_{AGND}\right) \qquad \text{Equation 2}$$

The SC integrator is a discrete system, in that the integrator output voltage can only be changed during discrete time intervals. To switch the Schmitt trigger, the integrator signal should be greater than or equal to the trigger threshold. This results in two additional integration column sample clock periods for each output signal, half-period integration time. This is shown in Figure 2.

Figure 2. Converter Operation



The upper bound, N_{sup}, and the lower bound, N_{inf}, for half-period integration time in units of column sample cycles can be estimated by using the following equations:

$$N_{sup} = \left[\frac{V^{th}_{up} - V^{th}_{low}}{\Delta V}\right] + 2; \quad N_{inf} = \left[\frac{V^{th}_{up} - V^{th}_{low}}{\Delta V}\right] \qquad \text{Equation 3}$$

The [ ] denote the integer part. The sample period for the SC block is the column clock signal, divided by 4, or:

$$T_i = \frac{4}{F_c} \qquad \text{Equation 4}$$

F_c is the column frequency. Supposing $N_{inf} >> 2$, $N_{cyc} = N_{inf} \sim N_{sup}$.

This takes into account that a single period total integration time is a doubled half-period time:

$$T_{out} = 2T_i \cdot N_{cyc} \qquad \text{Equation 5}$$

Combining Equations (1) – (5), the converter output frequency is given by:

$$F_{out} = \frac{F_c}{8} \cdot \left(1 + \frac{R_2}{R_1}\right) \cdot \frac{ACap}{FCap} \cdot \frac{V_{in}}{V_{dd} - V_1 - V_0} \qquad \text{Equation 6}$$

Note It is useful to substitute:

$$\beta = \left(1 + \frac{R_2}{R_1}\right)^{-1} \qquad \text{Equation 7}$$

This is because β can be assigned as a ***RefValue*** parameter in PSoC Designer when a programmable threshold comparator is used as a Schmitt trigger building block. So, the final expression for the V/F output frequency, F_{out}, is given by:

$$F_{out} = \frac{F_c}{8\beta} \cdot \frac{ACap}{FCap} \cdot \frac{V_{in}}{V_{dd} - V_1 - V_0} \qquad \text{Equation 8}$$

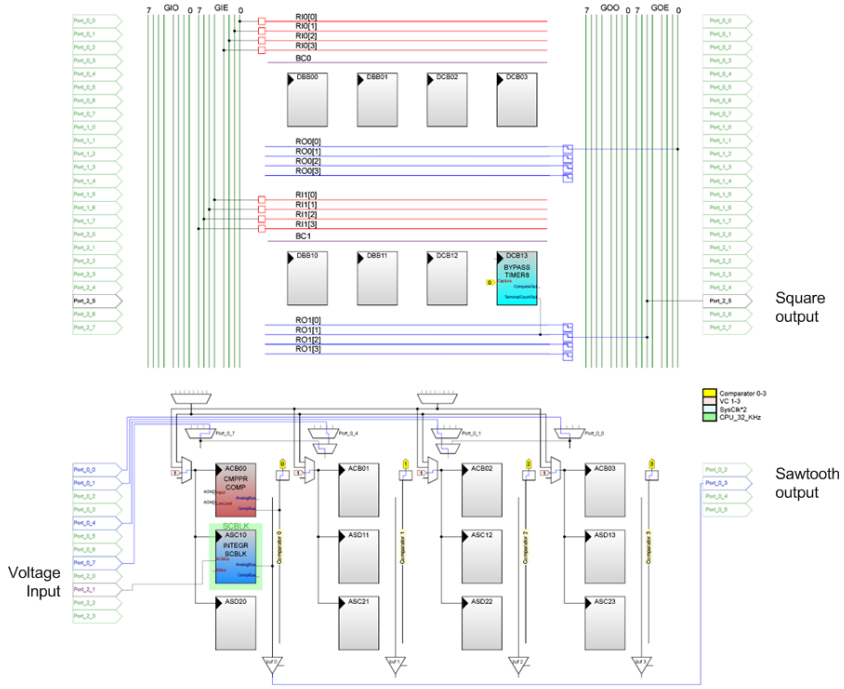
A more accurate expression for V/F converter output frequency can be obtained using the value of N_{inf} for an output signal half-period integration time estimation:

$$F_{out} = \frac{F_c}{8} \left\{ \beta \frac{V_{dd} - V_1 - V_0}{V_{in}} \frac{FCap}{ACap} + 2 \right\}^{-1} \qquad \text{Equation 9}$$

PSoC Implementation

The V/F converter placement is shown in Figure 3. The converter has been placed in the *Column_0*. The programmable threshold comparator has been used to make the Schmitt trigger. The feedback resistors were rerouted manually in the firmware to the non-inverting operational amplifier input. The inverting input was directly connected to the integrator output. Because the integrator uses auto-zero mode, the SC output alternates between demanded output value and the AGND level for each clock period. However, the integrator has no influence on converter operation due to Schmitt trigger hysteresis. The designer can disable auto-zero mode in the integrator when neither sawtooth signal symmetry nor 50% duty cycle for a rectangle signal are important. This allows for larger output maximum frequencies.

Figure 3. PSoC Internals



In this example, the integrator has been placed in ASC10. The configurable SC block has been used to make the integrator. The *ComparatorBus_0* was set as the modulator source. The **FCap** was set to 32 and the **ACap** to 1 to get the maximum possible integration steps per given input voltage. The input signal comes directly from the P2[1] input pin. The SC block serves an additional level-shifting function. To process PSoC V_{ss} ground-related input signals, the **ARefMux** reference was set to REFLO and the **RefMux** was set to $V_{dd}/2 \pm V_{dd}/2$. Users should set **ARefMux** to AGND when they want to work with AGND-related input signals, such as those that come from another analog block. The integrator output voltage is sent to the P0[3] pin.

The Timer_8 User Module is required to pass the comparator bus signal to an external pin. The timer function has been changed to the CRC and pass mode has been enabled in the firmware. This module is required only when the digital V/F converter output is directly passed to an external pin. If output is sent to another digital module, the pass block is not required.

Test Results

Figure 4 illustrates the converter output signals. Figure 5 demonstrates use of the converter as a frequency modulator.

Figure 4. Converter Output Signals

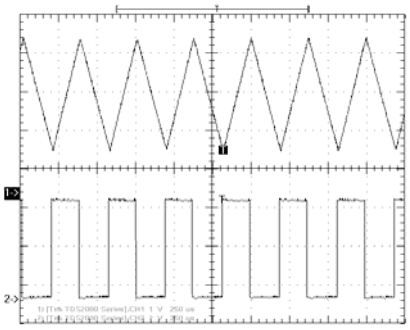
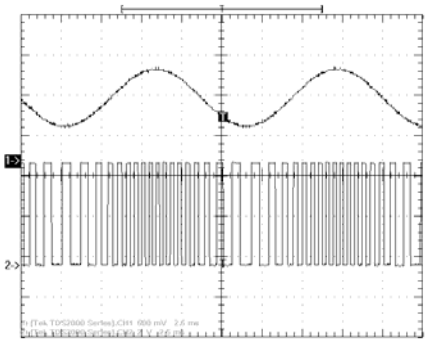


Figure 5. Converter as Frequency Modulator



To study converter transfer characteristics, the output frequency has been measured for various input voltages. See Figure 6. The relation between minimum and maximum frequency is near 100, which makes the converter suitable for many practical applications. Figure 7 depicts the transfer characteristic slope as a function of input voltage. Note that the slope decreases with increasing input voltage due to the constant value in the half-period integration time. See Equation (3). To examine this, differentiate Equation (9) by V_{in}. Note that some noise in the output data is caused by the low cost 3.5-digit, multi-meter used for measurement.

Figure 6. Transfer Characteristics

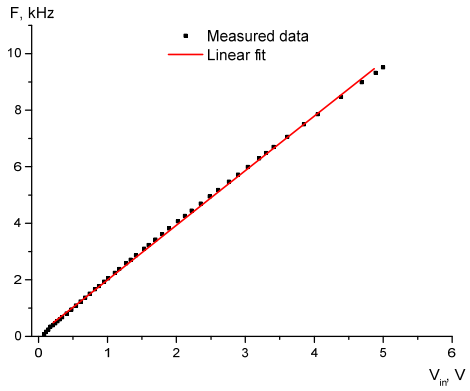
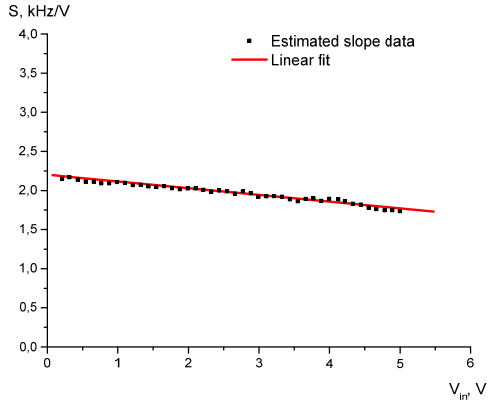
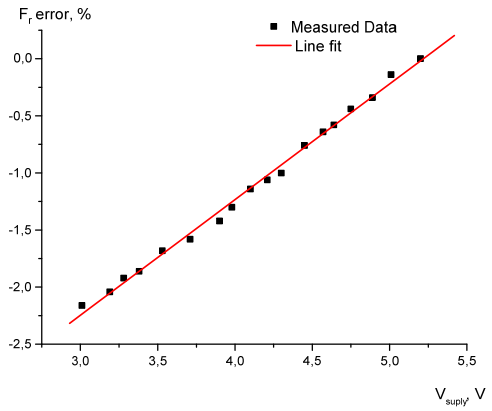


Figure 7. Transfer Characteristic Slope vs. Input Voltage



To study the influence of power supply level on output frequency, the PSoC supply was varied from 3.0V to 5.25V and the input voltage was fixed to half the supply level. Figure 8 illustrates the relative frequency variation obtained during these measurements. The 5.25V supply was used as a reference level.

Figure 8. Output Frequency Variation vs. Supply Level



Finally, the difference between calculated and measured frequencies was estimated. For the 2.5V input signal and 5V supply level, the internal 24 MHz generator measured the frequency as 4993 Hz. The frequency calculated from Equation (8) is near 5212 Hz, which provides the relative frequency error -4.2%. The primary error source is the assumption that the difference between comparator thresholds is exactly equal to that of the integer number of the switched capacitance integrator voltage. As a result, the real half-period integration time is longer than the time evaluated by Equation (5). The more accurate equation, (9), predicts the value at 4938 Hz and error at 1.1%.

The Design Modifications

The proposed voltage-to-frequency converter can be used in various applications. Some adaptation may be required to suit some situations. The integrator can be built using a CT block with an external resistor and capacitor. This will reduce possible jitter in the output signal on maximum frequencies, thereby improving the voltage conversion accuracy (when high stability passive components are used!) and linearity because the transfer characteristic slope is constant for the whole V_{in} range. Because this design uses the power supply value as the converter reference voltage, the output frequency is dependent on the power supply value.

This is fine for sources such as strain gauges and some pressure sensors, which provide the radiometric output signal, but is not very good for devices that supply absolute voltage. In these situations, the two comparators that check the integrator signal relative to the internal reference can be used to switch a “memory cell” such as a Schmitt or LUT-based RS trigger to a control analog modulator.

Source

The main routine source code.

```
void main()
{
   CMPPR_COMP_CR0 |= BIT(2); //connect the
RTopMux to opam output
   CMPPR_COMP_CR1 = (CMPPR_COMP_CR1 & 0xC0)
| 0x2F; //set NMux and PMux connections
   CMPPR_COMP_CR2 &= BIT(6); //The output
latch is always transparent
   CMPPR_Start(CMPPR_HIGHPOWER);

   AMD_CR0 |= 0x04;
   INTEGR_Start(INTEGR_HIGHPOWER);

   BYPASS_FUNC_REG = BYPASS_FUNC_REG & 0xFC
| 0x02;
   BYPASS_CONTROL_REG |= 0x03;
   BYPASS_Start();

   while(1); //loops forever here
}
```

About the Author

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Background: Victor earned a radiophysics diploma in 1996 from Ivan Franko National Lviv University, a PhD degree in Computer Aided Design systems in 2000, and is presently working as Associate Professor at National University "Lvivska Polytechnika" (Lviv, Ukraine). His interests involve the full cycle of embedded systems design including various processors, operating systems and target applications.

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In March of 2007, Cypress recataloged all of its Application Notes using a new documentation number and revision code. This new documentation number and revision code (001-xxxxx, beginning with rev. **), located in the footer of the document, will be used in all subsequent revisions.

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