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UOFM
MASTERS 2007

11038 PSA

I²C™ Development using the PICkit™ Serial Analyzer

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Class Objective

When you finish this class you will:

- Explain the I²C™ protocol
- Use the PICkit™ Serial Analyzer to exchange I²C messages to a target device
- Configure the MSSP peripheral for I²C slave mode
- Program the MSSP peripheral for I²C slave mode

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Agenda

- I²C™ Protocol Overview
- PICkit™ Serial Analyzer
- Configuring the MSSP peripheral for I²C slave mode
- Programming the MSSP peripheral as an I²C slave

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I²C™ Protocol Overview

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I²C™ Protocol Overview

- Introduction
- Hardware Overview
- Communication Elements
- Message Formatting

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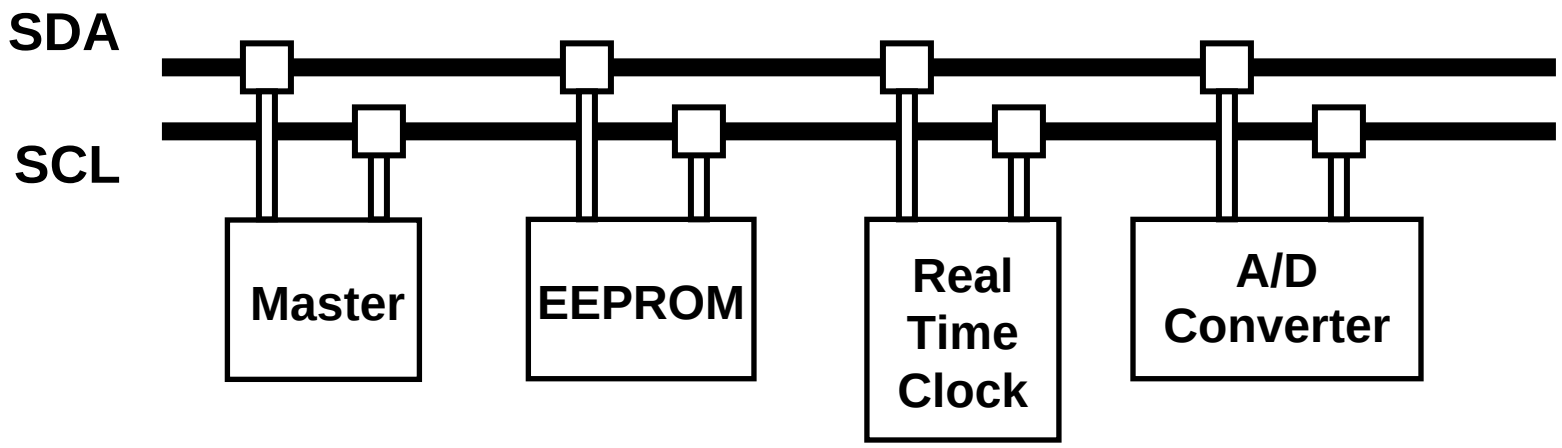
I²C™ Introduction

- **NXP (formerly Philips Seminconductor) Inter-Integrated Circuit (I²C) Specification**

  Specification: www.standardics.nxp.com/literature/books/i2c/pdf/i2c.bus.specification.pdf

- **Synchronous,**
- **Master-Slave Protocol,**
- **Bidirectional,**
- **Half Duplex Serial Interface**



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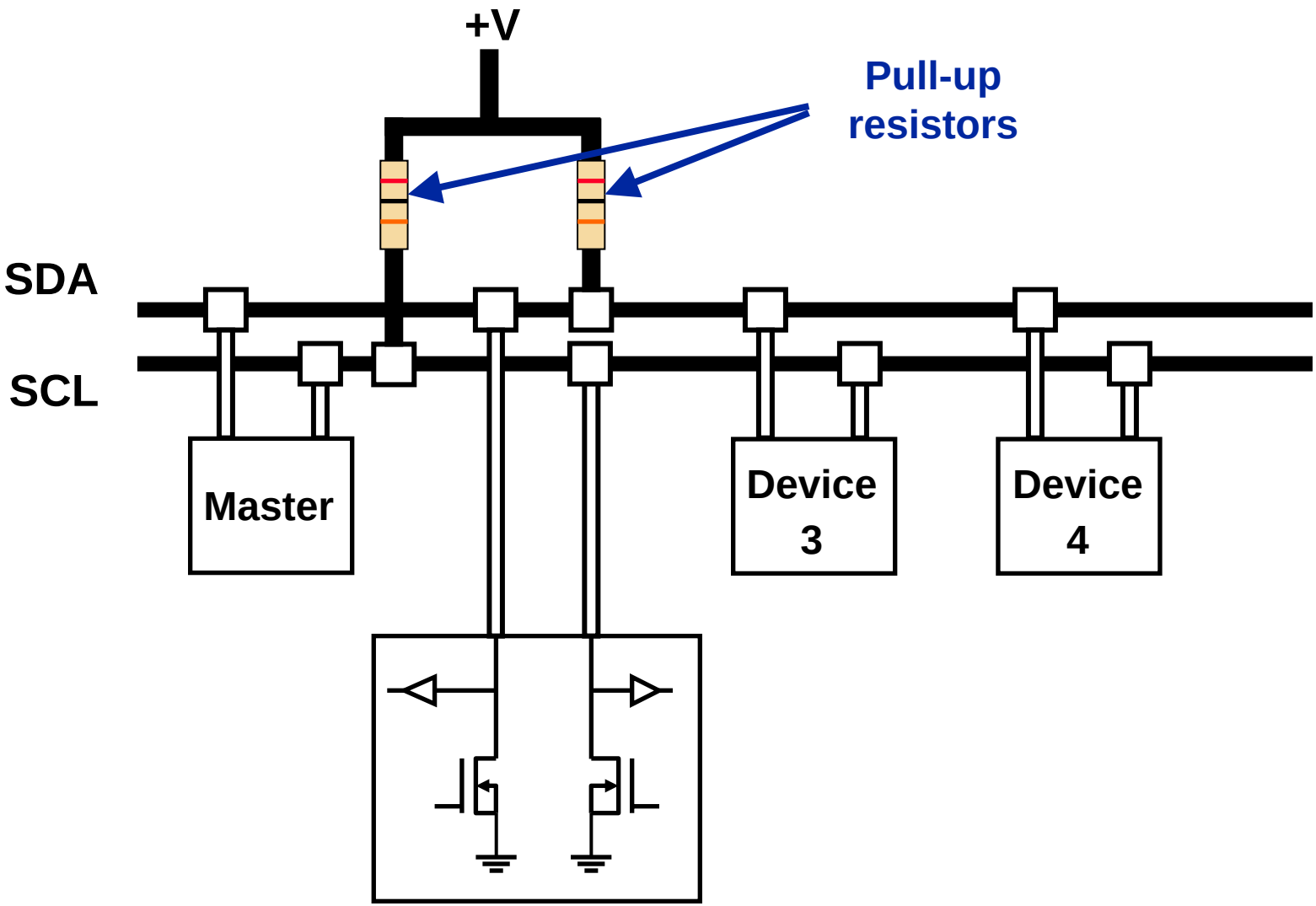
I²C™ Hardware Overview



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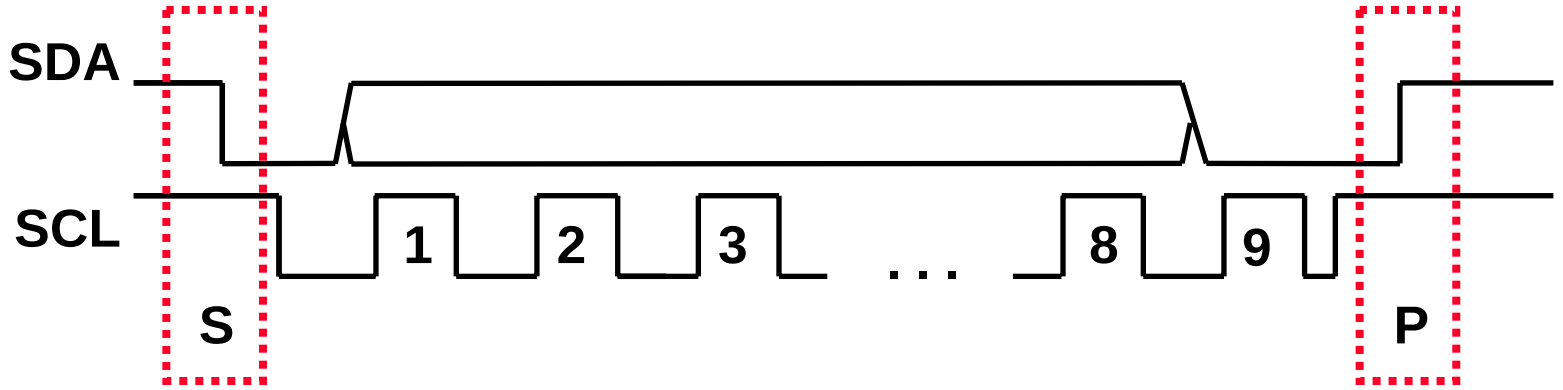
I²C™ Communication Elements

- **Start** and **Stop** Condition:
  - Generated by Master
  - After Start Condition: Bus is **Busy**
  - After Stop Condition: Bus is **Free**



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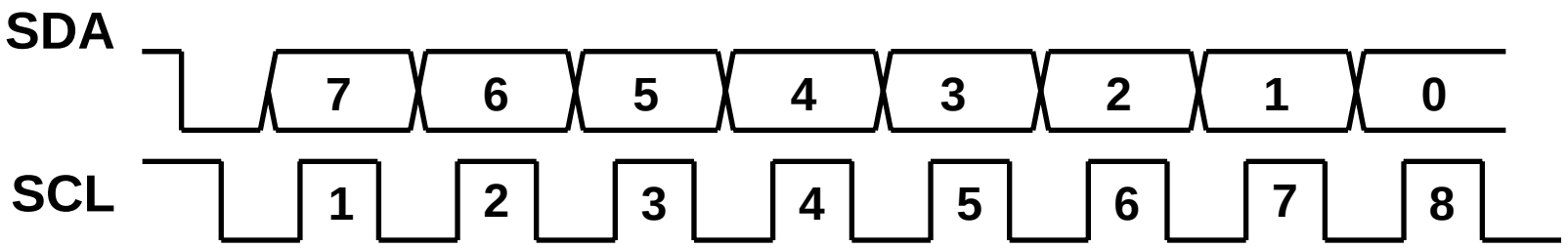
I²C™ Communication Elements

- **Data Transfer**
  - 8 bits of data are sent on the bus
  - Data is valid when SCL is high
  - Types of Data: **Address** Byte, **Data** Byte



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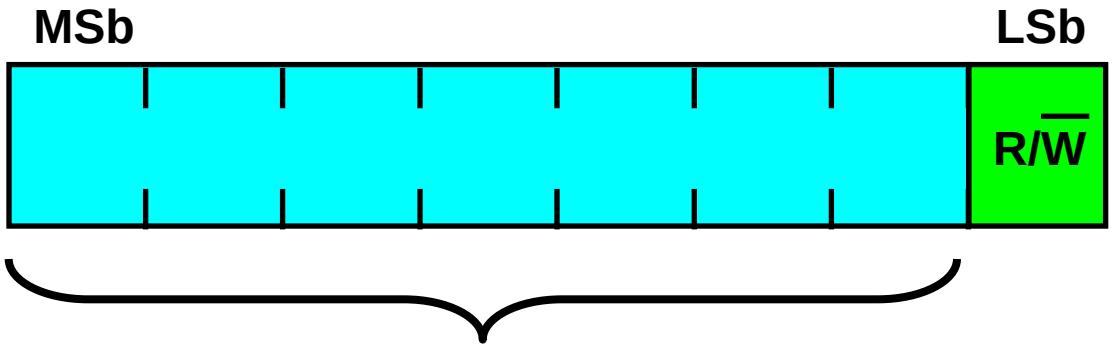
I²C™ Communication Elements

- **Slave Address**
  - 7 bits (10 bits also exists)
  - First byte following the start condition
  - Read/$\overline{\text{Write}}$ Bit



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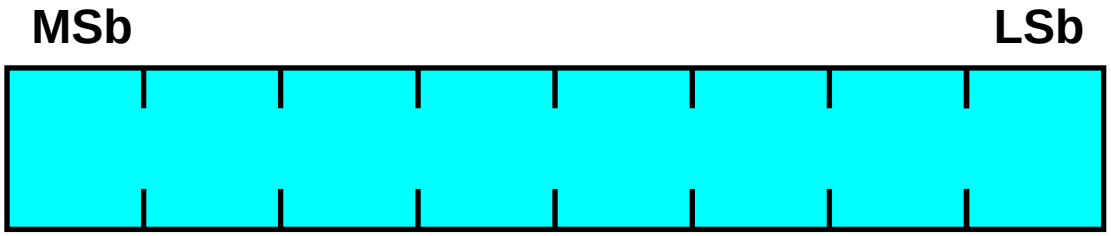
I²C™ Communication Elements

- **Data Byte**
  - 8 bits
  - Data can be read or written to/from I²C device



Data Byte

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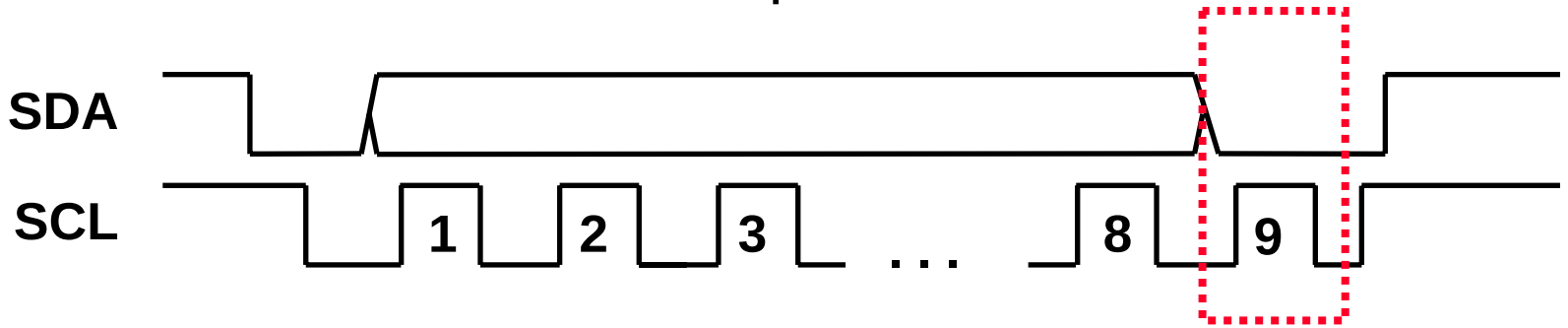
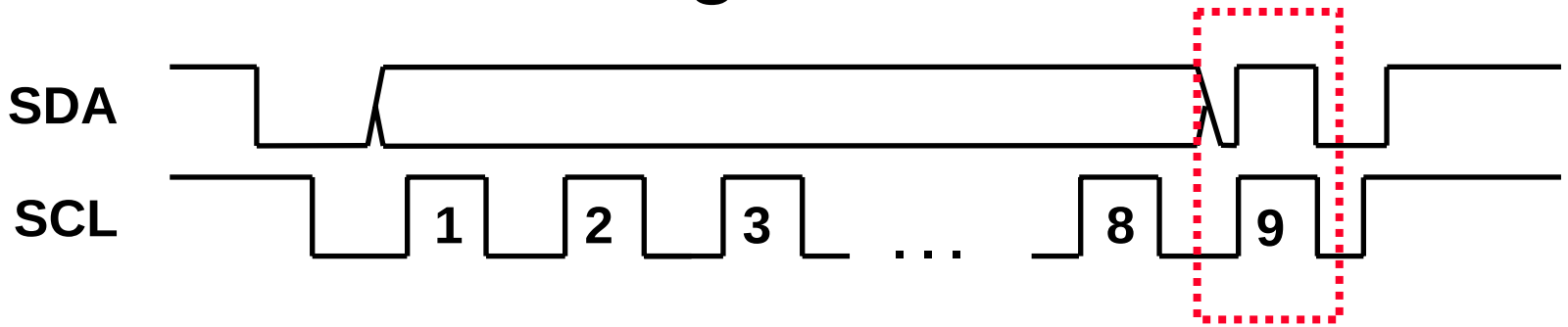
I²C™ Communication Elements

- **Acknowledge**
  - Generated by master or slave by holding the SDA low on the 9th clock pulse



- **Not-Acknowledge**



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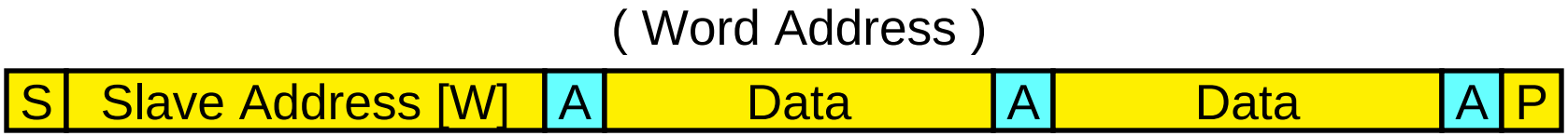
I²C™ Message Formatting

- **Master Write to Slave**



Legend:

S = **Start** Condition A = **Acknowledge**

P = **Stop** Condition $\overline{A}$ = **No Acknowledge**

= Master to Slave = Slave to Master

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I²C™ Message Formatting

- **Master Read from Slave**

Legend:

S = **Start** Condition

P = **Stop** Condition

A = **Acknowledge**

Ā = **No Acknowledge**

= Master to Slave

= Slave to Master

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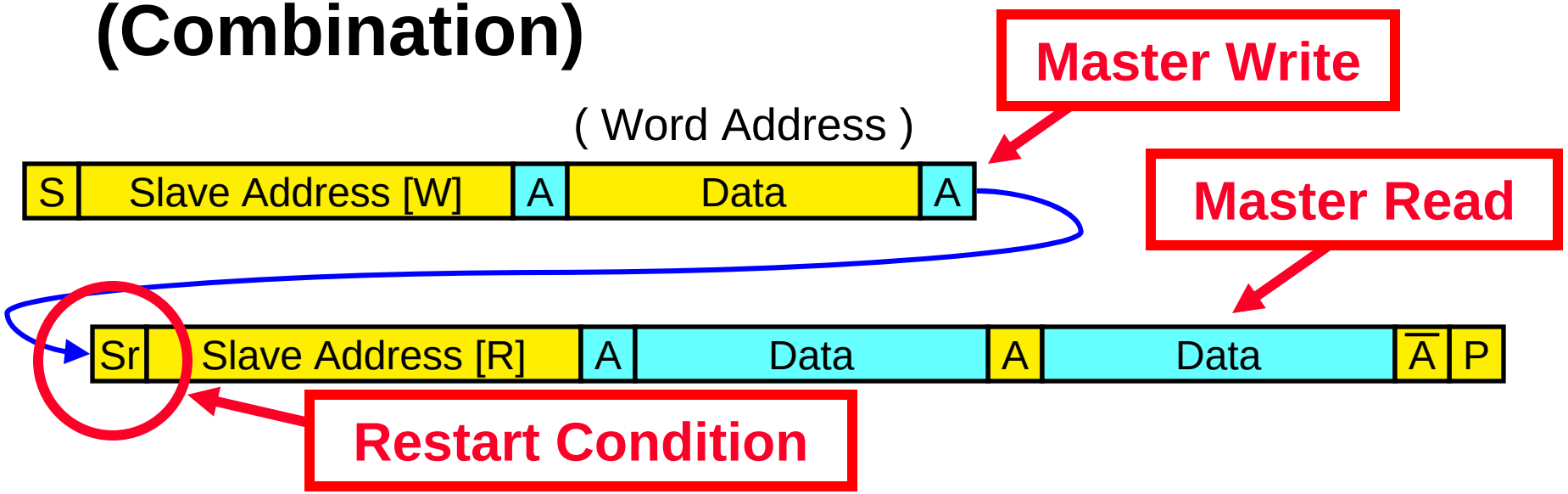
I²C™ Message Formatting

- **Master Write then Read from Slave (Combination)**



Legend:

S = **Start** Condition

P = **Stop** Condition

A = **Acknowledge**

$\overline{A}$ = **No Acknowledge**

= Master to Slave

= Slave to Master

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I²C™ Protocol Overview

- **Summary**
  - Introduction
  - Hardware Overview
  - Communication Elements
  - Message Formatting

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PICkit™ Serial Analyzer

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PICkit™ Serial Analyzer

- **PICkit Serial Analyzer**
- **28-Pin Demo Board**
- **PC Program**
  - 28-Pin Demo Board Demonstration
  - I^2C™ Basic Operations
- **Hands On Lab #1**
  - PICkit Serial Analyzer Operation

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PICkit™ Serial Analyzer
DV164122

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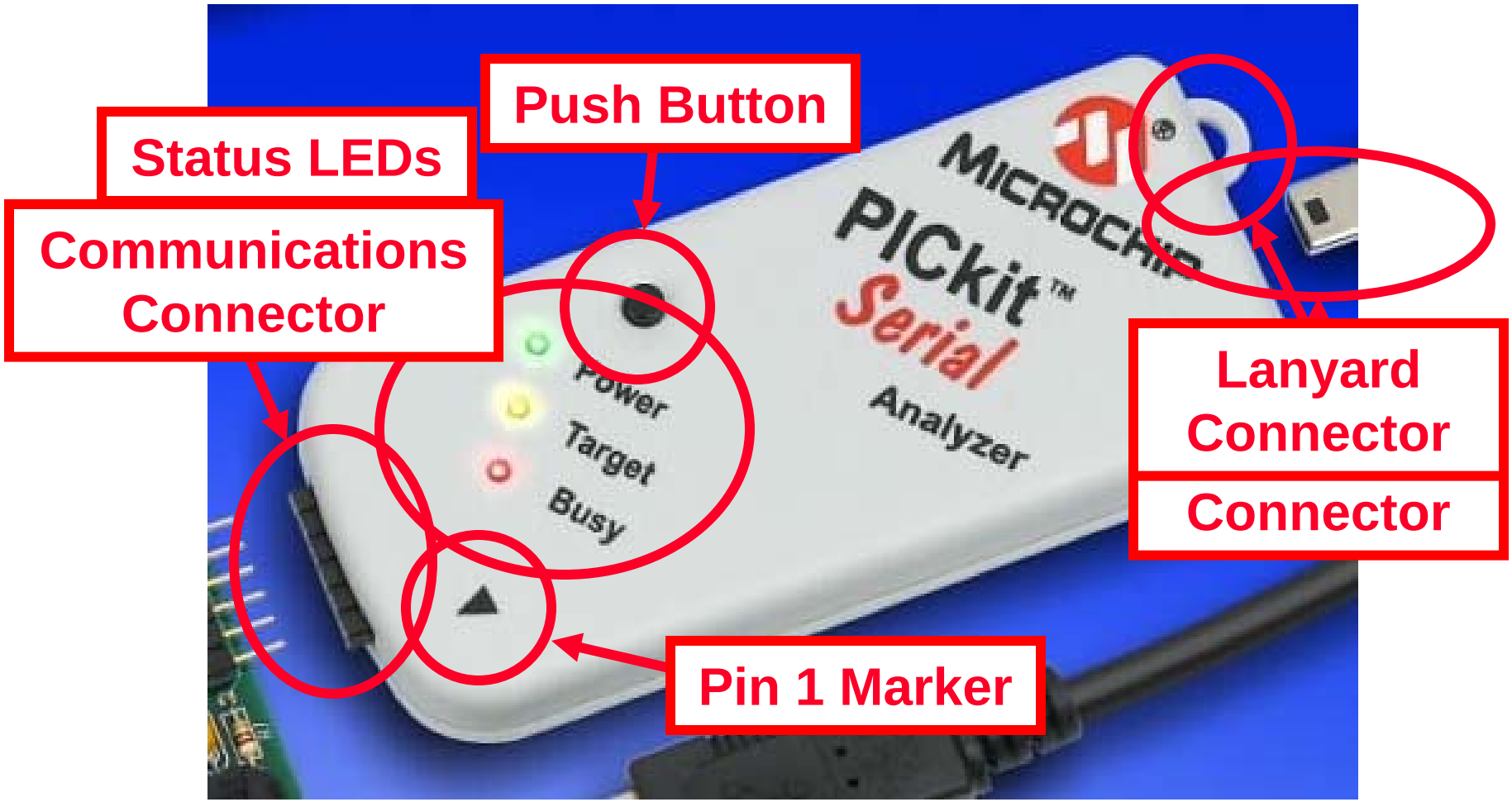
PICkit™ Serial Analyzer



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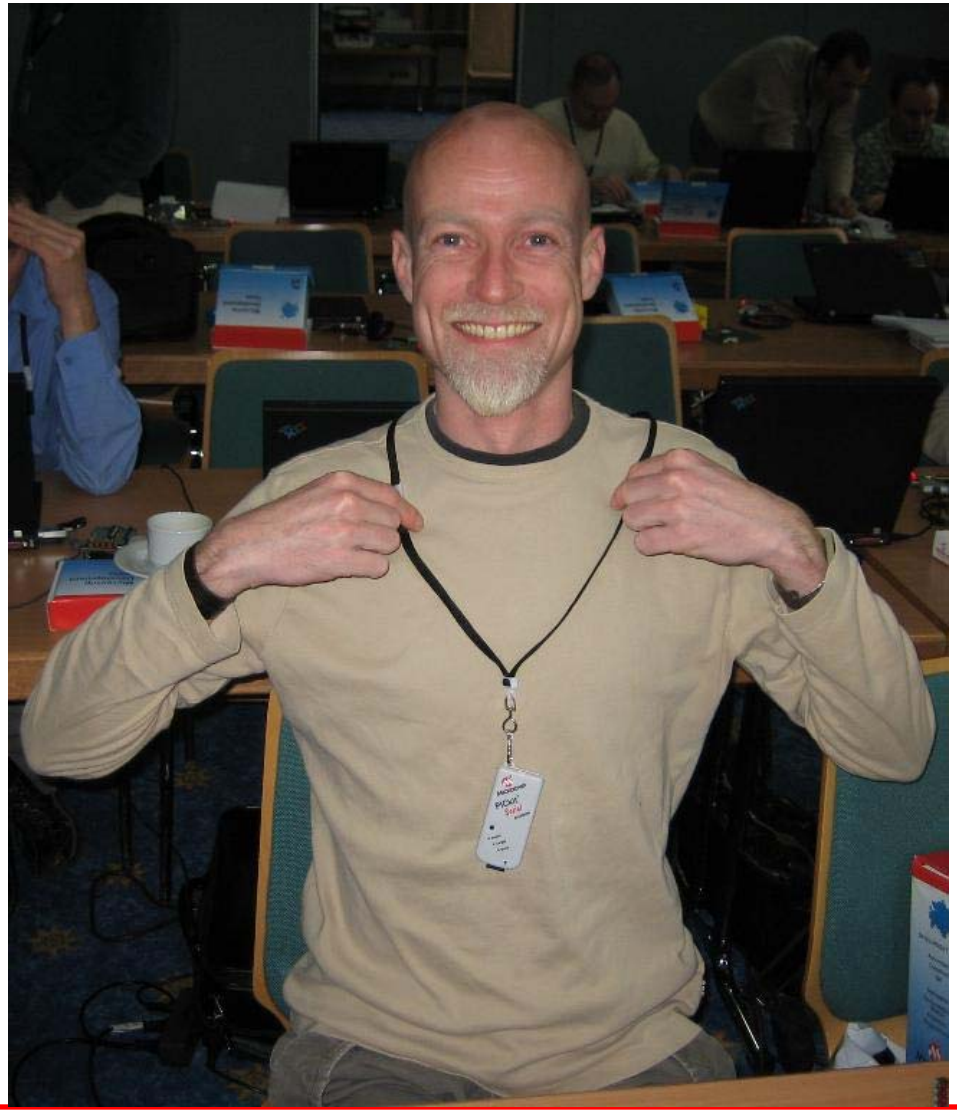
PICkit™ Serial Analyzer



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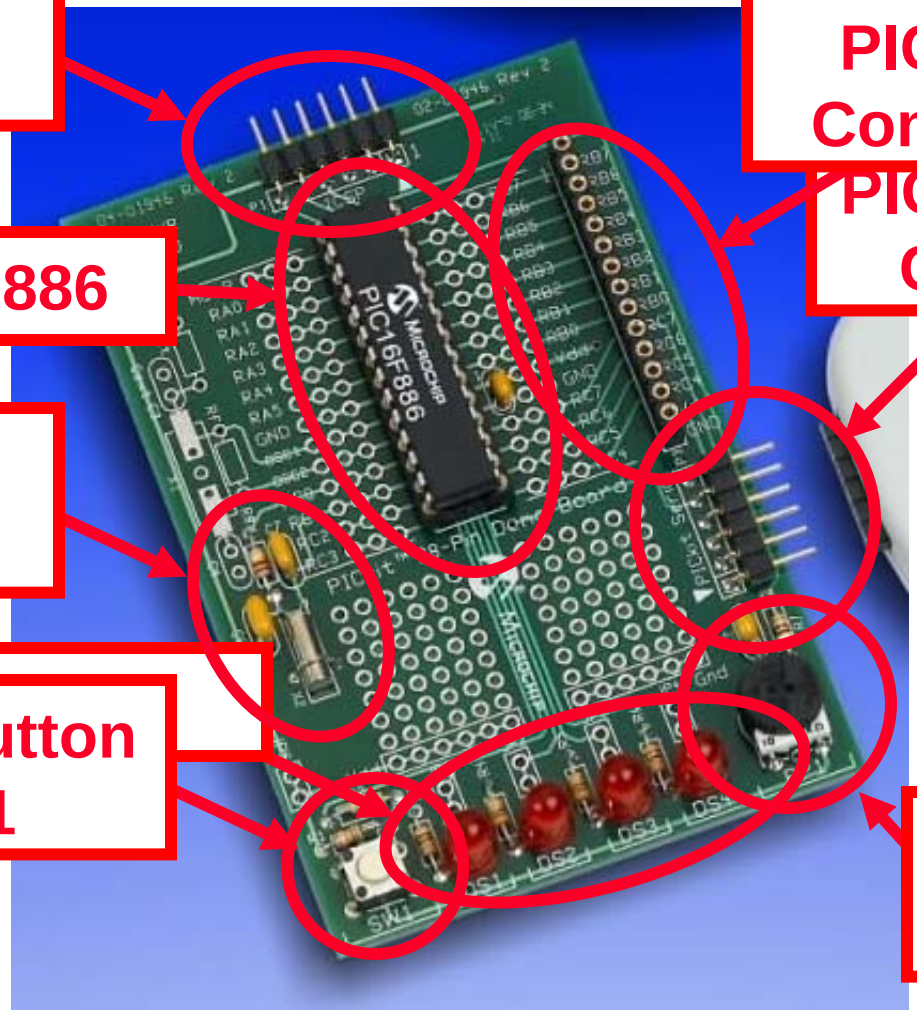
28-Pin Demo Board



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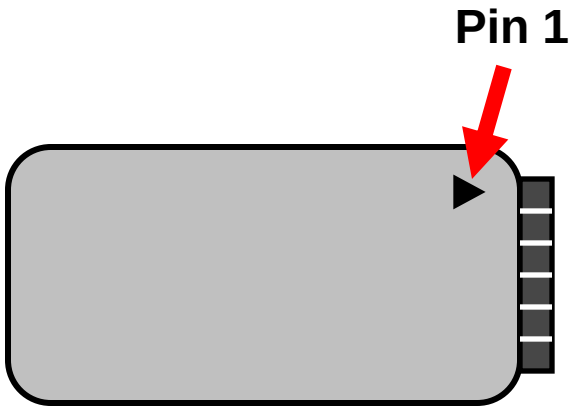
PICkit™ Serial Analyzer

- **Pin Assignments**



Pin	I²C™	SPI	USART
1	--	CS	TX
2	+V	+V	+V
3	GND	GND	GND
4	SDA	SDI	--
5	SCL	SCK	--
6	--	SDO	RX

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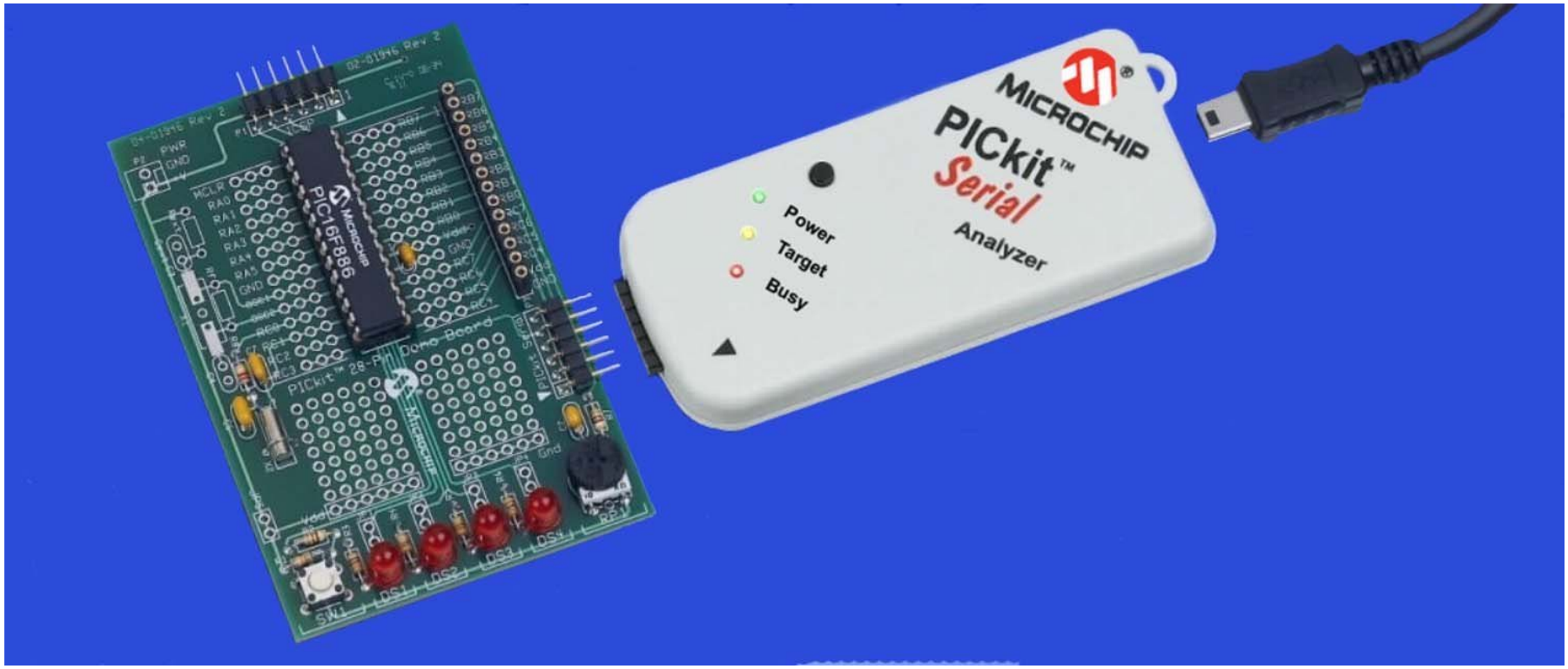
PICkit™ Serial Analyzer

- **Board Connection**



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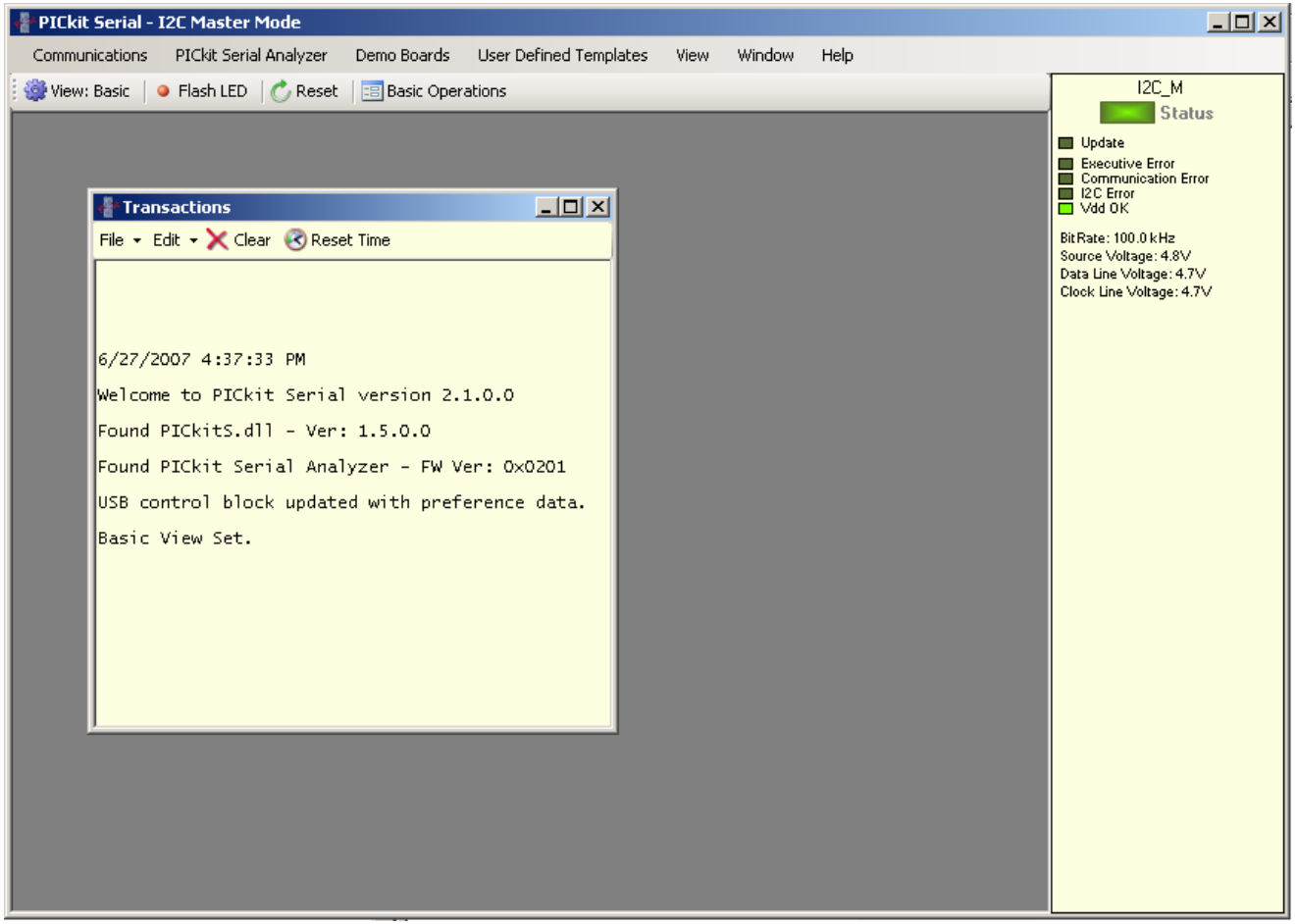
PICkit™ Serial Analyzer

- **PC Program**



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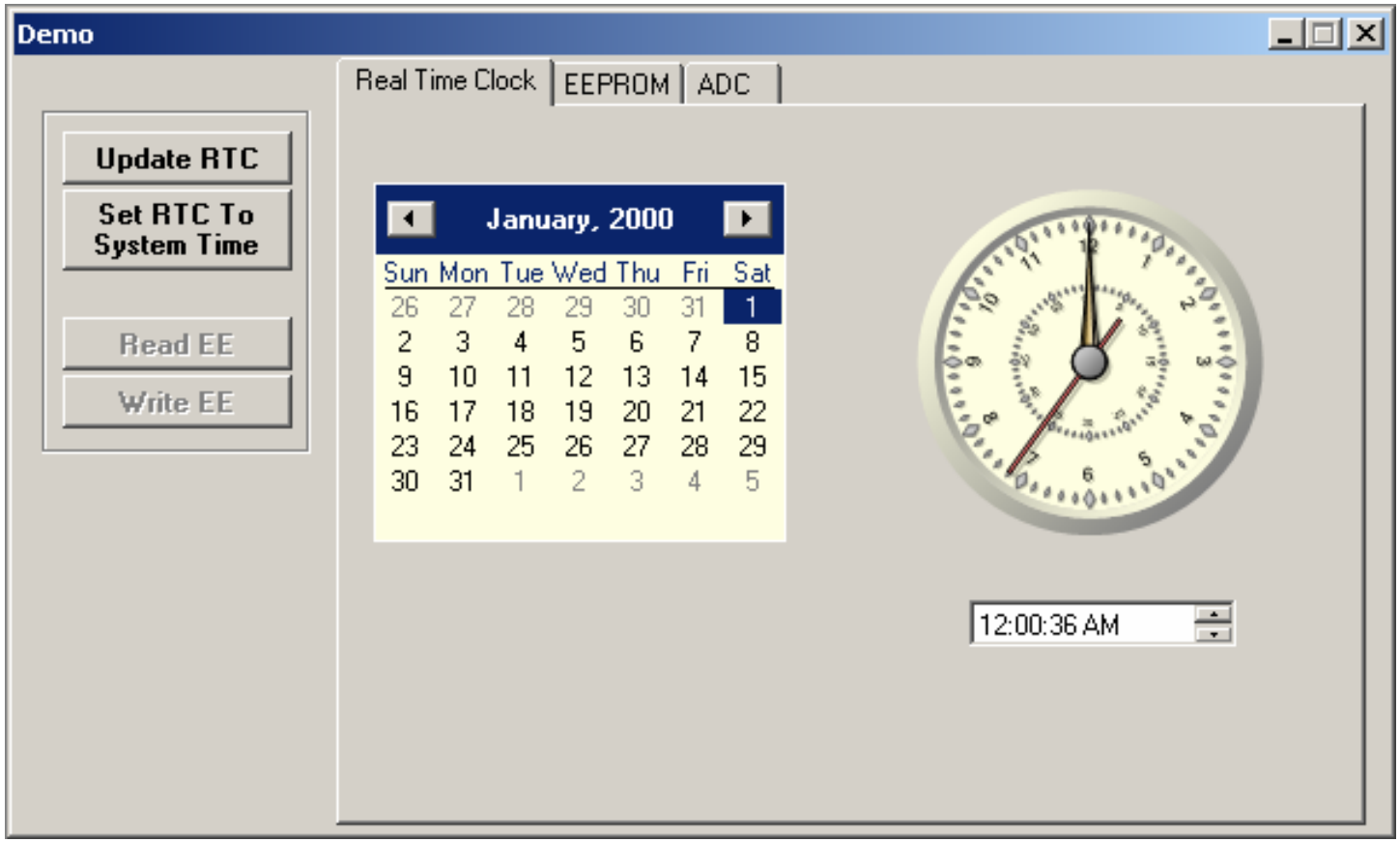
28-Pin Demo Board

- **RTC Demonstration**



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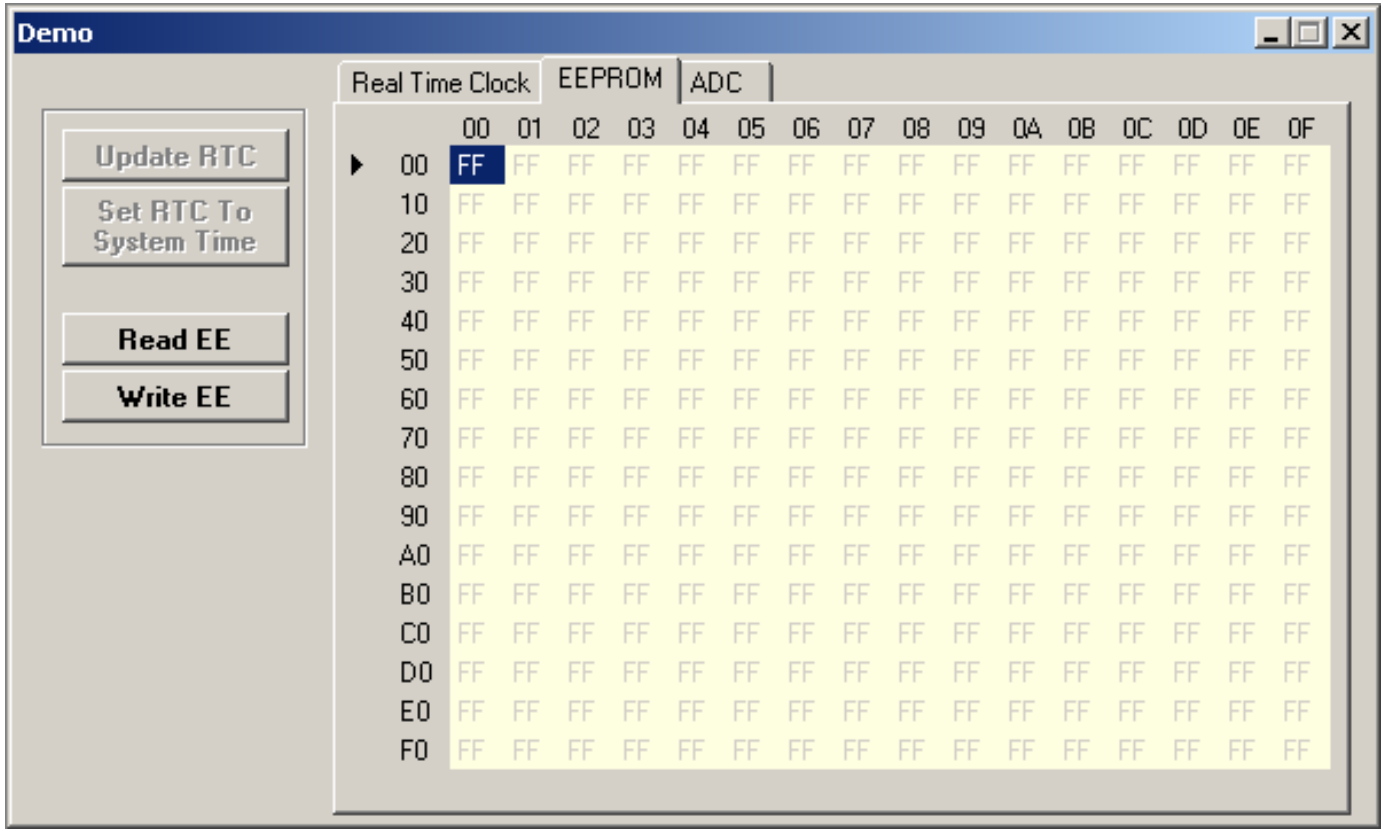
28-Pin Demo Board

- **Serial EEPROM Demonstration**



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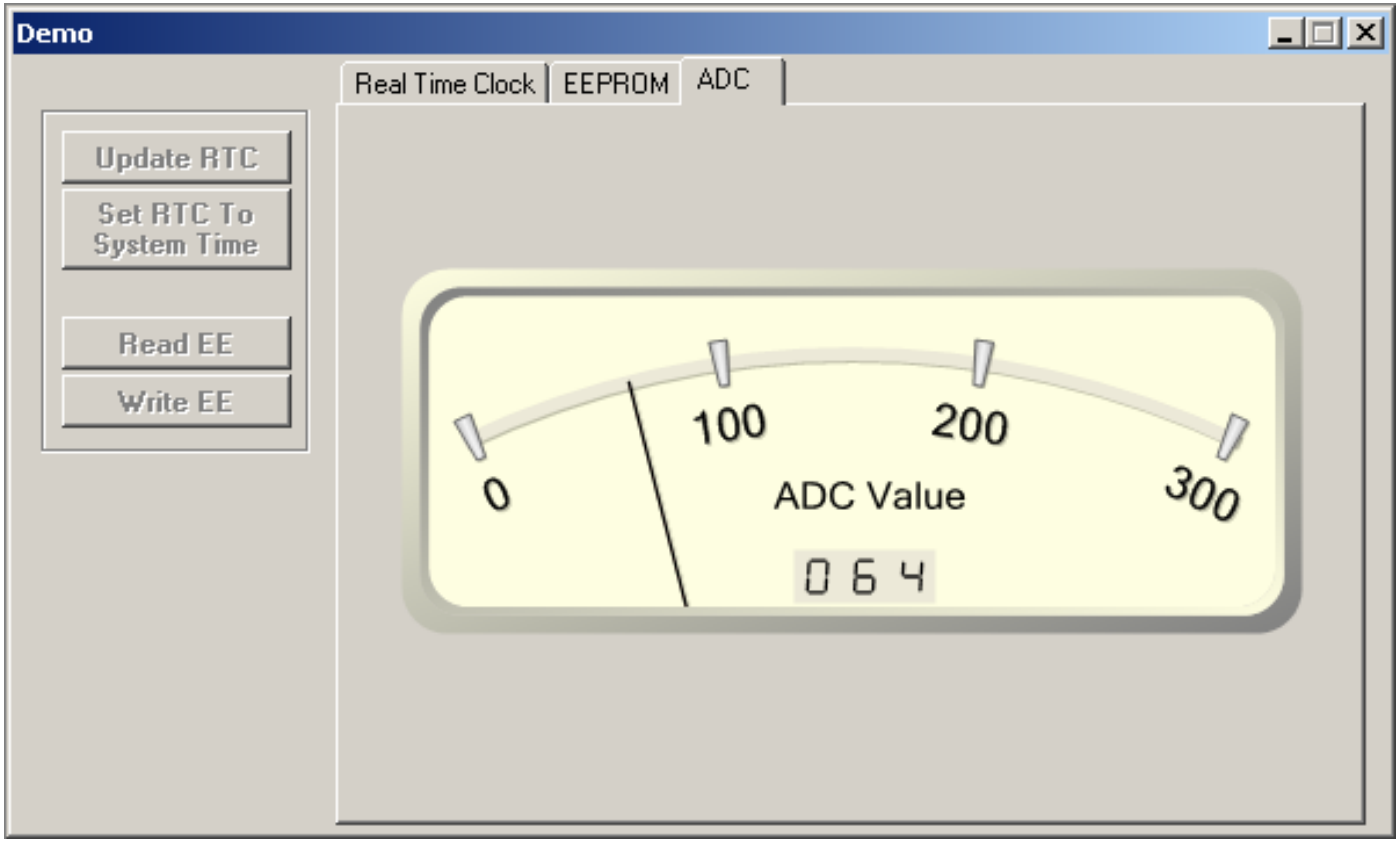
28-Pin Demo Board

- **ADC Demonstration**



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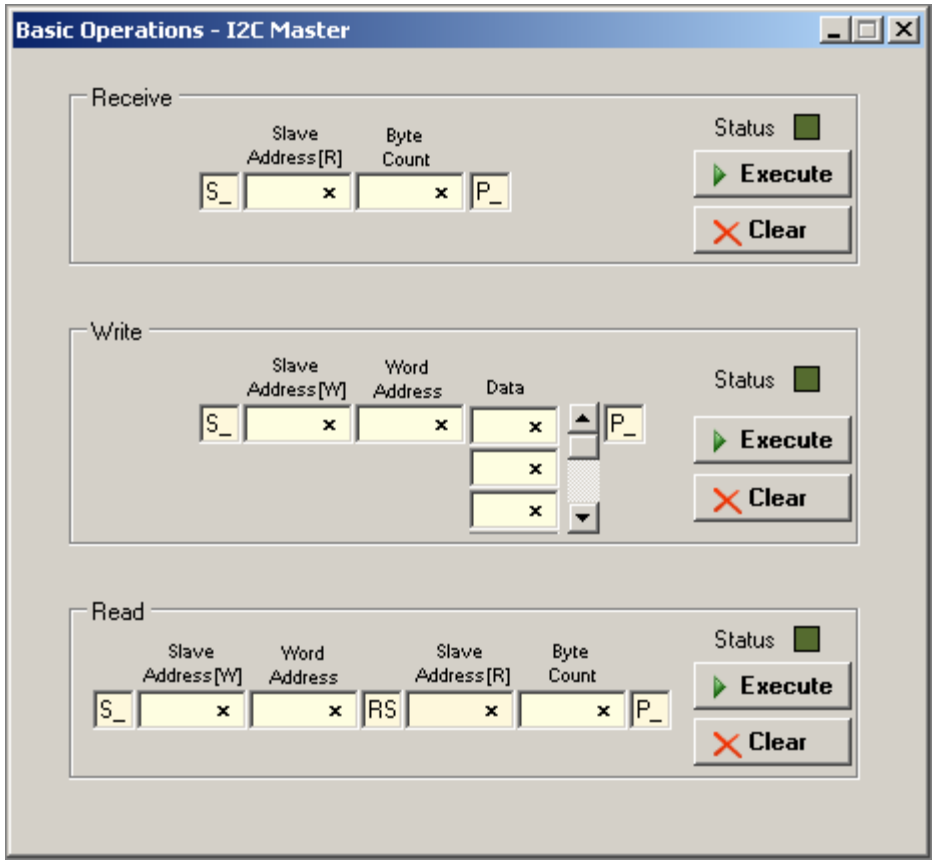
PICkit™ Serial Analyzer

- **I²C™ Basic Operations**



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Hands On Lab #1

PICkit™ Serial Analyzer Operation

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PICkit™ Serial Analyzer

- **Summary**
  - **PICkit Serial Analyzer**
  - **28-Pin Demo Board**
  - **PC Program**
    - 28-Pin Demo Board Demonstration
    - I^2C™ Basic Operations
  - **Hands On Lab #1**
    - PICkit Serial Analyzer Operation

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Configuring the MSSP Peripheral for I²C™ Slave Mode

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MSSP Peripheral

- MSSP I²C™ Modes
- Registers
- Block Diagram
- Address Masking Feature
- Interrupts

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MSSP I²C™ Modes

- **Supports:**
  - Master/Multi-Master Mode
  - Slave Mode
  - 7 or 10-bit Addressing
- **Configurations:**
  - I²C Master Mode
  - I²C Slave Mode
  - I²C Slave Mode with Start and Stop bit interrupts enabled
  - I²C firmware controlled master, slave is idle

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SSPCON Register

SSPCON Register

WCOL	SSPOV	SSPEN	CKP	SSPM3	SSPM2	SSPM1	SSPM0

SSPEN: Synchronous Serial Port Enable Bit
1 = Configures SDA and SCL as serial port pins.

SSPM<3:0>: Synchronous Serial Port Mode Select Bits
1110 = I^2C Slave Mode, 7-Bit Address with Start/Stop bit interrupts enabled

WCOL = Write Collision Detect Bit
SSPOV = Receive Overflow Indicator
CKP = Clock Polarity Bit

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SSPSTAT Register

SSPSTAT Register

SMP	CKE	D/$\overline{A}$	P	S	R/$\overline{W}$	UA	BF

D / $\overline{A}$	= Data / Not Address Bit
P	= Stop Bit
S	= Start Bit
R / $\overline{W}$	= Read / Not Write Bit
BF	= Buffer Full Bit

SMP	= Slew Rate Control for High Speed Enable
CKE	= SPI Clock Edge Select
UA	= Update Address Bit (for 10-bit address mode)

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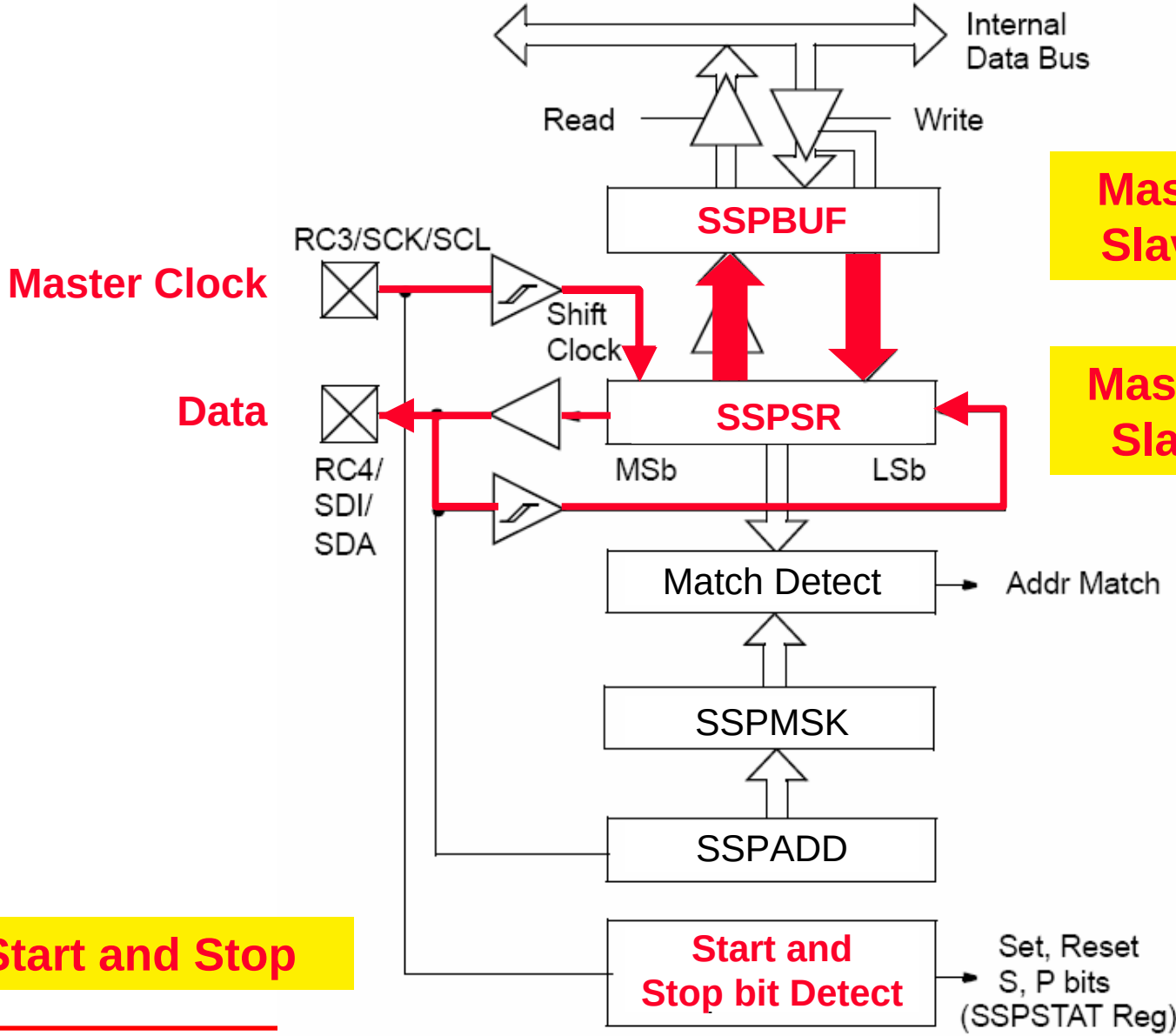
MSSP I²C™ Block Diagram



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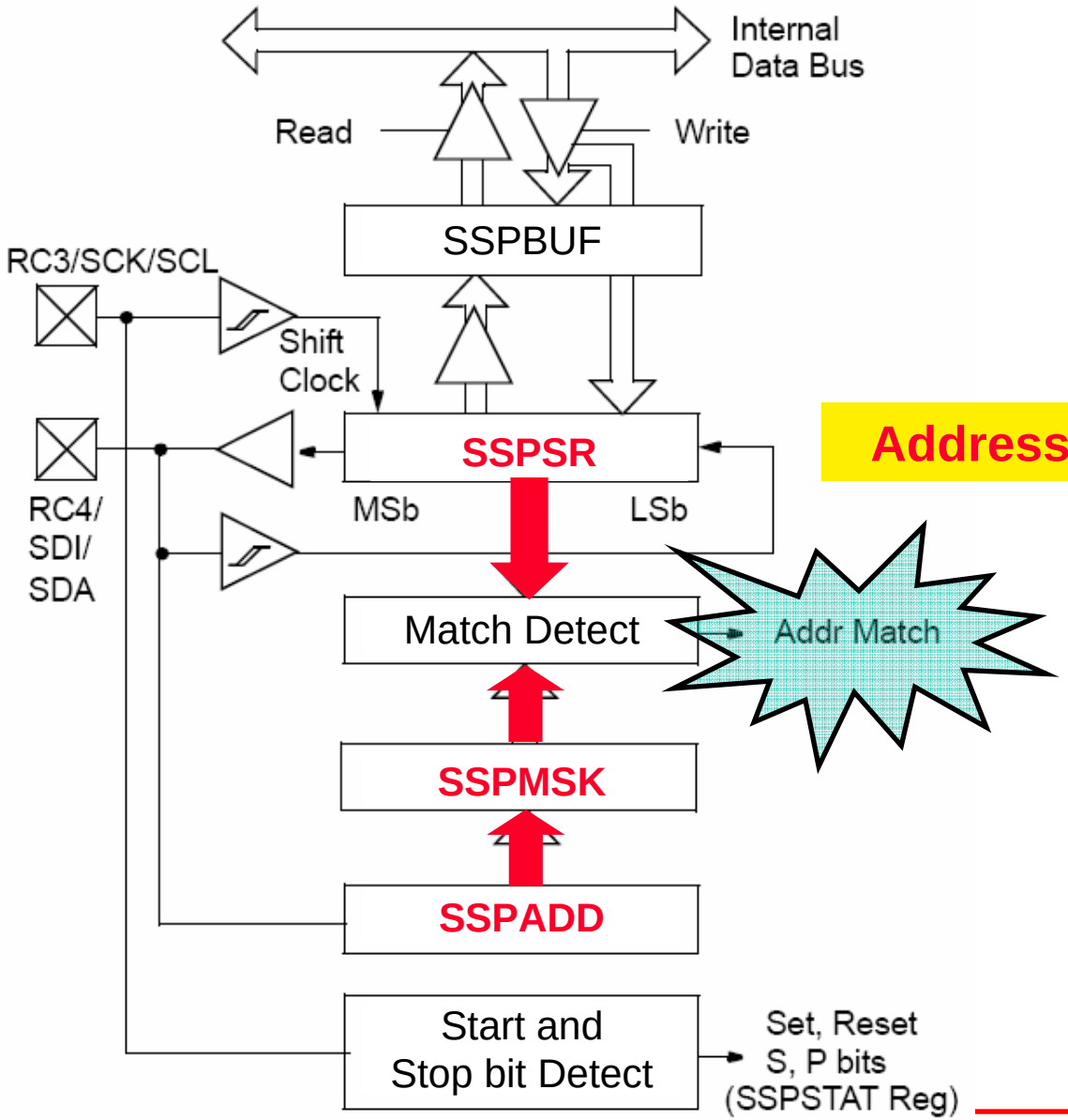
MSSP I²C™ Block Diagram



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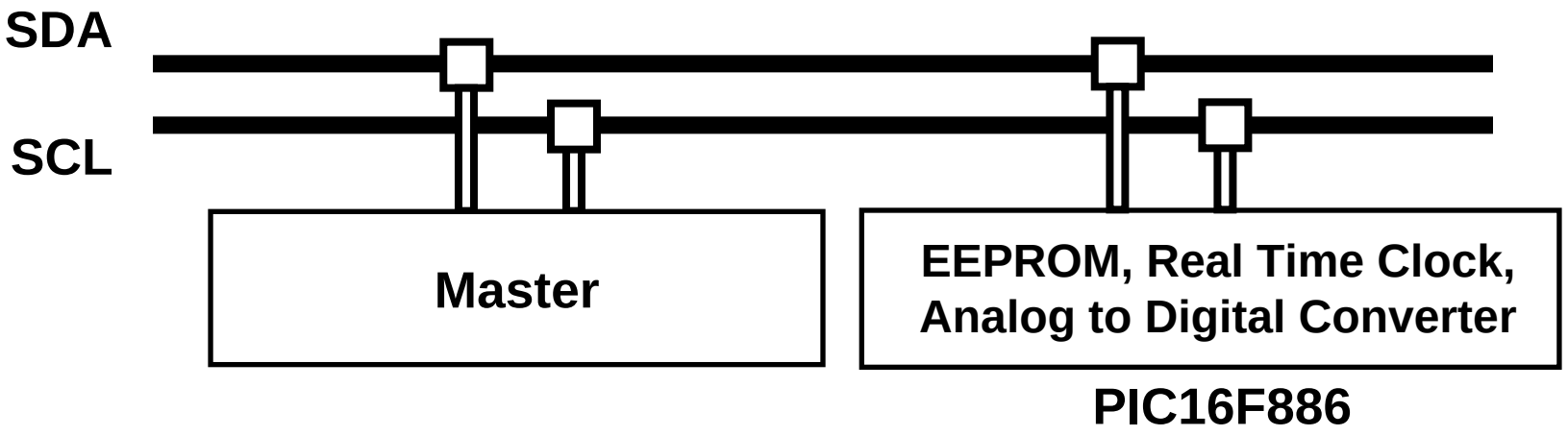
Address Masking Feature

- What is it?
  - It allows a PIC® MCU to ACK more than one address.
- What is it good for?
  - Integrating multiple I²C™ devices in one PIC MCU



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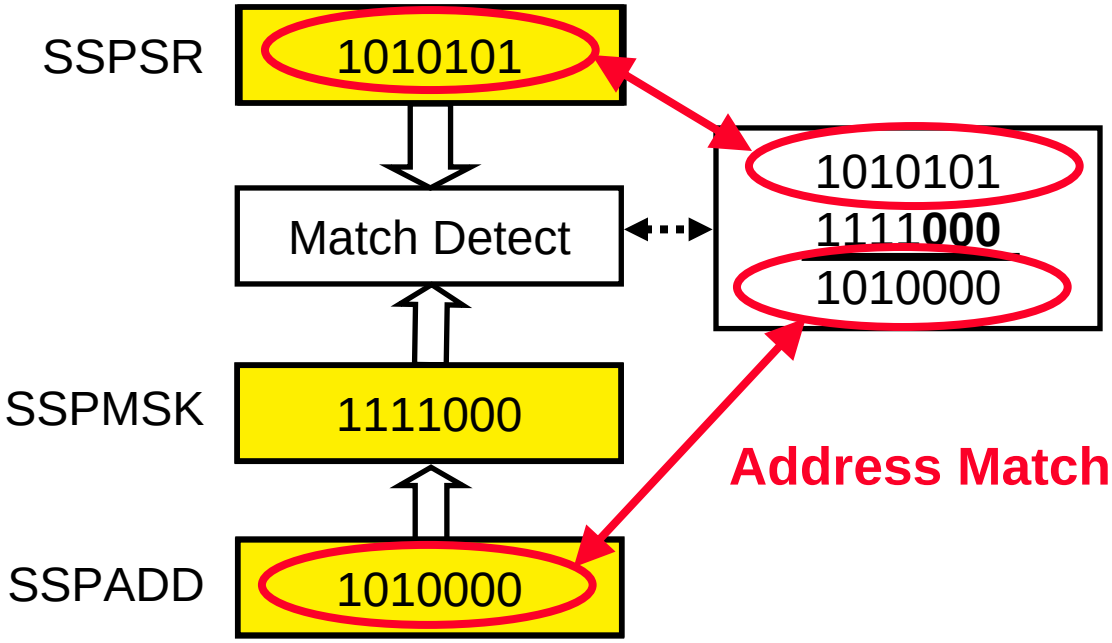
How Address Masking Works



- **Allows device to acknowledge multiple addresses**
- **Turns masked bits into don't cares**

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Configuring SSPMSK Register

SSPCON Register

WCOL	SSPOV	SSPEN	CKP	SSPM3	SSPM2	SSPM1	SSPM0

SSPM<3:0>: Synchronous Serial Port Mode Select Bits
1001 = Load SSPMSK register at SSPADD SFR Address

SSPMSK Register

MSK7	MSK6	MSK5	MSK4	MSK3	MSK2	MSK1	MSK0

- **Two Step Process**
  1. **SSPCON, SSPM<3:0>** = 1001
  2. Accessed through **SSPADD** register

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Configuring SSPADD Register

SSPCON Register

WCOL	SSPOV	SSPEN	CKP	SSPM3	SSPM2	SSPM1	SSPM0

SSPM<3:0>: Synchronous Serial Port Mode Select Bits
1110 = I^2C Slave Mode, 7-Bit Address with Start/Stop bit interrupts enabled

SSPADD Register

ADD7	ADD6	ADD5	ADD4	ADD3	ADD2	ADD1	ADD0

Reserve Addresses

- B‘0000 000’ – General Call Address
- B‘0000 001’ – CBUS address
- B‘0000 010’ – Reserved for different bus format
- B‘0000 011’ – Future Purposes
- B‘0000 1XX’ – Hs-mode master code
- B‘1111 1XX’ – Future Purposes
- B‘1111 0XX’ – 10-bit Slave Address

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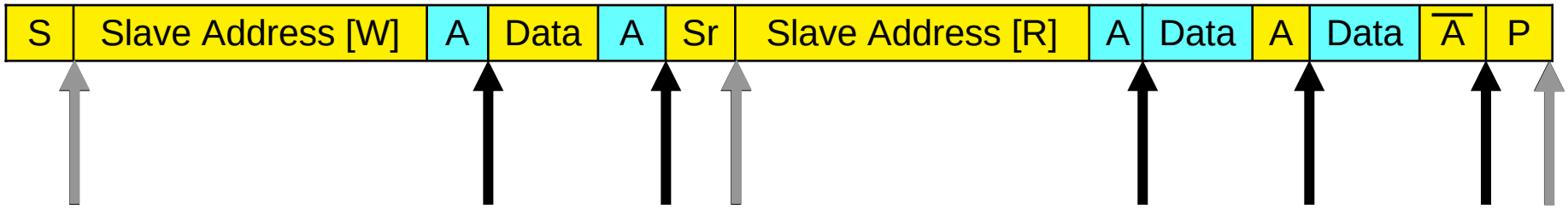
I²C™ Interrupt Events

PIR1 Register

--	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF



- Start and Stop Conditions
- Data Transmit and Receive

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Interrupt Status and Enable

PIE1 Register

--	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE

PIR1 Register

--	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF

INTCON Register

GIE	PEIE	T0IE	INTE	RABIE	T0IF	INTF	RABIF

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MSSP Peripheral

- **Summary**
  - Introduction
  - Registers
  - Block Diagram
  - Address Masking Feature
  - Interrupts

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Programming the MSSP peripheral as an I²C™ slave

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Programming the MSSP

- **Firmware Overview**
- **Events**
- **I²C™ Slave State Machine**
  - Master Write
  - Master Write then Read (Combination)

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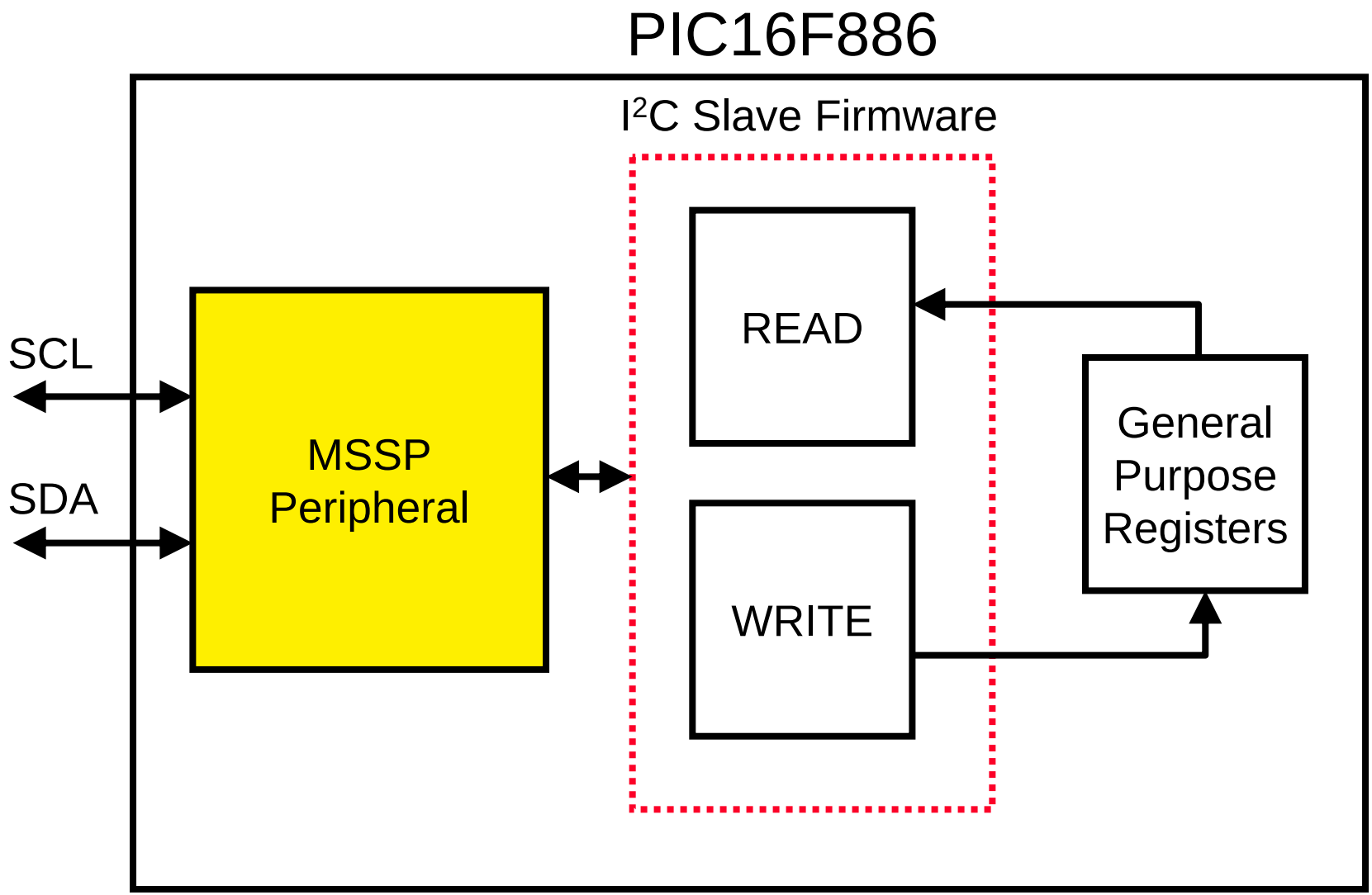
I²C™ Slave Mode Firmware Overview



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Events

- **An Event is a:**
  1. Start or Restart Condition
  2. Master Write Address
  3. Master Write Data
  4. Master Read Address
  5. Master Read Data
  6. Stop Condition

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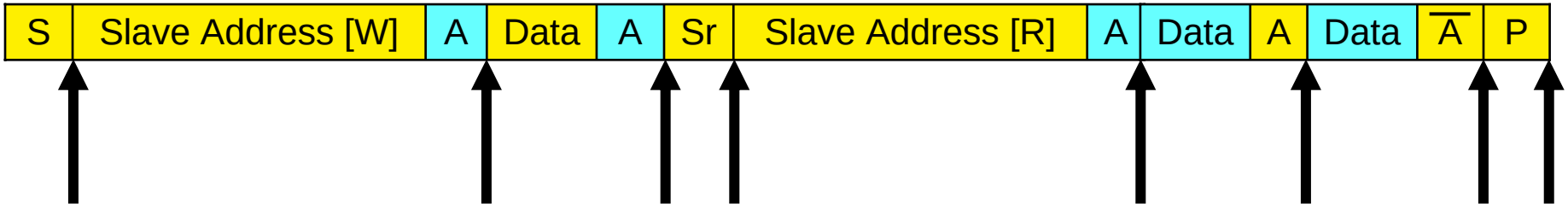
Events

- SSPIF bit indicates when an event has occurred

PIR1 Register

--	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF



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Events

- Events will be identified by bits in the SSPSTAT register

SMP	CKE	D/$\overline{A}$	P	S	R/$\overline{W}$	UA	BF

D / $\overline{A}$ = Data / Not Address Bit
P = Stop Bit
S = Start Bit
R / $\overline{W}$ = Read / Not Write Bit
BF = Buffer Full Bit

SMP = Slew Rate Control for High Speed Enable
CKE = SPI Clock Edge Select
UA = Update Address Bit (for 10-bit address mode)

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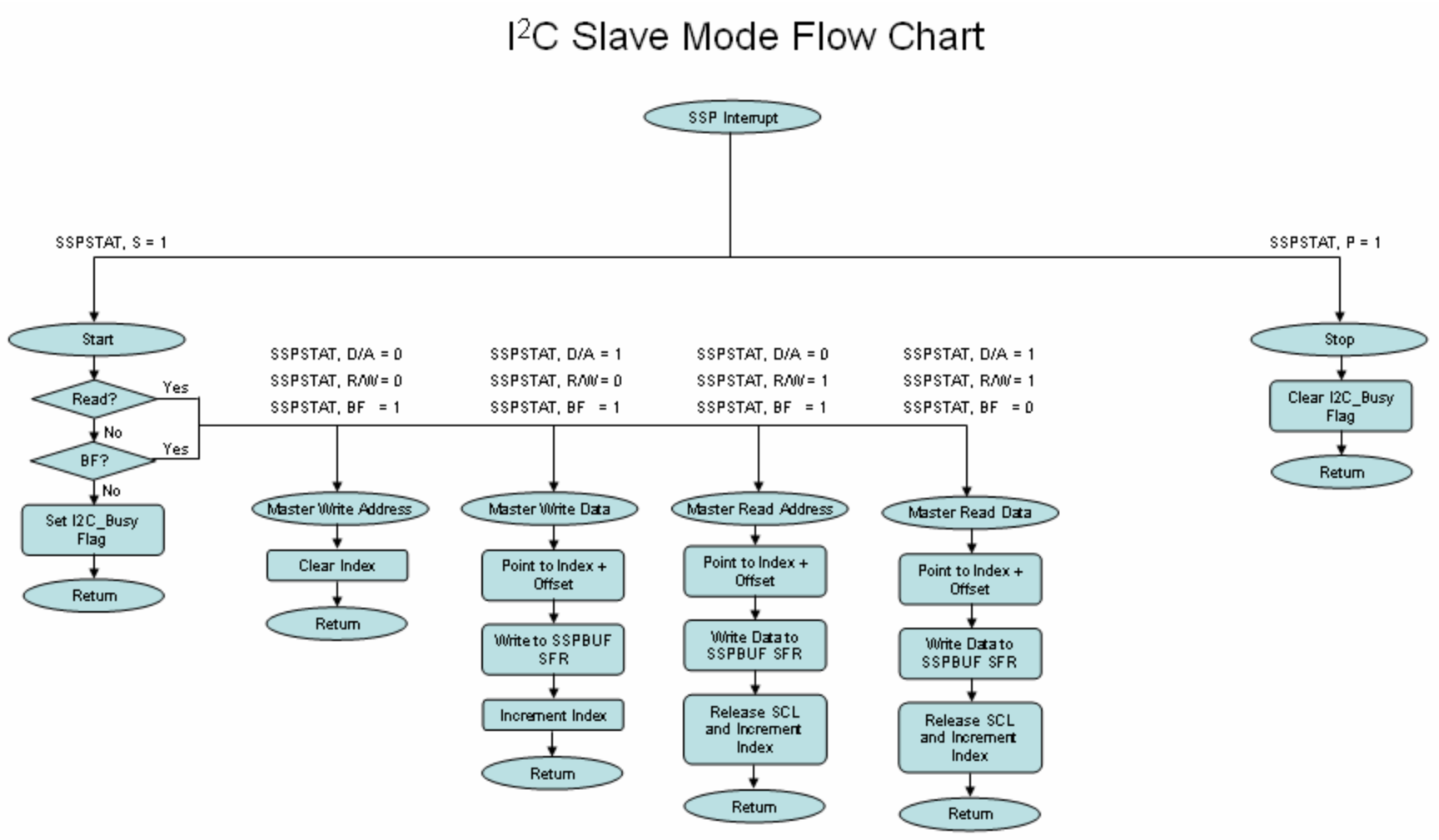
Events



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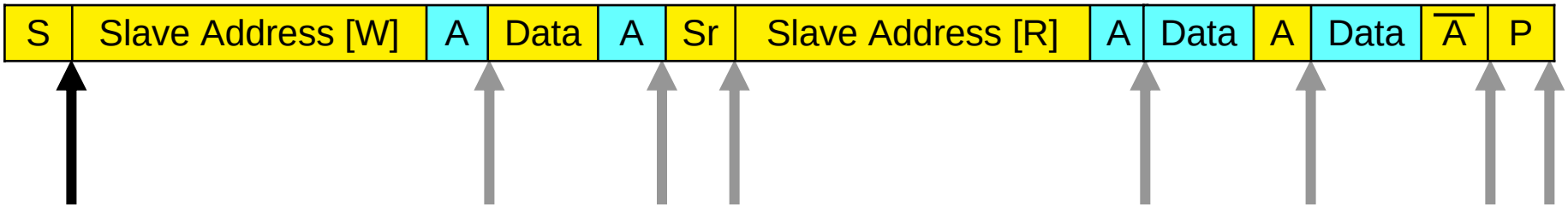
Events

- **Start Condition**
  - Bus is busy



SSPSTAT Bits

- **S = 1**

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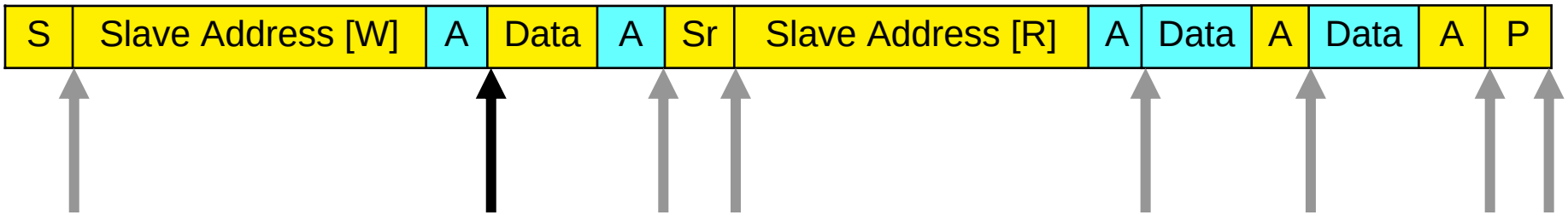
Events

- **Master Write Address**
  - Master has sent a write request with a matching slave address



SSPSTAT Bits

- **D/$\overline{A}$ = 0**
- **R/$\overline{W}$ = 0**
- **BF = 1**

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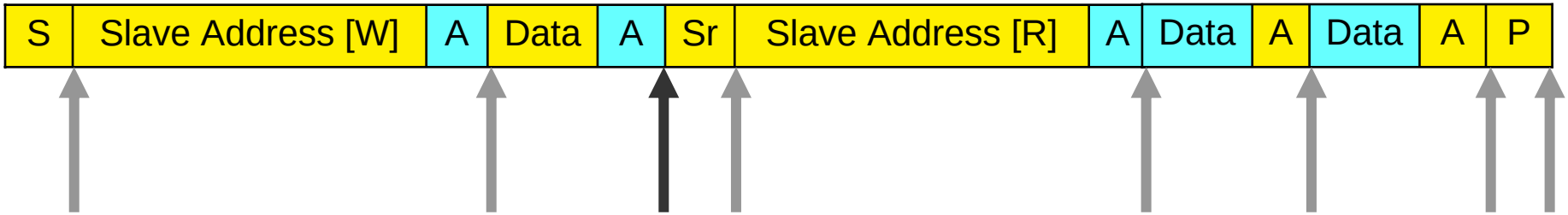
Events

- **Master Write Data**
  - Master has sent a data byte following a write request



SSPSTAT Bits

- **D/$\overline{A}$ = 1**
- **R/$\overline{W}$ = 0**
- **BF = 1**

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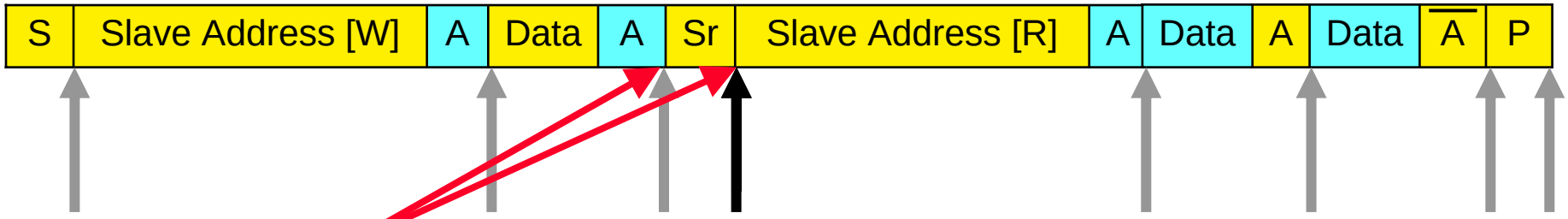
Events

- **Restart Condition**



Interrupts may overlap

SSPSTAT Bits

Check Buffer Full and Read Flag

- **S = 1**
- **R/$\overline{W}$ = 0**
- **BF = 0**

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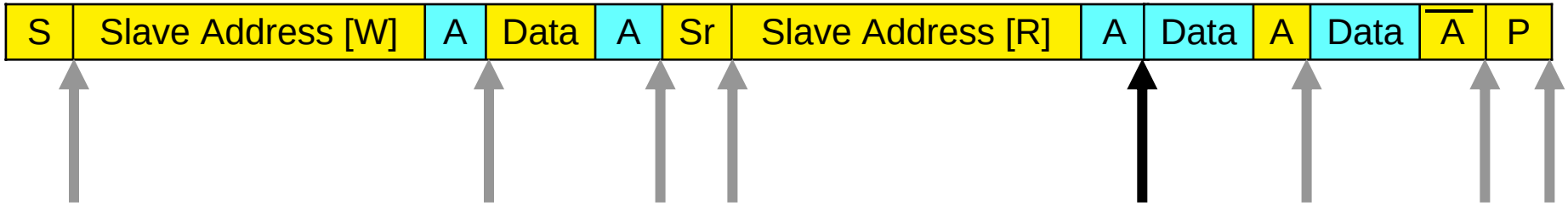
Events

- **Master Read Address**
  - Master has sent a read request with a matching slave address



SSPSTAT Bits

- **D/$\overline{A}$ = 0**
- **R/$\overline{W}$ = 1**
- **BF = 1**

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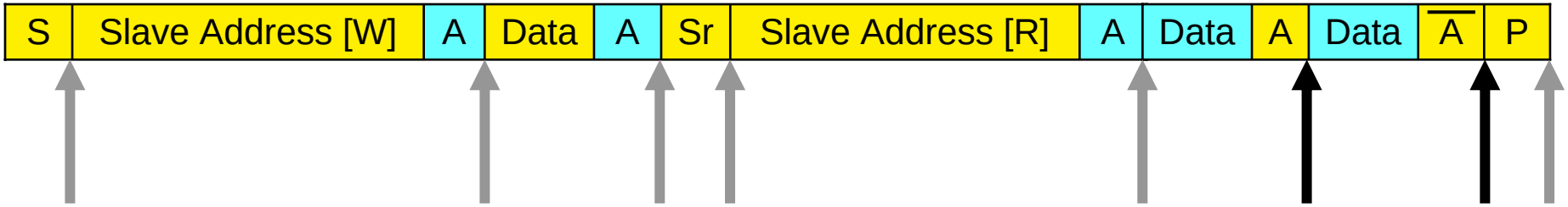
Events

- **Master Read Data**
  - Master has read a data byte after a matching slave address and read request has been sent



SSPSTAT Bits

- **D/$\overline{A}$ = 1**
- **R/$\overline{W}$ = 1**
- **BF = 0**

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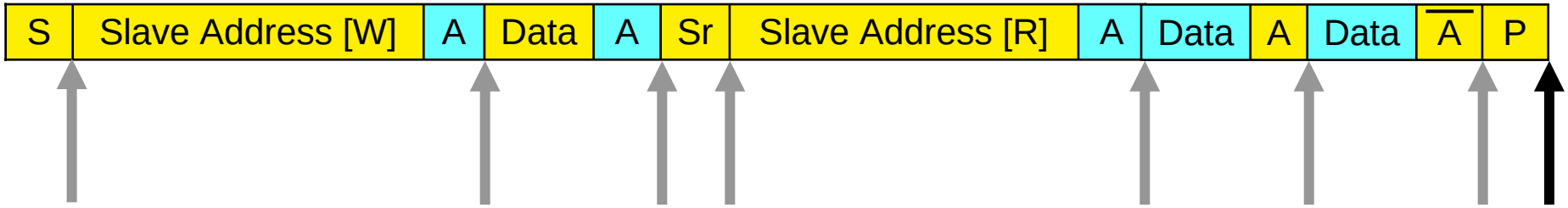
Events

- **Stop Condition**
  - The end of communication
  - The bus is free



SSPSTAT Bits

- **P = 1**

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Events Summary

- **We now know:**
  - How to decode each event:
    - **Write Events**
    - **Read Events**
    - **Start/Stop Conditions**

- **Next: actions to perform at each event**
  - Two types of message formats:
    - **Read, Write**

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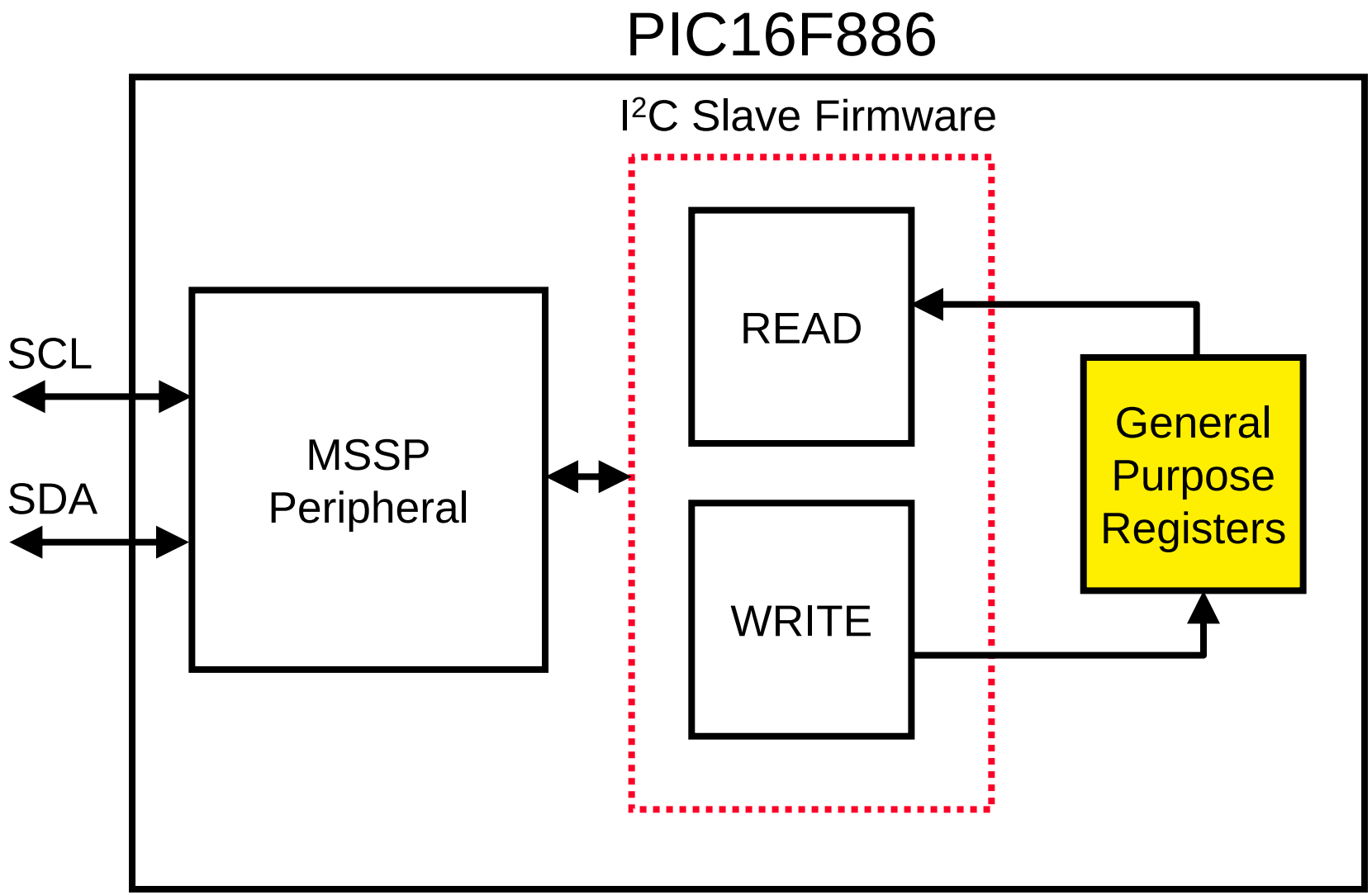
I²C™ Slave Mode Firmware Overview



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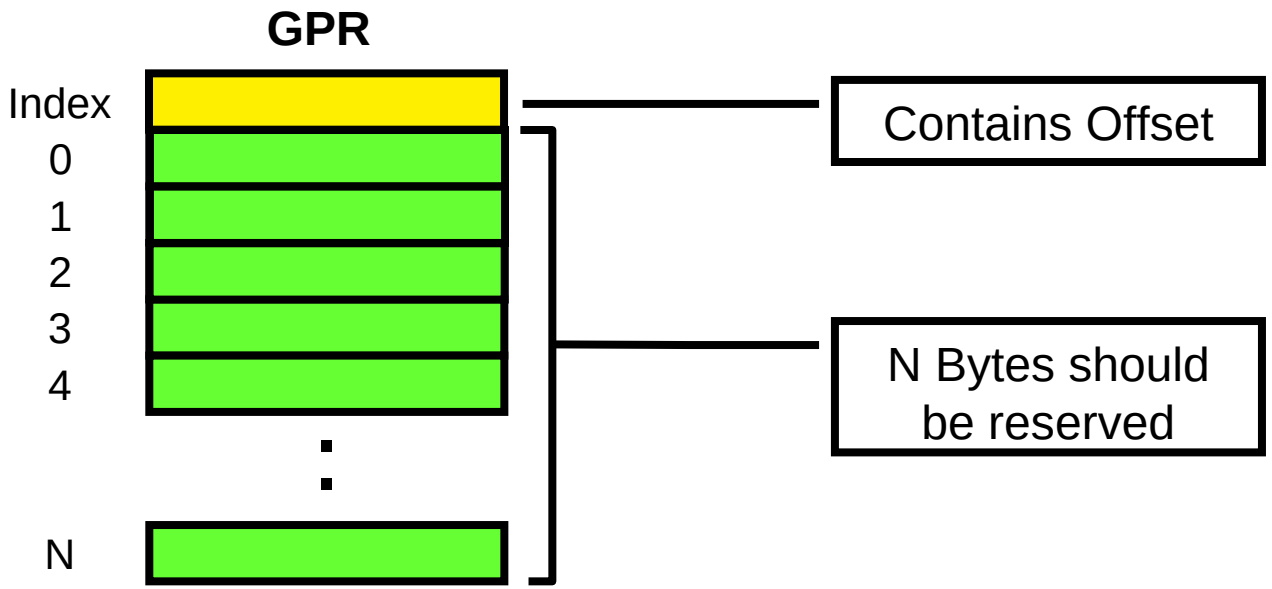
I²C™ Slave State Machine

- **General Purpose Registers**
  - Data must be sequential



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Assembly Code Example

```
#define DEVICE_RAM_LENGTH .9  ; Device RAM Length

#define BYTE0                 (DEVICE_RAM + 0x01)
#define BYTE1                 (DEVICE_RAM + 0x02)
#define BYTE2                 (DEVICE_RAM + 0x03)
#define BYTE3                 (DEVICE_RAM + 0x04)
#define BYTE4                 (DEVICE_RAM + 0x05)
#define BYTE5                 (DEVICE_RAM + 0x06)
#define BYTE6                 (DEVICE_RAM + 0x07)
#define BYTE7                 (DEVICE_RAM + 0x08)
#define BYTE8                 (DEVICE_RAM + 0x09)

udata

DEVICE_RAM  res   DEVICE_RAM_LENGTH
```

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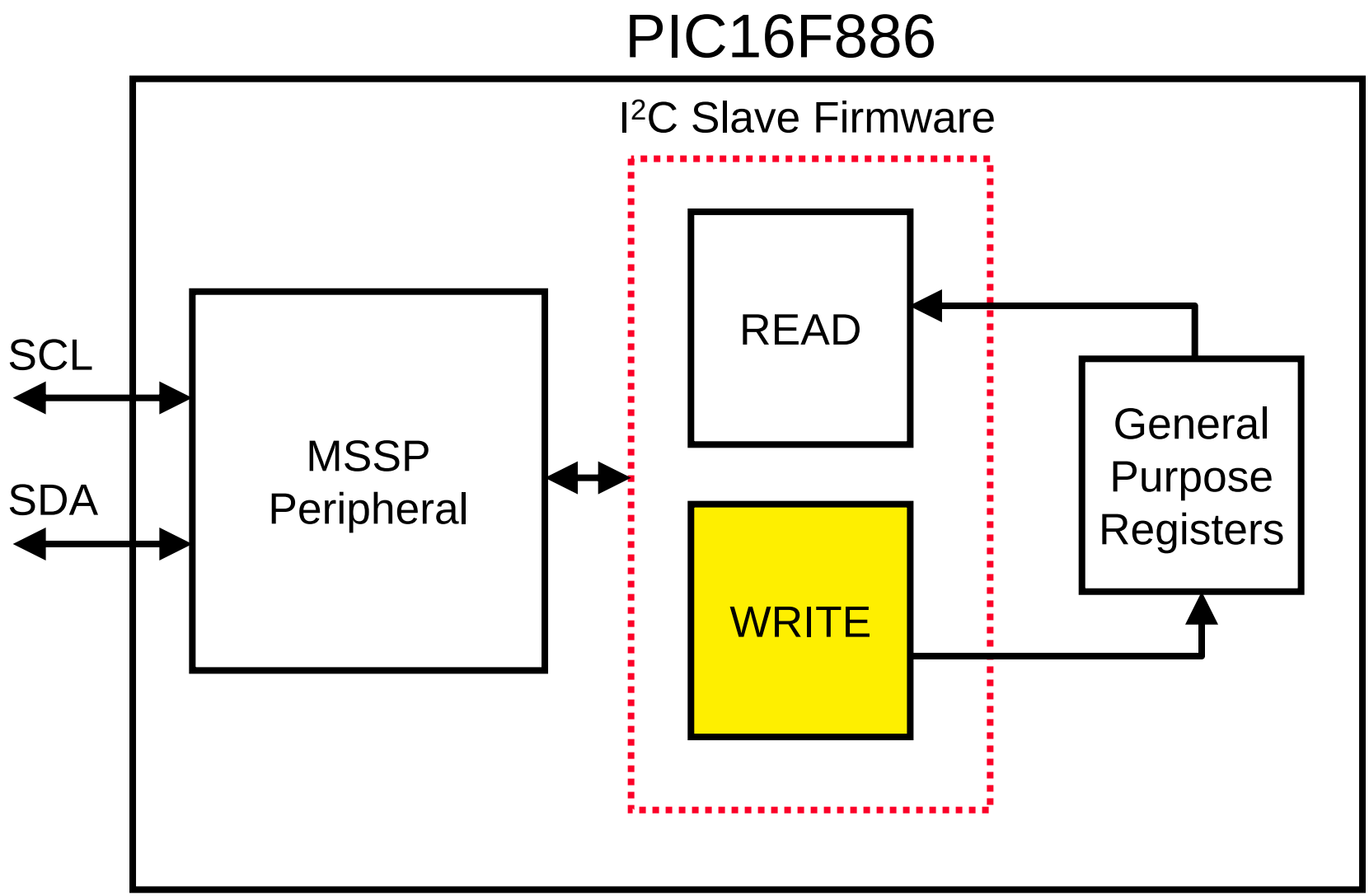
I²C™ Slave Mode Firmware Overview



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I²C™ Slave State Machine

- **Master Write**

S	Slave Address [W]	A	0x01	A	0x10	A	P

Write data byte (0x10) to word address (0x01)

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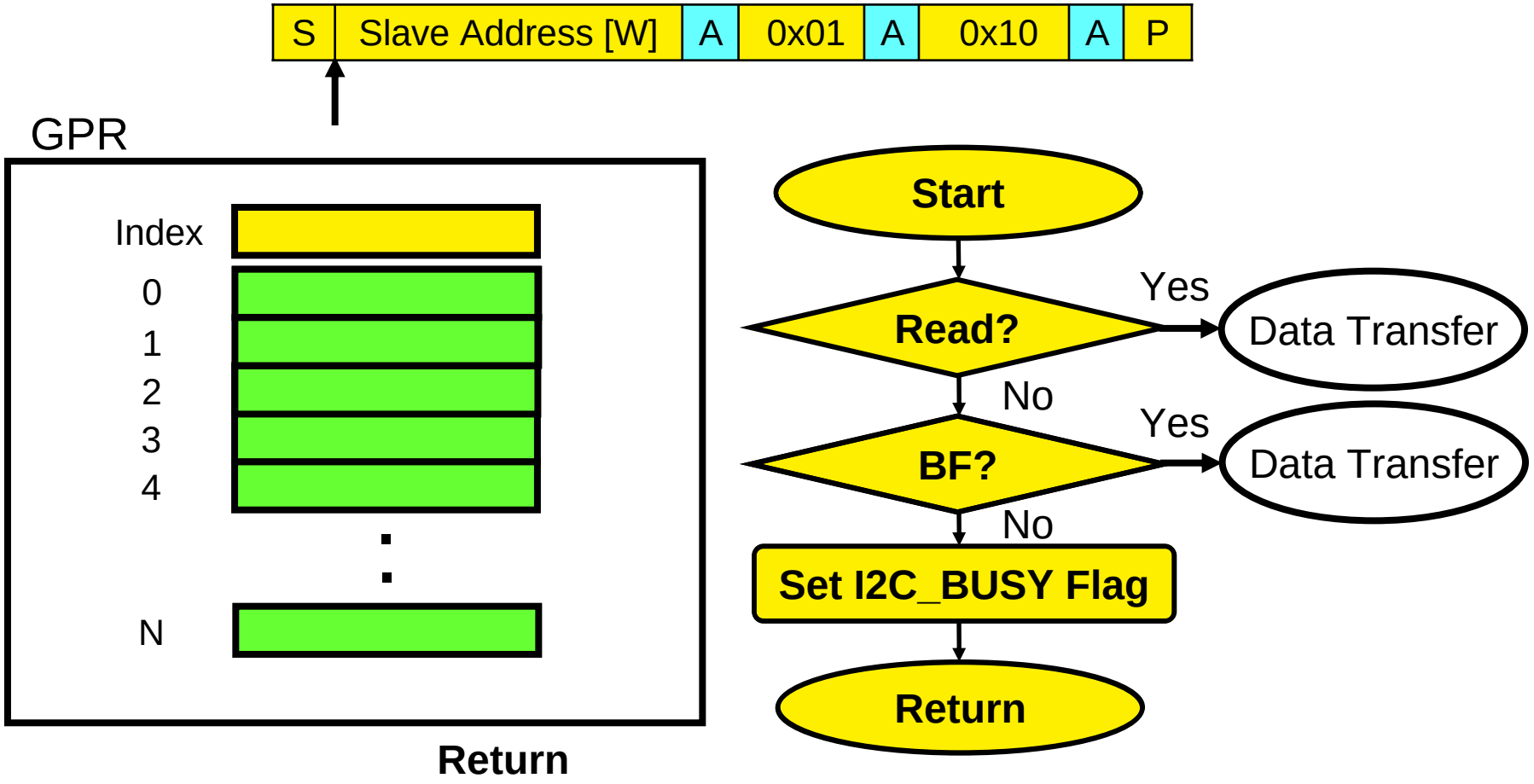
I²C™ Slave State Machine

- **Master Write**



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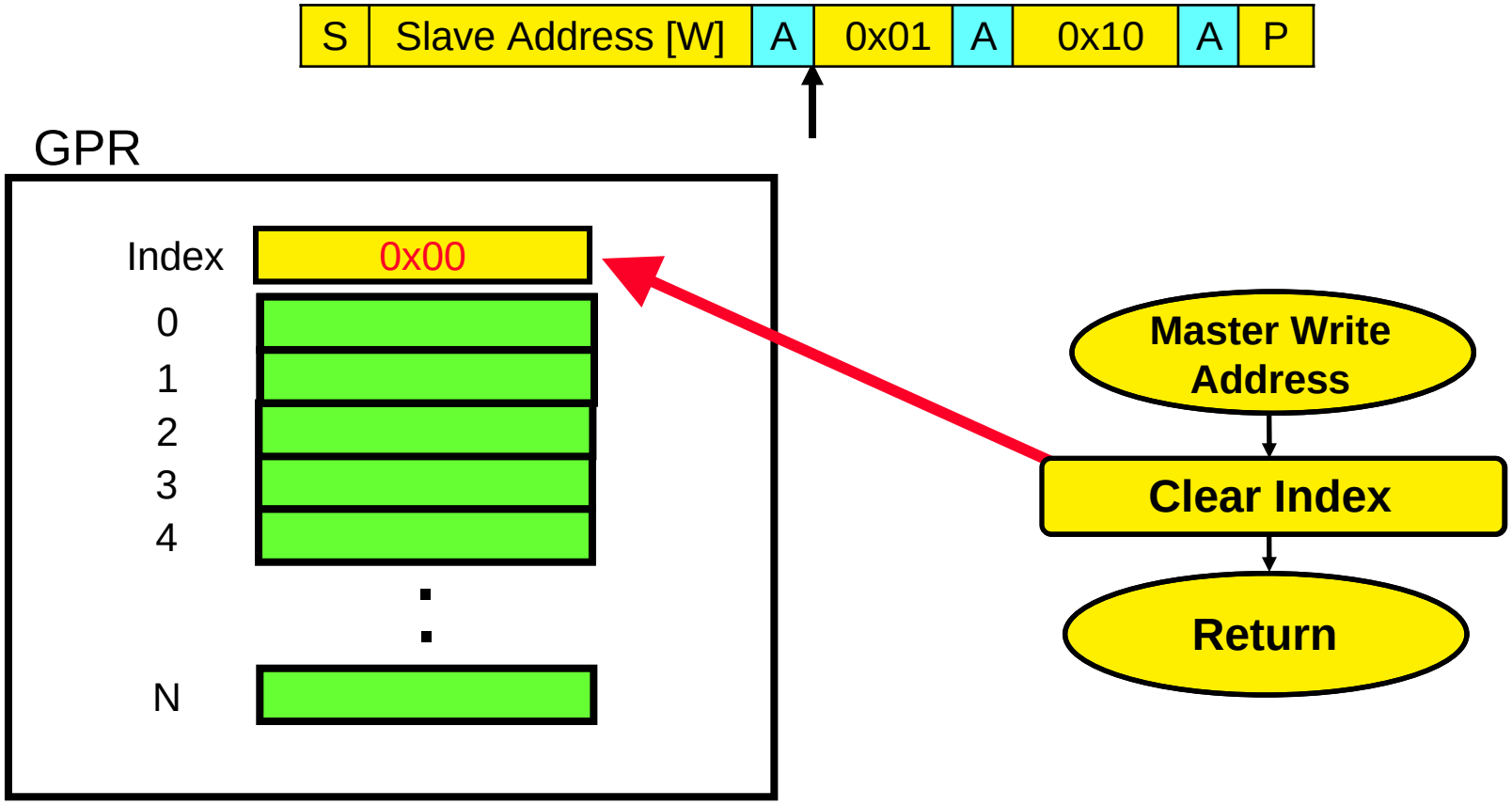
I²C™ Slave State Machine

- **Master Write**



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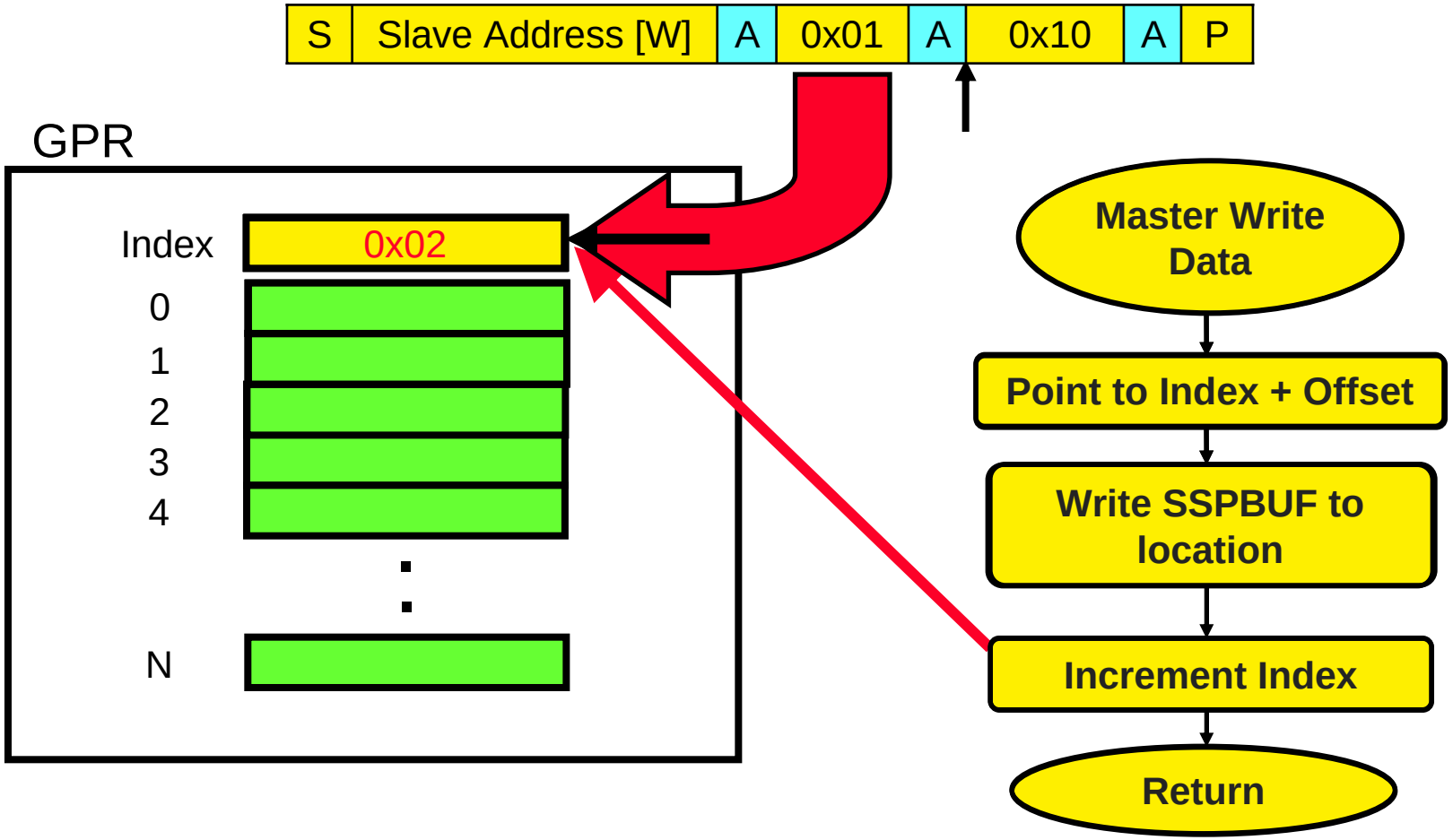
I²C™ Slave State Machine

- **Master Write**



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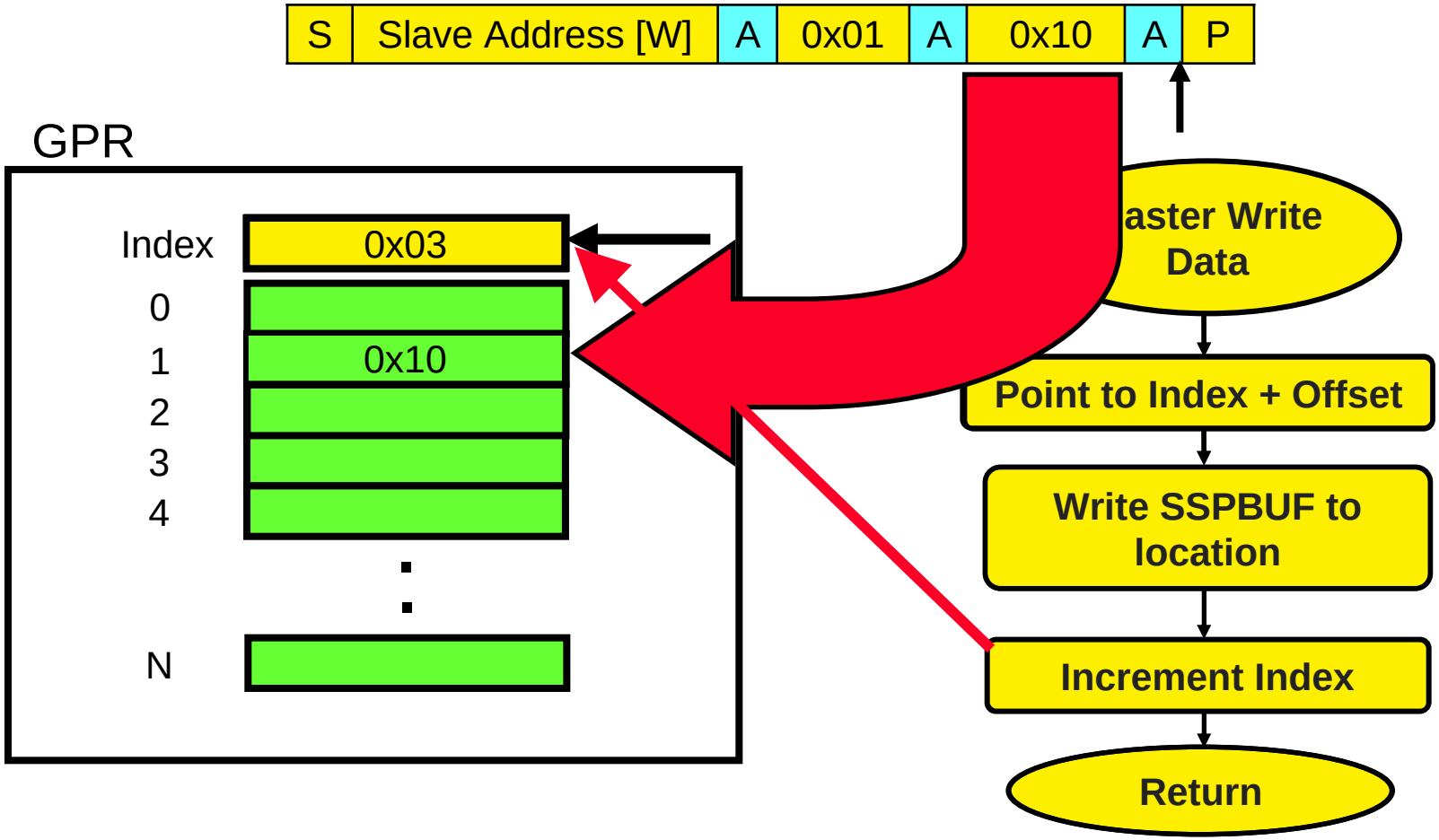
I²C™ Slave State Machine

- **Master Write**



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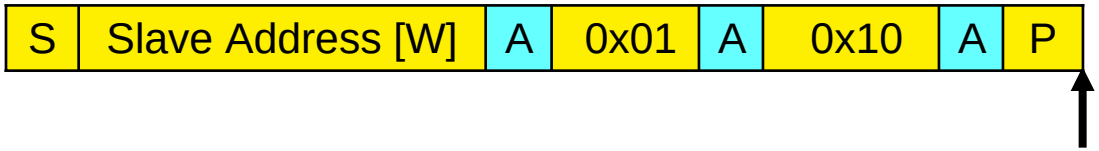
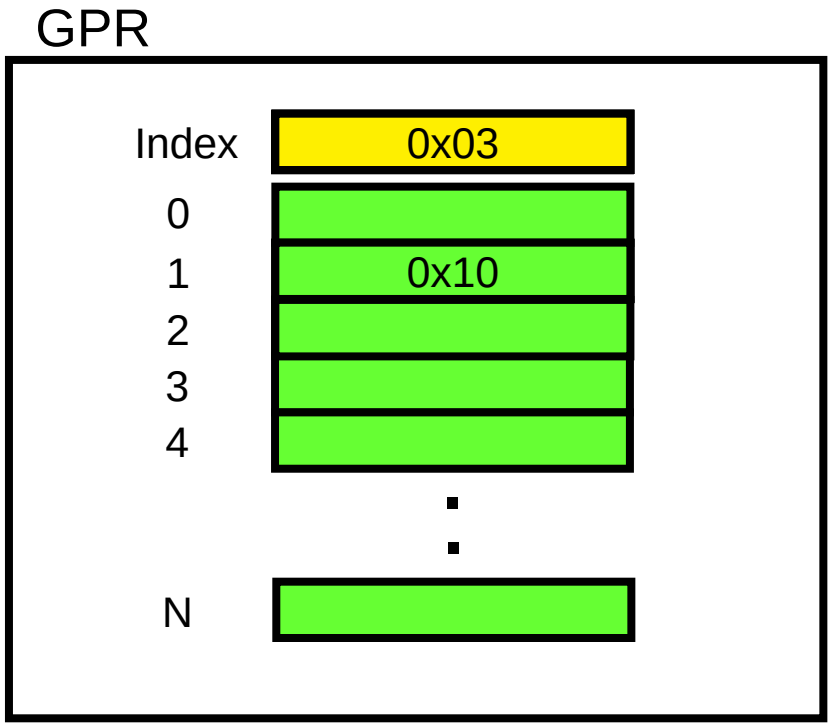
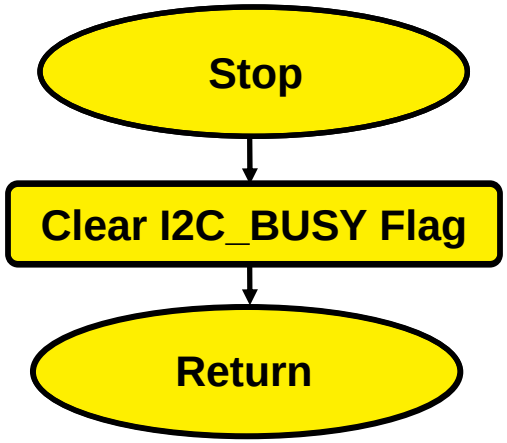
I²C™ Slave State Machine

- **Master Write**







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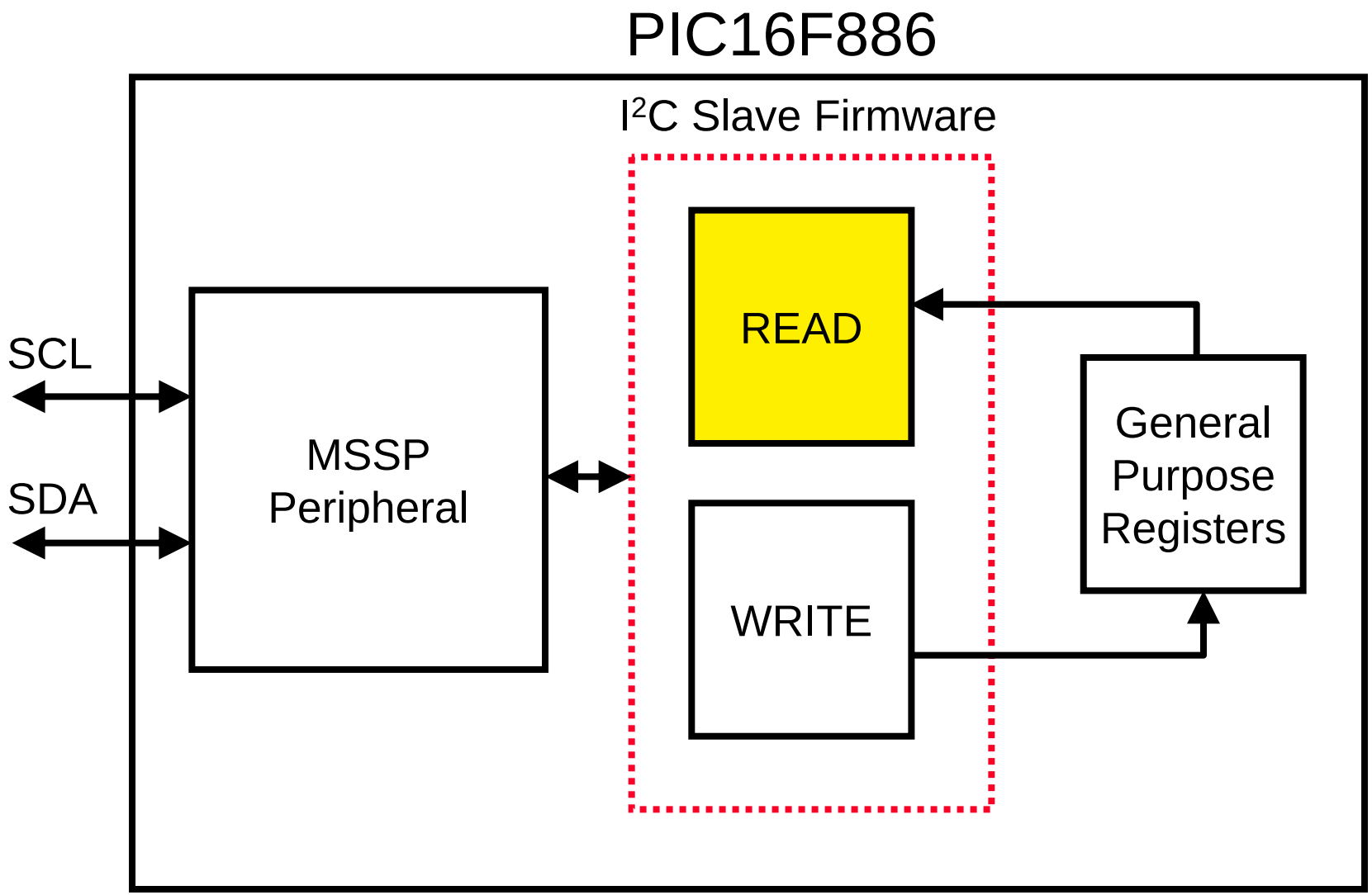
I²C™ Slave Mode Firmware Overview



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I²C™ Slave State Machine

- **Master Write then Read (Combination)**

Read two data bytes starting from word address (0x02)

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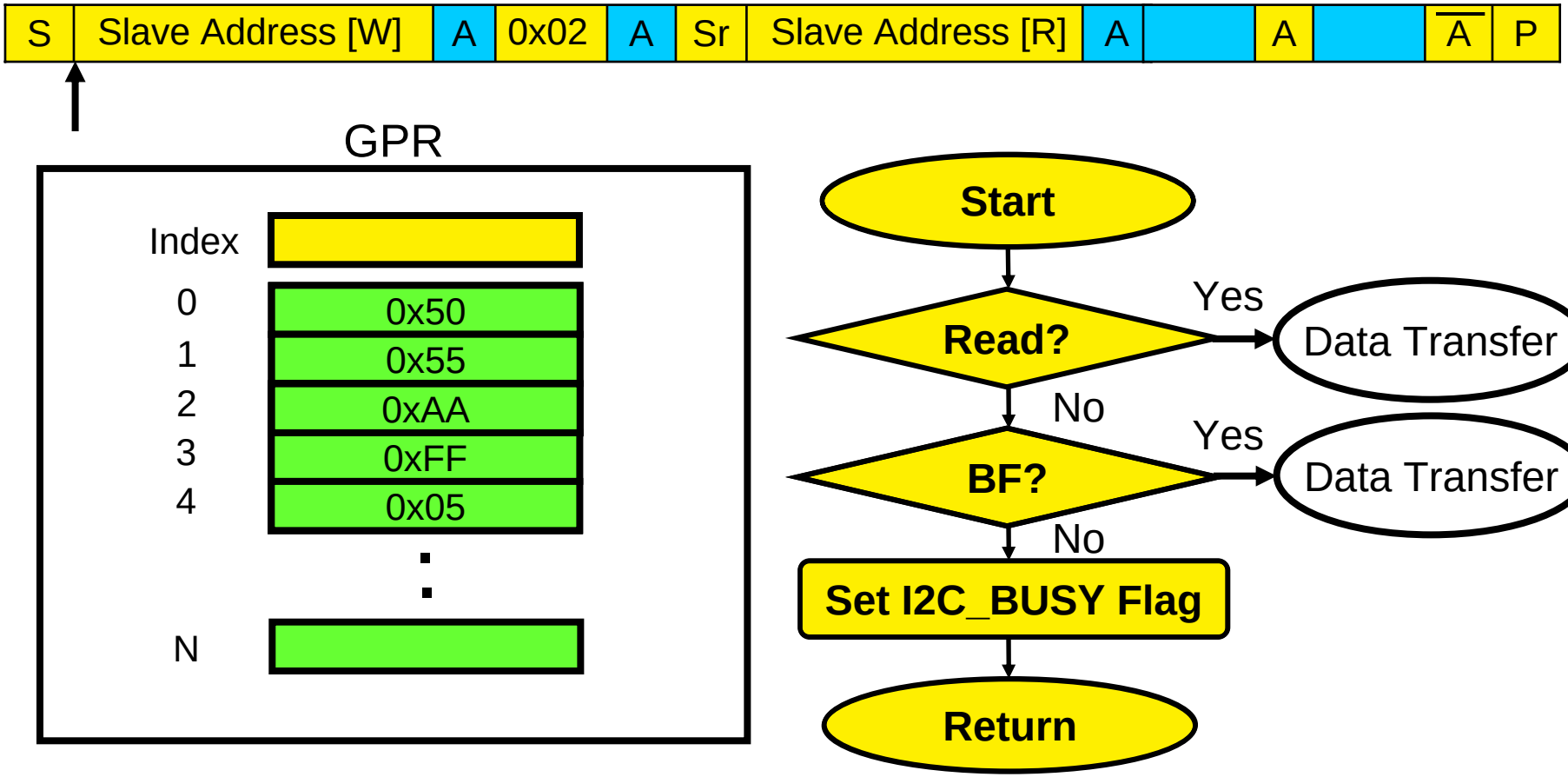
I²C™ Slave State Machine

- **Master Write then Read (Combination)**



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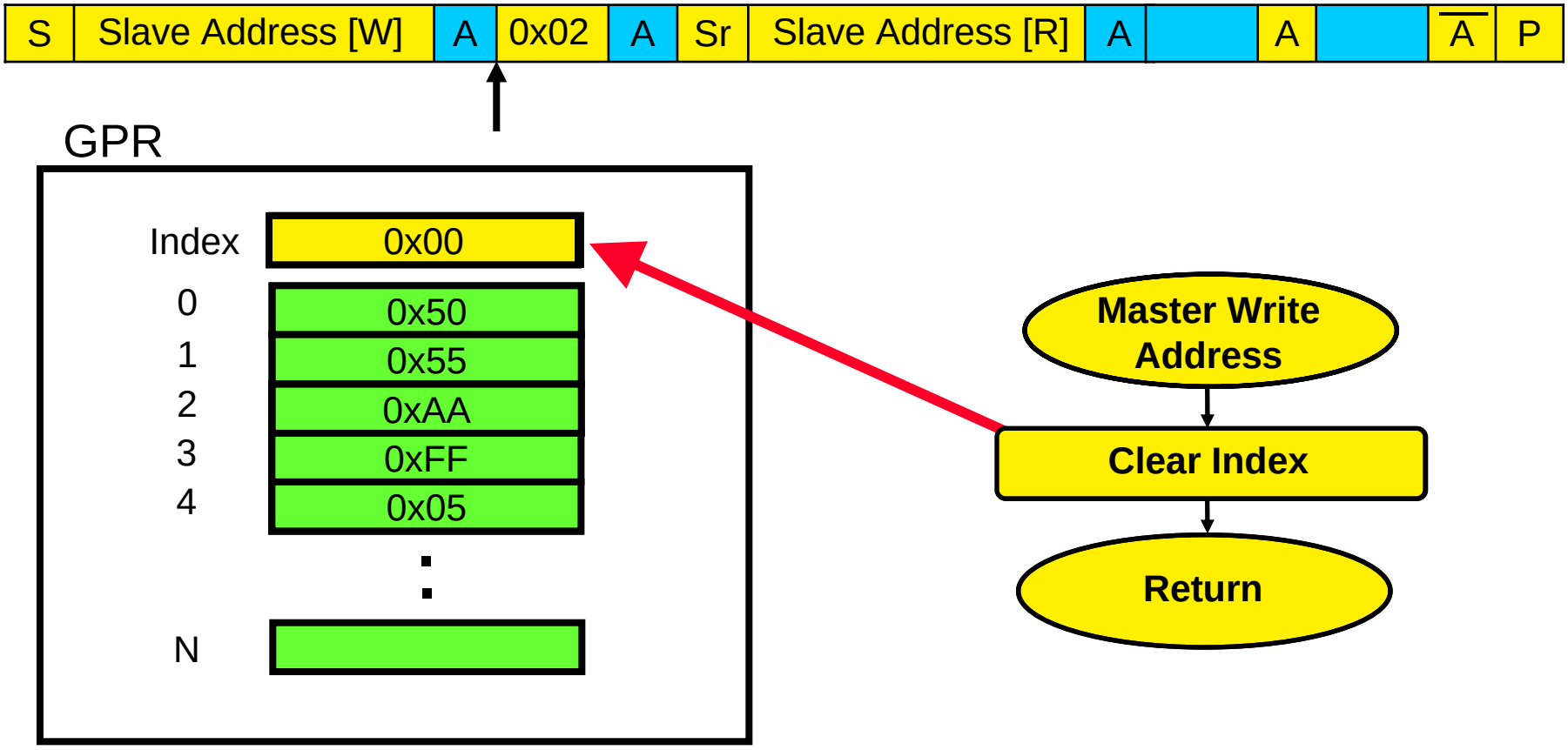
I²C™ Slave State Machine

- **Master Write then Read (Combination)**



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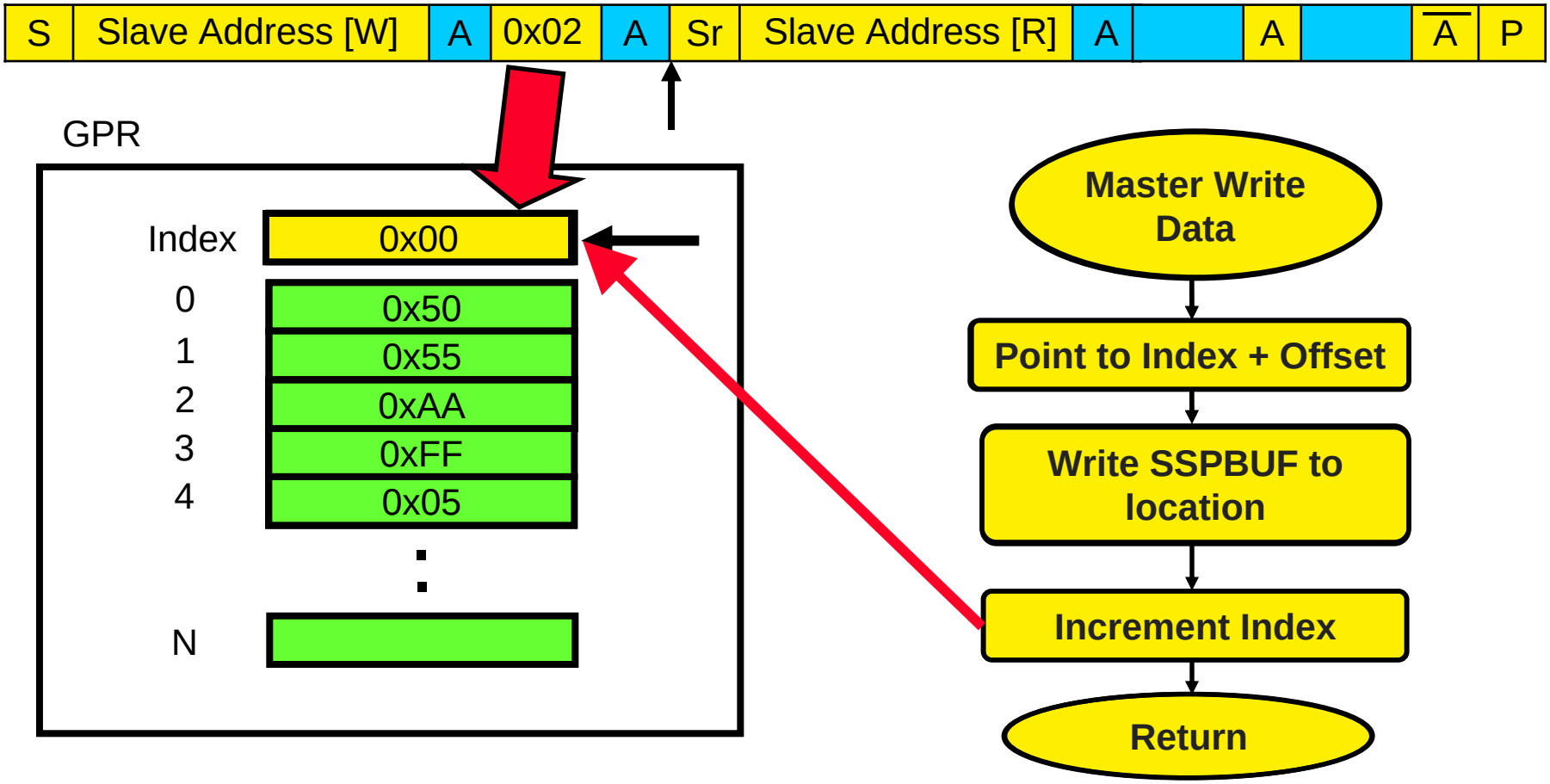
I²C™ Slave State Machine

- **Master Write then Read (Combination)**



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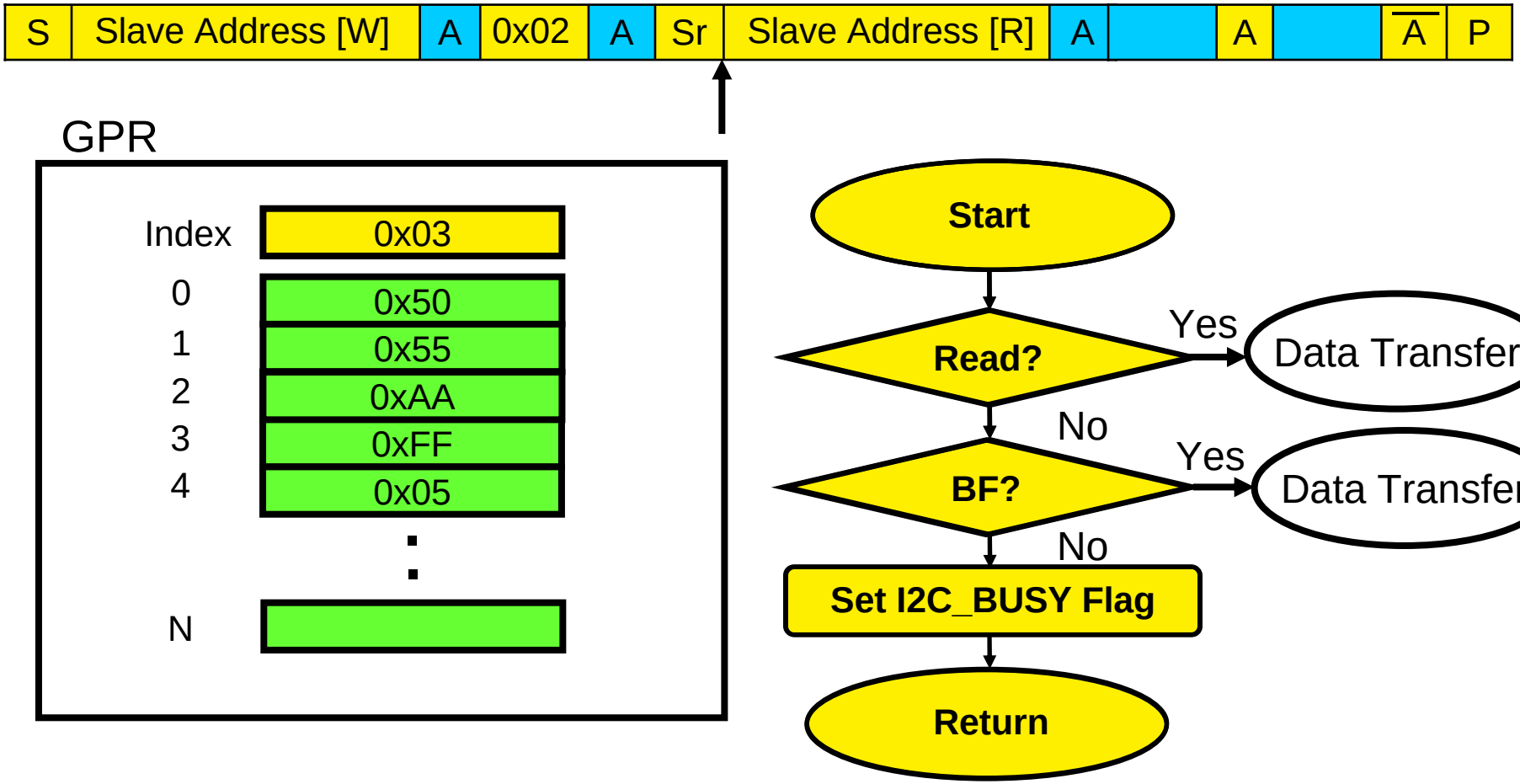
I²C™ Slave State Machine

- **Master Write then Read (Combination)**



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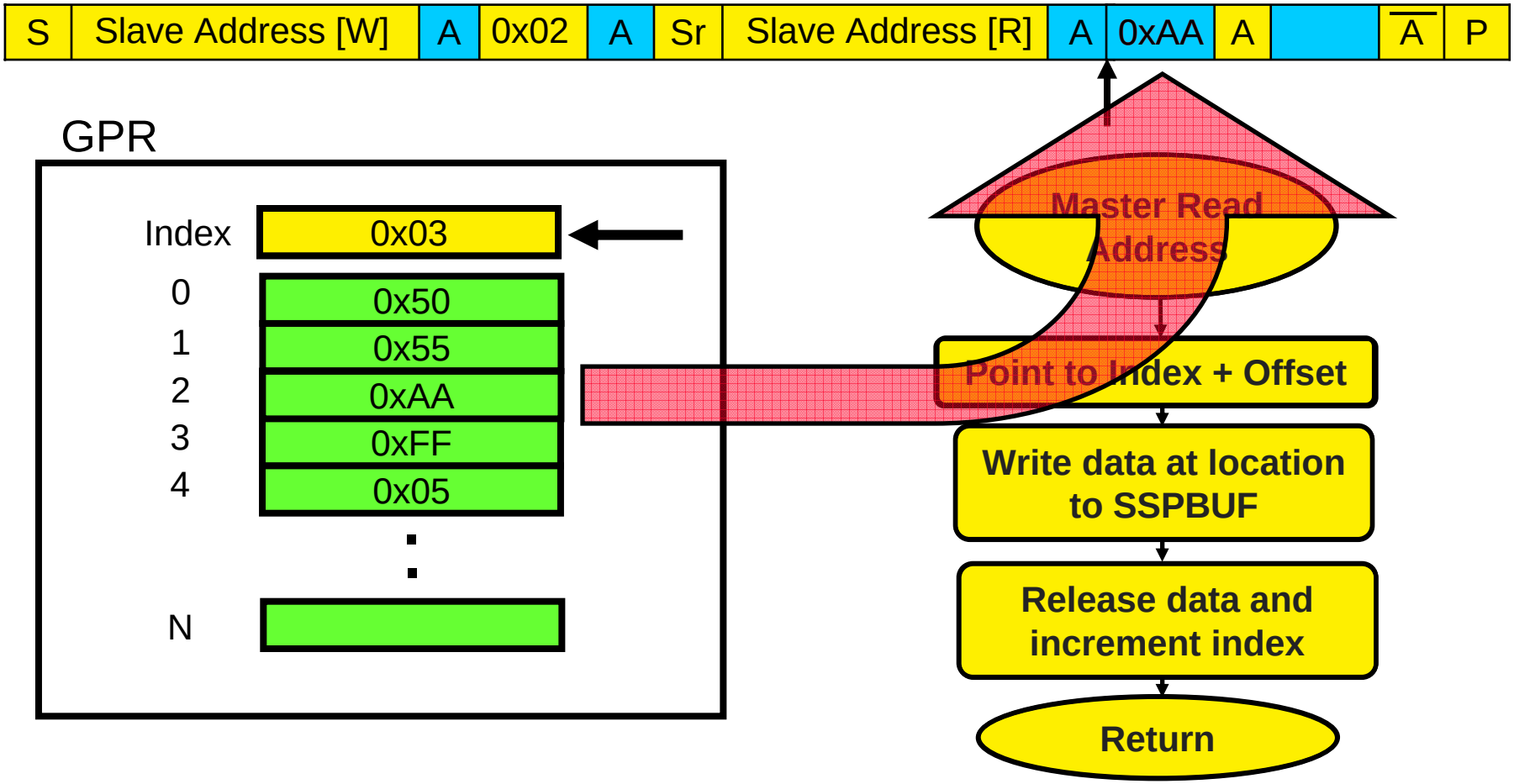
I²C™ Slave State Machine

- **Master Write then Read (Combination)**



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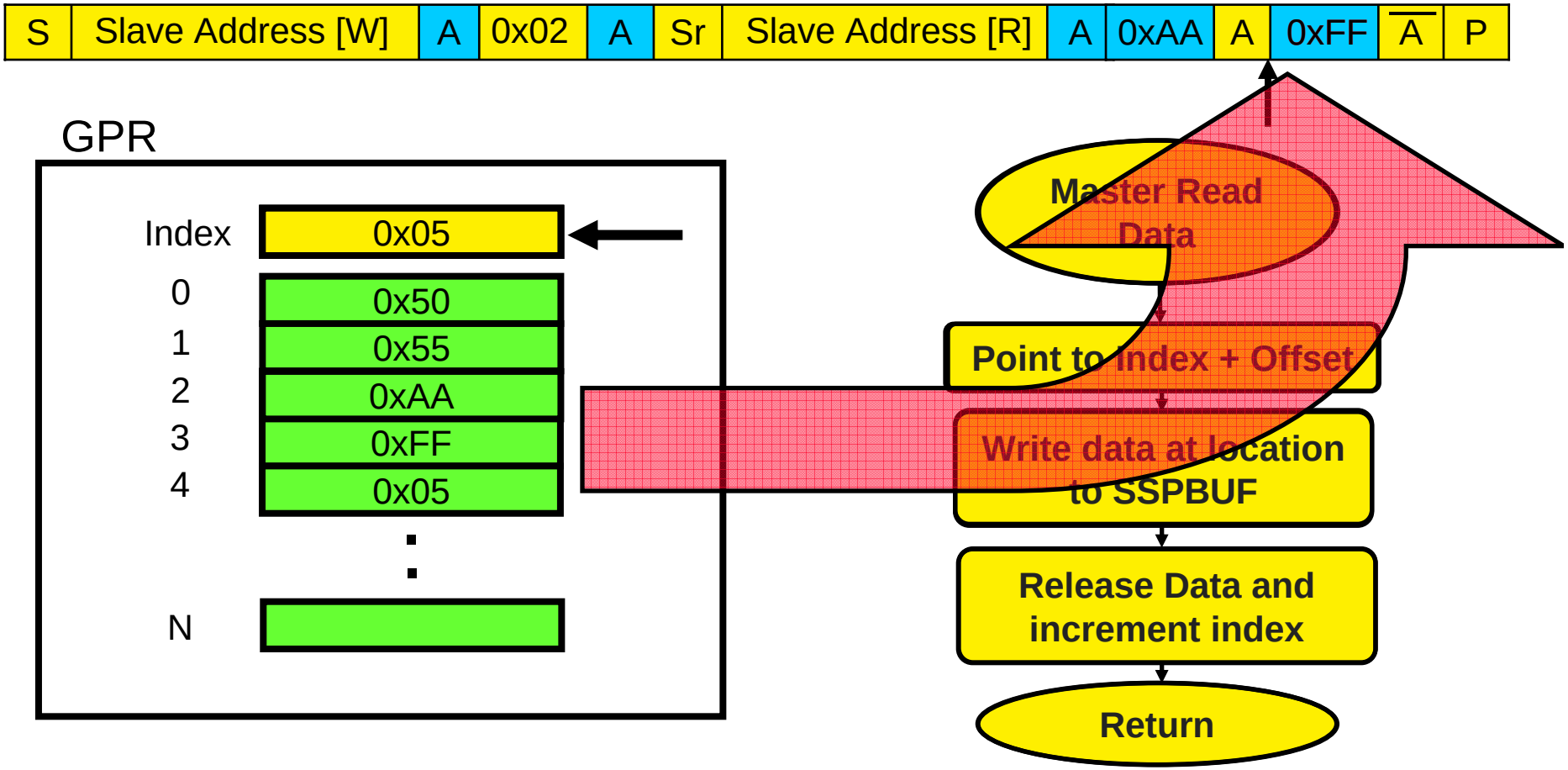
I²C™ Slave State Machine

- **Master Write then Read (Combination)**



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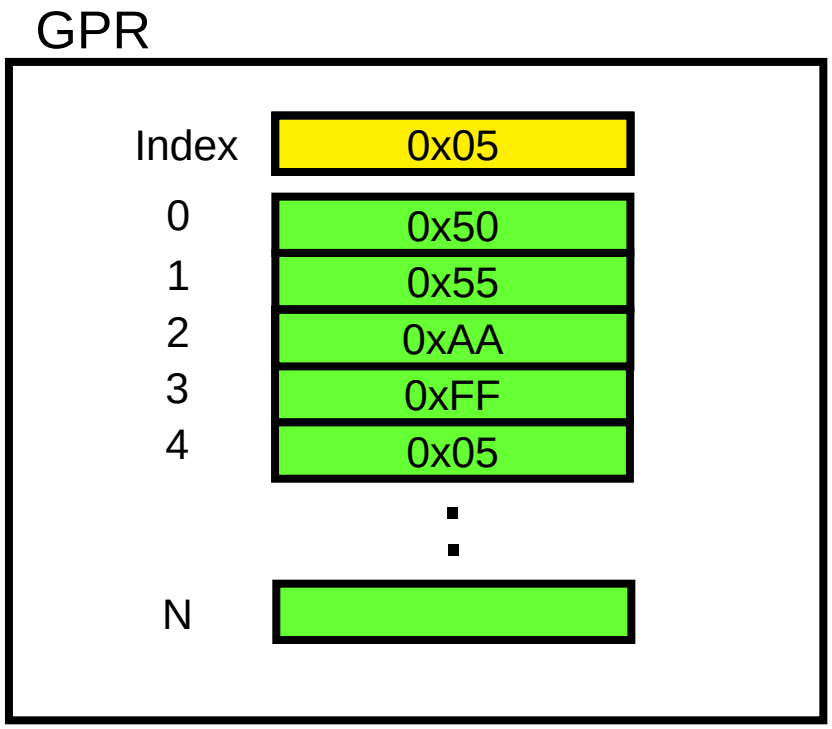
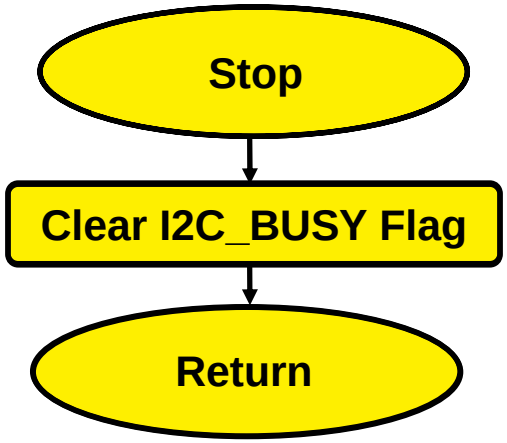
I²C™ Slave State Machine

- **Master Write then Read (Combination)**

S	Slave Address [W]	A	0x02	A	Sr	Slave Address [R]	A	0xAA	A	0xFF	$\overline{A}$	P





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I²C™ Slave State Machine

- **Summary**
  - Performs operations to GPRs
  - Write Operation
  - Read Operation
  - MUST specify the word address
  - **Gotchas:**
    - SSPSTAT is updated during each interrupt event
    - Interrupt events may occur before an event is serviced

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Programming the MSSP

- **Summary**
  - Firmware Overview
  - Events
  - I^2C™ Slave State Machine
    - Master Write
    - Master Write then Read (Combination)

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Summary

- I²C™ Protocol Overview
- PICkit™ Serial Analyzer
- Configuring the MSSP peripheral for I²C slave mode
- Programming the MSSP peripheral as an I²C slave

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Bonus Material

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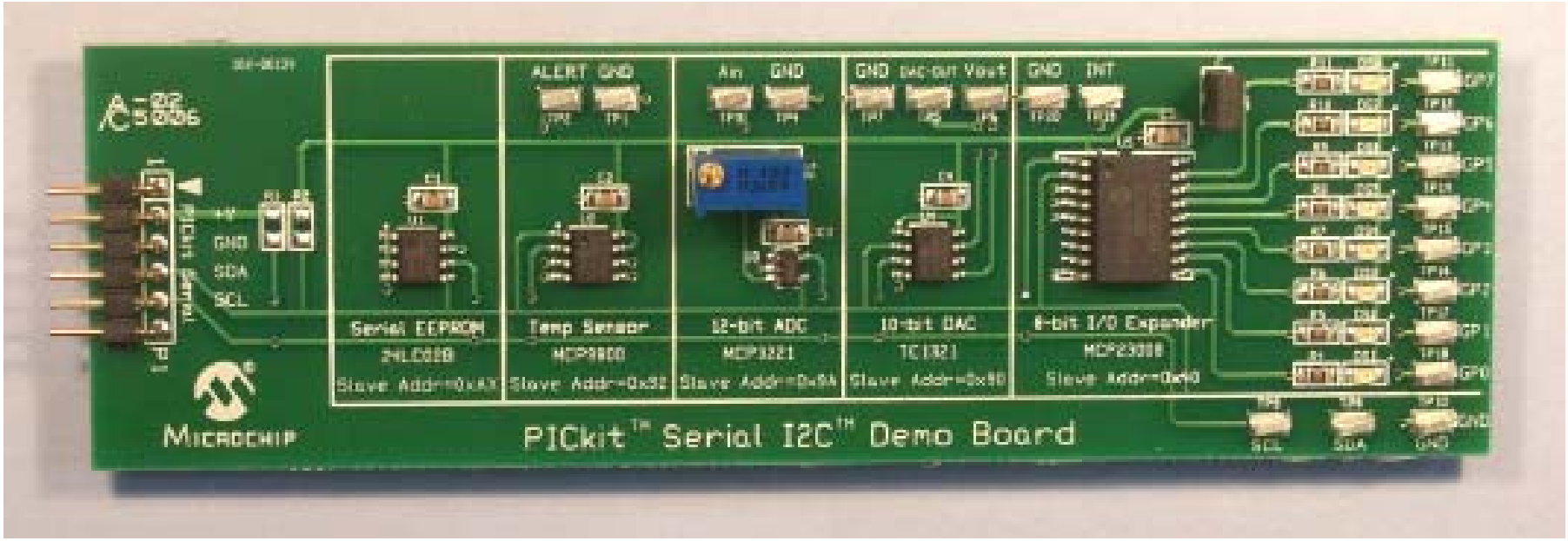

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