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11092 PFC

Digital Power Factor Correction (PFC) using the dsPIC30F6010A

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Class Agenda

- Significance of Power Factor in power conversion systems – 20 min
- How to achieve Power Factor Correction? – 15 min
- Digital PFC Design and Implementation using dsPIC® DSC – 15 min
- Compensator Design – 20 min
- Feed Forward Compensation – 15 min
- Demonstration – 20 min

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Class Objectives

- Basics of PFC hardware
- PFC digital control loop implementation using dsPIC® DSC
- Design of voltage, current and feed forward control loops

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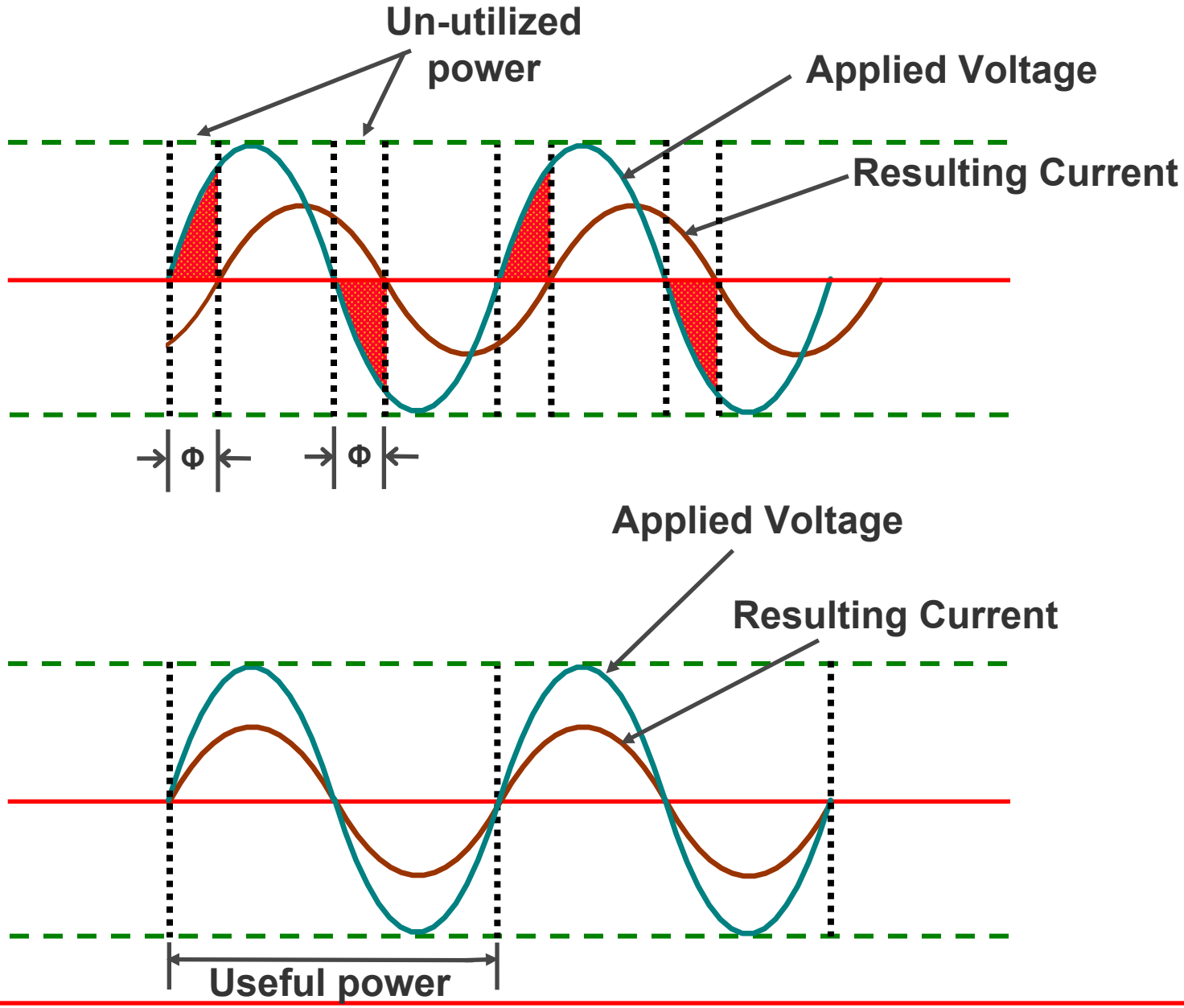
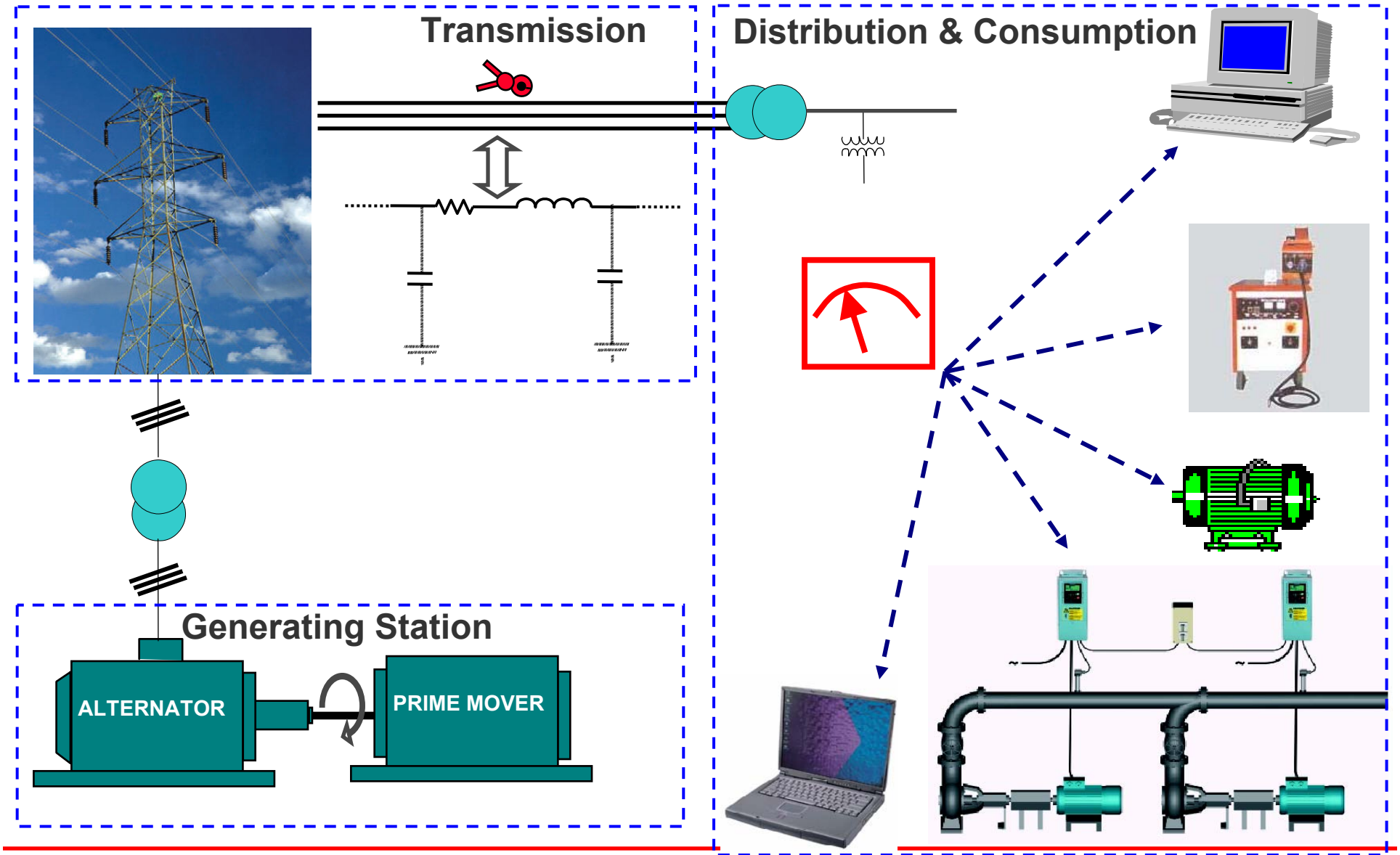
What is Power Factor?



Sources of Poor Power Factor?



Power Factor Degradation

Case 1

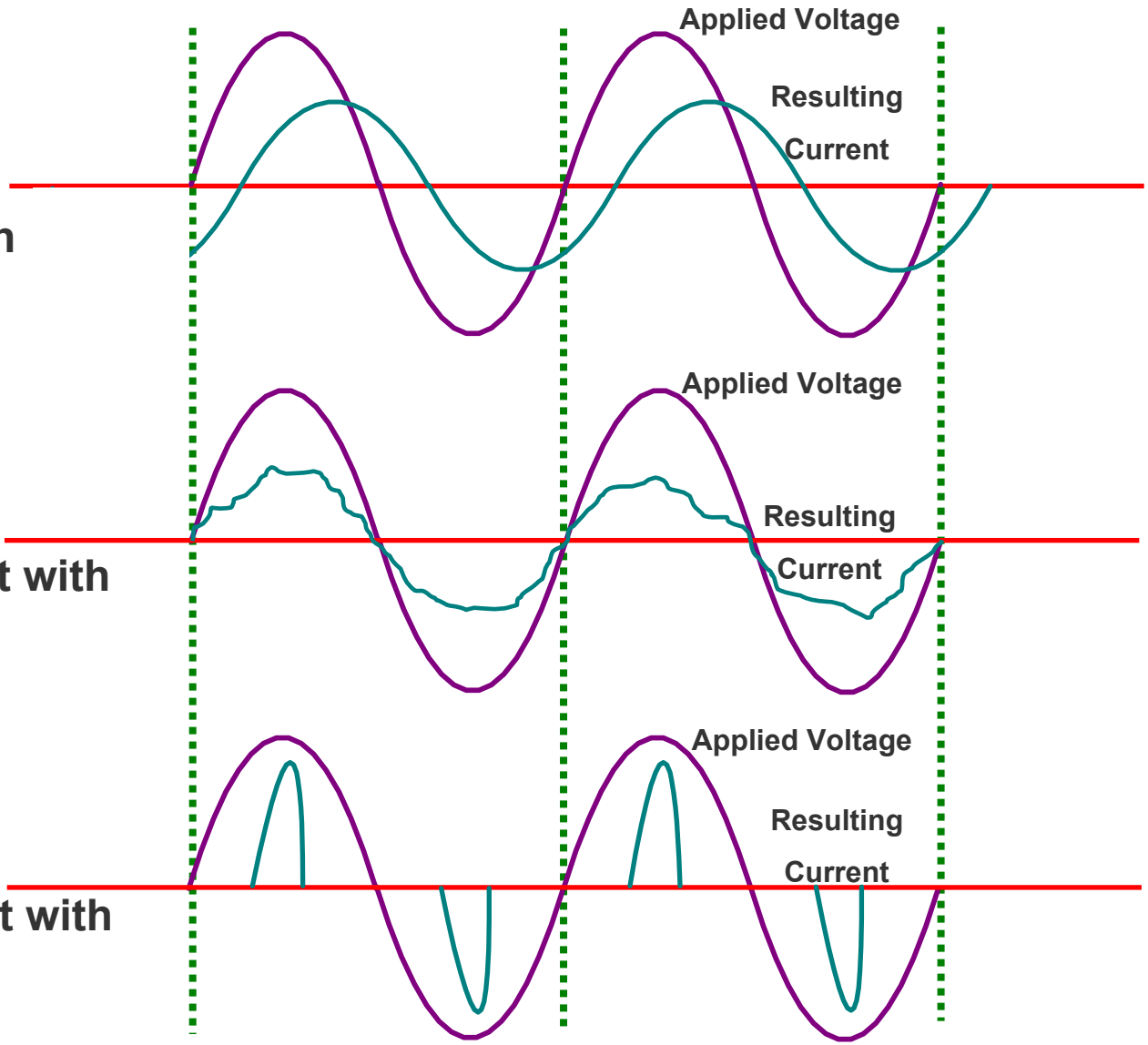
Sinusoidal Current with phase shift

Case 2

Non-Sinusoidal Current with no phase shift

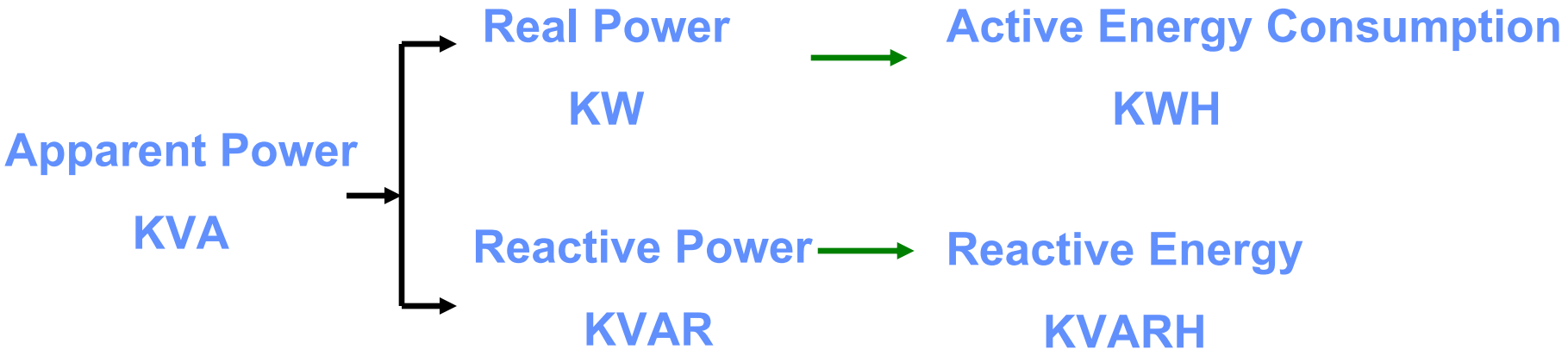
Case 3

Non-Sinusoidal Current with phase shift



How is PF measured ?

PF provides a relation between working power and apparent power

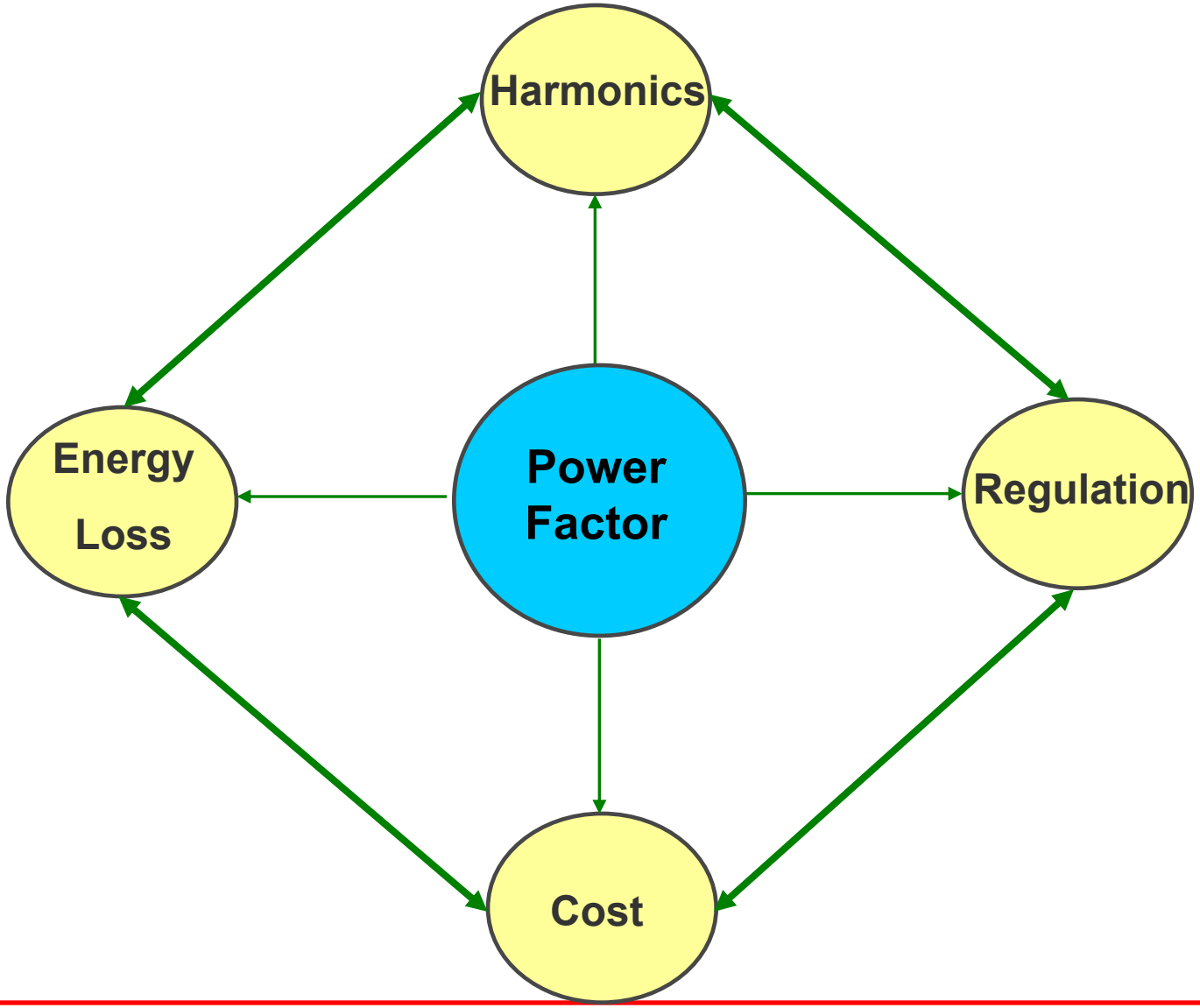


$$Power\ Factor = Real\ Power\ /\ Volt\ x\ Ampere$$

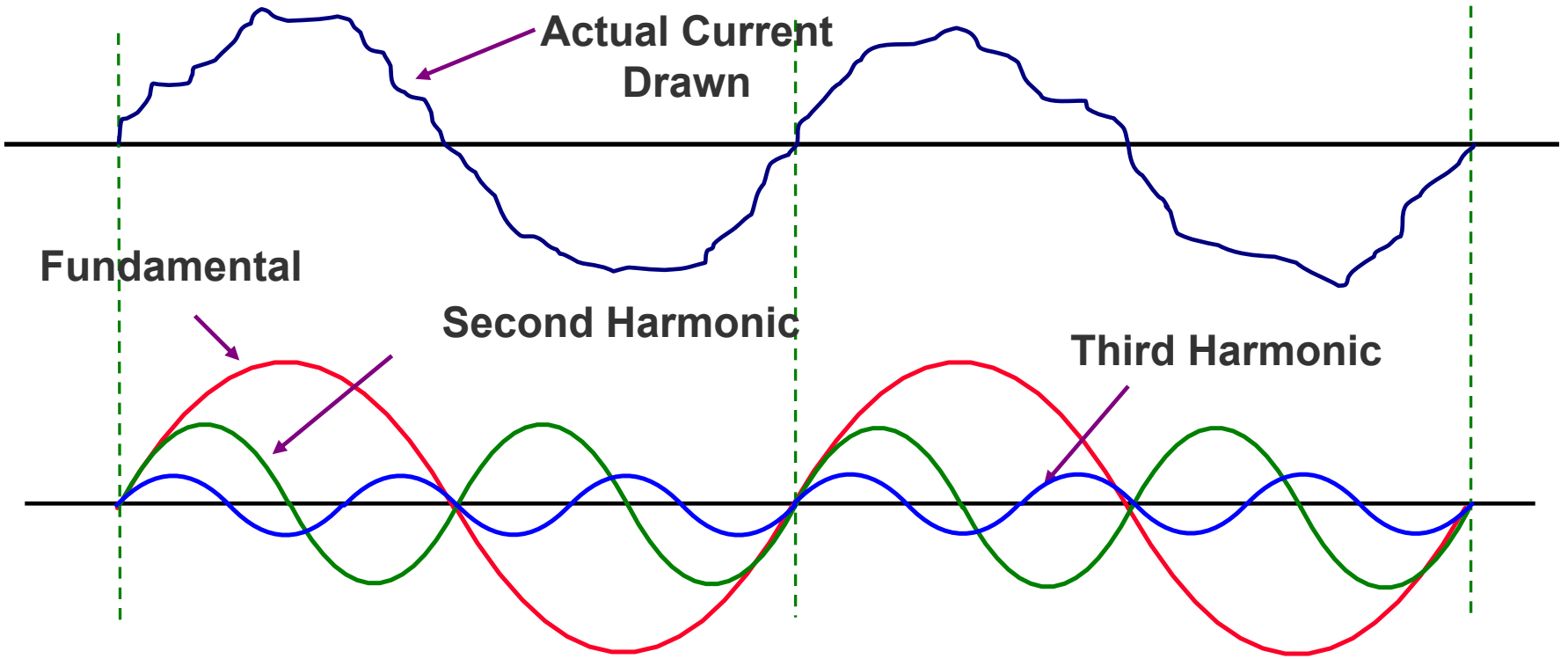
$$PowerFactor = \underbrace{\cos\phi}_{\text{Displacement Factor}} \cdot \underbrace{\sqrt{\frac{1}{1 + (I_2/\ I_1)^2 + (I_3/\ I_1)^2 + \ldots}}}_{\text{Distortion Factor}} = \frac{\cos\phi}{\sqrt{1 + THD^2}}$$

THD : Total Harmonic Distortion

Why is Power Factor Important ?



Current Harmonics



Problems caused:

- Erroneous operation of system components
- Interference with neighboring equipment
- Overheating of transformers, motors, lighting ballasts etc…

Regulations

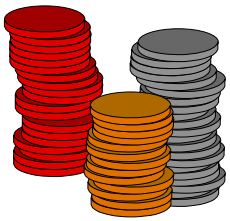
EN 61000-3-2 (IEC 1000-3-2) ***Valid from January 2001***

- Equipment with <= 16A per phase, 230V line voltage
- Equipments categorized into four:
  - Class A : General
  - Class B : Portable Tools
  - Class C : Lighting
  - Class D : Equipment with special line current shape
- Up to 40 harmonic currents are imposed limits
  - Class A : Absolute Limits
  - Class B : Absolute Limits
  - Class C : Relative Limits
  - Class D : Both Relative and Absolute Limits
- Based on IEC 555 (EN60555)

IEEE 519

- Recommended practices and requirements from IEEE for harmonic control in electrical power systems

Cost



- **Customers are charged penalties for Poor PF**
  - Electric utilities' generation, transmission and distribution capacities need to be larger
  - Power losses in the distribution system resulting in voltage sags, over heating and even premature failure of equipment
  - Components with higher rating needed for sustaining high harmonic peak currents

Energy loss

- Energy losses in active and passive elements
  - **they operate at higher RMS and peak currents**
- Energy needed by reactive elements
  - **un-utilized energy returned back to the grid**
- Energy losses in transmission and distribution systems

Goal of Power Factor Correction!

- **Shape the input current to follow the voltage**
  - Reduce current harmonics and improve THD
  - Reduce circulating currents due to reactive power
  - Reduce power rating of components due to lesser peak current
- **Regulate output voltage**
- **Meet regulatory requirements**
- **Reduce operating costs**
- **Reduce system losses**
- **Effective utilization of energy**

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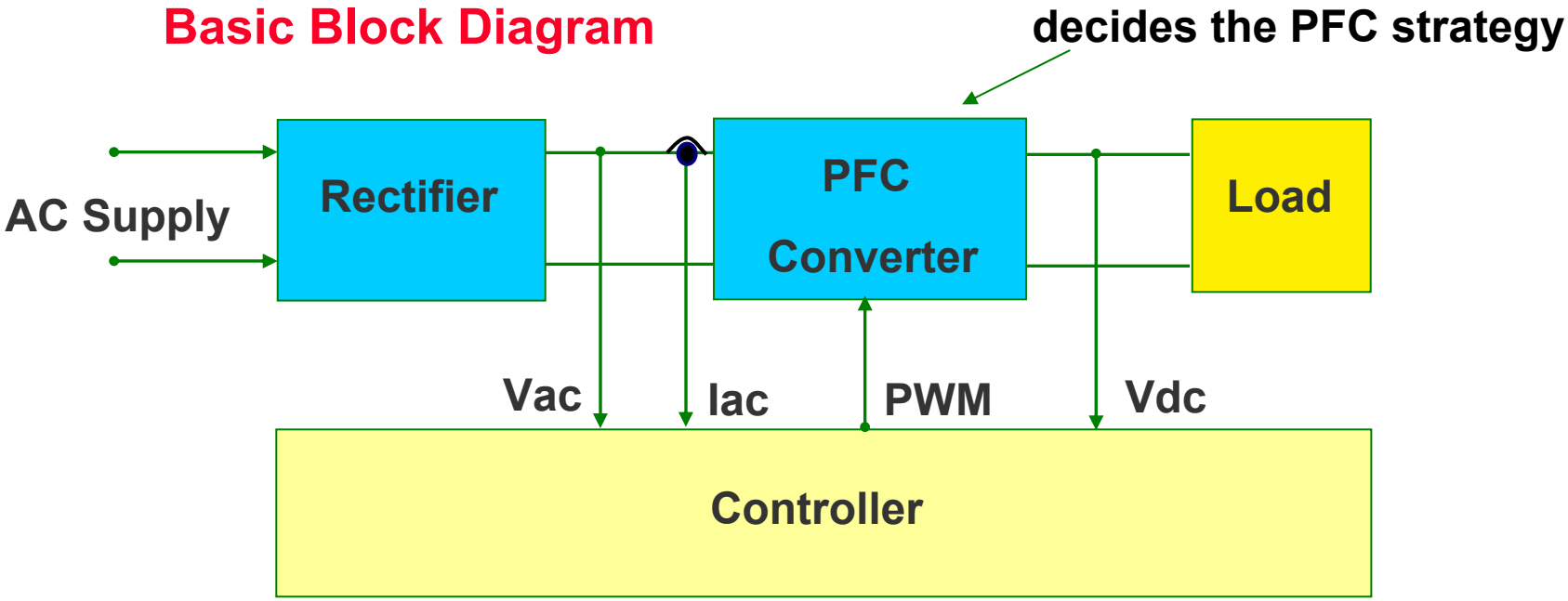
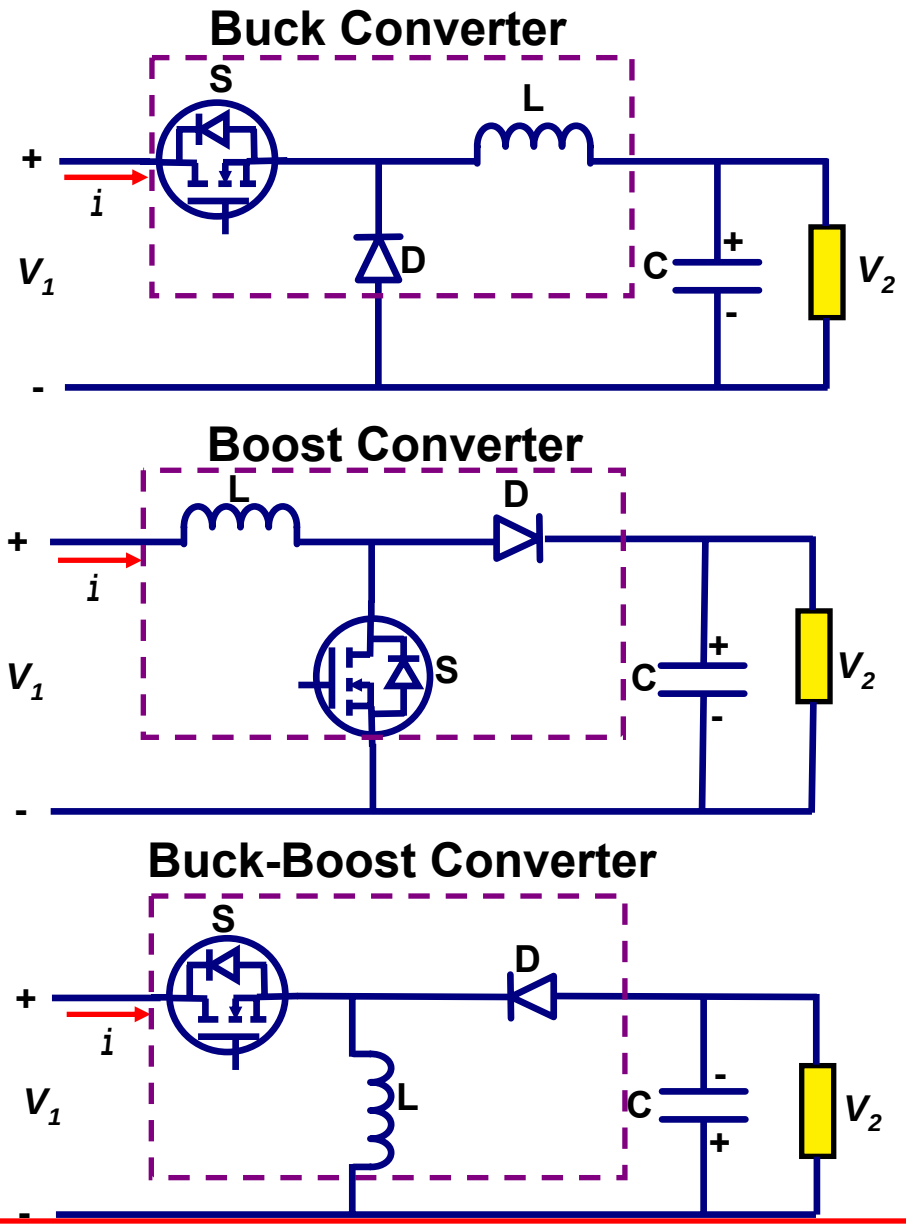
Basic Building Blocks

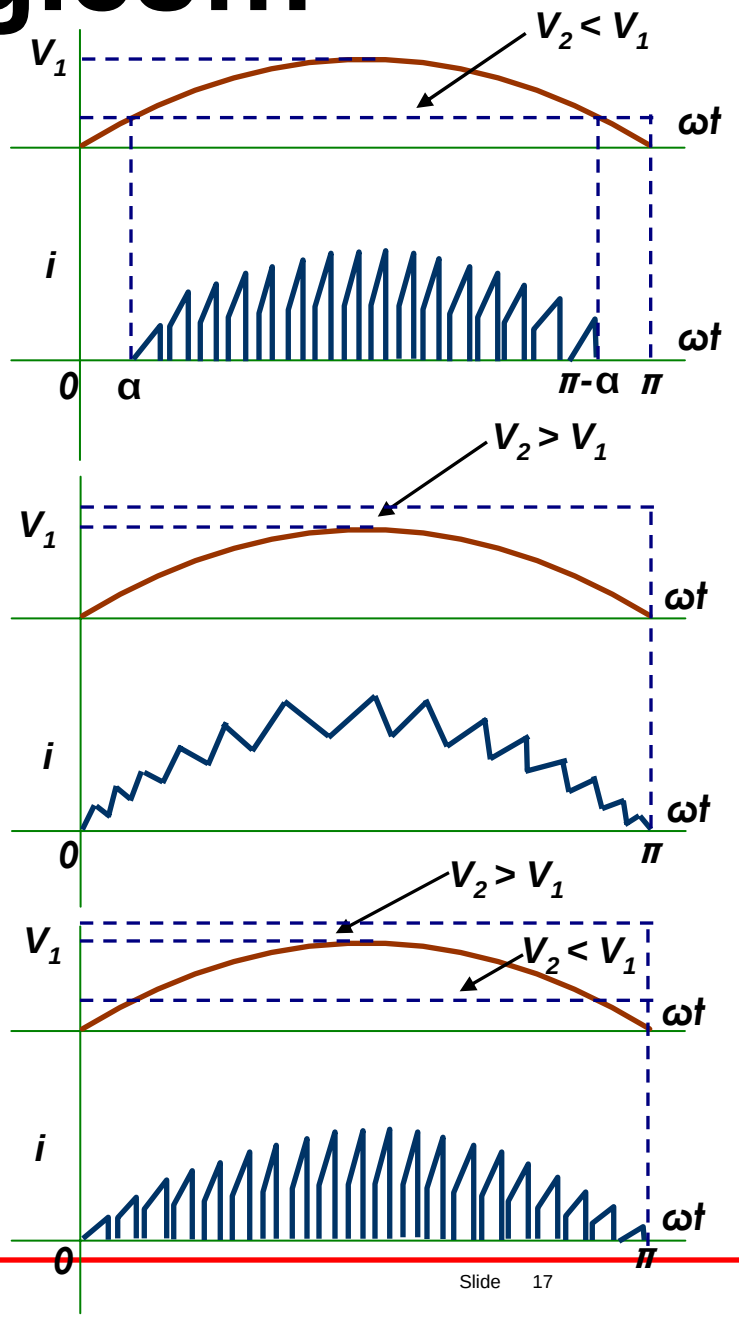
Basic Block Diagram



Basic Components of the PFC Converter

PFC Strategies…





Choice of PFC Circuit?

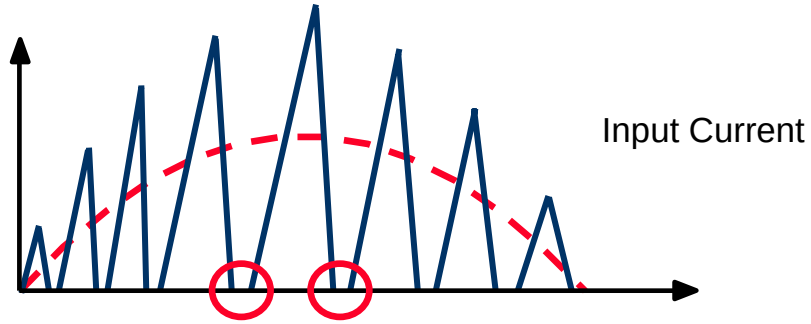
Comparison of the three converters:

Type of Converter	Output Voltage Polarity	Crossover Distortions	Line Current Shape
Buck	Positive	Yes	Always Discontinuous
Boost	Positive	No	Continuous*
Buck-Boost	Negative	No	Always Discontinuous

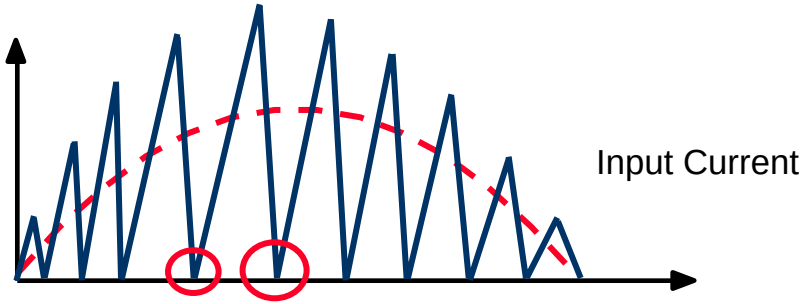
* Depending on load conditions and inductor selection

Operating Modes

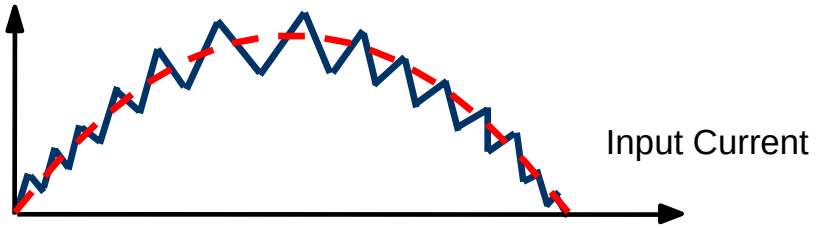
- **Discontinuous Conduction Mode**



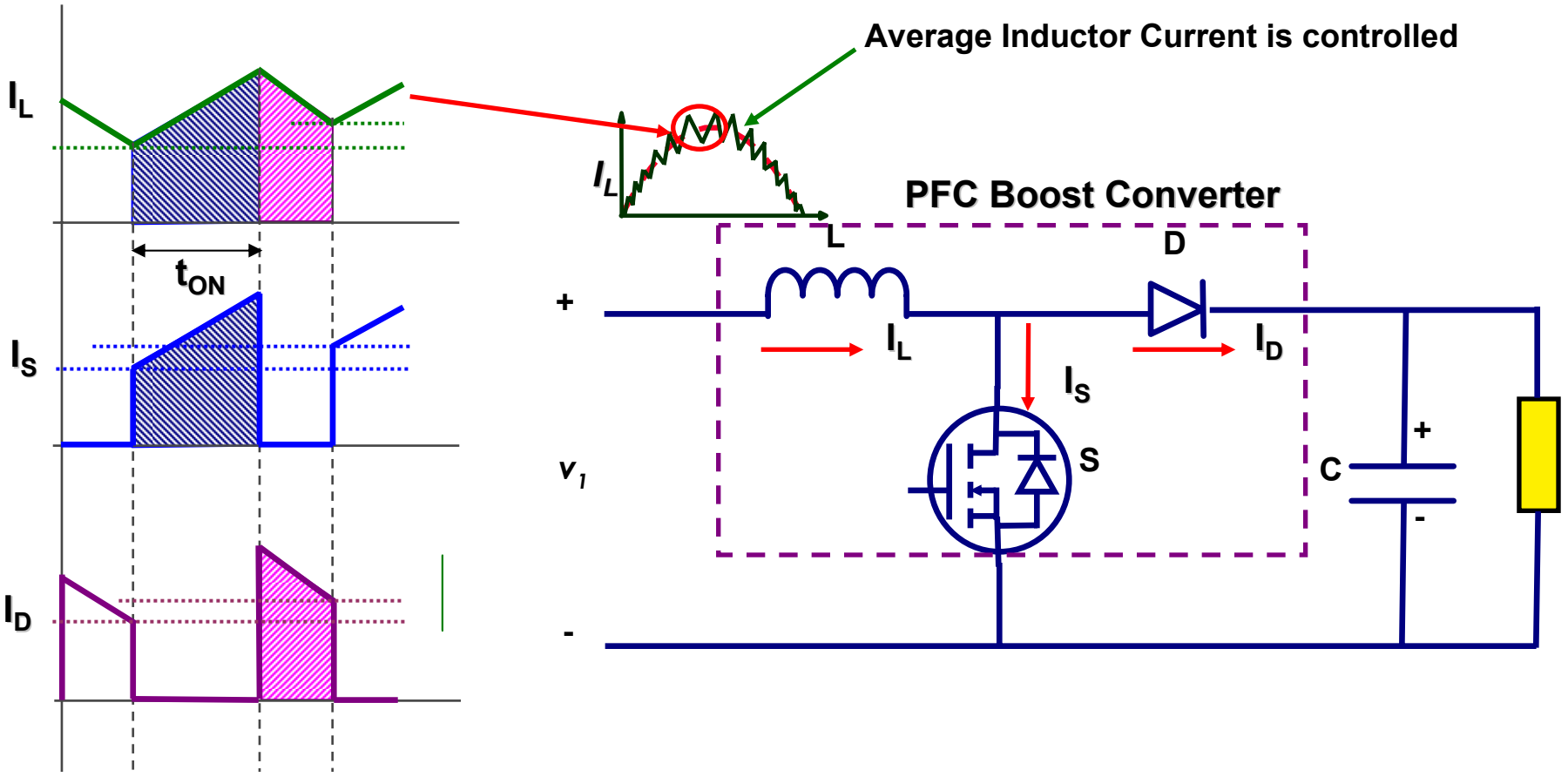
- **Critical Conduction Mode**



- **Continuous Conduction Mode**



Control Strategy



Average Current Mode Control

The average current through the inductor is made to follow the input voltage profile to improve Power Factor and minimize current harmonics

Digital vs. Analog Implementations

- Integration with other conversion applications
- On-the-fly change of operation mode
- Tuning of control loops without hardware change
- S/W migration for different power levels
- Monitoring of parameter limits and faults
- Implementation of multiple control loops
- Use left over MIPS & GPIO pins

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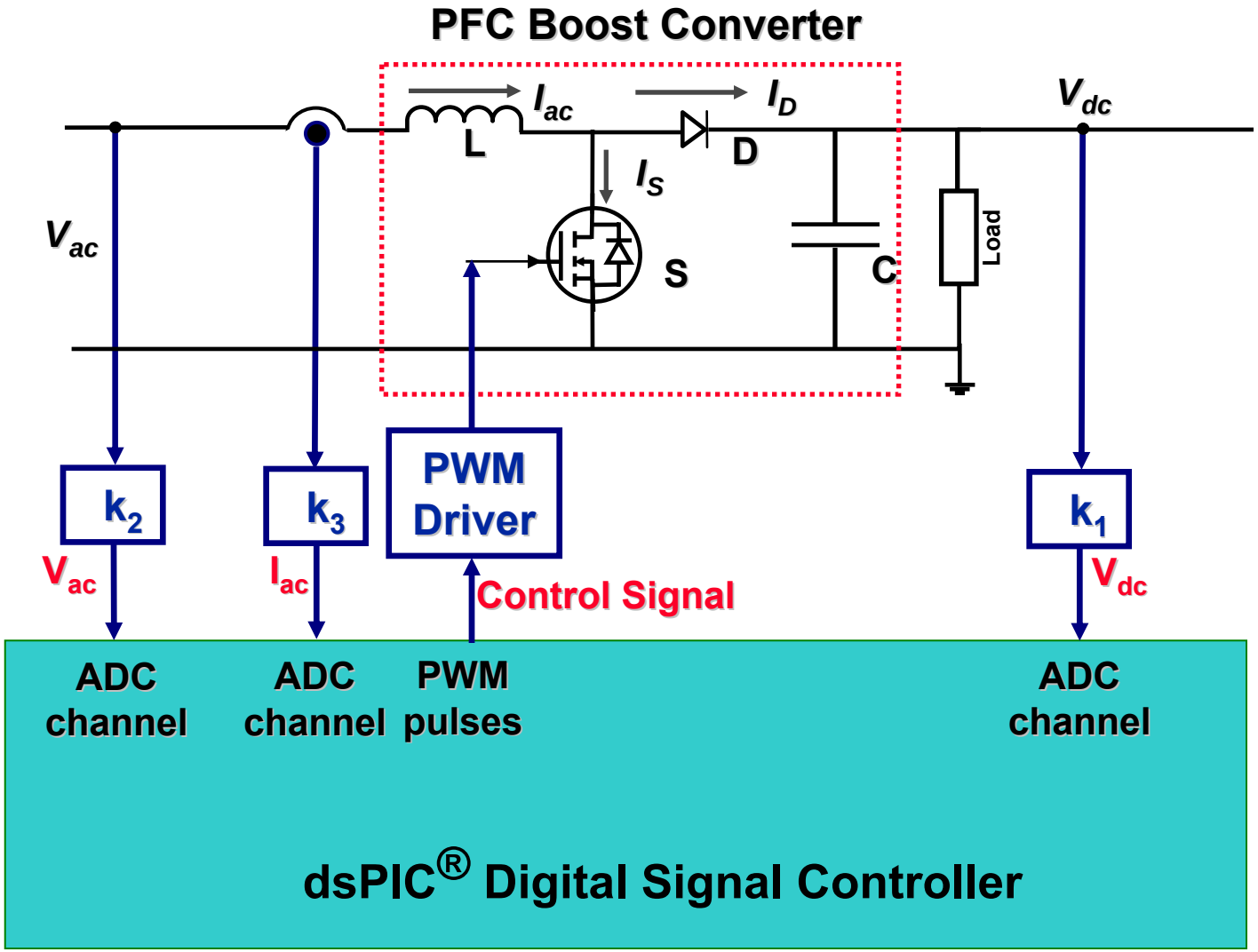
Design Parameters

Parameter	Symbol	Value
Output Power	P	400 watt
Input Voltage Range	V_{ACmin} and V_{ACmax}	85V, 264V
Input Frequency Range	f_{min} and f_{max}	40Hz, 66Hz
Output Voltage	V_{DC}	400V
Sampling Frequency	f_S	40kHz
Switching Frequency	f_{SW}	80kHz

Feedback and Control Signals



Using dsPIC® DSC for PFC

- **Peripherals and Resources Required:**
  - **ADC Module (10-bit)**
    - 3 Analog Channels
      - **V_{DC}, V_{AC} and I_{AC}**
  - **Output Compare Module**
    - 1 PWM Output
      - MOSFET Gate Pulses
  - **Timer Module**
    - 1 General Purpose Timer Output
      - Drives Output Compare Module and triggers ADC
  - **GPIO Ports**
    - Some I/O ports for diagnosis

Digital Representation of Variables

- Parameters and constants are represented in Q15 (1.15) format:

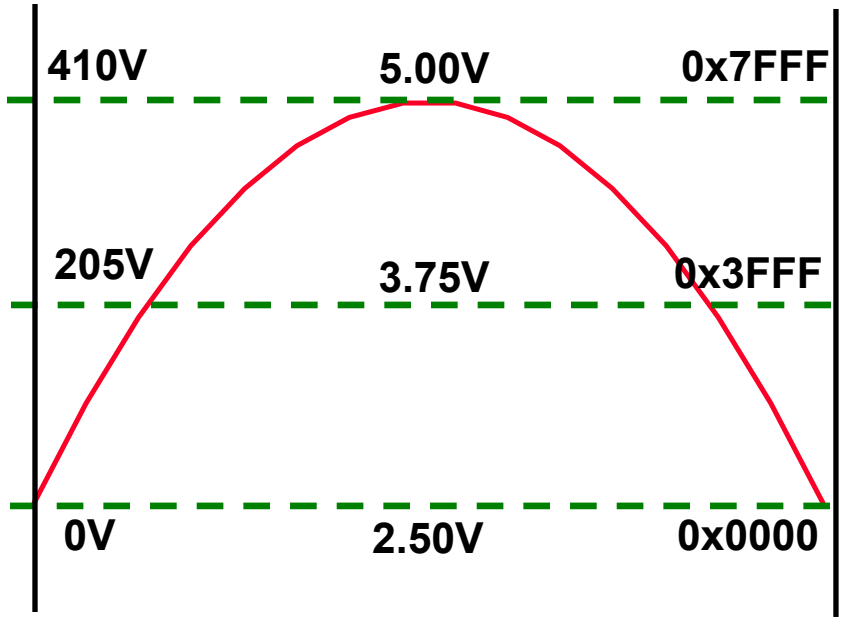
0x7FFF	32767	+ 0.999
0x0000	0	0.000
0x8000	-32768	- 1.000

- Scaling Constants are defined based on maximum conditions:

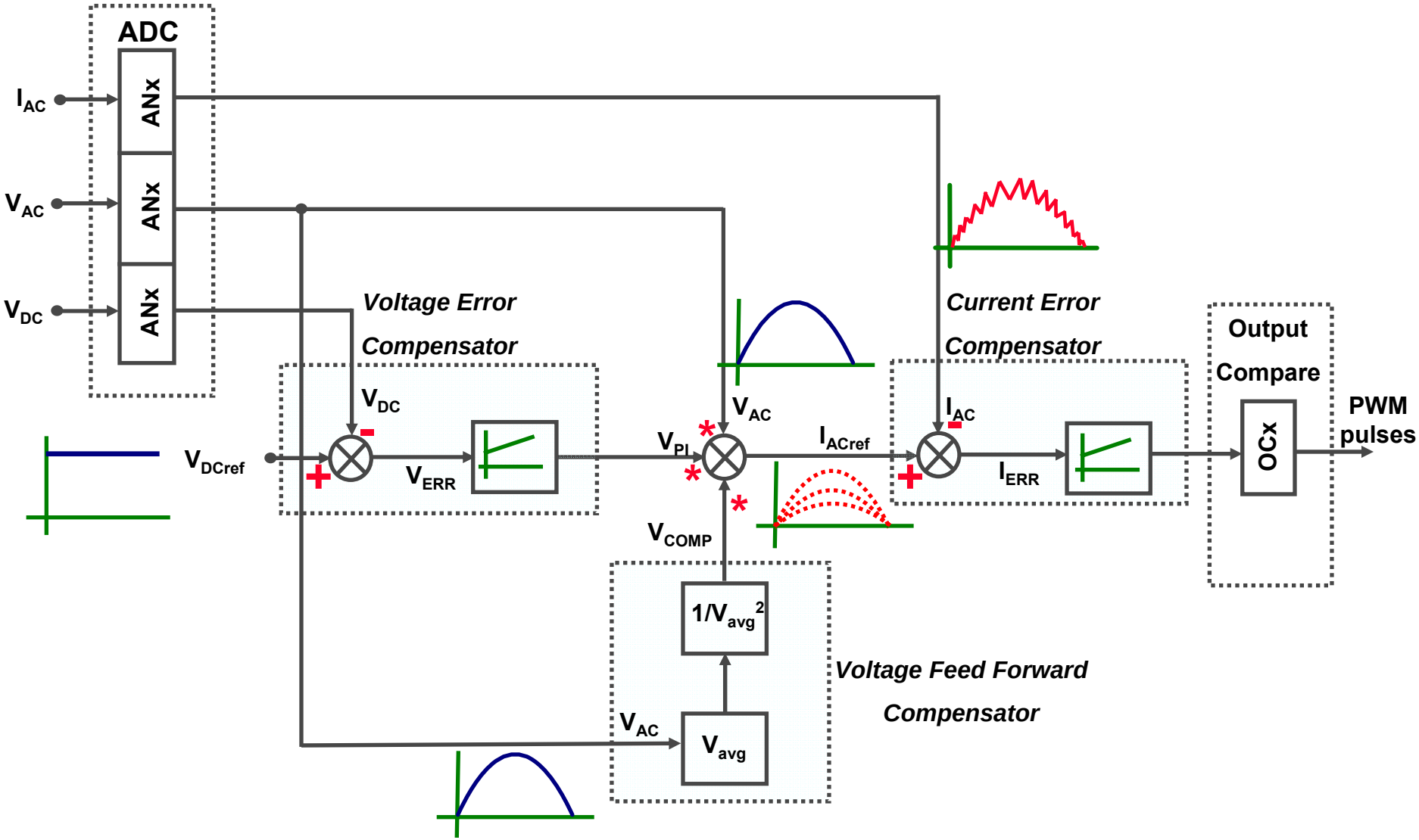
$$V_{DCmax(dig)} = V_{DCmax} * K_1 = 1$$

$$V_{ACmax(dig)} = V_{ACmax} * K_2 = 1$$

$$I_{ACmax(dig)} = I_{ACmax} * K_3 = 1$$



Digital Implementation



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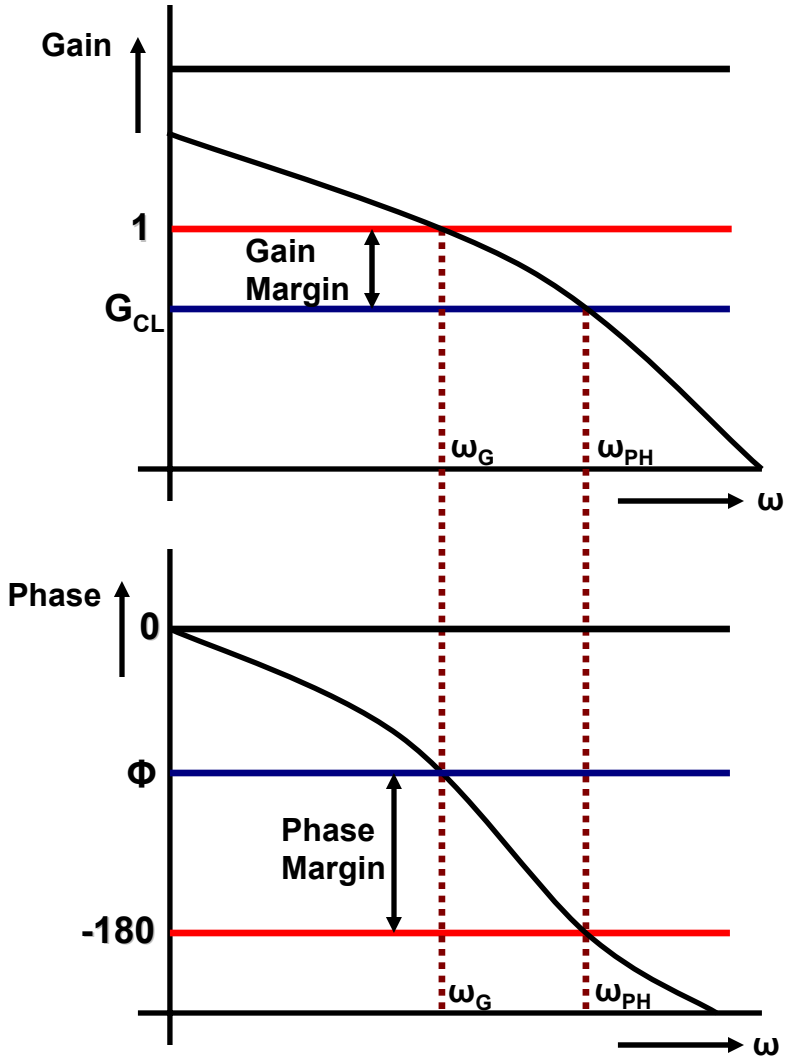
Compensators

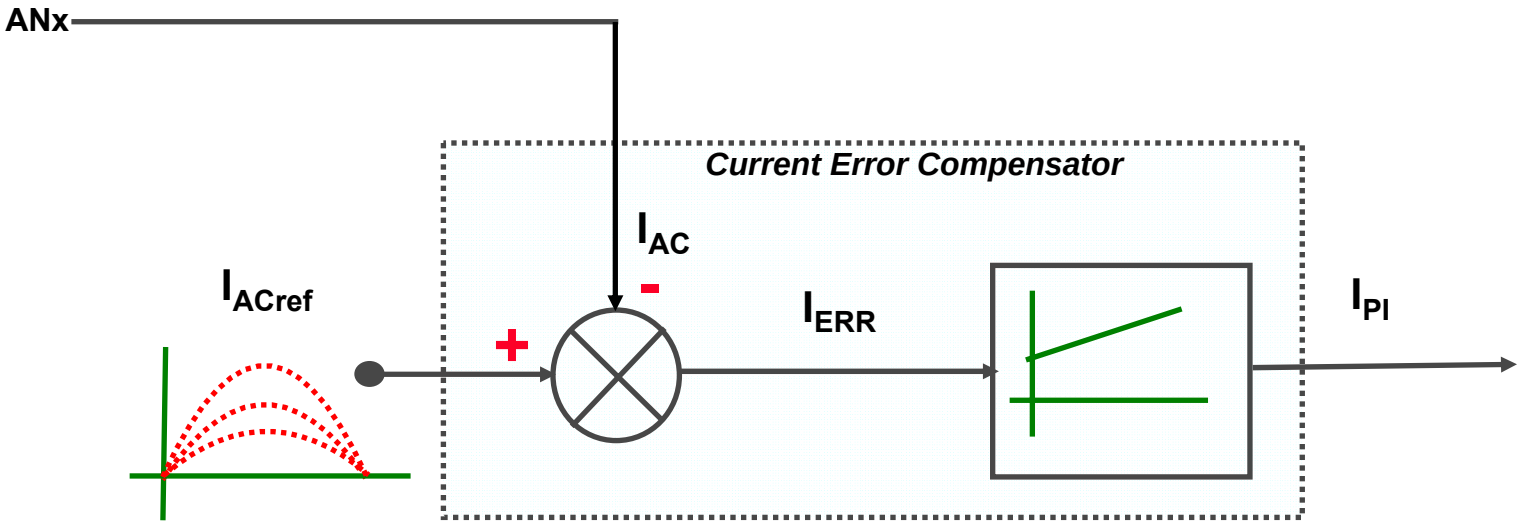
- **Current Loop Design**
  - Force the current to track the current reference signal
  - Wave shape same as the input voltage
  - Current Loop Bandwidth
    - Usually between 2 kHz to 10 kHz
    - To track a semi sinusoidal wave of 100 Hz or 120 Hz
- **Voltage Loop Design**
  - To maintain a constant DC output voltage
  - Voltage Loop Bandwidth
    - Usually 10 Hz to 20 Hz (well below the input frequency)
    - To remove the second harmonic ripple on DC bus
- **Voltage Feed Forward Design**
  - To maintain output power as determined by the load
  - Takes input voltage variations into consideration

Gain and Phase Margins

- **Gain Margin**
  - Amount of increase in gain to make the gain unity at phase cross over frequency
  - For stability, Gain Margin > 1
- **Phase Margin**
  - Amount of increase in phase to make the phase -180º at gain cross over frequency
  - For stability, Phase margin > 0
- **Rule of Thumb for a good design**
  - 1.7 <= Gain Margin <= 2.0
  - 30º <= Phase Margin <= 45º



Current Error Compensator Design



Current Loop Bandwidth : 8 kHz
Current Loop Phase Cross-Over Frequency : 8 kHz
Current Loop PI Compensator zero placement : 800 Hz

Current Loop Transfer Function

Small Signal High Frequency Model:

Open Loop Transfer Function : $G_{OL} = \partial I_{AC}/\partial D = V_{DC}/sL$

Closed Loop Transfer Function : $G_{CL} = G_{OL}.G_{COMP}.k_3$

Compensator Gain :

$$|G_{COMP}| = (2.\ \pi.\ f_{PH}\ .\ L)/(V_{DC}.k_3) = I_{PI}/I_{ERR}$$

Current Loop Compensation

Compensator Gain :

$$|G_{COMP}| = (2.\ \pi.\ f_{PH}\ .\ L) / (V_{DC}.k_3)$$

$$G_{COMP}(s) = G_{COMP}.(1+T_z.s) / T_z.s = k_P + k_I / s$$

where,

$T_z = 1 / (2.\ \pi.\ f_z)$

$f_z = 800$ Hz

Digital Implementation of PI Controller :

In Analog Domain,

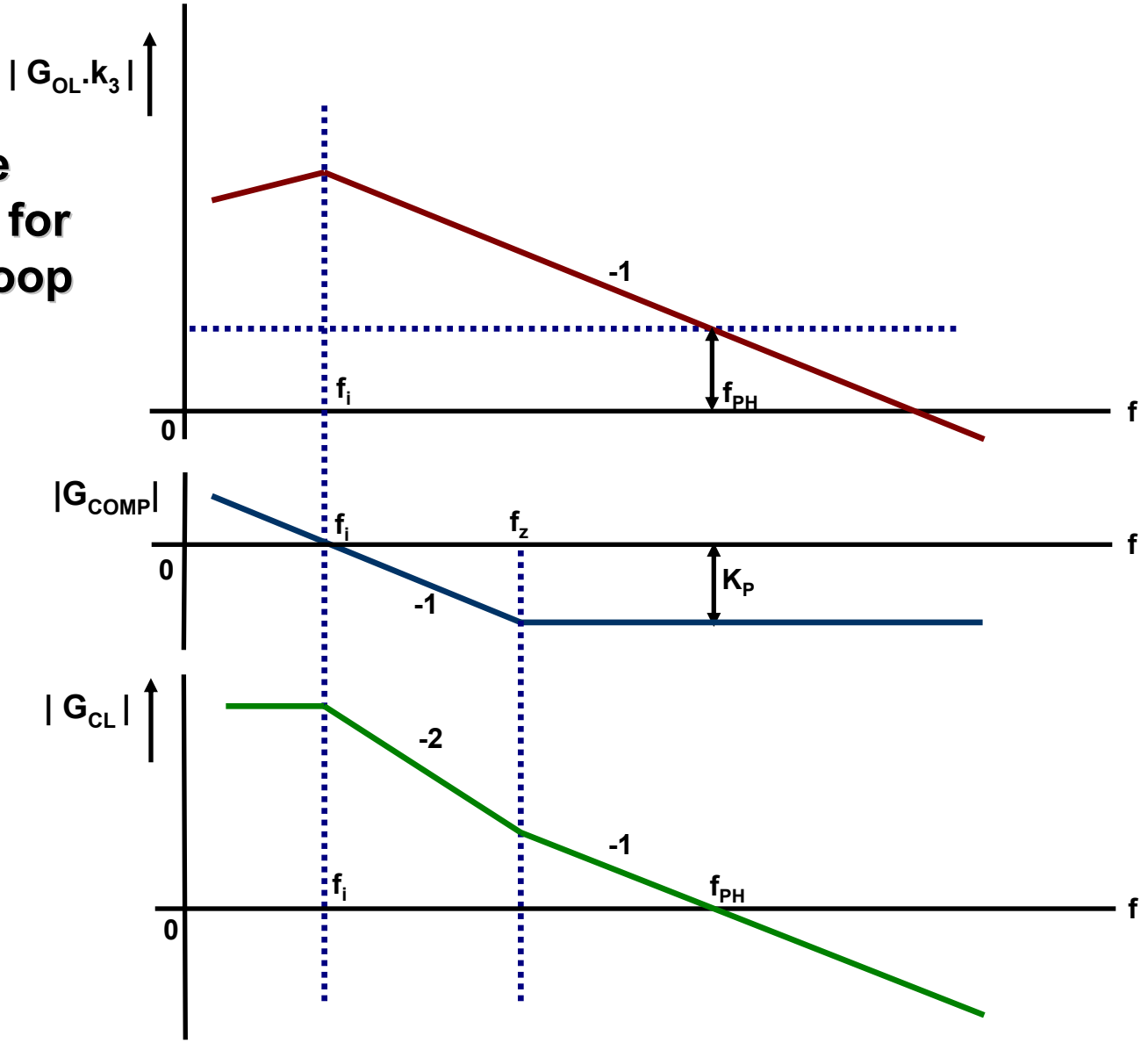
$$I_{PI}(t) = P_{(t)} + I_{(t)} = k_P.\ I_{ERR}(t) + k_I.\ \int I_{ERR}(t)\ .\ dt$$

In Digital Domain,

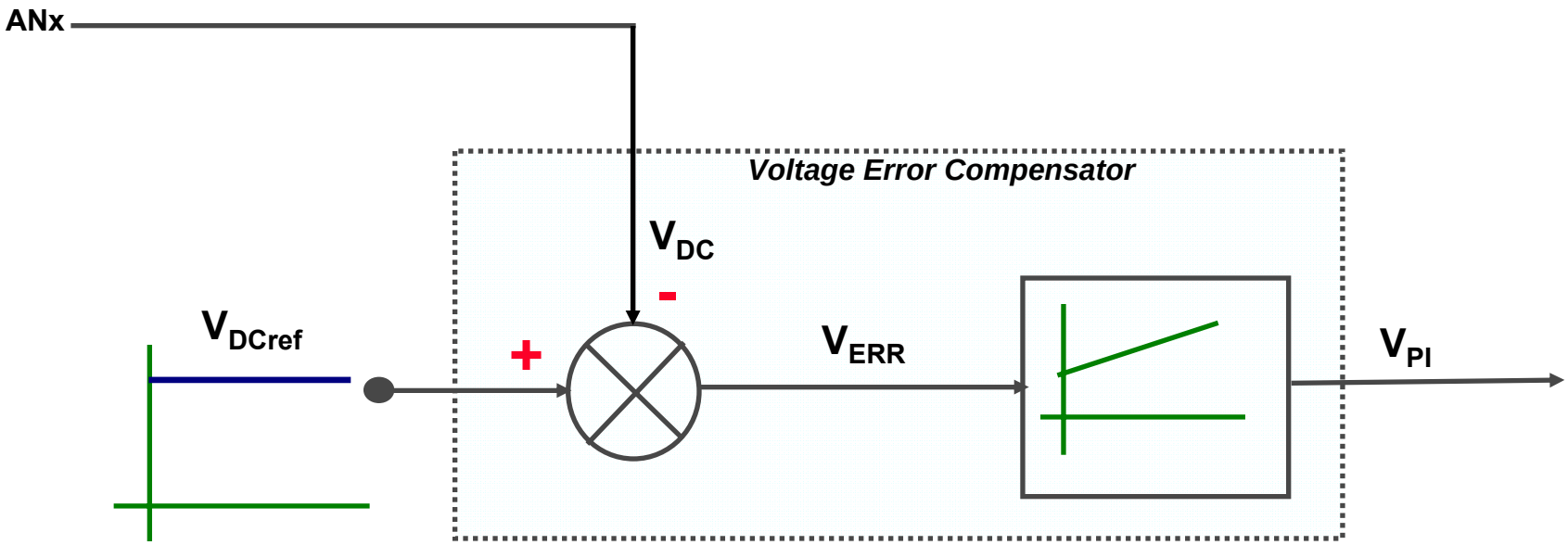
$$I_{PI(n)} = P_{(n)} + I_{(n)} = k_P.\ I_{ERR(n)} + \{\ I_{(n-1)} + k_I.\ T_s.\ I_{ERR(n)}\ \}$$

Current Loop Bode Plots

Magnitude Bode Plot for Current Loop



Voltage Error Compensator Design



Voltage Loop Bandwidth : 10 Hz
Voltage Loop Phase Cross-Over Frequency : 10 Hz
Voltage Loop PI Compensator zero placement : 10 Hz

Voltage Loop Transfer Function

Small Signal Low Frequency Model:

Open Loop Transfer Function : $G_{OL} = \partial V_{DC}/\partial V_{PI} = G_1/sC$

Closed Loop Transfer Function : $G_{CL} = G_{OL}. G_{COMP}. k_1. k_m$

Compensator Gain :

$|G_{COMP}| = V_{PI}/V_{ERR}$

$|G_{COMP}| = (2. k_2. k_3 . V_{DC}. V_{ACmax}^2)/(k_1.k_m. Z . V_{ACmin}^2)$

Voltage Loop Compensation

Compensator Gain :

$$|G_{COMP}| = (2.\ k_2.\ k_3\ .\ V_{DC}.\ V_{ACmax}^2) / (k_1.k_m.\ Z\ .\ V_{ACmin}^2)$$

$$G_{COMP}(s) = G_{COMP}.(1+T_z.s) / T_z.s = k_P + k_I / s$$

where,

$T_z = 1 / (2.\ \pi.\ f_z)$
$f_z = 10$ Hz

Digital Implementation of PI Controller :

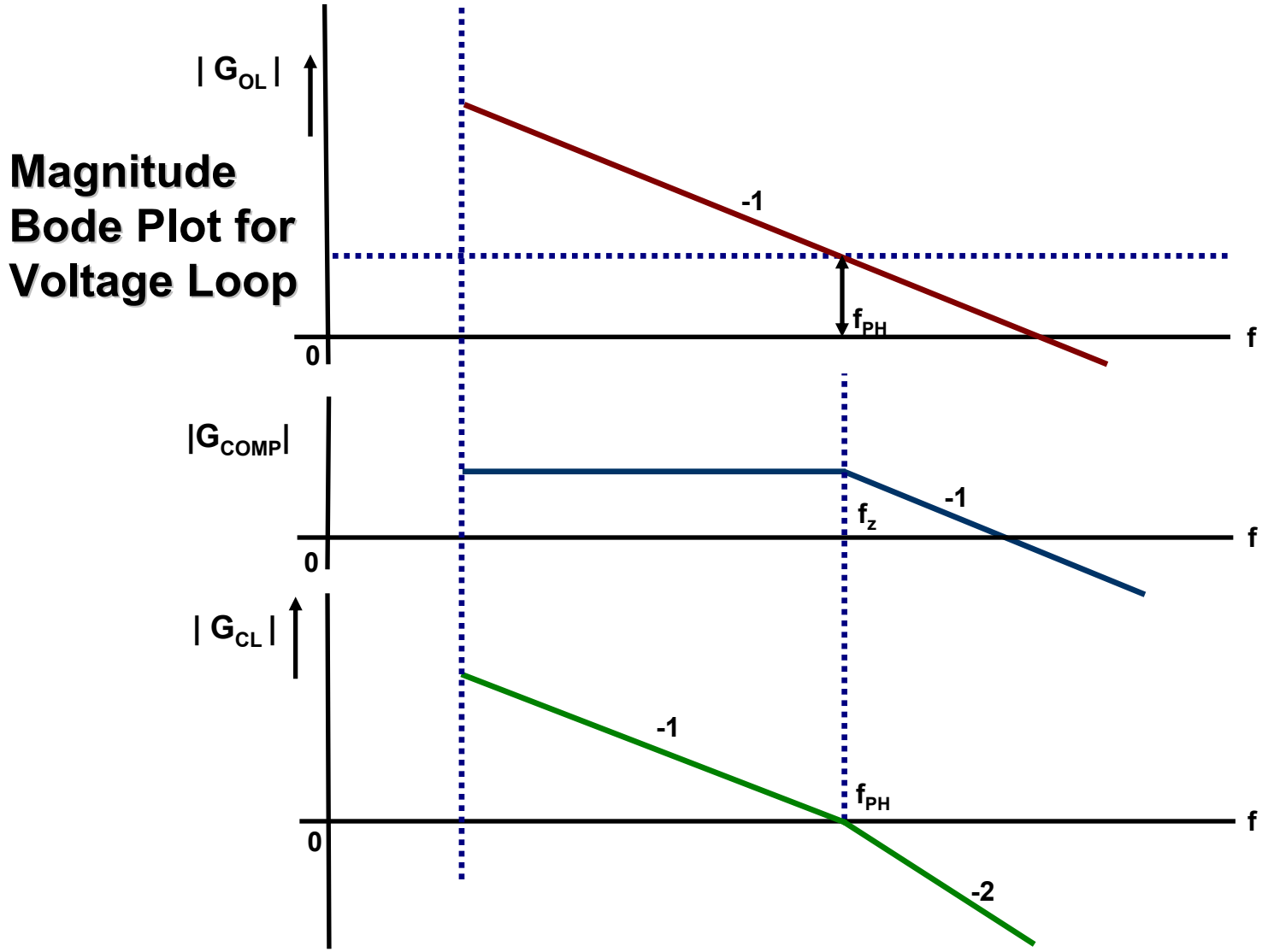
In Analog Domain,

$$V_{PI}(t) = P_{(t)} + I_{(t)} = k_P.\ V_{ERR}(t) + k_I.\ \int V_{ERR}(t)\ .\ dt$$

In Digital Domain,

$$V_{PI(n)} = P_{(n)} + I_{(n)} = k_P.\ V_{ERR(n)} + \{\ I_{(n-1)} + k_I.\ T_s.\ V_{ERR(n)}\ \}$$

Voltage Loop Bode Plots



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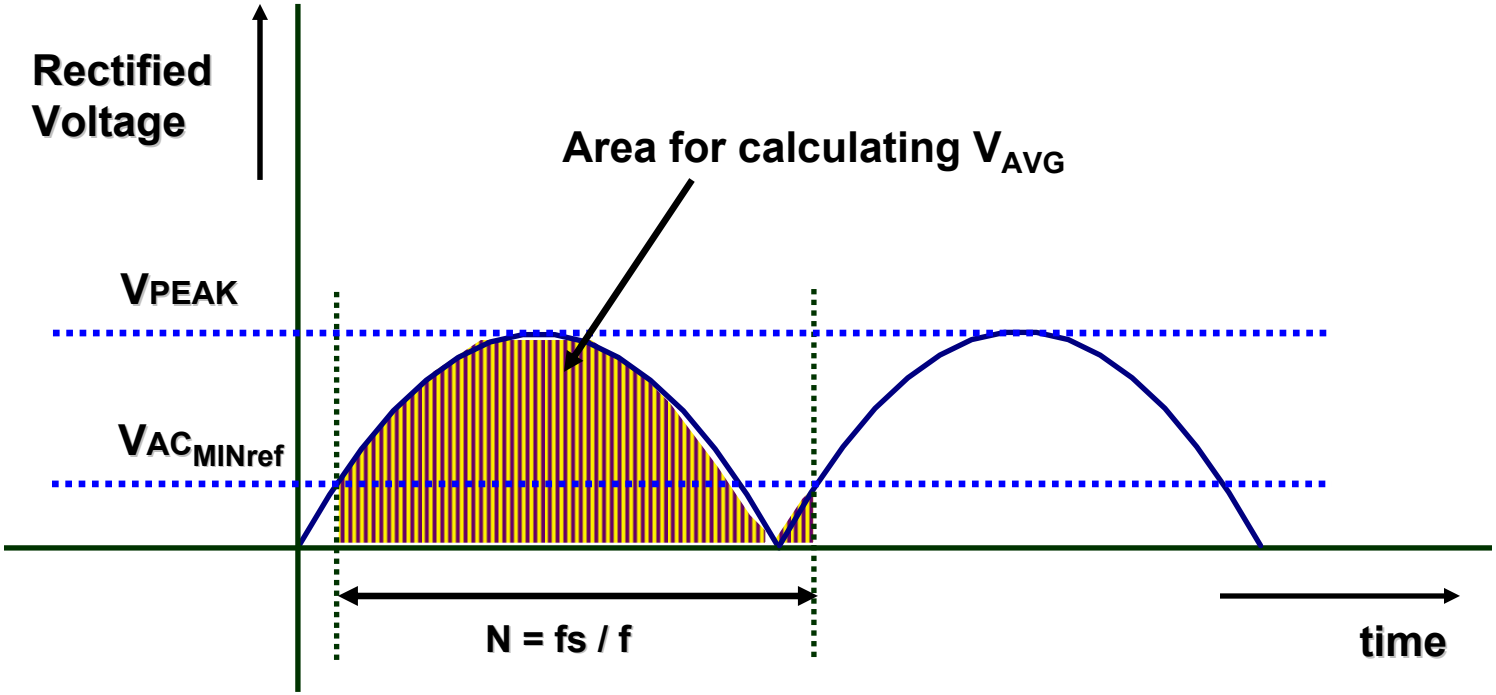
Average Voltage Computation

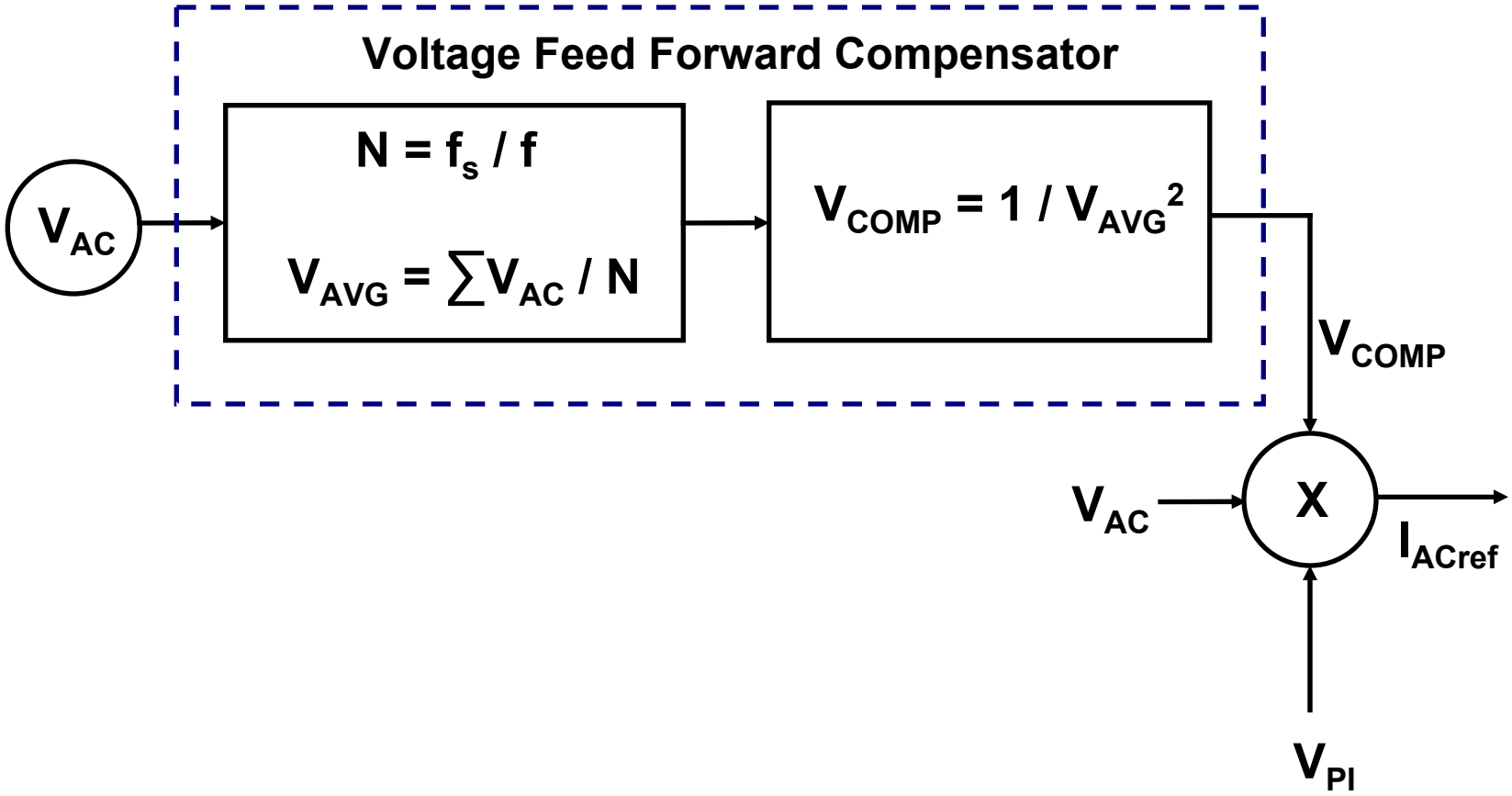


Average Voltage : $V_{AVG} = \sum V_{AC} / N$

Frequency Counts : $N = f_s / f$

where,
fs : Sampling Frequency
f : Twice the Input Frequency

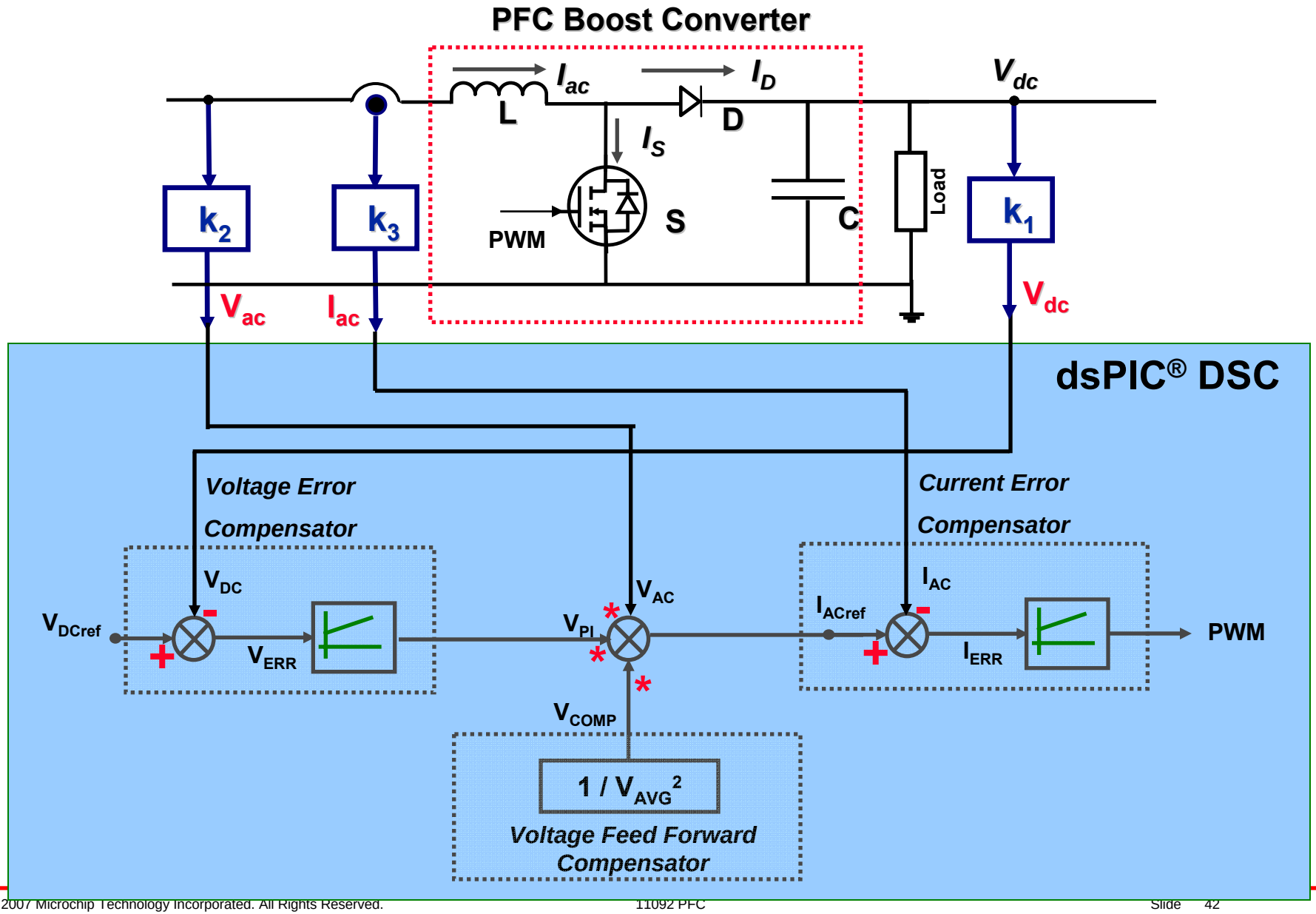
Voltage Feed Forward Compensation



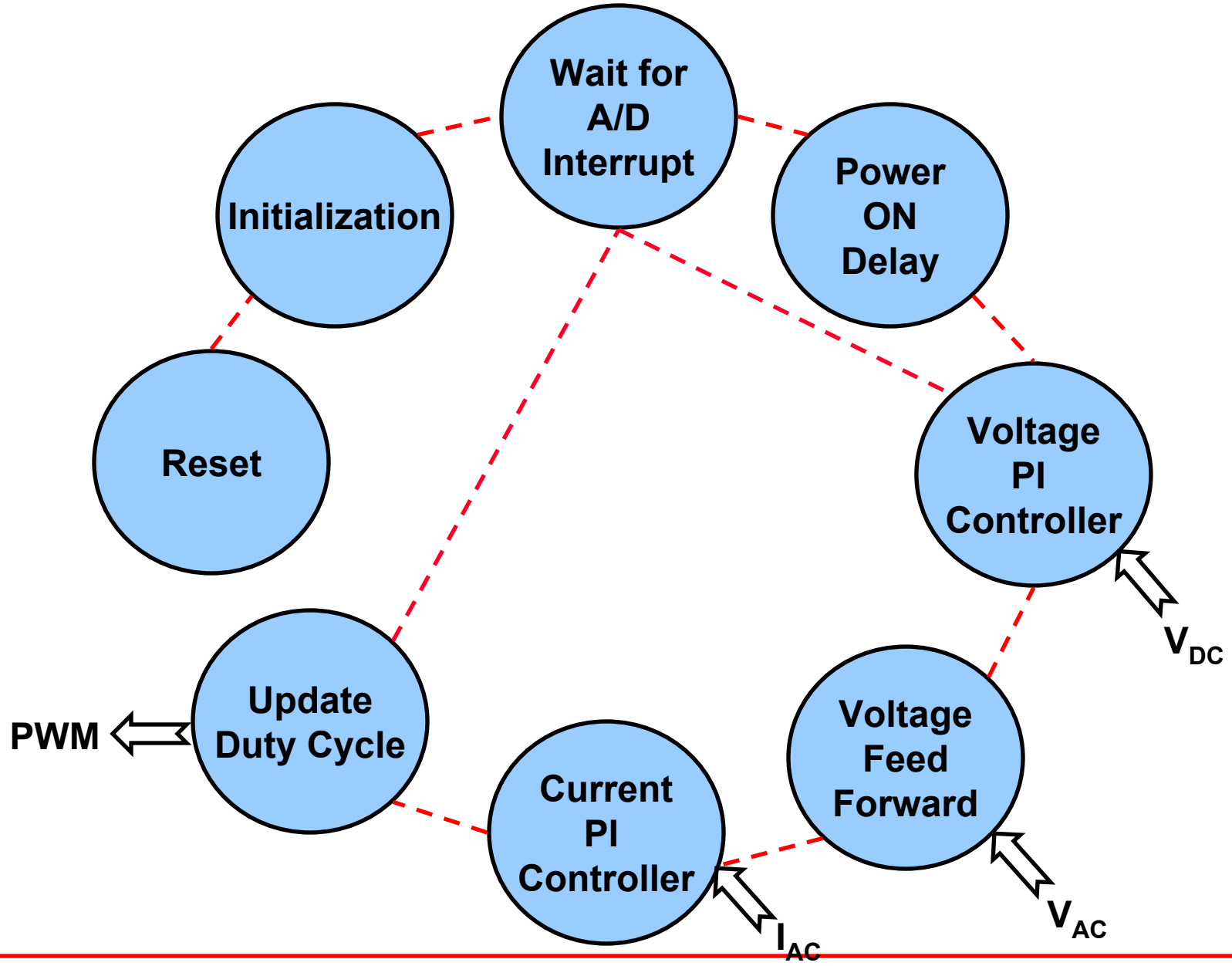
To maintain output power as demanded by the load

To take input voltage variations into consideration

Complete PFC Integration



PFC Decoded



Summary

- **Basics of PFC hardware**
  - Basic components and boost converter topology
- **How is the PFC digital control loop implemented on the dsPIC® DSC device?**
  - Representation of variables in digital domain
  - Digital Implementation of PI Controller
- **Design of voltage, current and feed forward control loops**
  - Decide Compensator parameters
  - Determine the closed loop transfer functions

Development Tools and Resources for this Class

- **Power Module**
  - dsPICDEM™ MC1H 3-Phase High Voltage Power Module
  - User's Guide for the Power Module
- **Development Boards**
  - dsPICDEM™ MC1 Motor Control Development Board
  - User's Guide for the Demo Board
- **Development Tools**
  - MPLAB® ICD 2 In-Circuit Debugger **OR**
  - MPLAB REAL ICE™ In-Circuit Emulator
- **Digital PFC Application Note**
  - To be released

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Thank You

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