11064 DFN

Designing for Noise in Embedded Systems

Class Objective

When you complete this class you will be able to:

- **Identify noise sources and understand their impact on Analog + MCU signal chains**
- **Develop noise budgets for a desired analog resolution, determining which noise source needs the highest attention**
- **Apply system design principals to reduce noise and its effects in your application**

Formulas & Constants

- **dx/dt or Δx/Δt**
  - Instantaneous rate of change of x relative to t
  - Δx/Δt is used interchangeably with dx/dt in this class
- **q = C v**
  - The charge (q) on a capacitor (C) is proportional to the voltage (V) across it
- **I = C dv/dt**
  - The current (i) flowing through a capacitor (C) is proportional to the rate of change of voltage (v) across the capacitor
- **V = L di/dt**
  - The voltage (v) across an inductor (L) is proportional to the rate of change of current (i) through the inductor
- **Capacitance of 1 cm² copper foil, 0.02” (0.5 mm) above GND plane:**
  - $\varepsilon_o \times \varepsilon_r \times$ Area/Distance = 0.9e-11F/m * 5 * $(0.01\text{m})^2$/0.0005m = 9 pF
  - If shielded between 2 GND planes: will provide 18 pF
- **Model of 2 mm of wire: narrow PCB trace or IC lead frame has 1 nH of inductance**

Agenda

Section 1:

- Understanding magnitudes of noise
  - Environment of an embedded system
  - Sources of Noise
  - E-Field Coupling
  - Measuring E-Field noise (lab exercises)
  - H-Field Coupling
  - Measuring H-Field noise (lab exercises)
  - Digital Noise and Power Supply Noise
  - Measuring Power Supply noise (lab exercises)

[15 minute Break]

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Agenda

Section 2:

- **Develop budgets for a desired analog resolution**
  - Building budgets
  - How to combine noise sources in budgets

Section 3:

- **Reducing noise and its effects**
  - Minimizing the impact of the major noise sources
  - PCB floor planning and layout, circuits and shielding

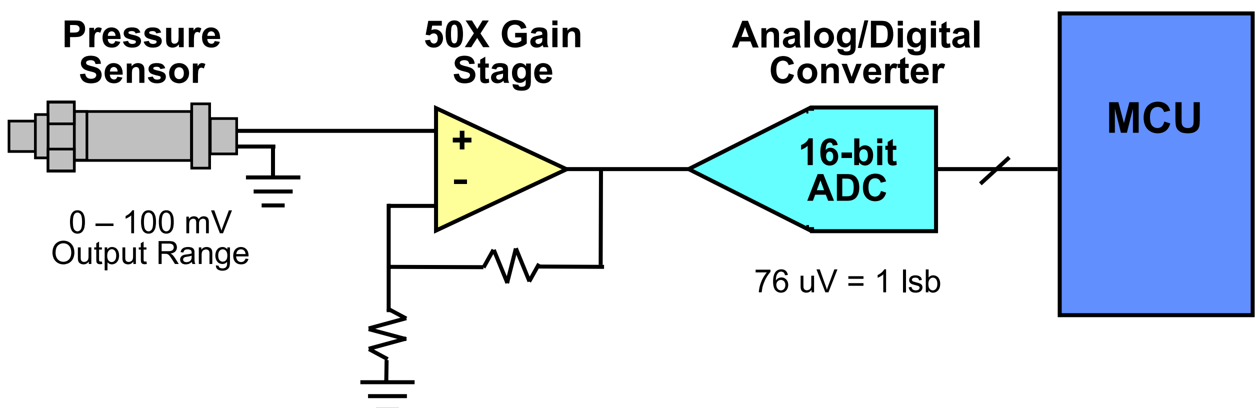
SECTION 1:
Understanding magnitudes of noise in Analog + MCU signal chains

Environment

- **WHAT IS NOISE?**
  - **Any undesired change in the analog or digital signal**
- **WHERE DOES NOISE COME FROM?**
  - **Digital Interface periodic noise**
  - **V_{DD} noise (random/periodic)**
  - **Magnetic coupling (H-field)**
  - **Capacitive coupling (E-field)**
  - **Vibration in ceramic caps and coaxial cables**
  - **I*R Ohms Law in PCB foil**
  - **Thermal change & gradients**
  - **Return currents through sensors**

How much noise is too much?

- Noise can be amplified by gain circuits in the application



How much noise is too much?

- **Analog Resolution: V_{PP} per lsb**
  - **The volts/lsb (least significant bit), or volts/quanta, of an ADC in an application indicate the magnitude of noise that can be tolerated in the system**

Desired Analog Resolution (bits)	Codes (# lsb's)	VPP per LSB	
		5V	3.3V
8	256	19,500 uV	12,900 uV
10	1,024	4,900 uV	3,200 uV
12	4,096	1,200 uV	806 uV
14	16,384	305 uV	201 uV
16	65,536	76 uV	50 uV
18	262,144	19 uV	13 uV
20	1,048,576	4.8 uV	3.2 uV
22	4,194,304	1.2 uV	0.8 uV
24	16,777,216	0.3 uV	0.2 uV

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Major Noise Sources

Source of Noise	Noise amplitude (worst case)[1] $V_{Peak\text{-}to\text{-}Peak}$
Digital Interfaces	160,000 uV
VDD noise	100,000 uV
Magnetic Field (8"), Appliance motor/controller	60,000 uV
Magnetic Field (2"), Switching Power Supply	50,000 uV
Magnetic Field (2"), MCU Clock 50-Ohm line	25,000 uV
Electric field of MCU (1")	1,700 uV
Vibration of Coax Cables	2,000 uV
Fluorescent Light at 1 foot	625 uV
Vibration/PCB stress on Ceramic Capacitors	500 uV
Thermal Gradients across solder joints	200 uV
Dielectric Absorption of Capacitors	200 uV
Current Spreading in PCB Copper Foil	150 uV

[1] The test conditions in which these measurements were taken are indicated in Appendix

Examine E-Field Coupling (electric/capacitive) and How To Predict

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Behavior of Coupled Charge

- **In physics, the space surrounding an electric charge has a property called an electric field**
- **The SI unit for electric charge is the Coulomb**
- **The Coulomb is defined as the quantity of charge that has passed through the cross-section of an electrical conductor in 1 second at 1 ampere**
  - 1 Ampere = 1 Coulomb/second
  - This represents the combined charge of approximately 6.24×10^{18} electrons or protons
- **The electric field exerts a force on other charge objects**
- **Coulomb's law is an inverse-square law, indicating the magnitude and direction of electrostatic force that one electrically charged object exerts on another.**

Michael Faraday, 1791-1867

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Behavior of Coupled Charge

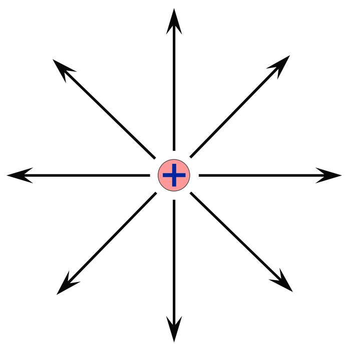
- **The magnitude of the force can be expressed as:**

  $F = (k_c\ q_1\ q_2)/r^2$, where

  - k_c = Coulomb Force Constant = $1/(4\pi\varepsilon_0)$ = 8.988×10^9 N m^2/C^2
  - q_1 = Charge on one body
  - q_2 = Charge on the other body
  - r = Distance between the two bodies
- **The magnitude of the Electrical Field (E) created by a single point charge (q) can then be expressed as:**

  $E = (1\ q)/(4\pi\varepsilon_0 r^2)$

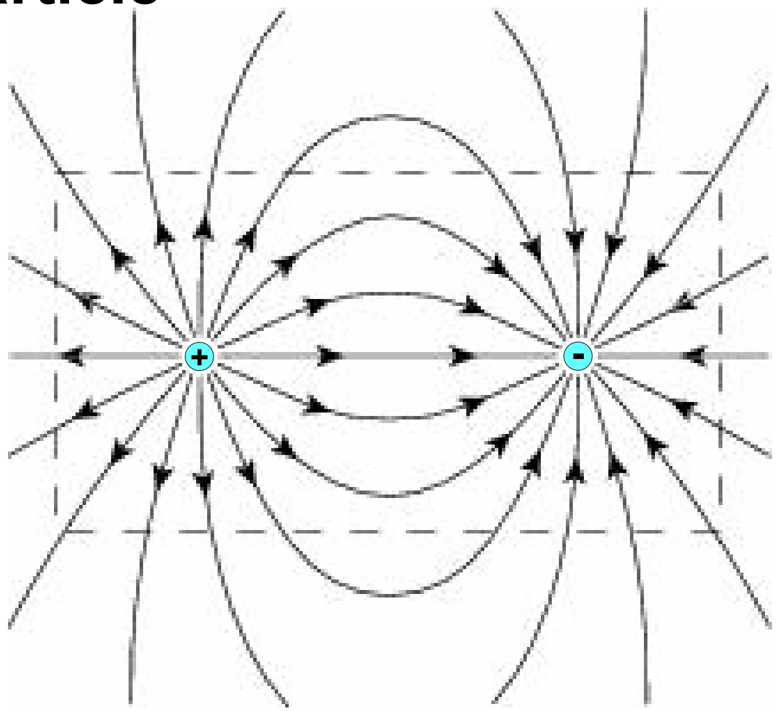
  - Units are volts/meter (V/m) or newtons/coulomb (N/C)



- For a positive charge q, the direction of E points along lines directed radially away from the location of the point charge.

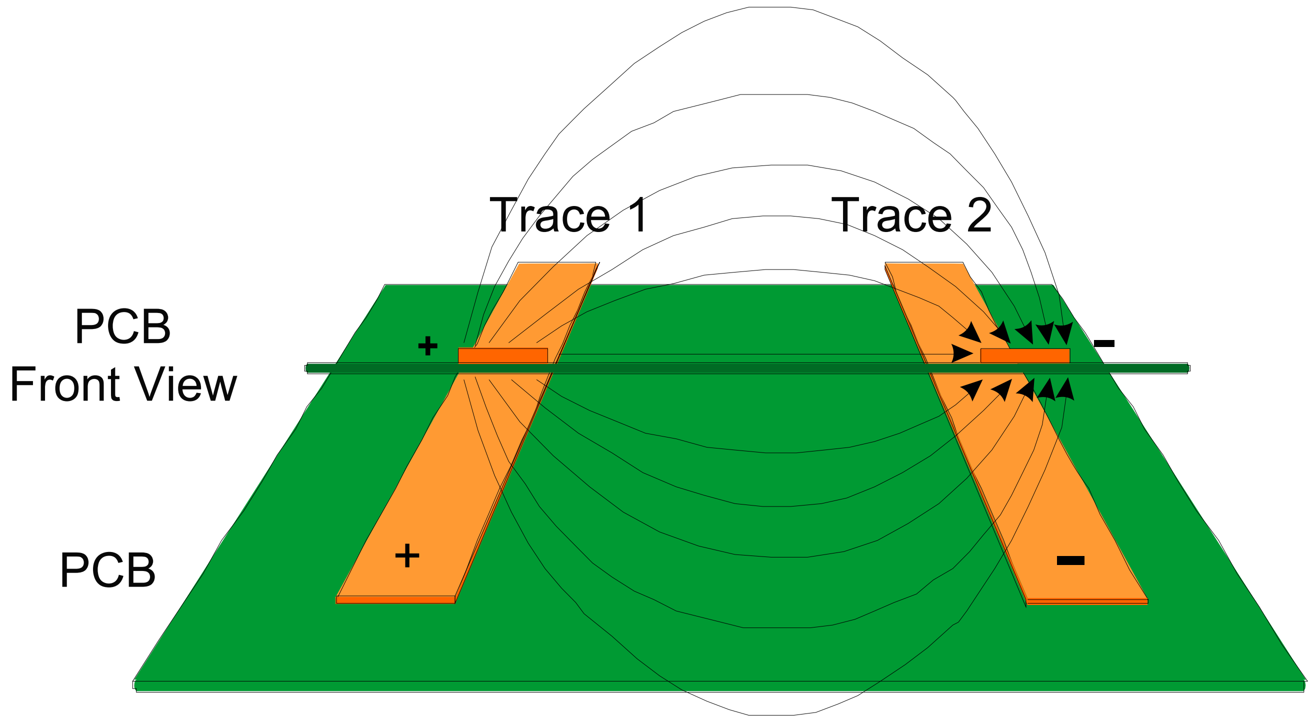
Behavior of Coupled Charge

- Electrical field, shown as electrical lines of force (flux), of two particles in space
- Note that the flux lines emanate from the positively charged particle to the negatively charged particle



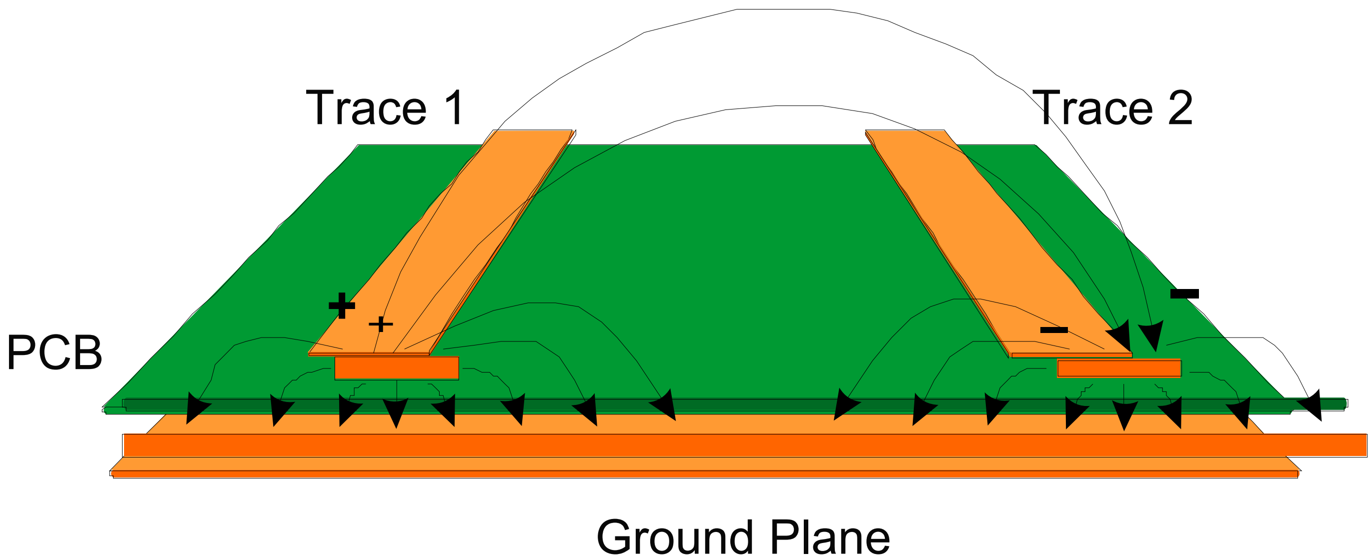
Behavior of Coupled Charge

- **The E-field occurs on both the top and bottom of the PCB**



Behavior of Coupled Charge

- **E-field between two traces with second layer ground plane**



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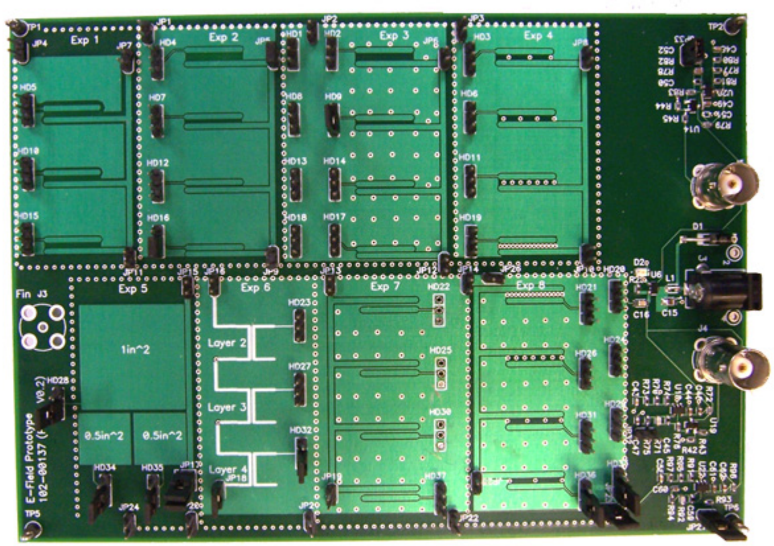
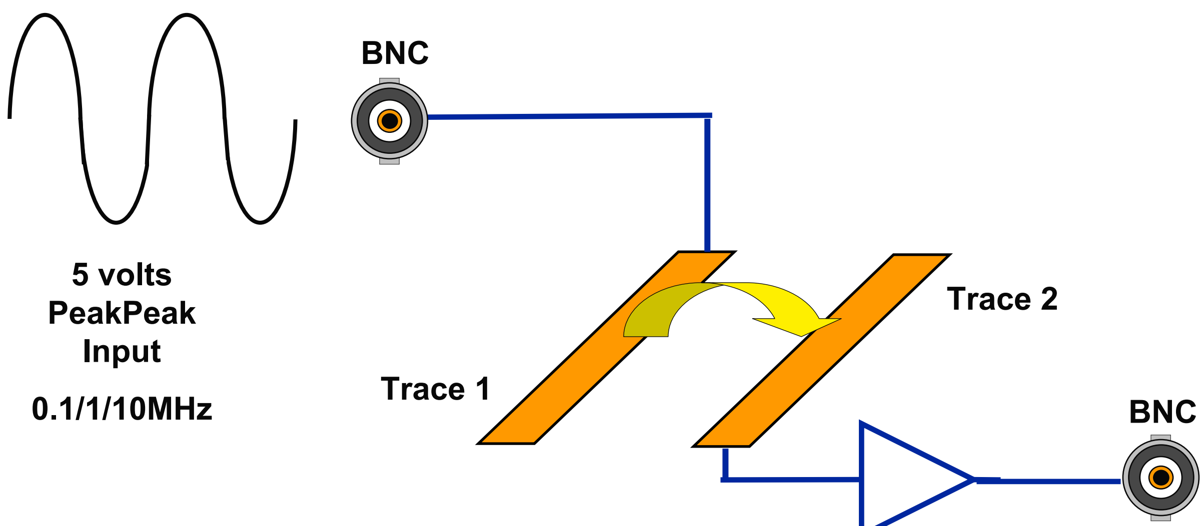
E-Field Coupling
Lab Exercises

- **This set of lab exercises will explore and quantify the effects of E-fields**
- **The E-Field Eval Board (104-00137) is designed to demonstrate E-field coupling under various conditions on a Printed Circuit Board (PCB)**
- **These experiments will help system designers understand the impact PCB layout techniques have on controlling E-field noise in their design**



E-Field Coupling
Lab Exercises

- **All 8 Experiments look at E-Field Noise Coupling from one trace to another trace on a PCB under various conditions**



5 volts
PeakPeak
Input

0.1/1/10MHz

1:1 gain up to 10MHz, or
10:1 Gain up to 1MHz
Jumper-selected Exp1-7

Gain of 10:1 built into Exp8

Rin~0.5MegOhm

?

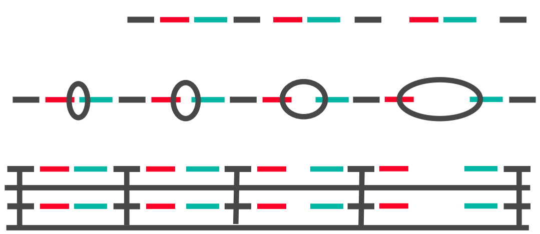
Hint

4mV to 115mv

!! Use ACcoupled !!

E-Field Board (104-00137) Lab Exercises

- Lab Results/Discussion



EXP8—like 3, but fixed spacing, variable #Vias

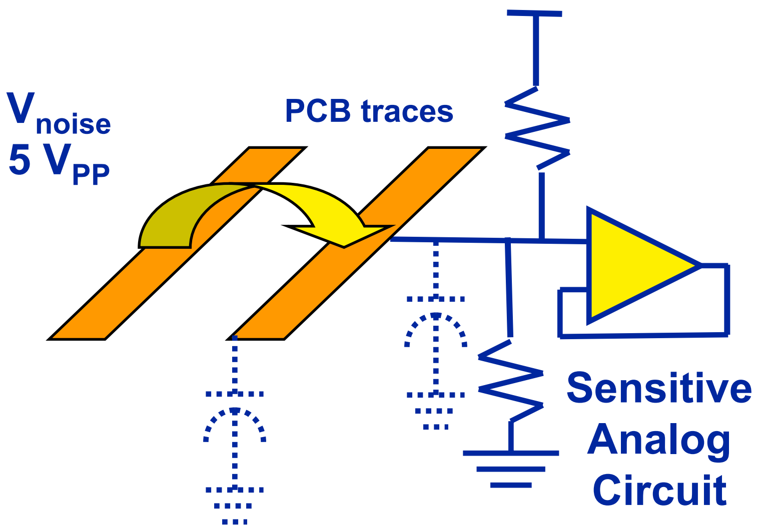
Experiment	Magnitude @ 100 kHz (mV)	Magnitude @ 1 MHz (mV)	Magnitude @ 10 MHz (mV)
1/1	56.20	62.50	54.60
1/2	64.00	73.40	64.00
1/3	67.10	78.00	67.10
2/1	115.00	132.00	114.00
2/2	95.30	109.00	95.30
2/3	68.70	78.10	67.10
2/4	45.30	50.00	43.70
3/1	48.40	53.40	43.40
3/2	25.00	26.80	21.80
3/3	11.50	12.50	10.30
3/4	6.56	7.50	6.25
3/5	50.00	57.10	46.50
3/6	27.10	30.90	25.00
3/7	9.06	10.30	8.43
3/8	4.37	4.68	4.06
8/1	150.00	99.30	9.68
8/2	137.00	88.10	8.59
8/3	128.00	84.30	8.28
8/4	135.00	87.50	8.59
8/5	92.10	61.20	6.25
8/6	81.20	53.10	5.62

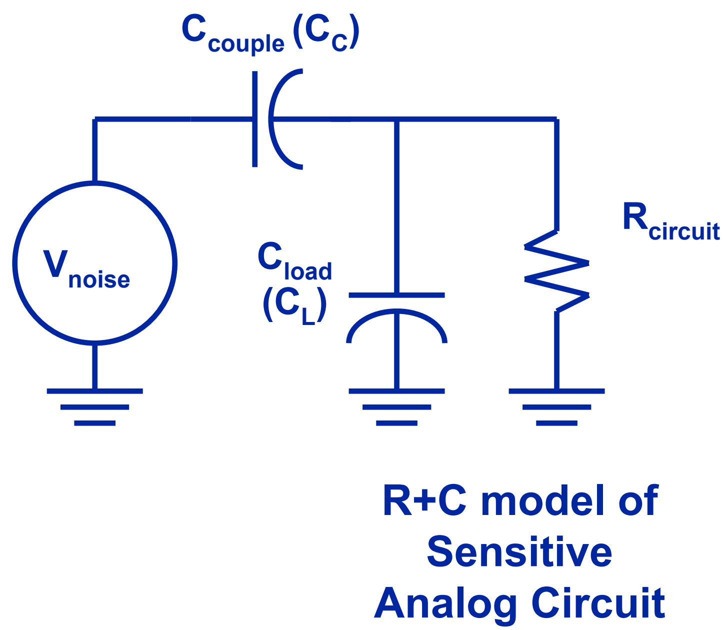
- What did we learn?
  - Spacing of traces matter!
  - Ground planes matter!
  - Frequency doesn't always matter

How to get smaller Voltages?
Reduce the resistance.

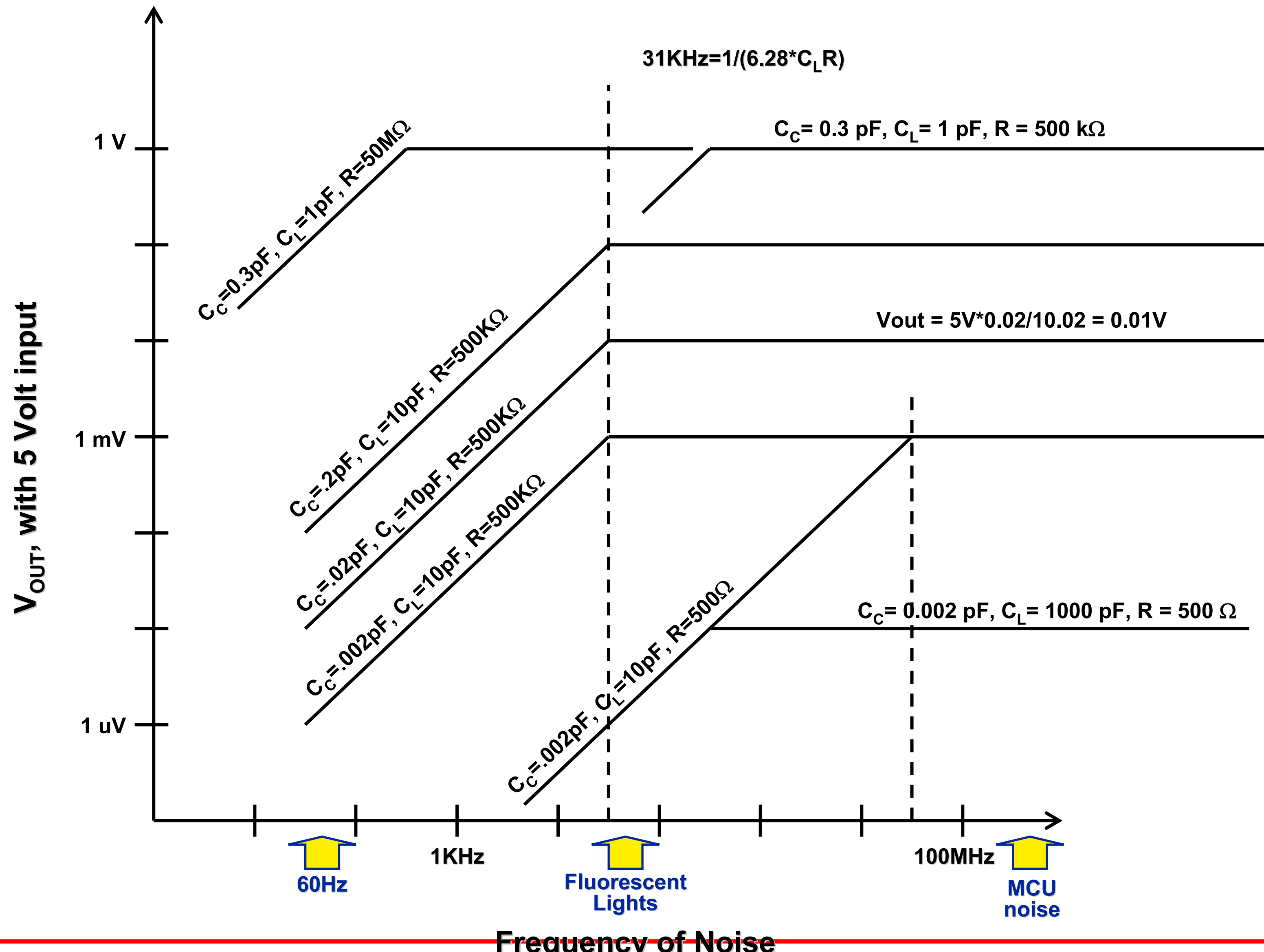
Behavior of Coupled Charge

- **Model as capacitive divider**
  - Like a scope probe but no DC path
- **Three variables: C_{couple}, C_{load}, $R_{circuit}$**





Behavior of Coupled Charge



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Measured Capacitive Coupling

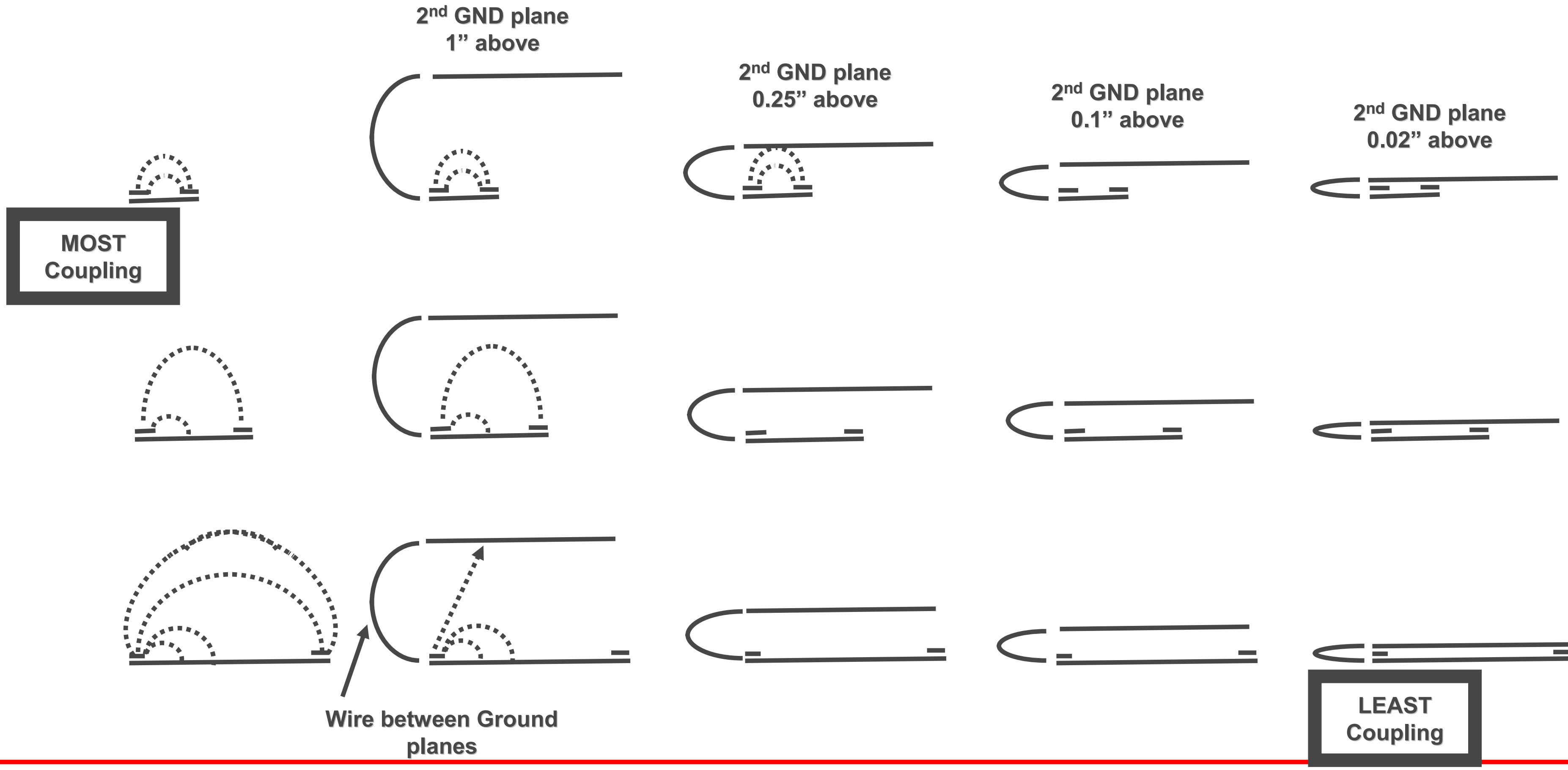
- **With parallel PCB traces of size 0.1” by 8”, a distance of 1/16” above ground plane**
  - Spaced 0.5”, model as 0.7 pF
  - Spaced 1” , model as 0.1 pF
  - Spaced 2”, model as 0.01 pF
  - Spaced 10”, model as 0.0001 pF
- **In general, coupled charge is $1/\text{Distance}^3$**
- **The induced voltage is Charge x Impedance**
- **Coupled charge is proportional to frequency, while Impedance is 1/frequency**
  - **These cancel, so coupled voltage is FLAT with frequency**
- **Above HighPass corner [Freq = $1/(2\pi*R*C)$]**
  - **Voltage is constant with frequency**

Capacitive Coupling from MCU trace at 2”

- **Coupling 1”, from 0.1”x2”, is 0.0006 pF (6 femtofarads)**
- **Coupling 2” away, will be $6/(2^3)$ = 6/8 = 0.75 fF**
- **Reduce area of each trace from 0.1”x 2” to 0.025”x 2”, or 4:1 on each, or 16:1 total; expect (6/8)/16 or 0.05 fF**
- **Assuming 10 pF capacity on the analog node, and 100 kΩ resistance (giving 1 uS tau, or 0.16 MHz F3db for HPF), the MCU clock waveform will be preserved in shape, but reduced in amplitude**
  - $V_{analog\_node} = V_{digital} \times 0.05\ fF/10{,}000\ fF = V_{digital}/200{,}000$
  - For a 5 V logic swing, expect 200,000:1 reduction => 25 uV_{PP}
- **Thus any 5 V signal, above 0.16 MHz, in a 0.05”x 2” trace, will couple 25 uV_{PP} onto another 0.05”x 2” trace, when separated by 2”**

Benefit of Two Grounds, surrounding the Signal Layer,

with Transmitter-Receiver spacing of 0.25, 0.5, 1.0inches



Benefit of Two Grounds, surrounding the Signal Layer

- **Measured with Network Analyzer**
  - **Various resonances with 6” wide movable-height shield plate**

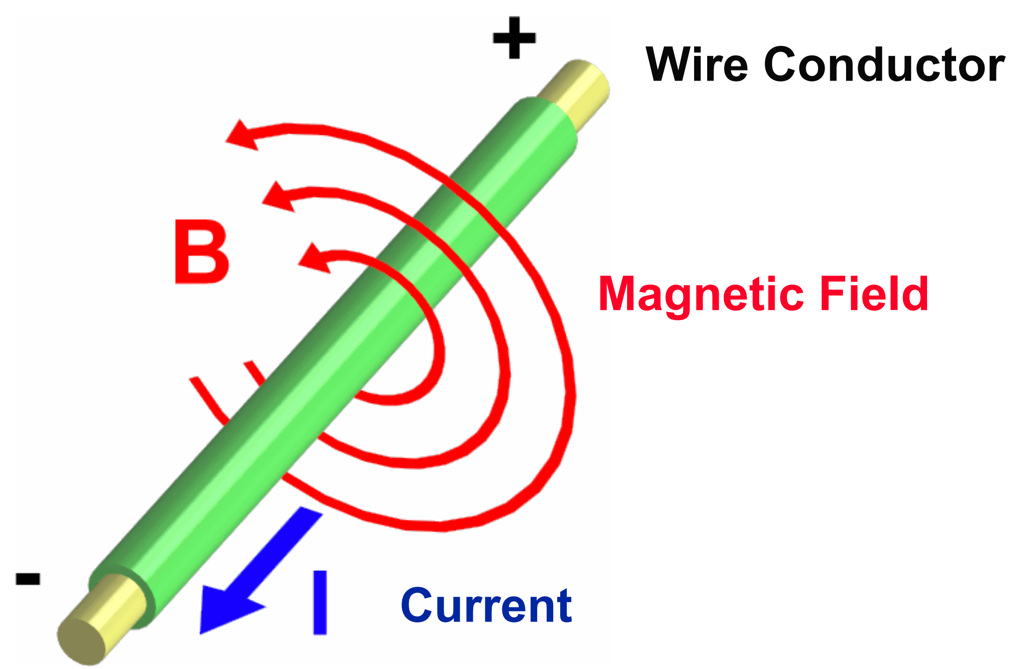
Trace separation (center-center)	Freq (MHz)	Coupling thru air (dB) No Shield	2nd shield 1” above (dB)	2nd shield 1/4” above (dB)	2nd shield 0.1” above (dB)	2nd shield 0.02” above (dB)
0.25”	0.1	-47 (Cal -12db)	-47	-52	-65	-83
0.25”	1	-47 (Cal -12db)	-47	-52	-65	-84
0.25”	10	-47 (Cal -13db)	-47	-52	-65 (-85@45MHz)	-90
0.25”	100	-54 (Cal -24db)	-53	-58	-50 (-26@85MHz)	-65
0.5”	0.1	-63	-64	-82	-88	-88
0.5”	1	-63	-64	-78	-95	-95
0.5”	10	-63	-64	-80	-90	-100
0.5”	100	-68	-69	-76	-75	-75
1.0”	0.1	-80	-87	-88	-88	-88
1.0”	1	-77	-82	-98	-95(-110@3MHz)	-95
1.0”	10	-77	-82	-100	-88*	-105
1.0”	100	-85	-88	-80 (peaking	-50*	-20dB @45MHz

Examine H-field Coupling (B-field or magnetic) and How to Predict

Behavior of H-Field Coupling

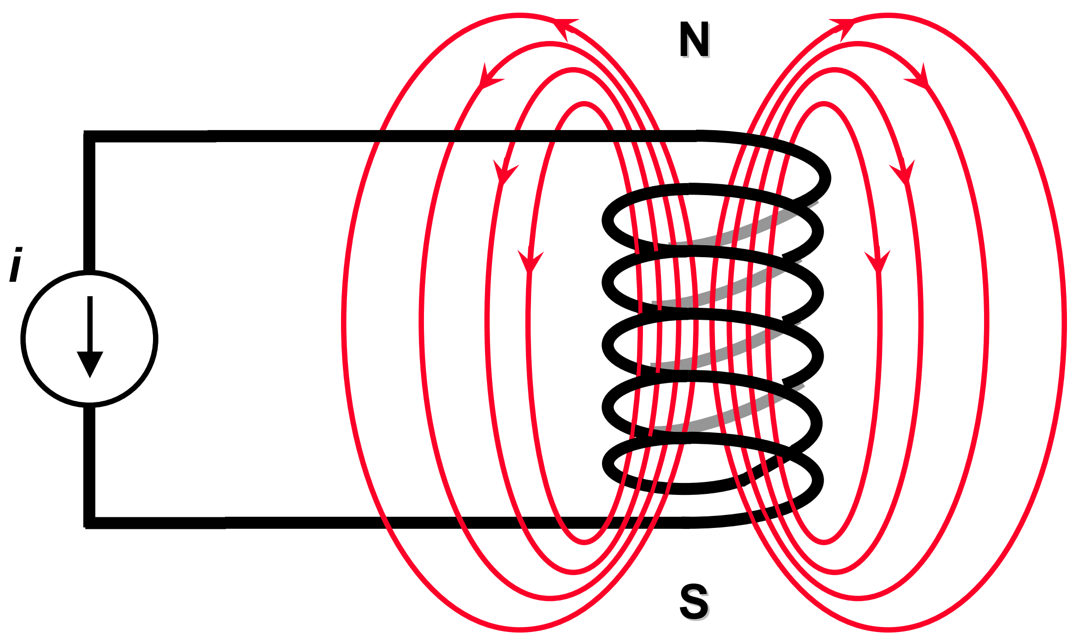
- **The SI unit of a magnetic field is the Tesla (T)**
  - 1 Tesla = 1 Webers/meter^2 = 10,000 Gauss
- **One Tesla (1 T) is defined as the field intensity generating one newton of force per ampere of current per meter of conductor:**
  - $T = N \cdot A^{-1} \cdot m^{-1}$
    $= kg \cdot s^{-2} \cdot A^{-1}$

T = Tesla
N = Newton
A = Ampere
m = Meter
Kg = Kilogram
S = Second



Behavior of Coupled Flux

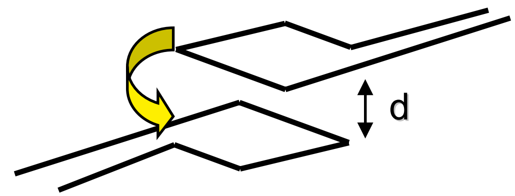
- Magnetic field, shown as magnetic lines of force (flux), through a coil
- The combined influence of all the turns produces a two-pole field similar to that of a simple bar magnet.
- One end of the coil is a north pole and the other end is a south pole



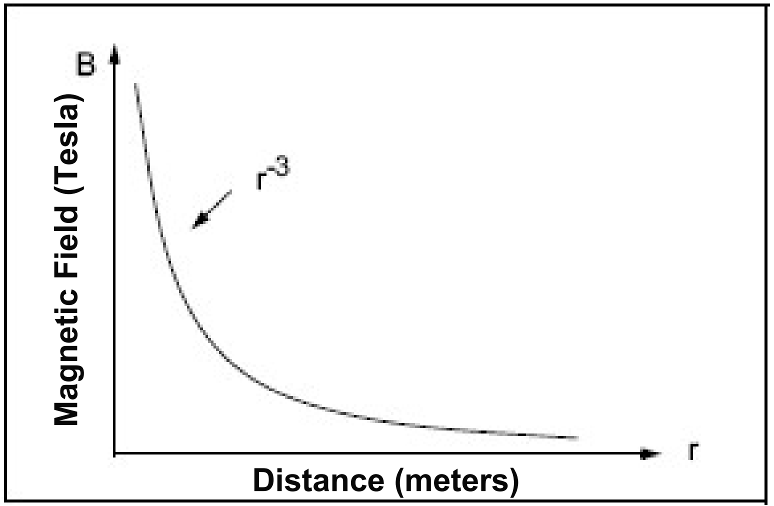
How Magnetic Coupling Upsets Analog Circuits

- **The magnetic field attenuates by 1/distance^3**

Given a magnetic field of 4 uT generated by a wire loop, acting on a second wire loop:

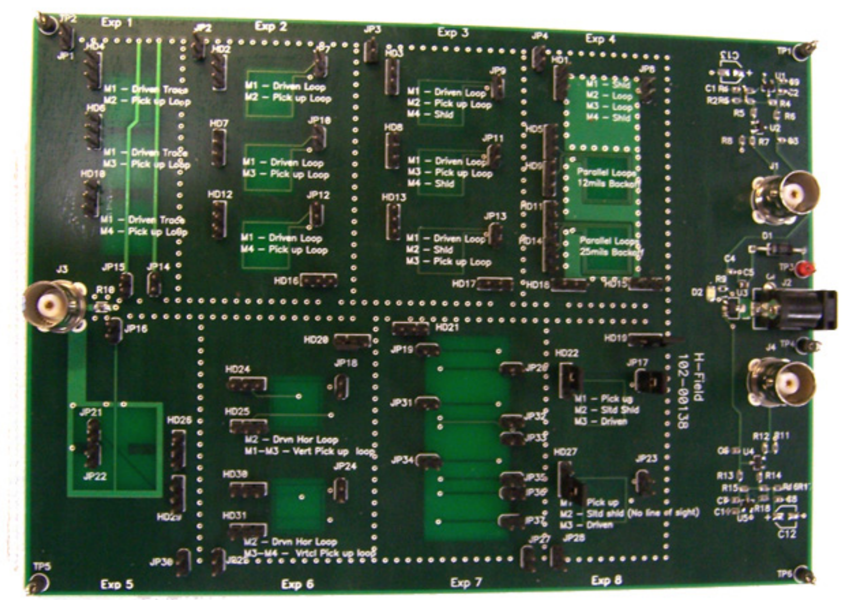


Distance between loops (cm)	Magnetic Field (uT)
1	4
2	0.5
4	0.063
8	0.008
16	0.001



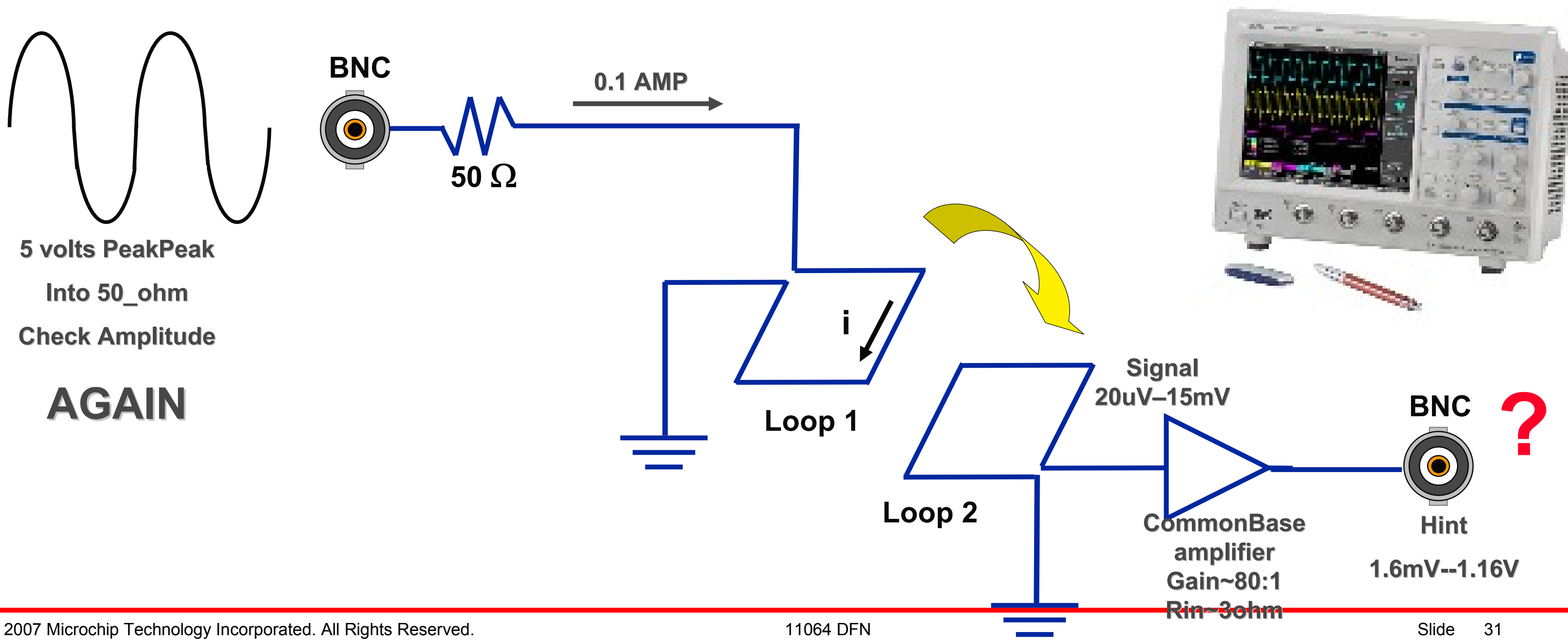
H-Field Coupling Lab Exercises

- This set of lab exercises will explore and quantify the effects of H-fields
- The H-Field Eval Board (104-00138) is designed to demonstrate H-field coupling under various conditions
- These experiments will help system designers understand the impact PCB layout techniques have on controlling noise in their design



H-Field Coupling Lab Exercises

- 7 Experiments look at H-Field Noise Coupling from one loop to another loop on a PCB under various conditions
- 1 Experiment looks at noise coupling between a trace and loop



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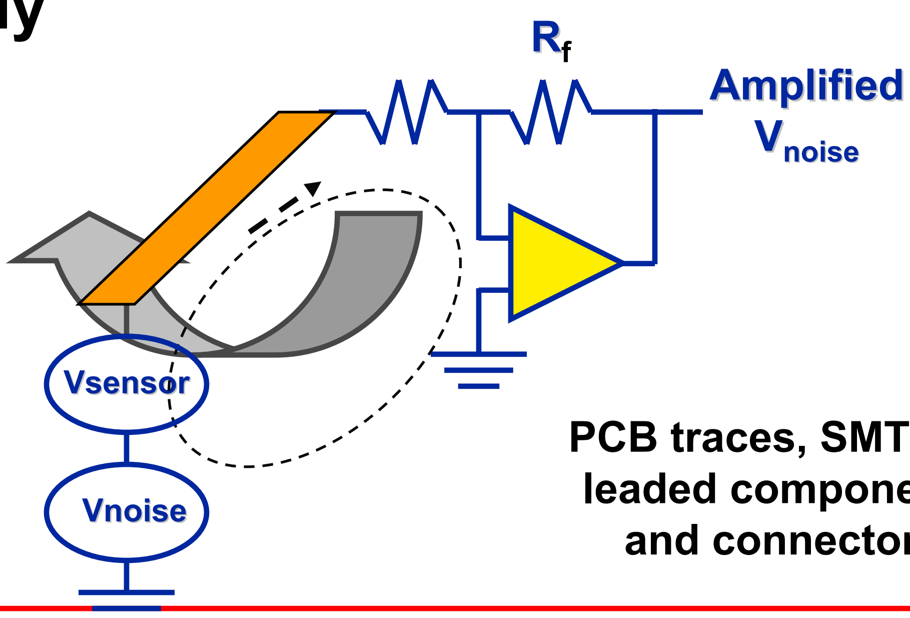
H-Field Board (104-00138) Lab Exercises

- **Lab Results/Discussion**
- **What did we learn?**
  - **Distance from fields matter!**
  - **Ground planes matter!**
  - **Frequency matters!**

Experiment	Magnitude @ 100 kHz (mV)	Magnitude @ 1 MHz (mV)	Magnitude @ 10 MHz (mV)
1/1	2.18	5	19
1/2	1.56	-	-
1/3	5.62	22	100
1/4	3.75	7.34	25
1/5	4.37	9.53	33.1
1/6	5	13.1	52.5
2/1	15.9	85.9	387
2/2	18.1	112	506
2/3	34.3	240	1.16V
3/1	10	14.6	8.12
3/2	13.4	50	250
3/3	31.2	210	1.08V
4/5	14	50	168
7/1	-	3	9.06
7/2	-	2.8	9.06
7/3	-	3.5	12.6
7/4	-	2.9	9.53
7/5	-	1.8	2.96

How Magnetic Coupling Upsets Analog Circuits

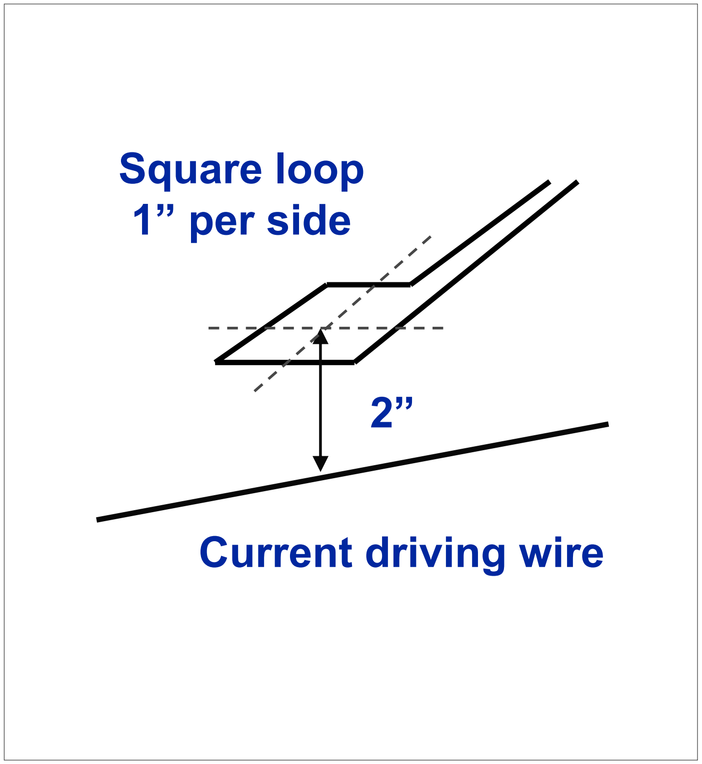
- **A changing magnetic field exerts a force on electrons**
  - In metals the electrons are free to move
- **A conductor, in a changing magnetic field, has an induced voltage**
  - Transformer, loop antenna, wire, metal sheet
- **Two straight conductors (wire or PCB), if not totally symmetric and precisely at 90 degrees, will couple magnetically**



PCB traces, SMT and leaded components and connectors

Magnetic Coupling
Wire-Loop, Calculated

What voltage is induced in a loop, some distance from a wire with changing current?



- $$V = \frac{NA\mu_o}{2\pi D}\frac{di}{dt}$$
  - N = Turns
  - A = Area (meter^2)
  - $\mu_o = 4\pi * 10^{-7}$ Henry/meter
  - D = Distance (meters) from wire to loop
- 15 V at 100 kHz, Rl =50 Ω

  (current is 50 mA average, assume 100 mA peak, rising to 100 mA in 1 us)

Magnetic Coupling Wire-Loop, Calculated

- Voltage = $\frac{N \times A \times \mu_o}{2\pi \times D} \times \frac{di}{dt}$

$$V = \frac{(1 \times (0.025)^2 \times 4\pi 10^{-7})}{(2\pi \times 0.05)} \times \frac{0.1\ A}{1\ uS}$$

$$V = (2.5 \times 10^{-9}) \times (1 \times 10^5)$$

V = 250 uV

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Magnetic Coupling Wire-Loop, Measured

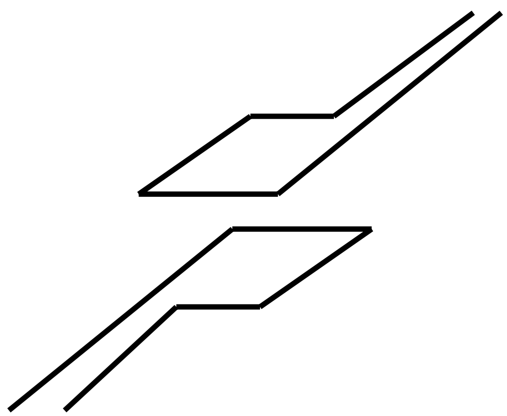
- Straight wire, di/dt = 0.1 A/uS
  - 100 kHz, 15 V_{PP}, Rl = 50 Ω total
- Pick-up loop 2” distant, 1”x 1” area
- Bring copper foil against test PCB and then measure

Frequency	di/dt (A/uS)	$V_{induced}$ (No plane)	$V_{induced}$ (Ground plane)
100 kHz sine ($16\ V_{PP}/50\Omega$)	0.1	300 uVpp	30 uVpp
100 kHz Net.Analyzer		-88 dBc floor	-89 dBc (20% drop)
1 MHz Net.Analyzer		-74 dBc	-92 dBc (8:1 drop)
10 MHz Net.Analyzer		-55 dBc	-81 dBc (20:1 drop)
100 MHz Net.Analyzer Nulls 40-70 MHz		-32 dBc	-43 dBc -95 dBc@40MHz

How Magnetic Coupling Upsets Analog Circuits

- Given two 1-turn square loops, $(0.5")^2$ area
- Separated by 1/8"
- With 0.1, 1.0 and 10 MHz driving one loop

Two square loops 0.5" per side, Separated by 1/8" air gap



Sine wave driving bottom loop

At 100 kHz:

di/dt = (V/R)(jω) = (V/R)(2π)(Freq)

= (0.315V/50Ω) * 2π*100 kHz

= 4,000 amp/sec

At 1 MHz:

di/dt = (V/R)(jw) = (0.315V/50Ω) * 2π*1 MHz

= 40,000 amp/sec

At 10 MHz:

di/dt = (V/R)(jw) = (0.315V/50Ω) * 2π*10 MHz

= 400,000 amp/sec

Table of Inductive Coupling

- **Using a Network Analyzer**
  - Actual measurements taken at 100 kHz, 1 MHz and 10 MHz
  - Other frequencies scaled up or down to indicate voltage magnitudes

Frequency	TX_{loop}	RX_{loop}	Ratio	$V_{received}$
Compute 100Hz				0.006 uVpp
Compute 1KHz				0.063 uVpp
Compute 10KHz				0.630 uVpp
Measure 100KHz	0dBm (0.63 Vpp)	-102 dBm	$0.8*10^{-6}$	5.000 uVpp
Measure 1MHz	0dBm (0.63 Vpp)	-80 dBm	$1*10^{-4}$	63.000 uVpp
Measure 10MHz	0dBm (0.63 Vpp)	-60 dBm	$1*10^{-3}$	630.000 uVpp
Compute 100MHz				6,300.000 uVpp
Compute 1GHz				63,000.000 uVpp

Switching Regulator Magnetic Fields

- Switching Regulator induced voltage
  - 16 watt supply, inductor 1 cm x 2 cm planar 18 uH
  - 500 kHz switch rate, measured with $(0.5")^2$ loop

Location	Voltage (peak to peak) 120 MHz & 50 MHz ringing
1/8” above	540,000 uV
1” above	110,000 uV
2” above	48,000 uV
1” @ 90^o above	50,000 uV
1” to side	115,000 uV
2” to side	55,000 uV

Magnetic fields of Motors

- AC induction motor, dsPIC® DSC controller, Power MOSFET/toroidal transformer as Power Driver; 460 volts, 1.5 amps for rated output
- Switching frequency at 30 kHz, to synthesize a variable frequency
- Strong spikes, with ringing at 7 – 10 MHz, Q approx 20 (-3db/cycle)
- Measure with $(.5")^2$ loop, a good model of typical circuit routing

Distance	Voltage Amplitude into 0.5"x0.5" loop
1"	0.4 V
2"	0.2 V
4"	0.1 V
8"	0.06 V

Thanks to Gurinder Singh for this data

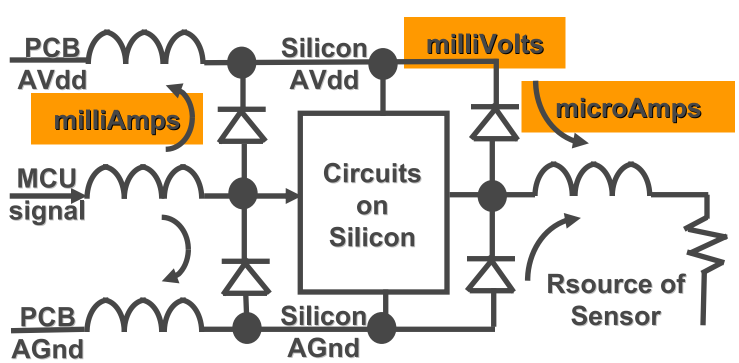
Now: take 15 minute break

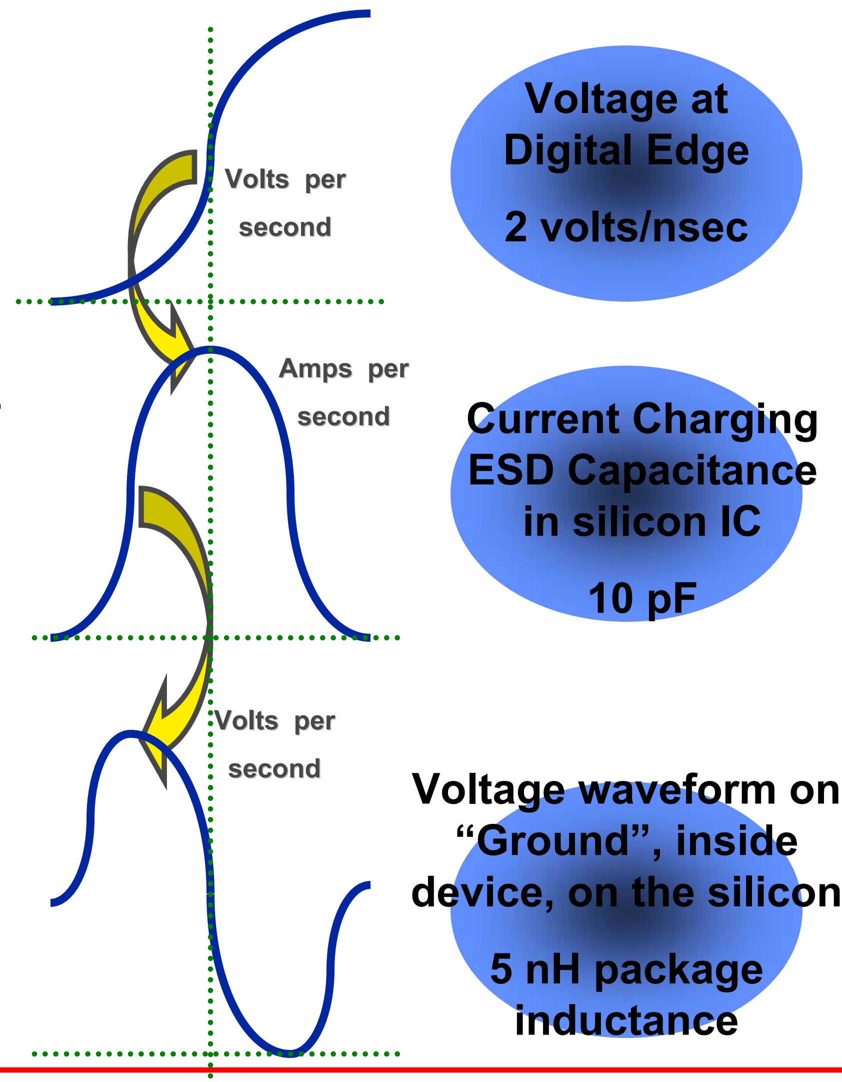
- **Topics Still to Come -------**
- **Digital Noise**
- **Power Supply Noise**
- **Lab #3: measure PSRR of LDO+OpAmp, and measure DC shift caused by Digital Noise**
- **Making a Budget**
- **Taking steps to reduce noise and effect, or "how to implement that budget"**

Digital Noise

Interaction between Logic Swings and Analog/Digital Signal Returns

- Large fast logic swings couple large peak currents into ESD structures of all IC interfaces. As currents take all possible paths back to the Micro-controller, V_{DD} and RTN/GND pins of ICs exhibit large instantaneous voltages: “noise”
- Slowing edge speeds by 10:1 provides a 100:1 reduction in V_{DD} and in GND noise. Slowing edge speed 100:1 provides 10,000:1 (80dB) less noise.





Digital Interfaces
Noise coupling into ESD Structures

- **Using the equation,** **$I = C*\Delta v/\Delta t$**
  - **Where I = current, C = capacitance, v = voltage, t = time**
  - **With C representing V_{DD} or GND ESD input capacitance on a silicon device**

I = 10 pF*(5 v/2.5 nS) = 20 mA average or **40 mA** peak in 1.25 nS

  - **This current returns through both VDD and GND pins (assume 50% in each)**

- **Using the equation,** **$V = L*\Delta i/\Delta t$**
  - **Where V = voltage, L = inductance, i = current, t = time**
  - **With L representing V_{DD} or GND ESD inputs inductance on a silicon device**

V = 5 nH *(20 mA [in GND]/1.25nS) = 80 mV Peak in GND,
or 160 mVpp
(Peak-to-Peak Voltage)

Digital Interfaces
Noise coupling into ESD Structures

- **Now, slowing the signal speed to 5 V/25 nsec = 4 mA peak/12.5 nsec**

  V = 5 nH*(4 mA/12.5 nsec) = 1.6 mV_{PP}

- **Slowing to 5 V/250 nsec (with R*C 4.7Kohm & 56pF filter) => 16 uV_{PP}**

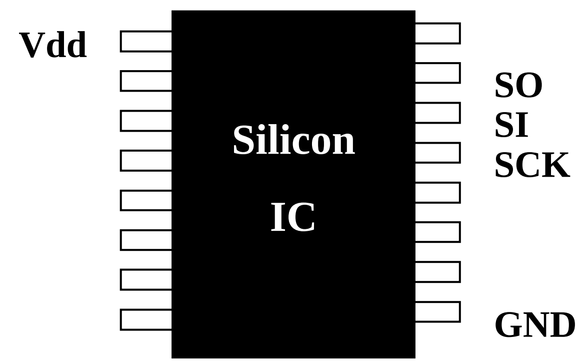
Rise Time	V_{PP}
2.5 nsec	160 mV
25 nsec	1.6 mV
250 nsec	16 uV

SUMMARY

- Digital Edges couple large peak currents into ESD structures on all IC pins
- Slowing edge speeds by 10:1 provides a 100:1 (40 db) reduction in V_{DD} and GND noise.
- Slowing edge speed 100:1 provides a 10,000:1 (80dB) reduction in noise.

Digital Interfaces
Noise of static logic levels

- **An MCU has 0.5 V/5 ns of noise on Vdd and GND caused by internal clocking. This noise appears on static outputs.**
- **IC ESD structure**
  - Capacity is 20 pF (total) on 3 SPI lines



- **Current into SPI pins is:**

  $I = C*\Delta V/\Delta T = 20\ pF*(0.5v/5nS) = 2\ mA/2.5\ nS$ (I_{peak} in ½ t_{rise})

  Current seeks return path, thru package inductance (5 nH) of IC

  $V = L*dI/dT = 5\ nH*(2\ mA/2.5\ nS) = 4\ mV/1.25\ nS$ (V_{peak} in 1/4 t_{rise})

  Thus, the "quiet" MCU causes 4,000 uV peak (8,000 uV_{PP}) in IC
- **Given: Substrate of the IC has 8,000 uV_{PP} digital noise**

  ESD input structure has 7 pF capacitance

  Analog input noise current is then

  $I = C*dV/dT = 7\ pF*(8,000\ uV_{PP}/1.25\ nS) =$ **45 uA**
- **So, with 100 Ω source, V = I*R = 45 uA * 100 = 4,500 uV_{PP}**

Power Supply Noise

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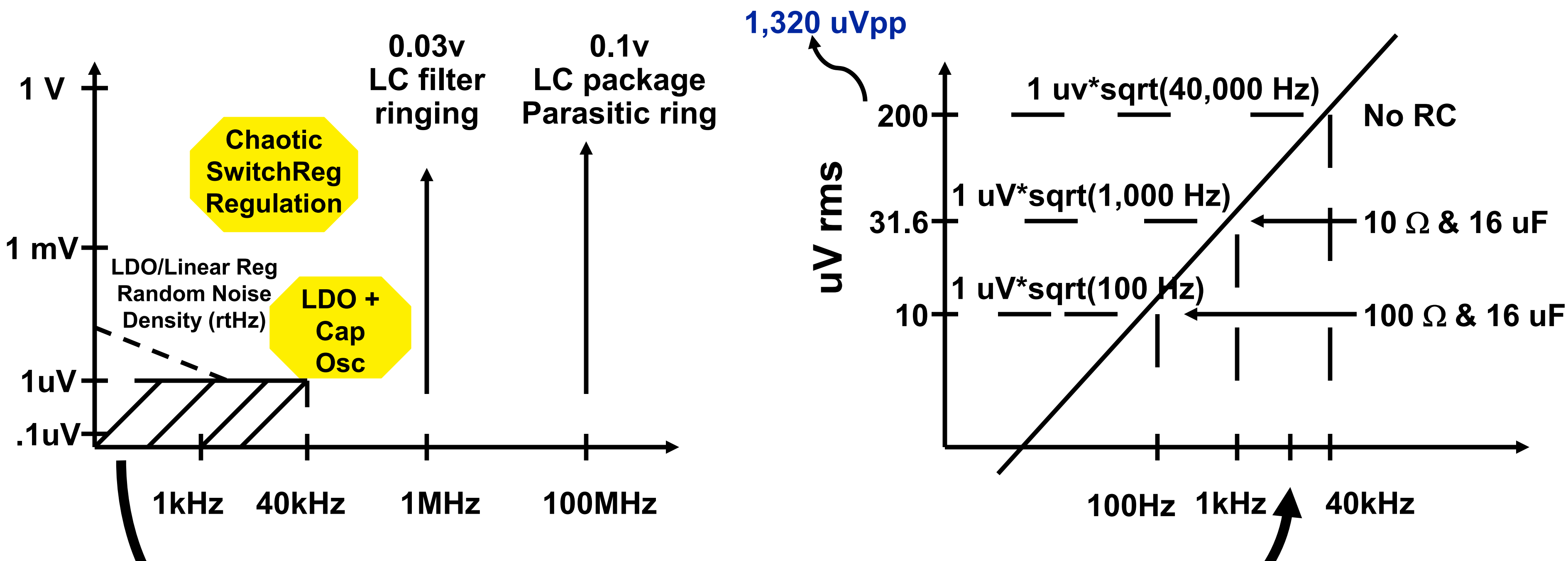
Power Supply Output Noise

- **System designers must deal with power supply noise interfering with low noise amplifiers, oscillators, and other sensitive devices**
- **Many voltage regulators have high output noise from switching circuits and unfiltered references.**
  - Ordinary three-terminal linear regulators will have several hundred nanovolts per root-hertz of white noise
  - Switching regulators may have switching noise ranging into the millivolt range covering a wide frequency spectrum.
- **And many devices generate noise that couple on to supply rails.**

Power Supply Output Noise

- This is what to expect from an LDO or Switching Regulator

What is the "root-Hertz" concept? Acknowledges NoisePower is proportional to Bandwidth, while NoiseVoltage is proportional to squareroot(Bandwidth)

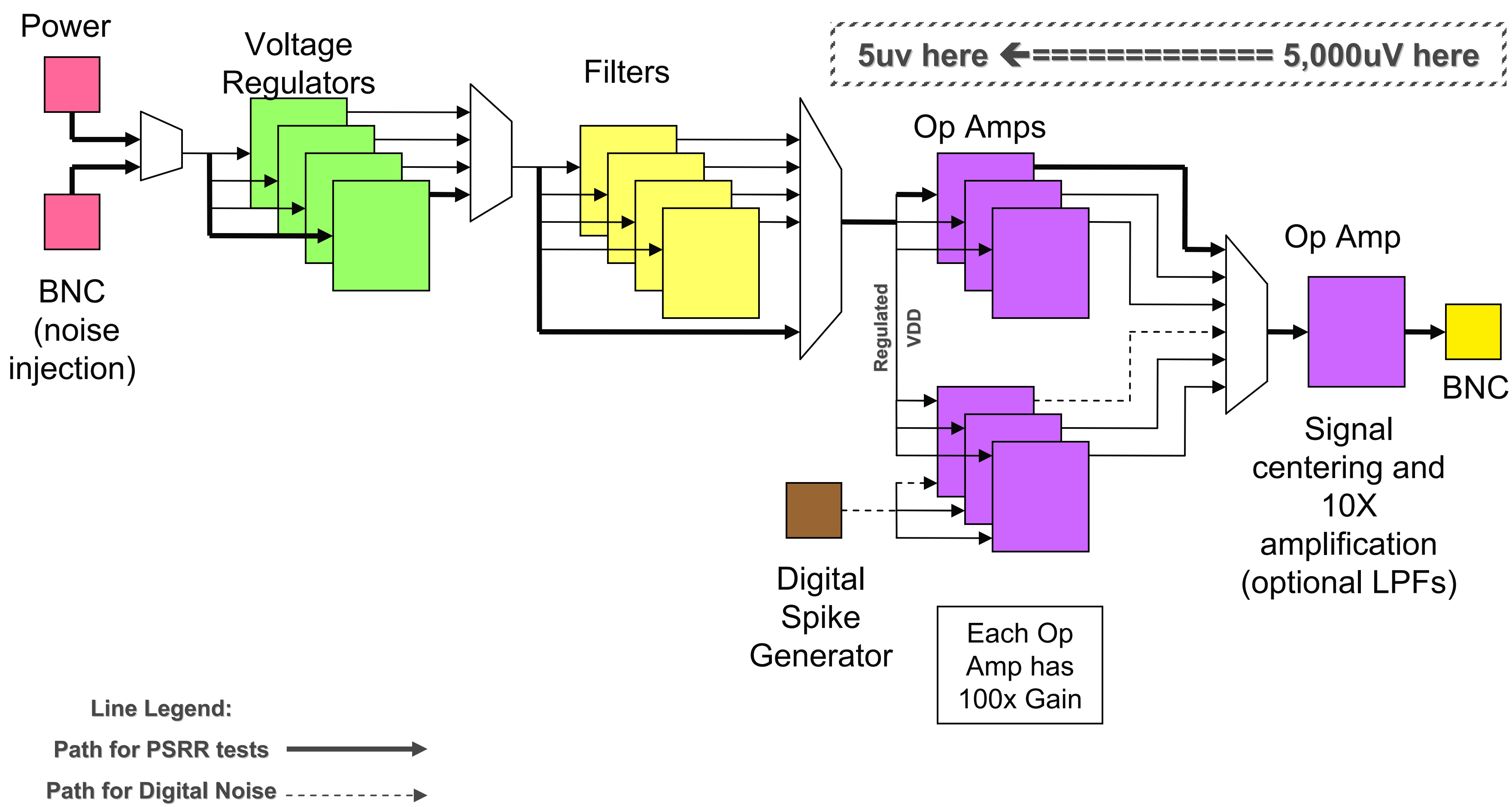


Convert the LDO thermal floor to Total Noise

PSRR and Digital Noise Lab Exercises

- **This set of lab exercises will explore and quantify the effects of Power and Digital Noise on system performance**
- **These experiments will help system designers understand the impact that Power and Digital Noise can have in their design**

PSRR and Digital Noise Board (104-00139) BLOCK DIAGRAM



PSRR and Digital Noise Board (104-00139) Lab Exercises

- **Lab Results/Discussion**

- **What did we learn?**

- **PSRR depends on Frequency**
- **PSRR depends on OpAmp Iddq**
- **PSRR depends on Regulator Iddq**

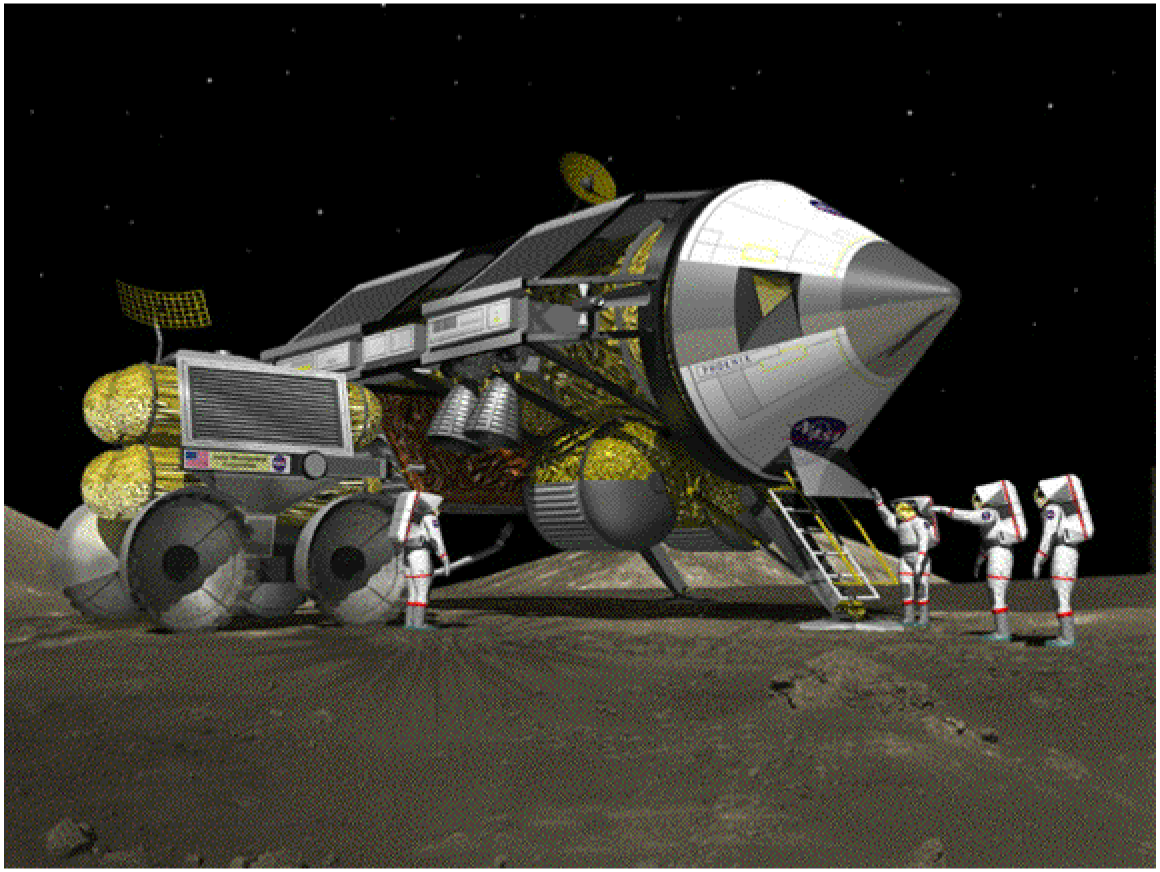
- **An RC filter is powerful method**
- **Why not FerriteBeads?**

- **Digital Noise causes DC_shifts**
- **Different IC pins have different DC_shifts**
- **Spike frequency affects DC_shift**

SECTION 2:
Developing a noise budget for a desired analog resolution

Building Budgets

- **Imagine you're on the moon and need to build an "oxygen budget" for a week . . .**



Building Budgets

- May be trial-and-error, as some noise contributions are very costly to reduce
- Start by assigning all noise sources the budget of $V_{Peak\text{-}to\text{-}Peak}/(\#Noise\_Sources)^{-2}$ Volts
- Examine circuit for impedances => capacitive coupling
- Examine PCB floor plan for loop areas => magnetic coupling
- Define/measure aggressor voltages, currents & rise times, both on and off PCB
- Define any DC currents flowing through/across the PCB
- Define Averaging— (for example, the MCP3551 22-bit Delta Sigma ADC averages 2048:1 (33dB or 5+ bits)

Recall Major Noise Sources

Source of Noise	Noise amplitude (worst case)[1] $V_{Peak\text{-}to\text{-}Peak}$
Digital Interfaces	160,000 uV
VDD noise	100,000 uV
Magnetic Field (8”), Appliance motor/controller	60,000 uV
Magnetic Field (2”), Switching Power Supply	50,000 uV
Magnetic Field (2”), MCU Clock 50-Ohm line	25,000 uV
Electric field of MCU (1”)	1,700 uV
Vibration of Coax Cables	2,000 uV
Fluorescent Light at 1 foot	625 uV
Vibration/PCB stress on Ceramic Capacitors	500 uV
Thermal Gradients across solder joints	200 uV
Dielectric Absorption of Capacitors	200 uV
Current Spreading in PCB Copper Foil	150 uV

[1] The test conditions in which these measurements were taken are indicated in Appendix

What limits apply?

- **Minimum PCB+IC_ESD capacitance is approximately 10 pF**
- **V_{DD} and I_{dd} and V_{signal} define resistance value and thus F3 db.**
  - If I_{dd}=1uA and V_{DD}=5v, then R_{signal} = 5 MΩ
  - 5 MΩ & 10 pF produces 50 uS Tau, or 3 kHz bandwidth. If system needs higher bandwidth, the I_{DD} MUST increase
- **For lower total noise, the capacitance MUST increase**
- **Thus, for high bandwidth and low noise, I_{DD} must rise**

What will FAIL?

- **Ignoring Power Supply Rejection of ICs**
- **Assuming the ADC quanta is the front-end quanta**
  - **Don’t forget to scale by amplification!**
- **Attempting [8-bit ADC + voltage gain of 10,000 => 2uV quanta] but using 8-bit (19.6 mV) noise methods**
- **Attempting quanta < 25 uV, near (2” away) an MCU, without planes**
- **Attempting low I_{DD} (high Resistor values) in high dv/dt systems**
- **Sharing V_{DD}, but using NO RCs to isolate IC’s V_{DD}**
- **Allowing large step changes in I_{DD}, on a quiet V_{DD}**
- **Ignoring need for 8 tau-settling for 12-bits, 12-tau for 18- bits (8.9 db of resolution per R*C time-constant tau)**

How to Build a Noise Budget

- To control RMS (1-sigma), use RootSumSquare
- To control Peak-Peak (what a human views), use Sum_Of_Absolute_Values_of_Peak-to-Peak
  - To achieve 1 mV_{PP}, across 6 noise sources, we need 1/6 uV_{PP} from each source; or 0.5 uV + 5 * 0.1 uV
  - Lazy – RSS all errors $sqrt(3^2+3^2+4^2+1^2+1^2) = 6$
  - Coward – Add all errors 3+3+4+1+1 = 12
- Wise: Acknowledge a MIX of RSS and Algebraic (if correlated) is appropriate

Interaction of PSR & Stage Gain

- **Combine Switching Regulator noise with [Gain = 100, Bandwidth = 1 MHz] amplifier**

Freq	DC	100 Hz	10 kHz	1 MHz	100 MHz
V_{DD} Noise	10 mV line/load	100 uV ripple	1 mV thermal	0.1 V LC rings	0.1 V IC rings
PSR	80 dB 10^4	80 dB 10^4	40 dB 10^2	0 dB 1	0 dB 1
Noise ReferToInput	1 uV	<<1 uV	10 uV	0.1 V	0.1 V
Stage Gain	100	100	100	100 F3dB	1
Stage Out NOISE!	100 uV	<<100 uV	1,000 uV	10 V	0.1 V

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Allowed Noise Voltage

- E Field @ 100 kΩ, H Field @ 0.5”², V_{DD} @ 1 MHz, Vibration @ 1/4”flex, I*R adjacent to 10 MHz sine/50Ω clock, Thermal @ 1 watt & 70°C/watt
- No amplification, no bandwidth LPF

# bits	Quanta @ V_{REF}=5V	V_{noise}, if 10, each RSS’d	E Field	H Field	V_{DD}	Vib	I*R	Therm
8	19,600 uV	6,200 uV	N	Y	Y	N	N	N
10	4,900 uV	1,550 uV	Y	↓	↓	Y	N	N
12	1,220 uV	400 uV	↓	↓	↓	↓	N	N
14	305 uV	100 uV	↓	↓	↓	↓	Y	Y
16	76 uV	25 uV	↓	↓	↓	↓	↓	↓
18	19 uV	6.3 uV	↓	↓	↓	↓	↓	↓
20	4.8 uV	1.6 uV	↓	↓	↓	↓	↓	↓
22	1.2 uV	0.4 uV	↓	↓	↓	↓	↓	↓
24	0.3 uV	0.1 uV						

Allowed Noise Voltage (A_v = 10)

- E Field @ 100 kΩ, H Field @ 0.5”^{2}, V_{DD} @ 1 MHz, Vibration @ 1/4”flex, I*R adjacent to 10 MHz sine/50Ω clock, Thermal @ 1 watt & 70°C/watt
- Amplification = 10x (20 dB), no bandwidth LPF

# bits	Quanta @ V_{REF}=5V	V_{noise}, if 10, each RSS’d	E Field	H Field	V_{DD}	Vib	I*R	Therm
8	19,600 uV	6,200 uV	Y	Y	Y	Y	N	N
10	4,900 uV	1,550 uV					Y	Y
12	1,220 uV	400 uV						
14	305 uV	100 uV						
16	76 uV	25 uV						
18	19 uV	6.3 uV						
20	4.8 uV	1.6 uV						
22	1.2 uV	0.4 uV						
24	0.3 uV	0.1 uV						

Allowed Noise Voltage
(A_V = 10, 100 Hz, no_vib, 0.1 watt)

- E Field @ 100 kΩ, H Field @ 0.5”^{2}, V_{DD} @ 1 MHz, Vibration @ 1/4”flex, I*R adjacent to 10 MHz sine/50Ω clock, Thermal @ 1 watt & 70°C/watt
- Amplification = 10x (20 dB), 100 Hz LPF (one-pole PASSIVE non-distorting)

# bits	Quanta @ V_{REF}=5V	V_{noise}, if 10, each RSS’d	E Field	H Field	V_{DD}	Vib	I*R	Therm
8	19,600 uV	6,200 uV	N	N	Y	N	N	N
10	4,900 uV	1,550 uV	N	Y		N	N	N
12	1,220 uV	400 uV	Y			N	N	N
14	305 uV	100 uV				N	N	Y
16	76 uV	25 uV				N	Y	
18	19 uV	6.3 uV				N		
20	4.8 uV	1.6 uV				N		
22	1.2 uV	0.4 uV				N		
24	0.3 uV	0.1 uV				N		

SECTION 3:
Taking steps to reduce noise and its effects

Methods to Improve (a potpourri of tricks)

To minimize effects of E-Fields & H-Fields

1) **Add Ground Plane!**
   - Can attenuate noise to less than 200 uV (even if digital clock trace is less than 40 mils above a sensitive analog signal)
2) **Add decoupling capacitors to all devices**
   - Use RC filters for analog ICs
3) **Minimize circuit loop areas**
   - Note, the *total* loop area is determined by the complete current path from the source to load, and the return to the source. (Recall that current always returns to its source.)
   - Reduce signal-path resistances (minimizes E-Field sensitivity)
4) **Add further ground paths**
   - Providing ground metal close to the signal trace takes advantage of the partial cancellation of the magnetic field outside the current loop
5) **Separate (by distance) circuits that have large currents**
   - These circuits act as emitters and will magnetically couple to circuits susceptible to noise Reduce bandwidth and impedance

Methods to Improve (a potpourri of tricks)

To minimize effects of E-Fields & H-Fields

6) **Reduce bandwidth and impedance**
7) **Add shields, and use thin dielectric, to reduce magnetic coupling**
   - Use copper layers of PCB to achieve, when possible

9) **Add more vias between ground planes**
   - Use 1 cm spacing to provide extra shielding around sensitive circuits

10) **Hide sensitive signals (including filtered V_{DD}) between two analog GND planes**

11) **Consider nested shields, with NO shared vias (except at 1 corner)**

12) **Use minimum via_surround, for less damage to planes**

Methods to Improve (cont'd) (a potpourri of tricks)

Digital Interfaces

1) Have one Shared GND plane, so you KNOW where currents, moving to and from Digital and Analog, will travel. Slit plane to guide those currents, if needed
2) Do not overlap Digital planes (VDD, GND) with Analog planes (VDD, GND)
3) Reduce energy coupled through Digital Interfaces

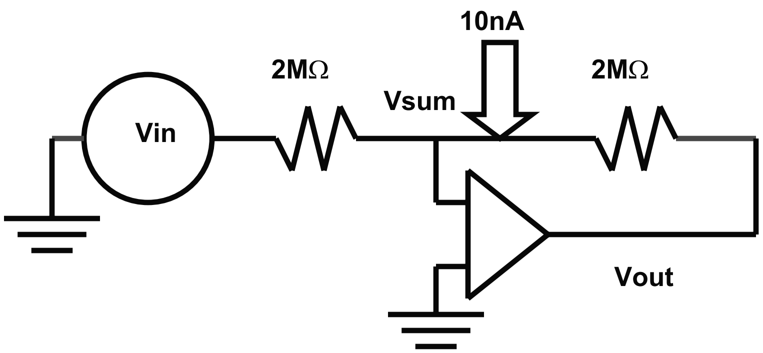
Power Supply

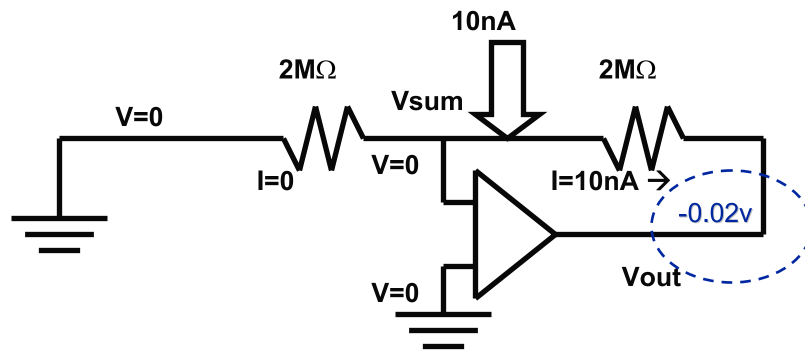
1) Filter Power coming into the system
   - Consider filtering V_{DD} to very sensitive circuits, with cascaded RCs
2) Reduce Vdd of Digital ICs (has inverse square law effect on noise)
3) Do not trust any V_{DD} plane; do NOT route V_{DD} over analog traces
4) Select ICs with better PSR to handle V_{DD} noise

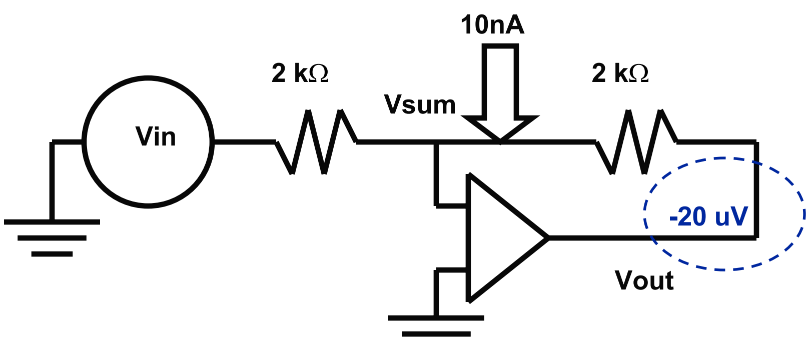
Miscellaneous

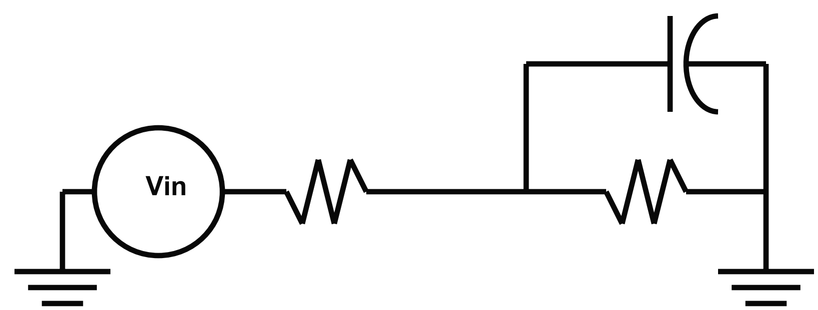
1) Avoid overdriving, even for nanoseconds [High Frequency noise upsets IC bias lines]
2) Improve cables
3) Control temperature

High Circuit Resistance causes E-field sensitivity









Predict the Thru-Air Capacitive Coupling, over a plane

- C_{couple} = Area1 * Area2 / Distance^3, if A1 & A2 are over a plane. Use to predict capacitive-divider
- $V_O = (V_{in}/1600) * (A1/0.2")*(A2/0.2") *(2"/distance)^3$
  - areas in square inches, distance in inches
- If node capacity (C_{load}) <> 10 pF, scale V_O by factor [10 pF/C_{load}]
- For frequencies below $1/(2\pi*R*C)$, reduce V_O by factor [$R*2\pi*frequency*C$]
- For accuracy, keep traces parallel, and keep trace length approximately same as “distance”

Tighten circuit loops to reduce magnetic coupling

- **Identify the sensitive nodes, such as nodes at amplifier inputs**
- **Either add R*C filters, or add Ground plane 3 to 20 mils away, or plan the layout for minimum included area. Put vias UNDER components, not at end or side. Tie IC GND pins to GND under the IC, not outside footprint.**
- **With poor PSR, magnetic coupling into GND pin or V_{DD} pin of IC at high frequencies deserves as much attention as signal nodes and paths. Locate Bypass Caps adjacent to IC, preferably parallel to output pin, so I_{out} fields are minimal.**
- **Consider placing components on BOTH sides of the PCB, for sensitive nodes, if that minimizes magnetic coupling and saves $ (separate shields).**

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Shielding E and H Fields

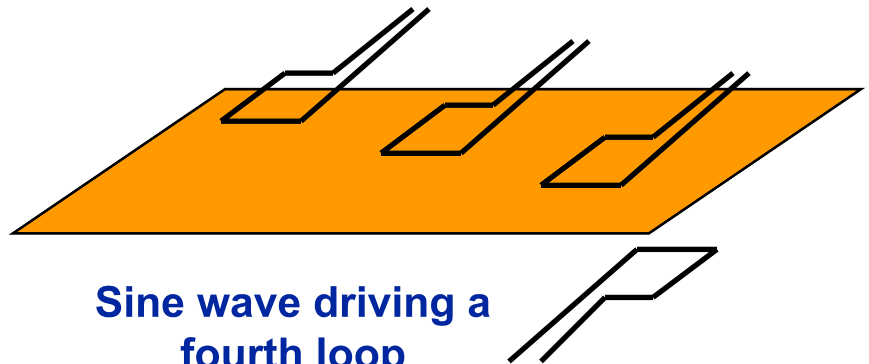
- E (electrostatic/electrodynamic) flux fields TERMINATE at charges
  - Since conductors have charges, conductors are good shields
- A high-resistance E-field shield performs poorly
  - Induced currents (the famous “displacement current”) cause an I*R drop and thus a voltage gradient in the shield that appears on the “shielded” side
- H (magnetic) flux fields DO NOT TERMINATE
  - A PATH must be provided, around the region to protect

Reduction of Magnetic fields, adjacent to copper plane

- A close shield reduces induced voltage by 2x to 4x (6 – 12 dB), at all frequencies.

Freq (MHz)	0.060"	0.040"	0.020"
0.03	-74 dB	-74.0 dB	-77.1 dB
0.10	-63.7	-64.9	-71.4
0.20	-58.0	-59.4	-68.2
0.50	-50.4	-52.0	-62.1
1	-44.3	-45.7	-56.3
2	-38.6	-40.0	-50.6
5	-31.5	-32.9	-43.2
10	-27.2	-28.7	-38.7
20	-25.6	-27.0	-37.3
50	-26.6	-28.0	-37.8
100	-30 dB	-31.4 dB	-40.6 dB

Three loops $(0.5")^2$,
Height above plane is .060", .040", .020"



Sine wave driving a fourth loop

Transmit loop is +15dBm across 56Ω , or 60 mA_{PP} ; no 3dB pad

Reflection coefficent < -20 dB to 40 MHz; -14 dB at 100 MHz

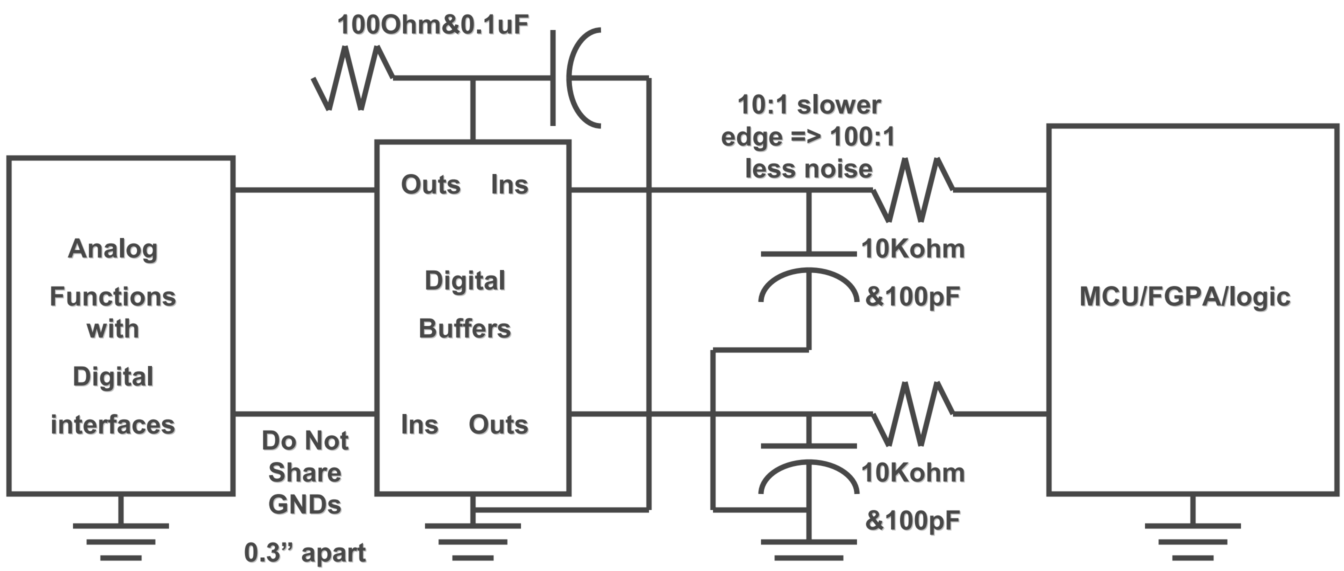
Used Av = 36 dB Common Base amplifier, F3 dB approx 40 MHz.

Network.Analyzer. bandwidth = 100Hz

Actual level was -50.6 – 36 = -87dBc

Digital Interfacing

- 5 V/2.5 nS into 10 pF, returning through 5 nH (V_{DD} & GND), generates 160,000 uV_{PP}
- A “quiet” logic level, 0.5 V/5 nS (package ringing at 100 MHz), into 10 pF, returning through 5 nH (V_{DD} & GND) generates 8,000 uV_{PP}
- Do you want analog RTN moving around?



Digital Interfacing

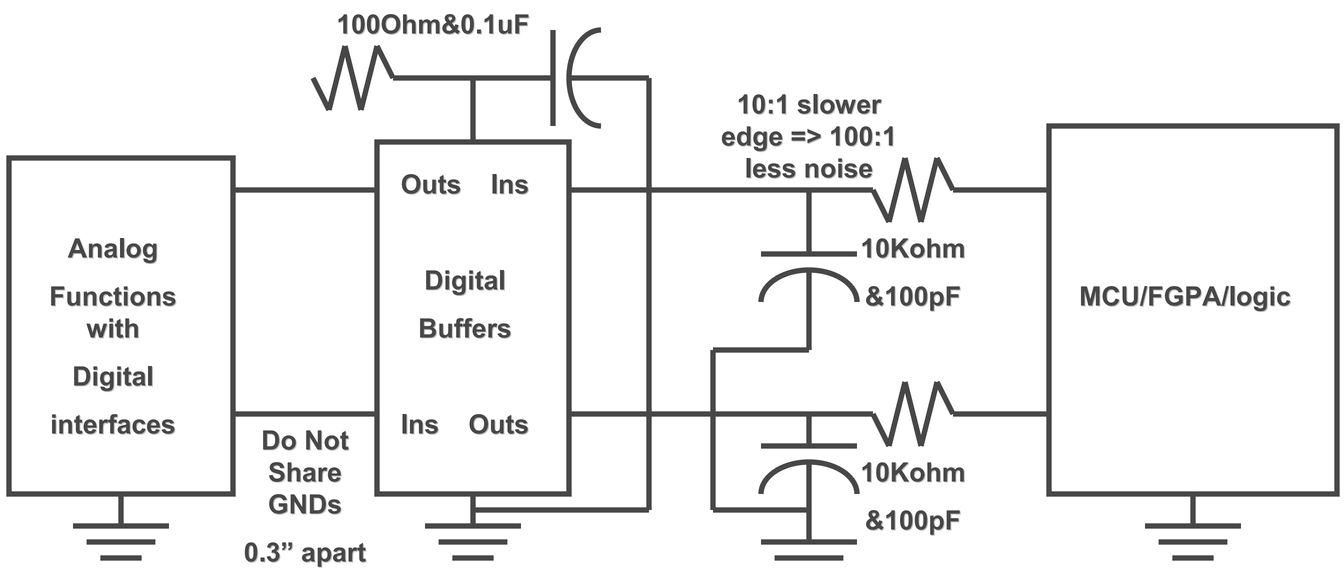
- **Solution:**

  (a) Allow 200 ns for ringing amplitude to drop to a few uV, and then WAIT for analog ICs to re-settle; or

  (b) Include 10 kΩ resistors in all Input lines, to reduce I_{peak} from 40 mA to 5 V/10k = 0.5 mA;

  (c) include 10 kΩ & 100 pF in all input lines;

  (d) include logic buffers with private V_{DD} and 10 kΩ



What Size Bypass Capacitors?

- View the system as handling pulses, and we need the tops of the pulses to be FLAT, so the ADC samples are accurate.
- Admit the ICs have finite Power Supply Rejection (PSR), thus High Frequency ΔV_{DD} causes $V_{signal_}$into_ADC to change.
- We want:

  ΔV_{DD}*PSR(frequency)*stage_gain << 1 quanta, as part of error budget.

  Model ΔV_{DD} as sum of :

  $\{ESR*\Delta I_{load} + \int(\Delta I_{load}/Cap)dt\}$.

What Size Bypass Capacitors?

- Example: A circuit with

{ (0.1 Ω ESR * (5 V/5 kΩ = 1 mA) = 100 uV) +

((1 mA*100 us/0.2 mF) = $5*10^{-4}$ = 500 uV) } = 600 uV ΔV_{DD}

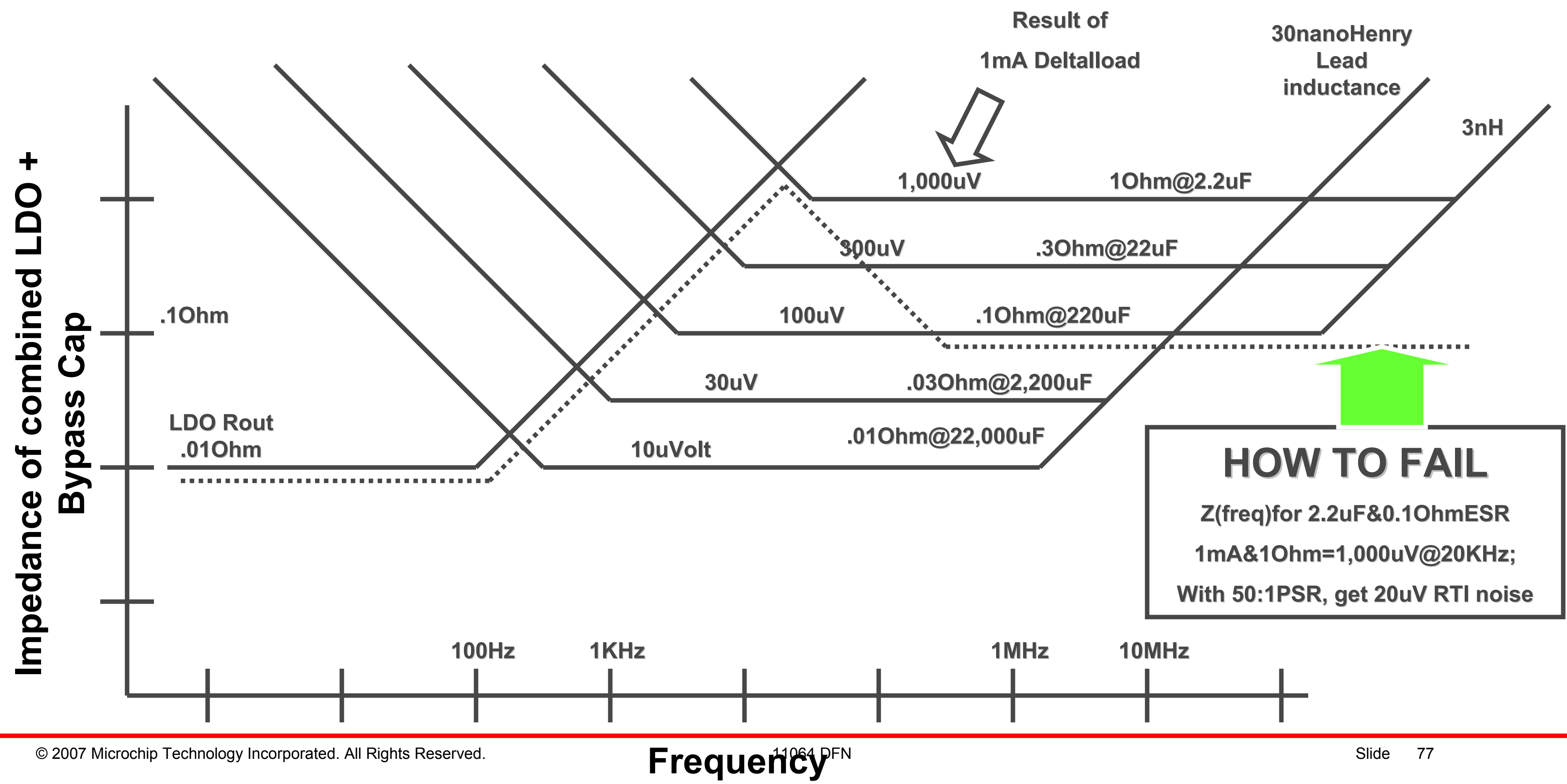
with PSR(10 kHz) = 40 dB, $\Delta V_{input\_referred}$ = 6 uV

with stage_gain of 10X, change[error] at ADC input is V_{signal} = 60 uV

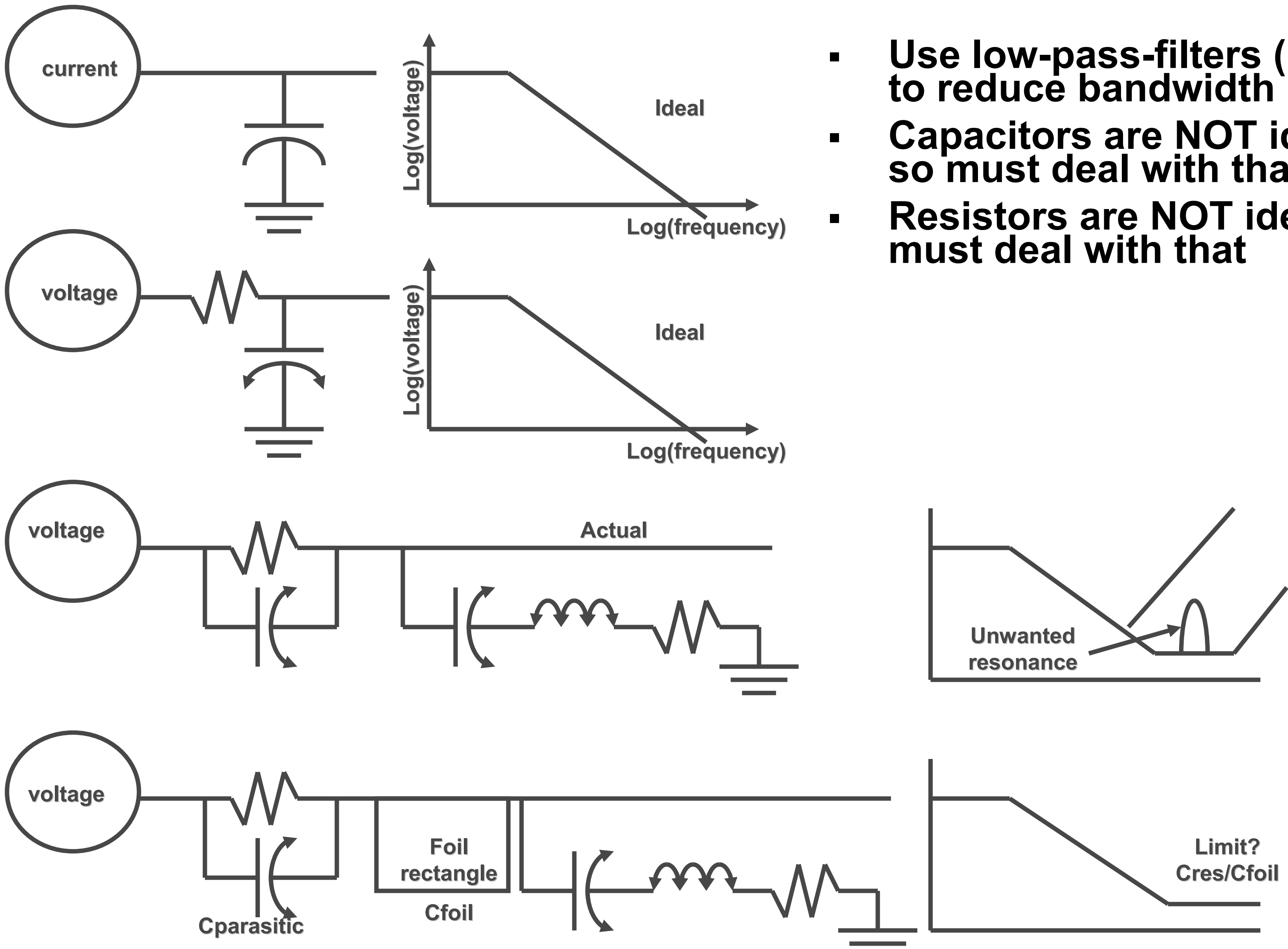
- How to Fail? Lots of amplification and high ESR bypass capacitors and changes in load current
- Solution? Keep currents constant, or pay up for large capacitors that have low ESR

What size and ESR of bypass capacitors?

- Interaction of LDO R_{out} and ESR of leaded bypass capacitors
- Δload of 1 mA, and 1 Ω R_{out} at 20 kHz, produces 1,000 uV
- With 50:1 PSR at 20 kHz, Referred_to_Input noise at IC is 20 uV



Successful Bandwidth Reduction



- Use low-pass-filters (R+C) to reduce bandwidth
- Capacitors are NOT ideal, so must deal with that
- Resistors are NOT ideal, so must deal with that

PCB Floor planning

- **Organize:**

  Sensor → Analog amplifier → ADC → logic → Power Supply
- **Use large components and metal connectors as E-field shields.**
- **Use metal foil electrolytic capacitors as E-field shields**
- **Use multiple planes as H-field shields**
  - **Effective above 1 MHz**
- **Remember that an MCU placed 2” from an analog node will induce 25 uV_{PP}**

PCB Floor planning (cont’d)

- ANY 5 V signal, 2” from analog node, induces 25 uV? When?
- What will 117 VAC wiring do, 2” away?
- Plan the MCU bypassing FIRST, to minimize H-field. Then route MCU IOs.
- Remember heat will cause op amps to drift. Cut gaps in copper to reduce heat flow into analog region of PCB. Heat will cause many microvolts of DC across solder junctions, etc. Read up on Seebeck Effect.

Summary

You should now be able to:

- Understand the magnitudes of noise sources in Analog+MCU signal chains
- Develop a budget for a desired analog resolution
- Apply system design principals to reduce noise and its effects in your application

References

- Reference 1 High-Speed Signal Propagation: Advanced Black Magic, by Howard Johnson & Martin Graham, Prentice-Hall
- Reference 2 EDN Special Issue on EMI Feb 20, 1994
- Reference 3 Electronic Designers' Handbook, L. J. Giacolleto editor, McGrawHill 1977 2nd edition
- Reference 4 National Instruments zone.ni.com/devzone
- Reference 5 Grounding and Shielding Techniques for Instrumentation, Ralph Morrison; Wiley 1967
- Reference 6 "How to keep instruments accurate inside hot, noisy PCs", EDN Magazine April 13, 2000, Paul Packebush of National Instruments

Prove it works!

List of Appendices

Appendix	Title	Page
A	Diagnosing Noise	85
B	Achieving > 12-bit Resolution	86
C	How to Shield	92
D	Minimizing Magnetic Field of an IC	93
E	Low inductance bypass capacitors	94
F	Achieving 1 uV Noise Levels from V_{DD}	95
G	Non-PCB E-field issues	101
H	Properties of Copper	108
I	Magnitude of Noise Sources and conditions for their measurement	109
J	Full Descriptions of all Experiments on the Noise Evaluation Boards	111
K	More on Shielding E-Fields and H-Fields	114

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Appendix A
Diagnosing Noise

- Use a battery-powered scope, so power line HF will not find return path through the scope probe cable shield and probe GND lead
- Use SMA (screw) & BNC connectors (quick twist) to monitor noise
- If using scope probe, build a zero-length ground lead with solder wick around metal barrel of probe tip
- If you prototype above a single Ground plane, you may need a screen room
- The noise floor of a Spectrum Analyzer at a 10 kHz Resolution Bandwidth is approximately -100 dBm [6 uVpp]. With a FET probe, to boost input R to 1 MΩ, you have a sensitive tuned noise detective, suitable for probing ALL low/moderate amplitude nodes
- Look for oscillation: LDOs, Op amps, ADCs (yes!), Switching Regs chaotic servo-loop hunting (2 mV@2 kHz). Turn off MCU, and use Spectrum Analyzer to search for noise

Appendix B
Achieving > 12-bit Resolution

- **Additional design considerations for achieving high resolution in your application**
  - **Switched Capacitor ADCs**
  - **Settling**
  - **Dielectric Absorption**
  - **Leakages**
  - **Transient Events**
  - **Thermal**
  - **Etc.**

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Appendix B1 Switched Capacitor AnalogDigitalConverter NOISE FLOOR

- ADC sampling_cap has THERMAL NOISE, because of the sampling switch resistance. VnoiseRMS = squareroot[K*T/C] = sqrt[4e-21/C]
- This causes a SAMPLING ERROR; error statistics are Gaussian, as demanded by the CentralLimitTheorem for a large # of error contributions [the electrons in the switch].
- The Gaussian tails, at 0.1%, are +-3.3 RMS.
- These capacitors are INTERNAL to ADC. No way to filter out the noise.

Sampling Cap	V_{noise} rms	V_{noise} pp
10 pF	20 uV	132 uV
40 pF	10 uv	66 uV
100 pF	6.2 uV	41 uV
400 pF	3.1 uV	20.5 uV
4000 pF	1 uV	6.6 uV
40,000 pF	0.3 uV	2 uV
400,000 pF	0.1 uV	0.6 uV

How to achieve Lower Noise?

Use a non-switched-cap ADC,

And use a External SampleHold

With large Hold capacitor.

Appendix B2
Settling

- Op amp settling [8.9 dB dynamic range per Tau of settling]
- V_{DD} load changes(LDO regulation and/or I*R in R*C LPF
- V_{DD} ringing in Bypass Capacitors
- Dielectric absorption (signal path, V_{DD} path)
- Vdd regulator thermal sensitivity
- V_{REF} load changes
- Thermal changes across PCB metallic junctions, as loads change
- Thermal changes inside ICs: time constant of top 1u is 11 ns
- Time constant of 1000u cube (1mm) of silicon is 11 ms
- Load change of 1 mW, in 100 °C/Watt DIP, is 0.1 °C; thus Op amp with 5 uV/°C drift, will have 0.5 uV shift & 11 ms tau; Tektronix used special circuits to maintain constant power
- Movement of heat sources [human body is 300 watts]

Appendix B3
Dielectric Absorption

- NPO caps are good
- X7R are bad
- Polystyrene are good
- Electrolytics are bad
- ******Symptom: slow to settle(2 minutes) to final value
- After 5 V step, X7R provided 200 uV error thru 1 kΩ => 0.2 uA, with 30 second time constant (120 seconds to settle within thermal noise peak-peak band of 5-10 quanta)
- How to separate from Thermal settling?
- Cap leakage is f(temperature), => I*R error varies with temperature
- Some like Panasonic HFQ capacitors

Appendix B4
Leakages

- **A 0.1” by 2” trace has >> 10 MΩ resistance to ground**
- **When a SMA connector is installed, resistance to Ground is 4 MΩ to 11 MΩ, depending on residual solder flux.**
- **===> a CLEAN PCB is needed. Op amp circuits with 1 kΩ resistances, and 10 MΩ leakages, will have $10^3/10^7$ or 10^{-4} error, or 100 PPM, or 500 uV out of 5 V. Op amp circuits with 100 kΩ resistances will have 1% errors.**
- **Guarding may be used to reduce leakage errors. Surround the sensitive node with an “exact copy” of that voltage.**

Appendix B5
Other "noise" sources: etc

- ---------------- ADC sampling surges -------------
- Op amp rings, its V_{DD} rings
- 5 nH & 0.2 uF ring at 5 MHz
- ADC: C_{in} of 20 pF & C_{vdd_bypass} of 200,000 pF, 500 uV Vdd sag at op amp
- Op amp PSRR approx 1 at high freq => op amp output has 5 MHz
- Use silver_mica or C0G caps (per Bonnie Baker)
- ------------------- VDD/2 shared node ----------------
- Being a shared node, circuits will interact and perhaps oscillate.
- ------------------- Voltage Reference -------------------
- Noise, drift, PSRR at DC and HF, load shift
- Delta-sigma specific noise behaviors (MCHP and LLTC) with coherent narrow-band noise sources

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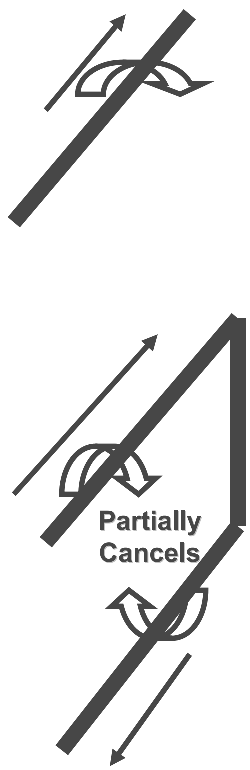
Appendix C
How to Shield

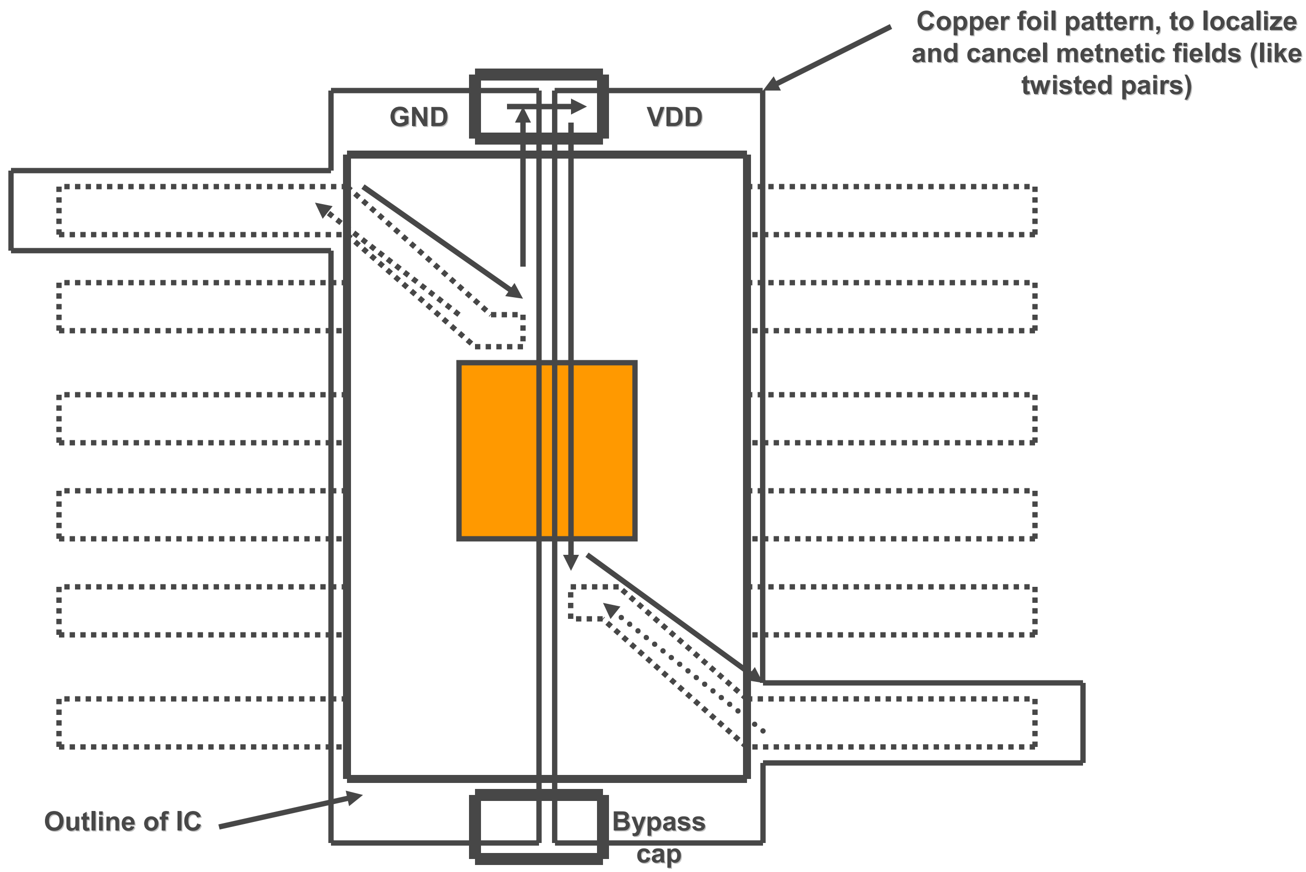
- A solid shield is best, but some openings are necessary.
- For magnetic shielding, attenuation is

  8.9 db * Thickness/SkinDepth
- Avoid seams and joints. If this is not possible, use conductive gaskets there
- Copper tape will shield non-blind vias against capacitive coupling. The tape MUST BE connected to local RETURN
- Read RF Design article “Low Transfer Impedance – a Key to Effective Shielding” RF Design July/Aug 1984, by Thomas Jerse, volume 7, page 29-32

Appendix D
Minimizing Magnetic Field of an IC

- **At high frequencies, most of the current will take the smallest loop, to partially cancel the magnetic field; this reduces the stored energy, allowing the fastest movement of charge. 1-ounce foil is 6-skin-depths thick @ 100MHz.**





Appendix E
Low inductance bypass capacitors

- The X2Y Corporation has 4-leaded surface-mount ceramic bypass capacitors; the ESL (equivalent series inductance) is reduced from 0.88 nH to 0.11 nH
- Unless you pay attention to copper trace inductance, and to using multiple vias, these capacitors will be wasted. But if you make the effort . . . . . .
- Best application requires 6 vias, to achieve mutual inductance cancellation.
- See www.X2Y.com for discussion of "spreading inductance". Used skillfully, you might reduce # digital bypass caps by 5:1. That is lots of PCB area. Read App Note HFPGA.pdf and 3009.pdf, on using ultra-thin PCB di-electrics to improve digital bypassing.
- If careless, can achieve 10 nH inductance with a single SMT bypass cap+via+traces+planes, because of the magnetic fields cooperating to BOOST the stored energy and inductance.

Appendix F
Achieving 1 uV Noise Levels from V_{DD}

- Why power supplies have poor rejection of high frequency noise, and how output-impedance degrades as frequency increases
- Limitations of “use a big capacitor” mindset

Appendix F1
PSRR and V_{DD} noise

- **Power Supplies are noisy and unstable and change with loads.**
- **Analog ICs need QUIET supply voltages (PSRR approx 1 at 1 MHz)**
- **Linear Regulators have finite line and load regulation at DC, and non-zero thermal noise (assume 1 mV); assume LDO PSRR is 1 at 1 MHz**
- **Switching Regulators have same issues, and add 0.1 V ringing at L_{extn}+C_{filter} frequency, and 0.1 V ringing at $L_{package}$+C_{esd}**
- **How to succeed:**

  (A) with supply noise increasing above 60 Hz, must provide filtering above 60 Hz [tau = 2.5 ms; 100 uF & 25 Ω]

  (B) Keep currents constant

  (C) Provide a private regulator

  (D) treat the regulator as sensitive IC [filter ITS input above 60 Hz]

  (E) use cascaded R*C filter sections

  (F) remember a capacitor has non-zero ESR and ESL, thus difficult to achieve over 100:1 noise attenuation even with R*C filtering.

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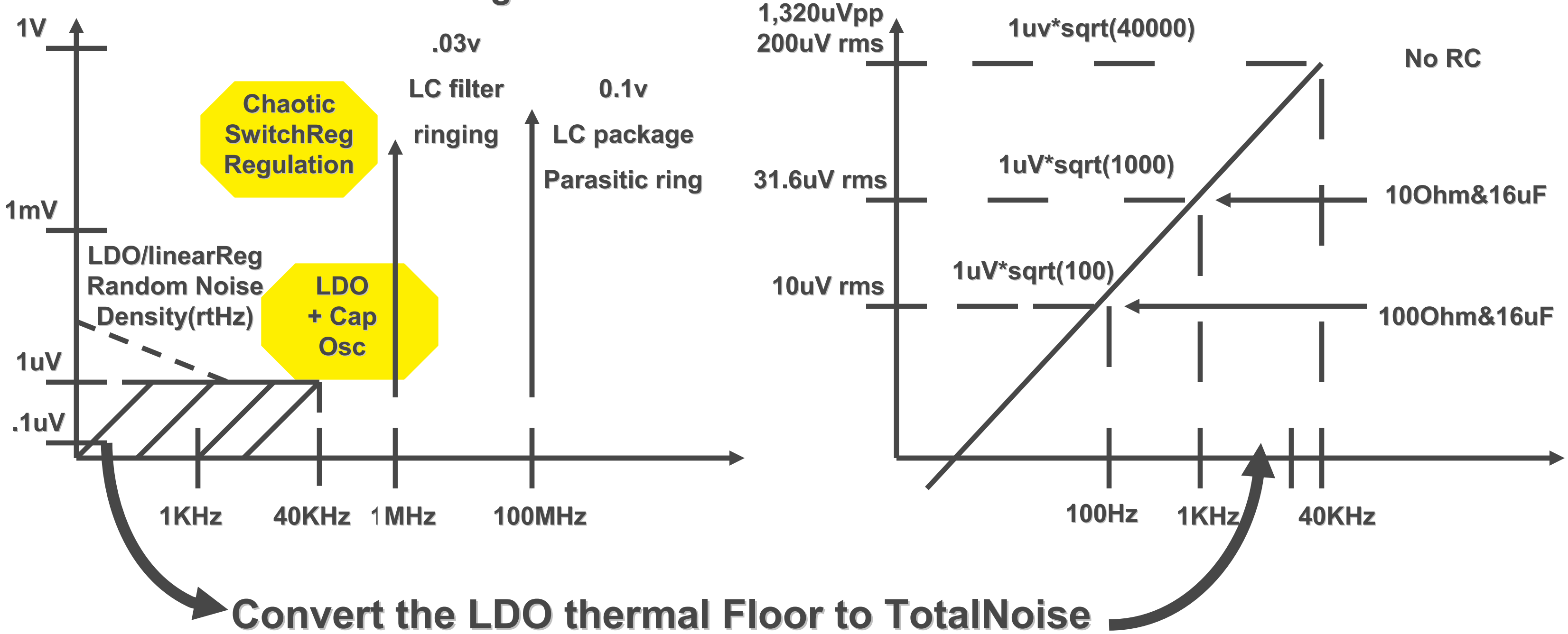
Appendix F2
Power Supply Output Noise

- **Output Noise (random & periodic) Spectrum of Power Supply**

What is the "root-Hertz" concept?
Acknowledges NoisePower is proportional to Bandwidth, while NoiseVoltage is proportional to squareroot(Bandwidth)

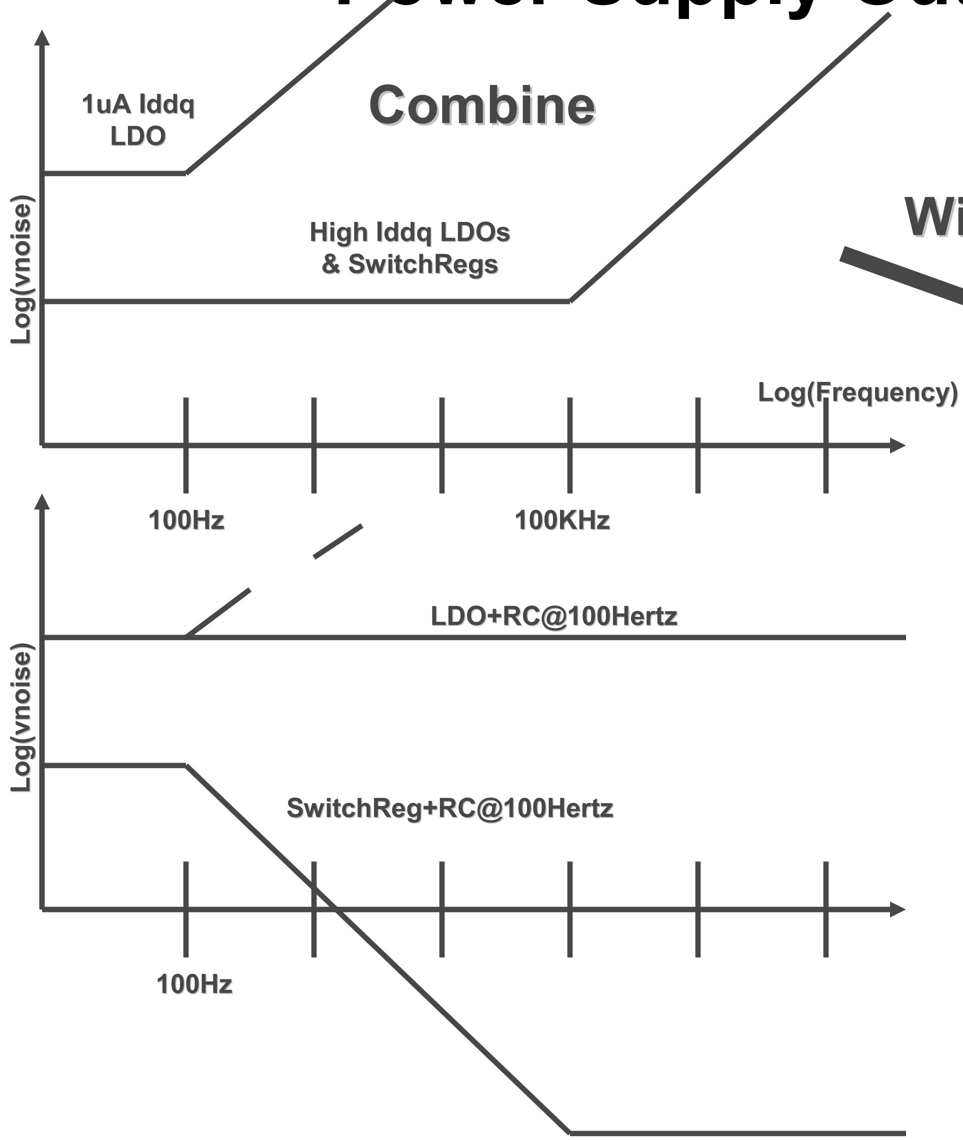
This is what to expect from that LDO or that SwitchReg

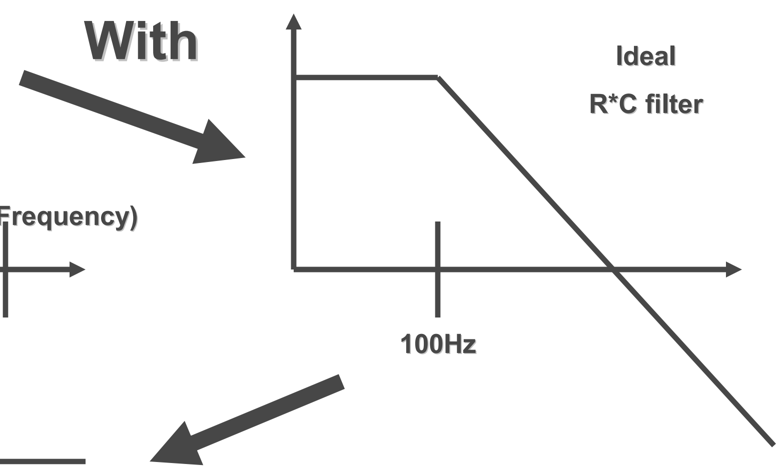


Appendix F3
Why Power Supplies have poor High Frequency Rejection

- (#1) Power Supplies have regulator/feedback/servo loops. Feedback loops have limits on how fast they function well. To function at higher frequencies, control circuits would consume more power.
- Thus Vreg of Power Supply tracks any “high frequency” on Vin because the regulation behavior is less effective.
- If you want, and are willing to pay for, improved “high frequency” performance from your Power Supply, the Iddq will probably be higher, because I=C*dV/dT in the control circuitry.
- (#2) Power Supplies use large transistors to control (switch, throttle) the energy. Those large transistors have large junctions and thus large capacitance between Vin and Vreg.
- At “high frequencies”, that capacitance is a path the energy uses to skip around the regulation circuit.
- P.S. #1 and #2 also apply to the “high frequency” power supply rejection of your favorite opamp or ADC or voltage-reference or DAC or…..

Appendix F4
Power Supply Output Impedance



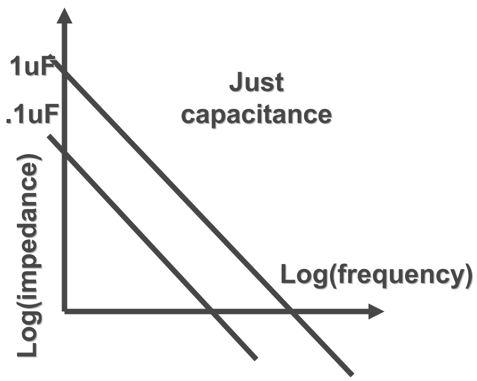


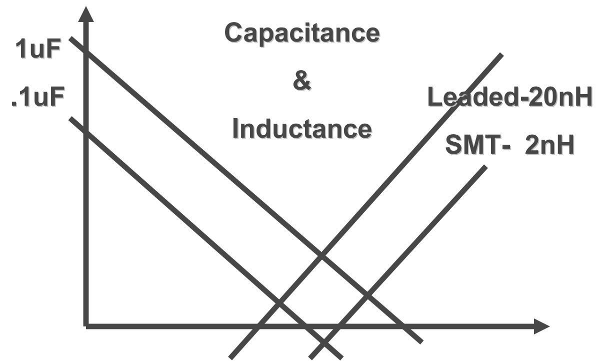
- Different Power Supplies have different Rout, Zout, Freg_corner, Noise Floors and Noise Peaks, line_regulation and drift. How to manage these various parameters?
- The BIG cap……..

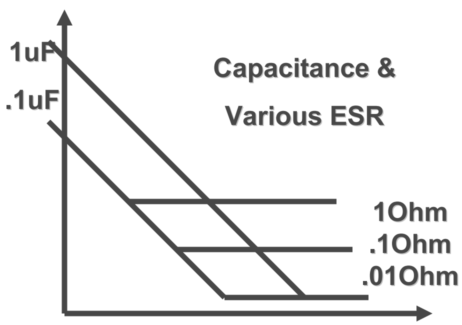
Appendix F5
ESR & ESL of capacitors

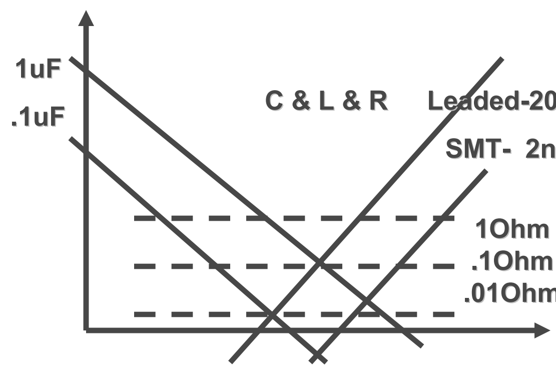
- Our available low-pass component has many flaws: ESL, ESR.
- High Z => poor noise control: 0.1 Amp*1Ω >> 0.1A*0.01Ω

Capacitor	F_{ring} for C + 10 nH
10 uF	0.5 MHz
1 uF	1.6 MHz
0.1 uF	5 MHz
0.01 uF	16 MHz
1000 pF	50 MHz
100 pF onchip	160 MHz =>EMI









Parallel Caps	Caps + 10 nH
1u || 1uF	2MHz
1uF || .01uF	16MHz
1uF || 100pF	160MHz

Appendix G
Non-PCB E-field issues

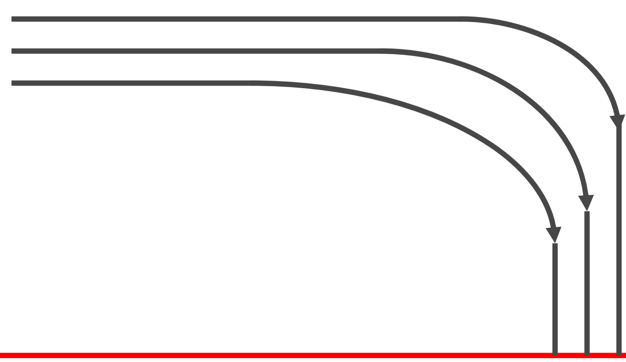
- ICs are NOT shielded
- Shielding Effectiveness of Coaxial Cables
- E-fields into sensors

Appendix G1
ICs are NOT shielded

- The silicon area of an op amp is approximately 0.05*0.05", the same area as a via
- Can the silicon be shielded?
  - Yes, if there is a "shield" pin
- Where to connect the "shield" pin?
  - –V, +V, Vout
- Low $I_{dd\ (quiescent)}$ ICs are particularly vulnerable.
- The susceptibility is TOTALLY dependent on layout. Thus from IC to IC, within a family, within a company, across companies, your results will vary. Evaluate each IC.

Appendix G2
Shielding Effectiveness of Coaxial Cables

- Coaxial Cable shielding depends on maintaining centering of shield and center conductor, for best cancellation of Magnetic fields. [page 106, section 8.5 Morrison Ref#5]
- Do not crush the cable. Do not bend the cable sharply. When bending a cable bundle, separate the cables in region of bend. (We seek 10^5 or 10^6 isolation, thus unusual methods are needed.)
- Copper will oxidize or tarnish. When oxidized, the currents in a strand of the braid cannot move into another strand, and a circular coaxlal current cannot exist. With circular currents REQUIRED in shield, to develop a magnetic field in opposition to field generated by center-conductor currents, a BRAIDED shield is not optimum. Use solid-shield coax. Or Braid+FoilShield coax cable.



Appendix G3
What type of Coax Shield?

- Belden 9116 1-braid is 60% coverage; Belden 7916 is 2-braid with 40% and 60%, with (1 - 0.6x0.4) = 1 - 0.24 = 76% coverage.
- How to do better? To better block the inflow of E-field flux lines?
- "We've seen the use of high-density braid-and-foil shielding clean up some nasty RFI problems in home CATV distribution, turning a cable signal that was nearly unwatchable due to multi-path problems (off-air signals entering the cable through the shield) into clean and clear reception."
- www.bluejeanscable.com/articles/shielding/htm
- With nominal CATV level of 0 dB mV across 75 Ω, with a "clean signal" requiring at least 50 dB SNR and perhaps 60 dB, the permitted interference is 1 mV/316 or 1 mV/1000, or 3-1 uV.
- This accomplished with Belden 1694A coax.

Appendix G4
E-fields into sensors

- **Per Morrison page 34 [Ref#5], in a room, induced current per square foot, by the 60 Hz environment is approximately 0.1 uA, which can be modeled as a 2 pF capacitor to 117 Vac.**

- **Verify Morrison:**
  - **I = C*dV/dT; C = 10^{-11}F/M * 0.1M^2/1M = 10^{-12} = 1 pF (close enough)**
  - **I = 2 pF*117 Vac*2.828*377radians/second = 0.25 uA_{PP}**

- **Thus a $foot^2$ PCB or the chassis of laptop PC has 0.25 uA current seeking a return path. A sensor provides a fine return path.**

Appendix G5
Return Currents Upset Sensors

- **Various power supply, AC wiring, and digital wiring will use the SENSOR as a return path.**
- **Why? All possible paths are used**
- **How to prevent? Localize fields, prevent coupling of E-fields to “earth”, prevents AC power coupling to circuit boards, localize digital returns.**
- **How to cure? Insulate the sensor, use fiber-optic data links, use transformers for power and for synchronous-demod sensor conditioning (was used for NuclearTestSite instrumentation).**

Appendix G6
Capacitances causing Return Currents thru Sensors

Center-to-shield RG-58	33 pF/foot
Shield-to-metal-cable-tray RG-58	25 pF/foot
Center-wire-to-metal-tray RG-58	0.15 pF/foot [limits isolation]
#22 insulated wire, in bundle of #22	40 pF/foot
Strain Gauge bonded to structure	140 pF
ThermoCouple to structure	100 pF
Man standing on insulation	700 pF
Primary-to-secondary of small transformer	1,000 pF

- From page 34 of Morrison [Ref#5]

- Who cares? 117VAC coupling thru 1,000 pF (I=C*dV/dT) = (10^{-9}*117*2.828*377 radians/second) = 123 uA_{PP}; with 100 kΩ thermister sensor, 12.3 V appears across the sensor.

Appendix H
Properties of Copper

- **Electrical Conductivity: 6.58*10^{-7} Ω/inch or 16.7*10^{-7} Ω/cm**
- **Thickness of 1 ounce copper foil: 0.00137 inch** (1.4 mils, 35 μm)
- **Resistance of a 1" square of copper foil:**

  Ω = ρ * area/distance, thus for 1 ounce copper foil:

  Ω = 6.58*10^{-7} * (1)^2/0 .00137= 0.000480 Ω
- **Thus, ANY square of 1 ounce copper foil has resistance of 0.00048 Ω measured from opposite sides of the square (must fully contact all along each side)**
- **Density: 8,960 kg/meter^3**
- **Thermal Conductivity: 382 Watt/^{o}Kelvin*meter**
- **Specific Thermal Capacity: 385 Joule/^{o}Kelvin*kg**
- **Thermal time constant "thermal diffusivity":**

  113e^{-6} meter^2/second

  (ratio of heat stored to heat conducted)

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Appendix I
Summary of Errors

- Capacitive coupling into 0.05” by 0.5” trace
- Magnetic coupling into $(0.5")^2$ loop

Error Source	Condition	Voltage Error (RTI)	Bandwidth
Digital Interfaces	5 V/2.5 ns @ C_{ESD}= 10 pF RTN thru 5 nH	160,000 uVpp	400 MHz
V_{DD} noise (switch reg)	1 MHz noise, 0.1 Vpp, PSR = 0 dB	100,000 uV_{PP} RTI	1MHz
V_{DD} noise (1 mA step)	10 kHz step, ESR = 0.1 Ω , dV_{DD} = 0.1 mV; PSR = 40 dB	1 uV_{PP} RTI	10KHz
Magnetic coupling	Appliance Motor Controller @ 8”	60,000 uv @ 30 kHz	30 kHz
Magnetic coupling	Switching Regulator @ 2”	50,000 uV_{PP}	100 MHz
Magnetic coupling	PIC clock @ 2”, charging 50 pF, 5 V/5 nS	25,000 uV_{PP}	200 MHz
Magnetic coupling	117 VAC 1 A 60 Hz @ 2” (no twisted pair)	0.7 uV_{PP}	60 Hz
Capacitive Coupling	PIC 5 V/5 ns @ 1” into 0.05”x 0.5” (3 fF, 1 V/nS)	1,700 uv (5 V * 3 fF/10 pF)	200 MHz
Capacitive Coupling	117 VAC @ 2” into 0.05”x 0.5” (across enclosure)	50 uV (0.5 nA & 100 kΩ)	60 Hz
Capacitive Coupling	80 kHz fluorescent @ 5’ into 0.05 x .5” (40 pA)	40 uV @ 1 MΩ (4 uV @ 100 kΩ)	80 kHz

Summary of Errors (cont'd)

- Capacitive coupling into 0.05" by 0.5" trace
- Magnetic coupling into $(0.5")^2$ loop

Error Source	Condition	Voltage Error(RTI)	Bandwidth
Vibration Coax Cable	Sharp rap on middle of 2-meter RG58U	2,000 uV_{PP}	100 Hz
Vibration/X7R cap	¼" flexing of PCB at 8" from SMT cap	500 uV_{PP}	1 Hz-1 kHz
Thermal heat sinking	1 watt @ 70C/watt * 3 uV/°C [solder joint]	210 uV	DC
Thermal drift of Op Amp	70C/watt * 0.5 uV/°C offset voltage drift	35 uV	DC
Dielectric absorption	0.1uF X7R, charged to 5V, thru 1 kΩ R_{source}	200 uV_{PP} DC	Dielectric absorption
Current spreading in PCB	0.25" from strip line of 10 MHz sine clock (50 Ω)	150 uV (5v@-90dBc)	10 MHz
Current spreading in PCB	0.1" from 50 Ω term of 10 MHz sine clock	25 uV	10 MHz
Current flow in PCB	10 mA thru vias separated by via diameter	4 uV	all

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Appendix J
E-Field Board (104-00137)
Lab Exercise Descriptions

Exercise	Description	Number of PCB layers
1	Examine effect of E-field coupling with various ground distances surrounding traces.	Single layer
2	Examine effect of E-field coupling with various spacing between traces	Single layer
3a	Examine effect of E-field coupling with various spacing over a ground plane	Double layer
3b	Examine E-field coupling with various spacing between two ground planes	Triple layer
4	Examine E-field coupling with varying numbers of ground vias between the traces	Single layer
5	Effect of E-field coupling on Trace-to-metal-area	Double layer
6	Effect of E-field coupling referenced to a nearby shield at various distances	Four layer
7	Effect of E-field coupling with ground between traces at various depths	Four layer
8a	Effect of E-field coupling with varying numbers of ground vias between the traces over a ground shield	Double layer
8b	Effect of E-field coupling with ground vias between the traces between two fully-shielded ground planes	Three layer

H-Field Board (104-00138) Lab Exercises

Exercise	Description	Number of PCB layers
1	Driven Single Wire over Loop at different distances and centerings	2 layers
2	Driven Loop over Loop at different distances	2 layers
3a	Loop to Loop at different distances over ground plane	3 layers
3b	Loop to Loop with ground plane in between	3 layers
4a	Nested Loops at various distances from surrounding ground plate	1 layer
4b	Loop to loop completely surrounded by ground planes	4 layers
5	Induced voltage between traces at differing angles	3 layers
6	Vertical loop to Horizontal loop induction	4 layers
7	Inductive Coupling between "PCB Loops"	multi-layers

PSRR and Digital Noise Board (104-00139) Lab Exercises

Exercise	Description	Variables	Frequency Injection
1	Power Supply Rejection analysis at 5V. Response of various voltage regulators and op amps to Vdd noise (injected on Vsource).	3 Linear Regulators, 1 Switching Regulator, 4 Op Amps	100, 1k, 10 kHz
2	Power Supply Rejection analysis at 3V. Response of various voltage regulators and op amps to Vdd noise (injected on Vsource).	3 Linear Regulators, 1 Switching Regulator, 4 Op Amps	100, 1k, 10 kHz
3	Effects of noise spikes on Op Amp performance. 0.25 V spikes are injected on CS, Vout and Vin of Op Amps. Op Amp output is examined.	1 Linear Regulator, 4 Op Amps	100 kHz, 1 MHz, 10 MHz
4	How Power Supply Rejection is affected by Common Mode Voltage. Vref is varied on Op Amps. Op Amp output is examined.	3 Linear Regulators, 1 Switching Regulator, 4 Op Amps	100 kHz, 1 MHz, 10 MHz
5	Effects of E-Field on HS Op Amp	1 Linear Regulator, 1 Op Amp	Determined by E-Field
6	Effects of H-Field on MS Op Amp	1 Linear Regulator, 1 Op Amp	Determined by H-Field
7	Effects of Thermal (1/4 watt heat) on LS Op Amp	1 Linear Regulator, 1 Op Amp	100 kHz, 1 MHz, 10 MHz

Appendix K
Shielding E and H fields

- A perfect conductor is a fine magnetic shield
  - Any changing H-field induces a current at the surface of the shield, and ONLY at the surface (because of the ZERO resistance)
  - That induced current, per Lenz's law, has a magnetic field that exactly cancels the incoming H-field, at the surface.
  - Since copper and aluminum and steel (and gold and silver) are very imperfect conductors, E&H fields do enter the shielding material (even our V_{DD} and GND planes) some distance [characterized by "skin depth"]

Why are these fields so seldom a bother?

- Digital signals have 1 to 5 nS edges. The currents and voltages induced will be 2X the speed (derivative of "s" curve)
- Slow analog circuits, acting as Low Pass Filters, will absorb the fast energy and AVERAGE it
- Do not depend on [slow Unity Gain Bandwidth] op amps to reject the high frequency spikes and pulses and noise.
  - Why? The HF energy will couple through ESD junctions and gain-stage device junctions.
  - This coupling will SHIFT the I & V operating point of the transistors, and cause errors. The nonlinear operation of junction rectification causes operating-point shift.
- Use explicit R*C filters on input leads of ICs. And metal shields. And distance.
- The response of different semiconductors, to large fast energy events, will be different. Microchip has won some designs because our opamps were less upset by Cell phone/Bluetooth fields. <u>PCB layout is more important</u>!

Skin Effect

- Skin depth is:

  1/sqrt(π x conductivity x permeability x frequency)
- With zero resistance, magnetic fields do not penetrate the conductor at all
- With zero resistance, electric fields do not penetrate the conductor at all
- Metals are so conductive that even visible light is reflected
- Copper has resistance, thus magnetic & electric fields do penetrate
- Copper has resistance, and dissipates energy, thus fields attenuate as they go deeper
- Both fields (E & H) are attenuated by 1/e (37%) for each “skin depth”

Skin Effect (cont'd)

- To attenuate 100:1, need loge(100) = ln(100) = 4.6 skin depths.
- Use 100 MHz for frequency of MPU clock transition energy (5 nS up, 5 nS down)
- Copper skin depth for 100 MHz = 0.0066 millimeters (6.6 microns, 0.25 mils)
- Thickness of 1-ounce copper is 35 microns (1.4 mils)
- 1-oz copper has 35 micron/6.6 micron = 5.3 skin depths
- $e^{5.3}$ = 200.3 or 200:1 reduction in magnetic field, or 46dB less induced voltage
- Need MORE attenuation? Use more layers, or use 2-ounce copper, or use alum or steel or nickel [See table #skindepths]

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Table of Skin Depth for Copper, Aluminum and Steel

- 1-depth 37%; 4.6-depths 1%; 9.2-depths 0.01%; 13.8-depths 1ppm
- 1/16" aluminum reduces 1 MHz Switch Reg H-field to 1 ppBillion
- 1-ounce copper thickness 35u (1.4mil), or Skin Depth for 5 MHz

Freq (Hz)	Copper		Aluminum		Carbon steel SAE1045	
60	8.5 mm	340 mil	11 mm	440 mil	0.85 mm	34 mil
1k	2.1 mm	80 mil	2.7 mm	110 mil	0.21 mm	8.4 mil
10k	0.66 mm	25 mil	0.85 mm	34 mil	0.066 mm	2.6 mil
100k	0.21 mm	8 mil	0.27 mm	11 mil	0.021 mm	0.84 mil
1M	0.066 mm	2.5 mil	0.085 mm	3.4 mil	0.0066 mm	0.26 mil
10M	0.021 mm	0.8 mil	0.027 mm	1.1 mil	0.0021 mm	0.084 mil
100M	0.0066 mm	0.25 mil	0.0085 mm	0.34 mil	0.00066 mm	0.026 mil

Table derived from [HowardJohnson ref 1]

Steel Shielding

Steel Shield absorption (dB) vs. frequency, for 1/32" steel:

3.34*Thickness*sqrt(Frequency* Relative_Conductivity* Relative_Permeability) [Ref 6]

Frequency	Absorption (db)	Ratio
60	77	7000:1
100	100	100:000:1
1,000	316	
10,000	1000	
100,000	3168	
1,000,000	10,000	

The End

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